HARRIS

IRFD1Z0, IRFD1Z1 IRFD1Z2, IRFD1Z3

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 0.4A and 0.5A, 60V - 100V
- $r_{DS(on)}$ = 2.4Ω and 3.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

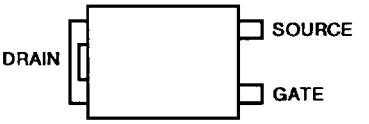
Description

The IRFD1Z0, IRFD1Z1, IRFD1Z2, and IRFD1Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin DIP package.

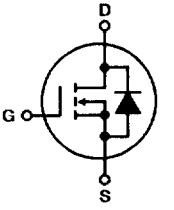
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	UNITS
Drain-Source Voltage (1)	V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	60	100	60	V
Continuous Drain Current T_C = +25°C	I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current	I_{DM}	4.0	4.0	3.2	3.2	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L 100μH)	I_{LM}	4.0	4.0	3.2	3.2	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

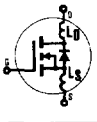
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2313**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD1Z0, 2	100	–	–	V	V_{GS} = 0V
		IRFD1Z1, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD1Z0, 1	0.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD1Z2, 3	0.4	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD1Z0, 1	–	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD1Z2, 3	–	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.25	0.35	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	–	50	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	20	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	5.0	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.25A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	1.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	1.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD1Z0, 1	–	–	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD1Z2, 3	–	–	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD1Z0, 1	–	–	4.0	A	
		IRFD1Z2, 3	–	–	3.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD1Z0, 1	–	–	1.4	V	T_A = 25°C, I_S = 0.5A, V_{GS} = 0V
		IRFD1Z2, 3	–	–	1.3	V	T_A = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

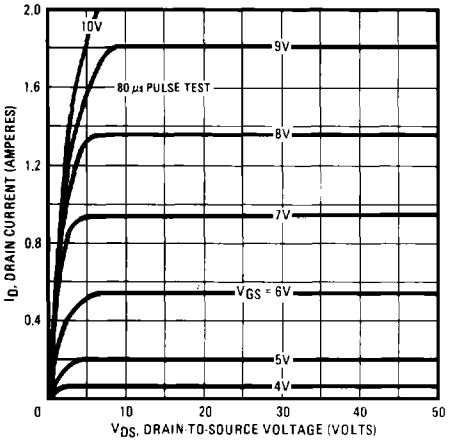


Fig. 1 – Typical Output Characteristics

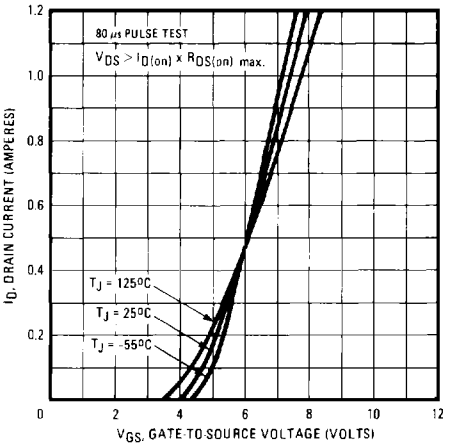


Fig. 2 – Typical Transfer Characteristics

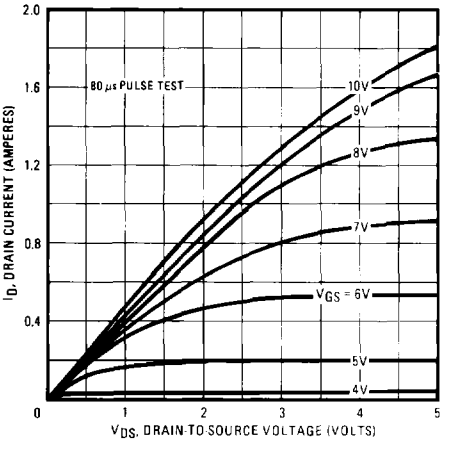


Fig. 3 – Typical Saturation Characteristics

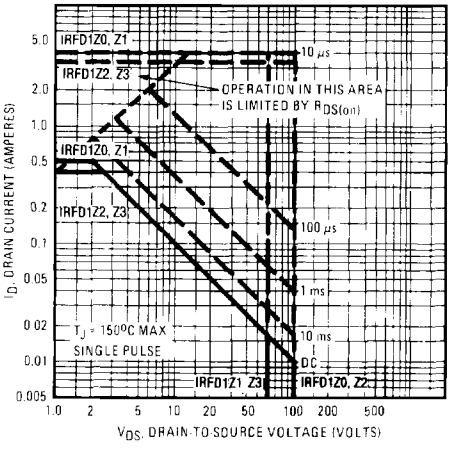


Fig. 4 – Maximum Safe Operating Area

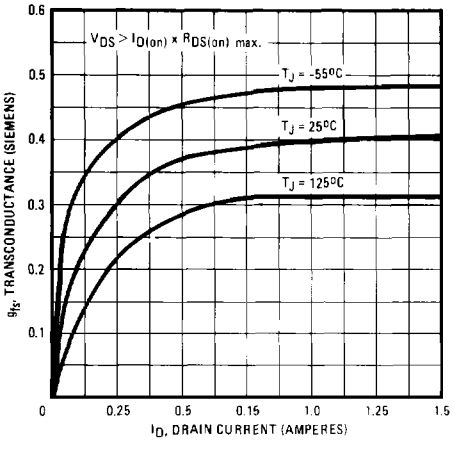


Fig. 5 – Typical Transconductance Vs. Drain Current

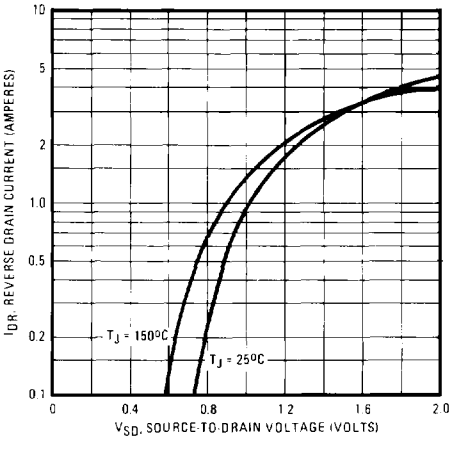


Fig. 6 – Typical Source-Drain Diode Forward Voltage

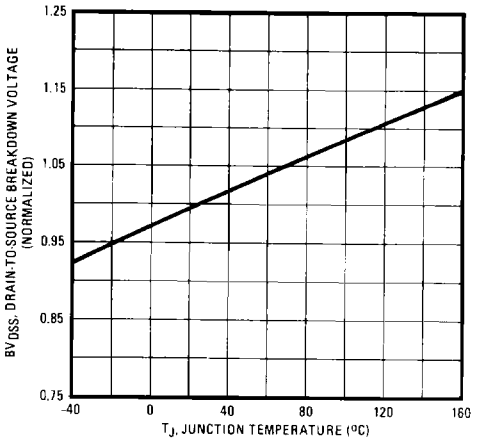


Fig. 7 – Breakdown Voltage Vs. Temperature

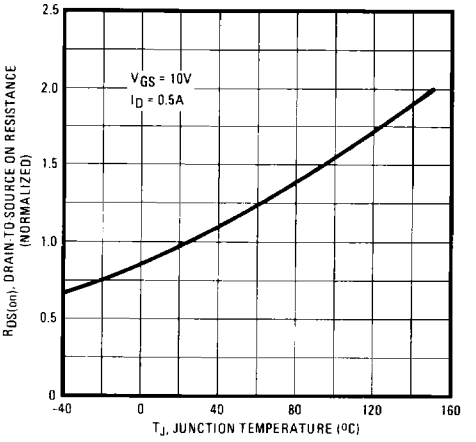


Fig. 8 – Normalized On-Resistance Vs. Temperature

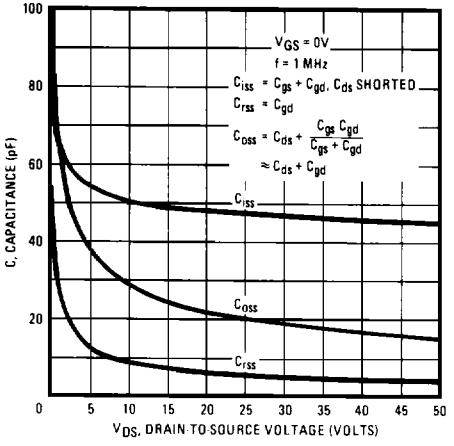


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

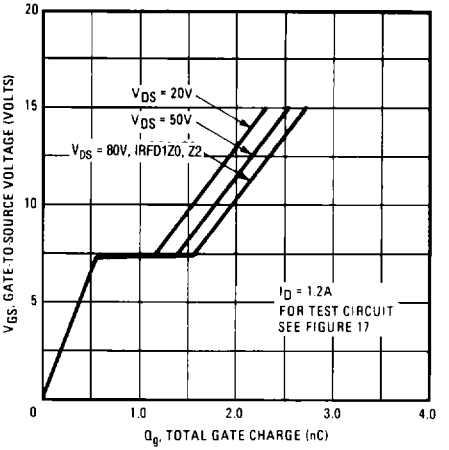


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

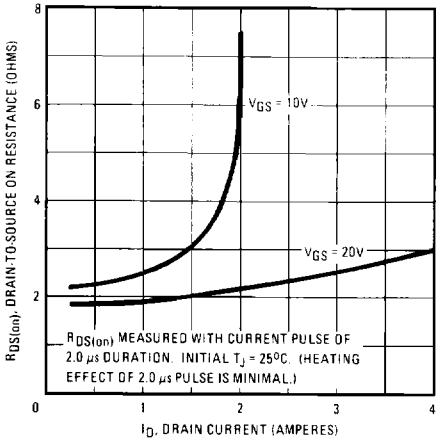


Fig. 11 – Typical On-Resistance Vs. Drain Current

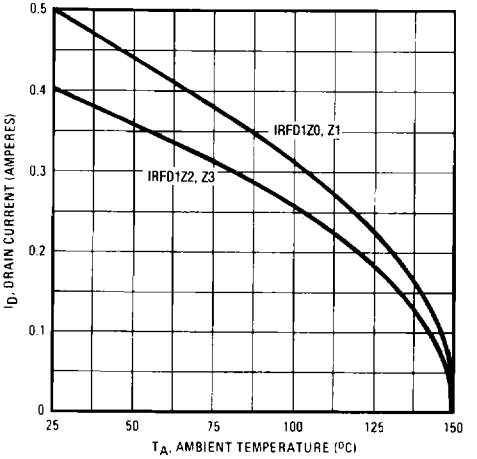


Fig. 12 – Maximum Drain Current Vs. Case Temperature

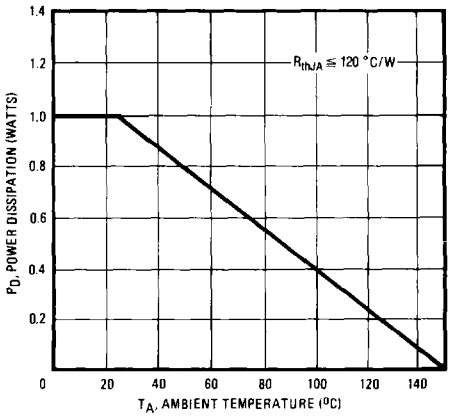


Fig. 13 – Power Vs. Temperature Derating Curve

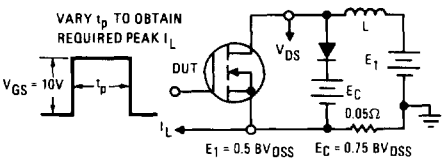


Fig. 14 – Clamped Inductive Test Circuit

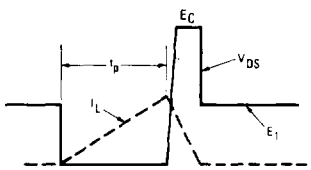


Fig. 15 – Clamped Inductive Waveforms

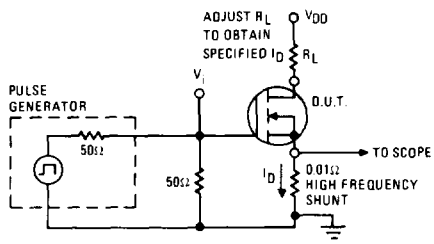


Fig. 16 – Switching Time Test Circuit

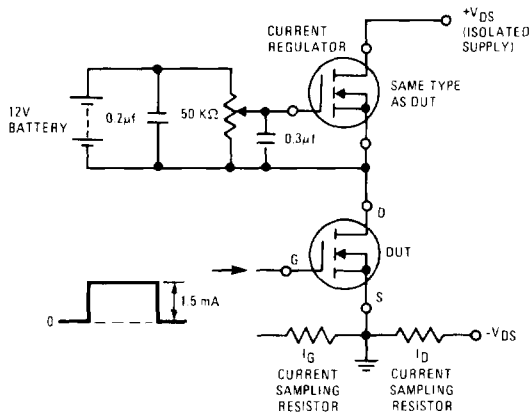


Fig. 17 – Gate Charge Test Circuit