LOW POWER PCIE GEN2/3 & QPI CLOCK FOR INTEL-BASED SERVERS

932SQL420

General Description

The 932SQL420 is a low power version of the CK420BQ synthesizer for Intel-based server platforms. The 932SQL420 is driven with a 25MHz crystal for maximum performance. It generates CPU outputs of 100Mhz. This device has a "low-drift" non-spread SAS/SRC PLL for use in systems that need to communicate across PCIe domains.

Recommended Application

Low Power CK420BQ

Key Specifications

- CPU, SRC, NS_SRC and NS_SAS cycle-cycle jitter <50ps
- Output to output skew <50ps
- Phase jitter: PCIe Gen2 <2.7ps rms
- Phase jitter: QPI <0.3ps rms
- Phase jitter: NS-SAS <1.3ps rms using long period phase jitter method

Features/Benefits

- 0.5% down spread capable on CPU, SRC and PCI outputs; reduce EMI
- Additional down spread amounts selectable via SMBus; maximal system flexibility
- 64-pin TSSOP and MLF packages; space savings

Output Features

- 4 - Low-Power HCSL-compatible (LP-HCSL) CPU outputs
- 2 - LP-HCSL NS_SAS outputs
- 2 - LP-HCSL NS_SRC outputs
- 3 - LP-HCSL SRC outputs
- 1 - LP-HCSL DOT96 output
- 1 - 3.3V 48M output
- 5 - 3.3V PCI outputs
- 1 - 3.3V 14.318M output

Pin Configurations

	64-TSSOP	
SMBCLK	1	64 SMBDAT
GND14	2	63 VDDCPU
AVDD14	3	62 CPU3_LPT
VDD14	4	61 CPU3_LPC
ᵛREF14_3x/TEST_SEL	5	60 CPU2_LPT
GND14	6	59 CPU2_LPC
GNDXTAL	7	58 GNDCPU
X1_25	8	57 VDDCPU
X2_25	9	56 CPU1_LPT
VDDXTAL	10	55 CPU1_LPC
GNDPCI	11	54 CPU0_LPT
VDDPCI	12	53 CPU0_LPC
PCI4_2x	13	52 GNDNS
PCI3_2x	14	51 AVDD_NS_SAS
PCI2_2x	15	50 NS_SAS1_LPT
PCI1_2x	16	49 NS_SAS1_LPC
PCI0_2x	17	48 NS_SAS0_LPT
GNDPCI	18	47 NS_SAS0_LPC
VDDPCI	19	46 GNDNS
VDD48	20	45 VDDNS
48M_2x	21	44 NS_SRC1_LPT
GND48	22	43 NS_SRC1_LPC
GND96	23	42 NS_SRC0_LPT
DOT96_LPT	24	41 NS_SRC0_LPC
DOT96_LPC	25	40 NC
AVDD96	26	39 GNDSRC
TEST_MODE	27	38 AVDD_SRC
CKPWRGD#/PD	28	37 VDDSRC
VDDSRC	29	36 SRC2_LPT
SRC0_LPT	30	35 SRC2_LPC
SRC0_LPC	31	34 SRC1_LPT
GNDSRC	32	33 SRC1_LPC

64-TSSOP

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

64-Pin MLF

Top pins (64→49): VDDXTAL, X2_25, X1_25, GNDXTAL, GND14, vREF14_3x/TEST_SEL, VDD14, AVDD14, GND14, SMBCLK, SMBDAT, VDDCPU, CPU3_LPT, CPU3_LPC, CPU2_LPT, CPU2_LPC

Left pins (1→16): GNDPCI, VDDPCI, PCI4_2x, PCI3_2x, PCI2_2x, PCI1_2x, PCI0_2x, GNDPCI, VDDPCI, VDD48, 48M_2x, GND48, GND96, DOT96_LPT, DOT96_LPC, AVDD96

Bottom pins (17→32): TEST_MODE, CKPWRGD#/PD, VDDSRC, SRC0_LPT, SRC0_LPC, GNDSRC, SRC1_LPC, SRC1_LPT, SRC2_LPC, SRC2_LPT, VDDSRC, AVDD_SRC, GNDSRC, NC, NS_SRC0_LPC, NS_SRC0_LPT

Right pins (48→33): GNDCPU, VDDCPU, CPU1_LPT, CPU1_LPC, CPU0_LPT, CPU0_LPC, GNDNS, AVDD_NS_SAS, NS_SAS1_LPT, NS_SAS1_LPC, NS_SAS0_LPT, NS_SAS0_LPC, GNDNS, VDDNS, NS_SRC1_LPT, NS_SRC1_LPC

932SQL420

64-Pin MLF

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

64TSSOP Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
2	GND14	PWR	Ground pin for 14MHz output and logic.
3	AVDD14	PWR	Analog power pin for 14MHz PLL
4	VDD14	PWR	Power pin for 14MHz output and logic
5	vREF14_3x/TEST_SEL	I/O	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
6	GND14	PWR	Ground pin for 14MHz output and logic.
7	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
8	X1_25	IN	Crystal input, Nominally 25.00MHz.
9	X2_25	OUT	Crystal output, Nominally 25.00MHz.
10	VDDXTAL	PWR	3.3V power for the crystal oscillator.
11	GNDPCI	PWR	Ground pin for PCI outputs and logic.
12	VDDPCI	PWR	3.3V power for the PCI outputs and logic
13	PCI4_2x	OUT	3.3V PCI clock output
14	PCI3_2x	OUT	3.3V PCI clock output
15	PCI2_2x	OUT	3.3V PCI clock output
16	PCI1_2x	OUT	3.3V PCI clock output
17	PCI0_2x	OUT	3.3V PCI clock output
18	GNDPCI	PWR	Ground pin for PCI outputs and logic.
19	VDDPCI	PWR	3.3V power for the PCI outputs and logic
20	VDD48	PWR	3.3V power for the 48MHz output and logic
21	48M_2x	OUT	3.3V 48MHz output
22	GND48	PWR	Ground pin for 48MHz output and logic.
23	GND96	PWR	Ground pin for DOT96 output and logic.
24	DOT96_LPT	OUT	True clock of low-power push-pull differential 96MHz output. External series resistors are needed for termination.
25	DOT96_LPC	OUT	Complementary clock of low-power push-pull differential 96MHz output. External series resistors are needed for termination.
26	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
27	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
28	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
29	VDDSRC	PWR	3.3V power for the SRC outputs and logic
30	SRC0_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
31	SRC0_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
32	GNDSRC	PWR	Ground pin for SRC outputs and logic.
33	SRC1_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
34	SRC1_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
35	SRC2_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
36	SRC2_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
37	VDDSRC	PWR	3.3V power for the SRC outputs and logic
38	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
39	GNDSRC	PWR	Ground pin for SRC outputs and logic.
40	NC	N/A	No Connection.
41	NS_SRC0_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
42	NS_SRC0_LPT	OUT	True clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
43	NS_SRC1_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
44	NS_SRC1_LPT	OUT	True clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
45	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
46	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.

64TSSOP Pin Descriptions (cont.)

| PIN #	PIN NAME	TYPE	DESCRIPTION
47	NS_SAS0_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
48	NS_SAS0_LPT	OUT	True clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
49	NS_SAS1_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
50	NS_SAS1_LPT	OUT	True clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
51	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
52	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
53	CPU0_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
54	CPU0_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
55	CPU1_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
56	CPU1_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
57	VDDCPU	PWR	3.3V power for the CPU outputs and logic
58	GNDCPU	PWR	Ground pin for CPU outputs and logic.
59	CPU2_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
60	CPU2_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
61	CPU3_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
62	CPU3_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
63	VDDCPU	PWR	3.3V power for the CPU outputs and logic
64	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant

64MLF Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDPCI	PWR	Ground pin for PCI outputs and logic.
2	VDDPCI	PWR	3.3V power for the PCI outputs and logic
3	PCI4_2x	OUT	3.3V PCI clock output
4	PCI3_2x	OUT	3.3V PCI clock output
5	PCI2_2x	OUT	3.3V PCI clock output
6	PCI1_2x	OUT	3.3V PCI clock output
7	PCI0_2x	OUT	3.3V PCI clock output
8	GNDPCI	PWR	Ground pin for PCI outputs and logic.
9	VDDPCI	PWR	3.3V power for the PCI outputs and logic
10	VDD48	PWR	3.3V power for the 48MHz output and logic
11	48M_2x	OUT	3.3V 48MHz output
12	GND48	PWR	Ground pin for 48MHz output and logic.
13	GND96	PWR	Ground pin for DOT96 output and logic.
14	DOT96_LPT	OUT	True clock of low-power push-pull differential 96MHz output. External series resistors are needed for termination.
15	DOT96_LPC	OUT	Complementary clock of low-power push-pull differential 96MHz output. External series resistors are needed for termination.
16	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
17	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
18	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
19	VDDSRC	PWR	3.3V power for the SRC outputs and logic
20	SRC0_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
21	SRC0_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
22	GNDSRC	PWR	Ground pin for SRC outputs and logic.
23	SRC1_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
24	SRC1_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
25	SRC2_LPC	OUT	Complementary clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
26	SRC2_LPT	OUT	True clock of low-power push-pull differential SRC output. External series resistors are needed for termination.
27	VDDSRC	PWR	3.3V power for the SRC outputs and logic
28	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
29	GNDSRC	PWR	Ground pin for SRC outputs and logic.
30	NC	N/A	No Connection.
31	NS_SRC0_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
32	NS_SRC0_LPT	OUT	True clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
33	NS_SRC1_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
34	NS_SRC1_LPT	OUT	True clock of low-power push-pull differential non-spreading SRC output. External series resistors are needed for termination.
35	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
36	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
38	NS_SAS0_LPT	OUT	True clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.

64MLF Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
39	NS_SAS1_LPC	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
40	NS_SAS1_LPT	OUT	True clock of low-power push-pull differential non-spreading SAS output. External series resistors are needed for termination.
41	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
42	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
43	CPU0_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
44	CPU0_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
45	CPU1_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
46	CPU1_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
47	VDDCPU	PWR	3.3V power for the CPU outputs and logic
48	GNDCPU	PWR	Ground pin for CPU outputs and logic.
49	CPU2_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
50	CPU2_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
51	CPU3_LPC	OUT	Complementary clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
52	CPU3_LPT	OUT	True clock of low-power push-pull differential CPU output. External series resistors are needed for termination.
53	VDDCPU	PWR	3.3V power for the CPU outputs and logic
54	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
55	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
56	GND14	PWR	Ground pin for 14MHz output and logic.
57	AVDD14	PWR	Analog power pin for 14MHz PLL
58	VDD14	PWR	Power pin for 14MHz output and logic
59	vREF14_3x/TEST_SEL	I/O	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
60	GND14	PWR	Ground pin for 14MHz output and logic.
61	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
62	X1_25	IN	Crystal input, Nominally 25.00MHz.
63	X2_25	OUT	Crystal output, Nominally 25.00MHz.
64	VDDXTAL	PWR	3.3V power for the crystal oscillator.

Block Diagram
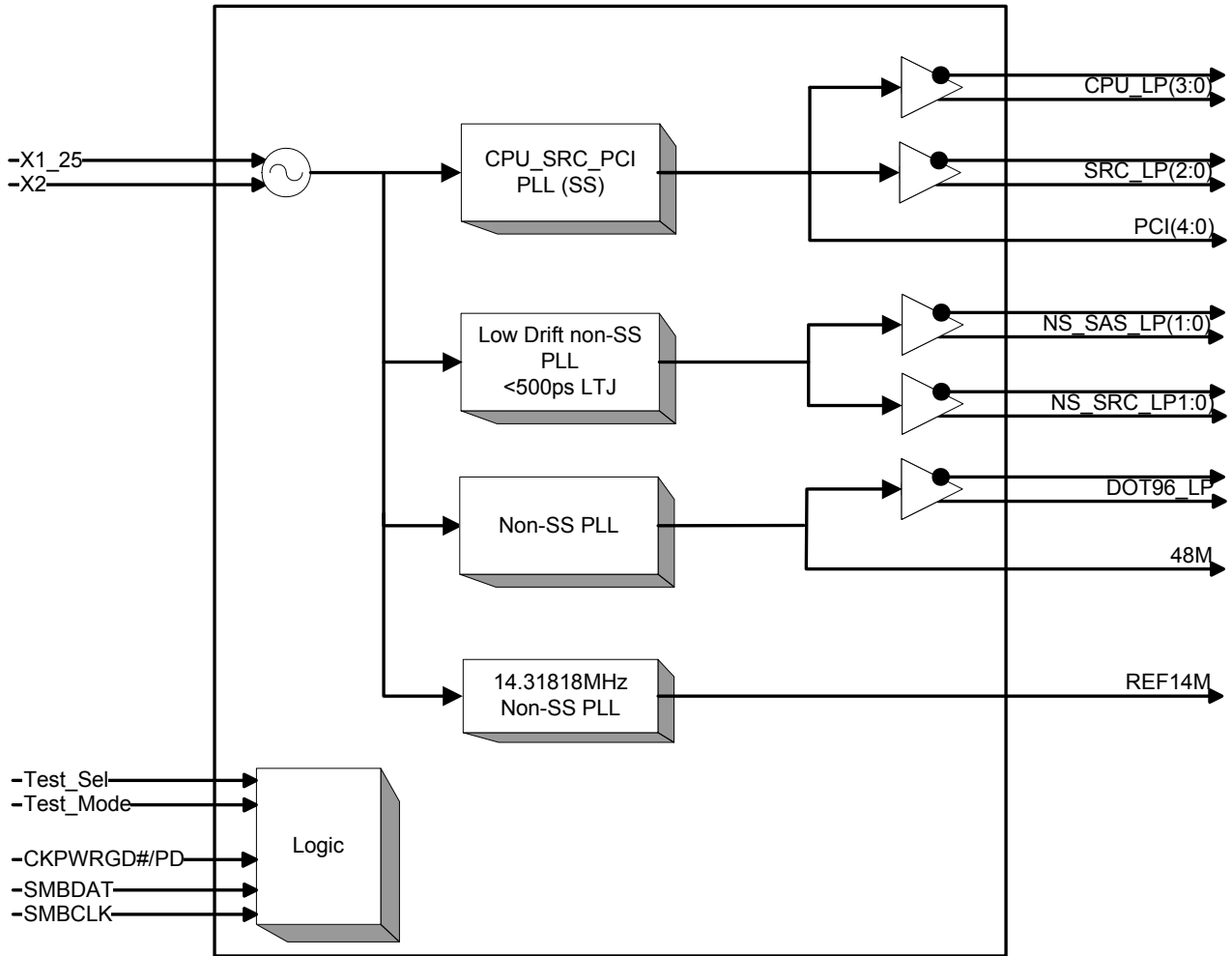
Power Supply and Test Loads

Power Group Pin Numbers

MLF		TSSOP		Description
VDD	GND	VDD	GND	
57	56	3	2	14MHz PLL Analog
58	60	4	6	REF14M Output and Logic
64	61	10	7	25MHz XTAL
2, 9	1, 8	12, 19	11, 18	PCI Outputs and Logic
10	12	20	22	48MHz Output and Logic
16	13	26	23	96MHz PLL Analog, Output and Logic
19, 27	22	29, 37	32	SRC Outputs and Logic
28	29	38	39	SRC PLL Analog
35	36	45	46	Non-Spreading Differential Outputs & Logic
41	42	51	52	NS-SAS/SRC PLL Analog
47, 53	48	57,63	58	CPU Outputs and Logic

Single-ended Output Termination Table

		Rs Value (for each load)	
Output	Loads	Zo = 50	Zo =60
PCI/USB	1	36	43
PCI/USB	2	22	33
REF	1	39	47
REF	2	27	36
REF	3	10	20

Differential Output Termination Table

DIF Zo (Ω)	Rs (Ω)
100	33
85	27

932SQL420 Differential Test Loads
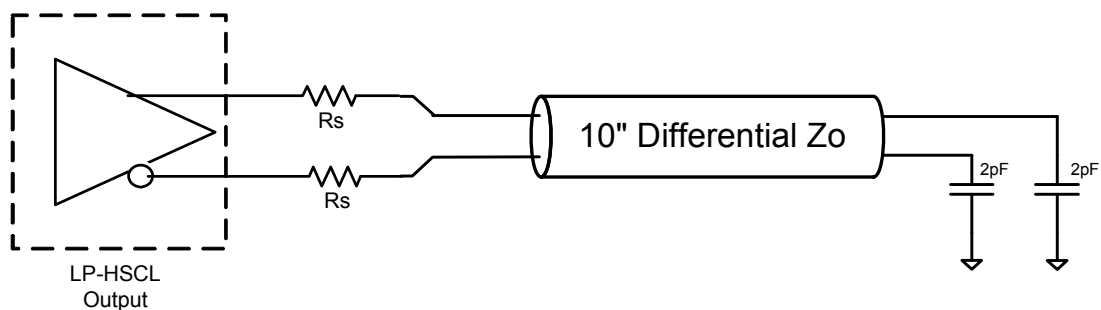
Functionality and CPU SAS Frequency Tables

932SQL420 Functionality

CPU	SRC	PCI	REF	NS_SAS NS_SRC	DOT96	USB	
100	100	33.33	14.318	100.00	96.00	48.00	MHz

Spread Spectrum Control Functionality

SS_Enable (B1b0)	CPU, SRC & PCI
0	OFF
1	-0.50%

932SQL420 Power Down Functionality

CKPWRGD#/PD	Differential Outputs	Single-ended Outputs	Single-ended Outputs w/Latch
1	Low/Low	Low	Low[1]
0	Running		

1. Single-ended outputs with a Latch will be Hi-Z until
the first application of CKPWRGD#.

CPU/SRC/PCI Margining Table

Line	Byte6 Bit2 FS2	Byte6 Bit1 FS1	Byte6 Bit0 FS0	CPU Speed (MHz)	SRC (MHz)	PCI (MHz)
0	0	0	0	97.00	97.00	32.33
1	0	0	1	98.00	98.00	32.67
2	0	1	0	99.00	99.00	33.00
3	0	1	1	100.00	100.00	33.33
4	1	0	0	101.00	101.00	33.67
5	1	0	1	102.00	102.00	34.00
6	1	1	0	103.00	103.00	34.33
7	1	1	1	104.00	104.00	34.67

NS_SAS Margining Table

Line	Byte5 Bit3 FS3	Byte5 Bit2 FS2	Byte5 Bit1 FS1	Byte5 Bit0 FS0	NS_xxx (MHz)
0	0	0	0	0	82.5
1	0	0	0	1	85.0
2	0	0	1	0	87.5
3	0	0	1	1	90.0
4	0	1	0	0	92.5
5	0	1	0	1	95.0
6	0	1	1	0	97.5
7	**0**	**1**	**1**	**1**	100.0
8	1	0	0	0	102.5
9	1	0	0	1	105.0
10	1	0	1	0	107.5
11	1	0	1	1	110.0
12	1	1	0	0	112.5
13	1	1	0	1	115.0
14	1	1	1	0	117.5
15	1	1	1	1	120.0

NOTE: Operation at other than the default entry is not
guaranteed. These values are for margining purposes only.

Clock AC Tolerances

	CPU, SRC	NS_SAS, NS_SRC	PCI	DOT96	48MHz	REF	
PPM tolerance	100	100	100	100	100	100	ppm
Cycle to Cycle Jitter	50	50	500	250	350	1000	ps
Spread	-0.50%	0.00%	-0.50%	0	0.00%	0.00%	%

Clock Periods–Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	100.000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
SRC, NS_SAS, NS_SRC	100.000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
PCI	33.333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2
DOT96	96.000	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2
48MHz	48.000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
REF	14.318	69.78429		69.83429	69.84128	69.84826		69.89826	ns	1,2

Clock Periods–Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2
PCI	33.25	29.49718	29.99718	30.07218	30.07519	30.07820	30.15320	30.65320	ns	1,2
SRC	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information for 932SQL420

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if X$_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N			
			ACK
O		X Byte	
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3$_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
			Beginning Byte N
ACK		X Byte	
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Read Address	Write Address
D3$_{(H)}$	D2$_{(H)}$

NOTE: Pin numbers refer to TSSOP

SMBus Table: Output Enable Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	24/25	DOT96 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 6	50/49	NS_SAS1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 5	48/47	NS_SAS0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 4	44/43	NS_SRC1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 3	42/41	NS_SRC0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 2	36/35	SRC2 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 1	34/33	SRC1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 0	30/31	SRC0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	REF14_3x Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4	62/61	CPU3	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 3	60/59	CPU2	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 2	56/55	CPU1	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 1	54/53	CPU0	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 0	CPU/SRC/ PCI	Spread Spectrum Enable	Spread Off/On	RW	Spread Off	Spread On	0

SMBus Table: Output Enable Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5	13	PCI4 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 4	14	PCI3 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 3	15	PCI2 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 2	16	PCI1 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 1	17	PCI0 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 0	21	48MHz Enable	Output Enable	RW	Disable-Low	Enable	1

SMBus Table: Differential Amplitude Control

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		CPU AMPLITUDE 1	CPU Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 6		CPU AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 5		SRC AMPLITUDE 1	SRC Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 4		SRC AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 3		DOT96 AMPLITUDE 1	DOT96 Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 2		DOT96 AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 1		NS-SAS/SRC AMPLITUDE 1	NS-SAS/SRC Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 0		NS-SAS/SRC AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1

SMBus Table: Spread Amount Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		SS AMOUNT[1]	Spread Amount (note	RW	00= -0.2%	10= -0.4%	1
Bit 0		SS AMOUNT[0]	B1b0 must be set to '1')	RW	01= -0.3%	11= -0.5%	1

SMBus Table: NS_SAS/NS_SRC Frequency Margining Table

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			RESERVED				0
Bit 6			RESERVED				0
Bit 5			RESERVED				0
Bit 4			RESERVED				0
Bit 3	-	FS3	Freq. Sel 3	RW			0
Bit 2	-	FS2	Freq. Sel 2	RW	See NS_SAS/NS_SRC Frequency Table.		1
Bit 1	-	FS1	Freq. Sel 1	RW			1
Bit 0	-	FS0	Freq. Sel 0	RW			1

SMBus Table: Test Mode and CPU/SRC/PCI Frequency Select Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Test Mode	Test Mode Type	RW	Hi-Z	REF/N	0
Bit 6	-	Test Select	Select Test Mode	RW	Disable	Enable	0
Bit 5	-		RESERVED				0
Bit 4	-		RESERVED				1
Bit 3	-		RESERVED				0
Bit 2	-	FS2	Freq. Sel 2	RW	See CPU/SRC/PCI Frequency Select Table		0
Bit 1	-	FS1	Freq. Sel 1	RW			1
Bit 0	-	FS0	Freq. Sel 0	RW			1

Note: Internal Pull up on 100M_133M# pin will result in default CPU frequency of 100 MHz.

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID (1h forB rev)	R	1 for B rev		0
Bit 6	-	RID2		R			0
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			1
Bit 3	-	VID3	VENDOR ID	R	0001 for ICS/IDT		0
Bit 2	-	VID2		R			0
Bit 1	-	VID1		R			0
Bit 0	-	VID0		R			1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is A bytes. (0 to 9		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			0

SMBus Table: Device ID Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DID7	Device ID (42 hex)	R	-	-	0
Bit 6		DID6		R	-	-	1
Bit 5		DID5		R	-	-	0
Bit 4		DID4		R	-	-	0
Bit 3		DID3		R	-	-	0
Bit 2		DID2		R	-	-	0
Bit 1		DID1		R	-	-	1
Bit 0		DID0		R	-	-	0

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 932SQL420. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	$^{\circ}$C	1
Junction Temperature	Tj				125	°C	1
Case Temperature	Tc				110	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, C_L = Full load;			250	mA	1
Powerdown Current	$I_{DD3.3PDZ}$				6	mA	1

[1] Guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics–Differential Current Mode Outputs

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45		55	%	1
Skew, Output to Output	t_{sk3SRC}	Across all SRC outputs, V_T = 50%			50	ps	1
Skew, Output to Output	t_{sk3CPU}	Across all CPU outputs, V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	CPU, SRC, NS_SAS outputs			50	ps	1,3
		DOT96 output			250	ps	1,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Zo=85Ω (differential impedance).

[3] Measured from differential waveform

Electrical Characteristics–Input/Supply/Common Parameters

$T_A = T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Input Frequency	F_i			25.00		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms	1,2
SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.5	33	kHz	1
Tdrive_PD#	t_{DRVPD}	Differential output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

DC Electrical Characteristics–Differential Current Mode Outputs

$T_A = T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1		4	V/ns	1, 2, 3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on			20	%	1, 2, 4
Rise/Fall Time Matching	ΔTrf	Rise/fall matching, Scope averaging off			125	ps	1, 8, 9
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value.			1150	mV	1, 7
Min Voltage	Vmin		-300				1, 7
Vswing	Vswing	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250		550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off			140	mV	1, 6

[1] Guaranteed by design and characterization, not 100% tested in production. Z_O=85Ω (differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than

[7] Includes overshoot and undershoot.

[8] Measured from single-ended waveform

[9] Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics–48MHz

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	20		60	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-29			mA	1
		MAX @V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	29			mA	1
		MAX @ V_{OL} = 0.4 V			27	mA	1
Clock High Time	T_{HIGH}	1.5V	8.094		10.036	ns	1
Clock Low Time	T_{LOW}	1.5V	7.694		9.836	ns	1
Edge Rate	t_{slewr/f_USB}	Rising/Falling edge rate	1		2	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			350	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Electrical Characteristics–Phase Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1			86	ps (p-p)	1,2,3,6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz			3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			3.1	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)			1	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)			0.5	ps (rms)	1,5,7
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)			0.3	ps (rms)	1,5,7
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)			0.2	ps (rms)	1,5,7
	$t_{jphSAS12G}$	SAS 12G			1.3	ps (rms)	1,5,8

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

[6] Applied to SRC outputs

[7] Applies to CPU outputs

[8] Applies to NS_SAS, NS_SRC outputs, Spread Off

Electrical Characteristics–PCI

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	V_O = V_{DD}*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-33			mA	1
		MAX @V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	30			mA	1
		MAX @ V_{OL} = 0.4 V			38	mA	1
Clock High Time	T_{HIGH}	1.5V	12			ns	1
Clock Low Time	T_{LOW}	1.5V	12			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Electrical Characteristics–REF

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	MIN @V_{OH} = 1.0 V	-33			mA	1
		MAX @V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	MIN @V_{OL} = 1.95 V	30			mA	1
		MAX @ V_{OL} = 0.4 V			38	mA	1
Clock High Time	T_{HIGH}	1.5V	27.5			ns	1
Clock Low Time	T_{LOW}	1.5V	27.5			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Test Clarification Table

| Comments	HW		SW		
	TEST_SEL HW PIN	TEST_MODE HW PIN	TEST ENTRY BIT B6b6	REF/N or HI-Z B6b7	OUTPUT
	0	X	0	X	NORMAL
Power-up w/ TEST_SEL = 1 (>2.0V) to enter test mode. Cycle power to disable test mode.	1	0	X	0	HI-Z
	1	0	X	1	REF/N
	1	1	X	0	REF/N
	1	1	X	1	REF/N
	0	X	1	0	HI-Z
If TEST_SEL HW pin is 0 during power-up, test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N FS_B/TEST_Mode pin is not used. Cycle power to disable test mode.	0	X	1	1	REF/N

B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)
B6b7: 1= REF/N, Default = 0 (HI-Z)

Package Outline and Package Dimensions (64-pin TSSOP)
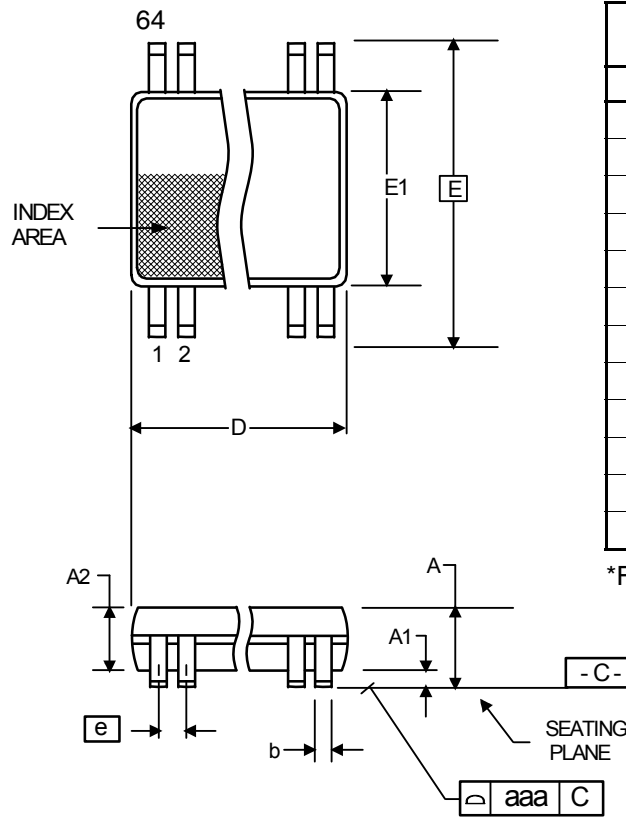
	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	–	1.20	–	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	0.32	0.41
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	16.90	17.10	.665	.673
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
aaa	–	0.10	–	.004
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.
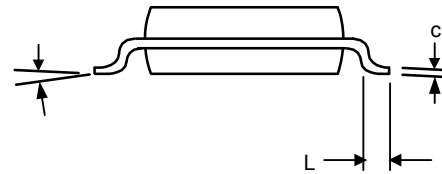
Package Outline and Package Dimensions (64-pin MLF)
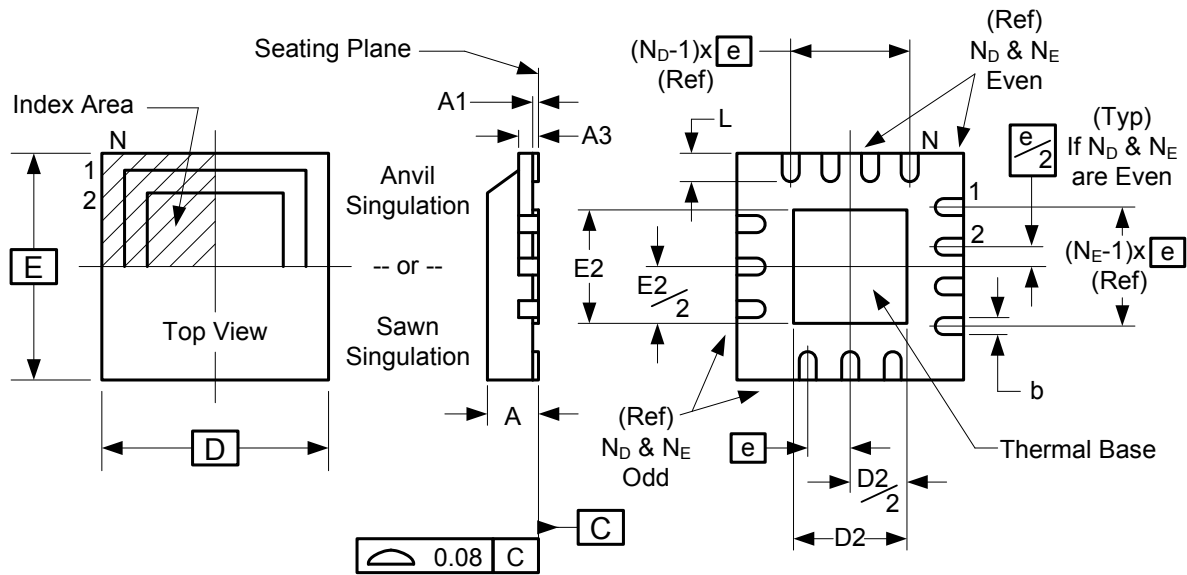
Symbol	Millimeters	
	Min	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	9.00 x 9.00	
D2 MIN./MAX.	6.00	6.25
E2 MIN./MAX.	6.00	6.25
L MIN./MAX.	0.30	0.50
N	64	
N_D	16	
N_E	16	

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
932SQL420BGLF	Tubes	64-pin TSSOP	0 to +70° C
932SQL420BGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C
932SQL420BKLF	Tray	64-pin MLF	0 to +70° C
932SQL420BKLFT	Tape and Reel	64-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate with the datasheet revision).

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

Rev.	Issue Date	Who	Description	Page #
0.1	4/26/2010	RDW	Initial Release	-
0.2	6/3/2010	RDW	Updated block diagram to remove the IREF resistor.	
0.3	10/24/2011	RDW	1. Updated power management table for Low Power Outputs (LPO) 2. Updated SMBus for LPO disabled state 3. Updated electrical tables with latest CK420BQ tables.	Various
0.4	12/5/2011	RDW	1. Updated frequency tables to match AP336 PLL programming 2. Added dif output amplitude control to Byte 3 3. Updated bytes 5 and 6 to reflect new frequency tables. 4. Updated bytes 11-45 to reflect PLL control registers and test bytes.	Various
0.5	1/19/2012	RDW	1. Updated CPU/SRC/PCI Margining Table 2. Updated NS_SAS Margining Table 3. Updated Current Consumption Table 4. Updated General Description and Output Features Table	Various
0.6	3/27/2012	RDW	1. Updated ordering information to B rev 2. Updated Rev ID in SMBus to reflect this.	Various
0.7	4/16/2012	RDW	1. Removed support for 133M on CPU a. 48M output becomes Output only and not latched b. B6[4] is now reserved and has default value of '1'. c. CPU frequency table now reduced to 8 entries. 2. DOT96 and NS_SAS/SRC amplitude bit are swapped to match A rev silicon (B3[3:2] and B2[1:0]) 3. 4 selectable spread amounts are added with control bits in B4[1:0]. i. See these bits for definition. 4. Differential output test loads now indicate Rs instead of specific value to allow for 100ohm or 85ohm terminations.	Various
0.8	6/20/2012	RDW	1. Updated Vendor ID/Revision ID byte from 0000 0001 to 0001 0001 2. Updated ordering information from AGLF/AKLF to BGLF/BKLF	Various

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
www.idt.com/go/clockhelp
pcclockhelp@idt.com

Corporate Headquarters
Integrated Device Technology, Inc.
www.idt.com