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FDG410NZ

Single N-Channel PowerTrench® MOSFET

20 V, 2.2 A, 70 mΩ

Features

- Max $r_{DS(on)}$ = 70 mΩ at $V_{GS} = 4.5$ V, $I_D = 2.2$ A
- Max $r_{DS(on)}$ = 77 mΩ at $V_{GS} = 2.5$ V, $I_D = 2.0$ A
- Max $r_{DS(on)}$ = 87 mΩ at $V_{GS} = 1.8$ V, $I_D = 1.8$ A
- Max $r_{DS(on)}$ = 115 mΩ at $V_{GS} = 1.5$ V, $I_D = 1.5$ A
- HBM ESD protection level > 2 kV (Note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Fast switching speed
- Low gate charge
- RoHS Compliant

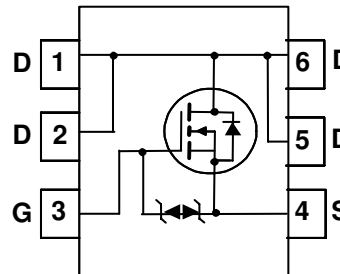
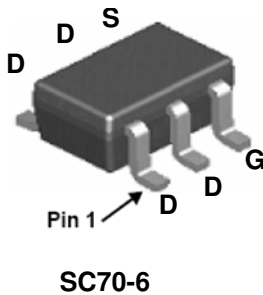


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low $r_{DS(on)}$ and gate charge (Q_g) in a small package.

Applications

- DC/DC converter
- Power management
- Load switch



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	2.2
	-Pulsed		6.0
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	0.42
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.38
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	300	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	333	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.41	FDG410NZ	SC70-6	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		17		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}$		50	70	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 2.0\text{ A}$		56	77	
		$V_{GS} = 1.8\text{ V}, I_D = 1.8\text{ A}$		67	87	
		$V_{GS} = 1.5\text{ V}, I_D = 1.5\text{ A}$		83	115	
		$V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$		71	100	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 2.2\text{ A}$		11		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		400	535	pF
C_{oss}	Output Capacitance			70	95	pF
C_{rss}	Reverse Transfer Capacitance			45	70	pF
R_g	Gate Resistance			2.8		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 2.2\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		5.3	11	ns
t_r	Rise Time			2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			2.3	10	ns
Q_g	Total Gate Charge		$V_{GS} = 4.5\text{ V}, V_{DD} = 10\text{ V}, I_D = 2.2\text{ A}$		5.1	7.2
Q_{gs}	Gate to Source Charge			0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.0		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain-Source Diode Forward Current			0.35	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.35\text{ A}$ (Note 2)		0.6	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 2.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		11	20	ns
Q_{rr}	Reverse Recovery Charge			2.5	10	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. $300\text{ }^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $333\text{ }^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

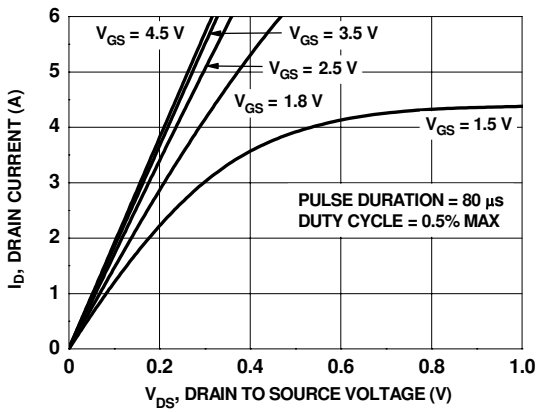


Figure 1. On Region Characteristics

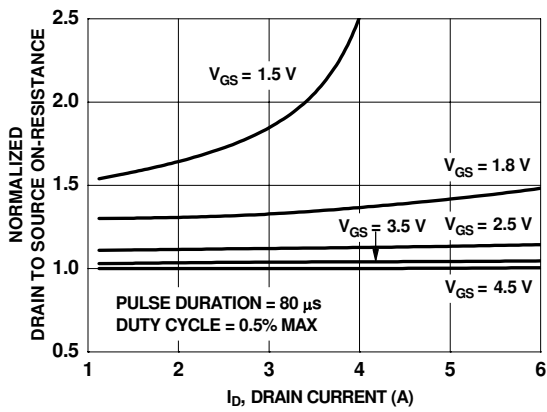


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

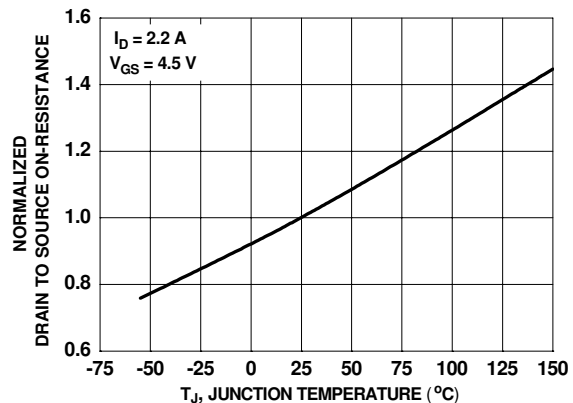


Figure 3. Normalized On Resistance vs Junction Temperature

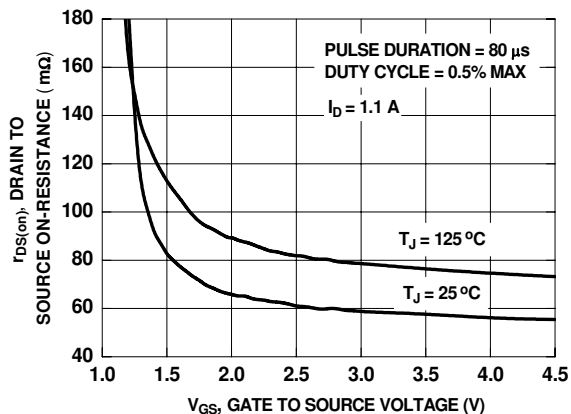


Figure 4. On-Resistance vs Gate to Source Voltage

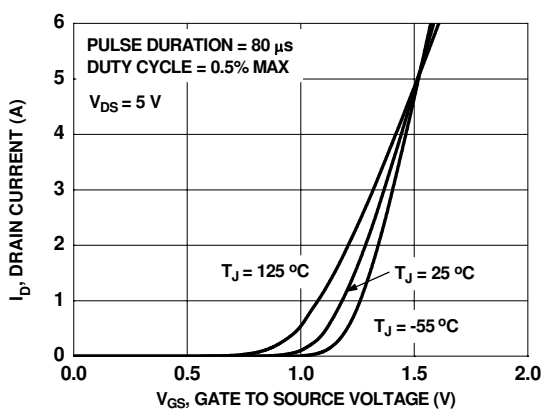


Figure 5. Transfer Characteristics

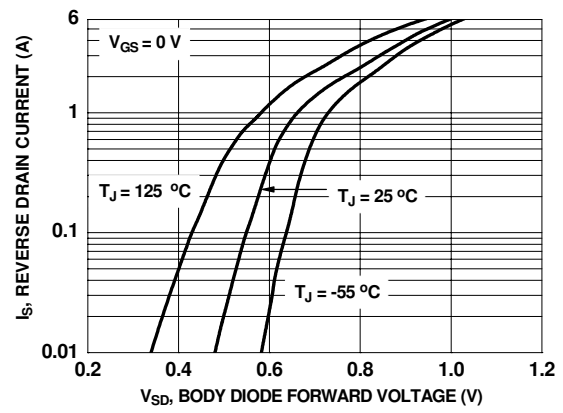


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

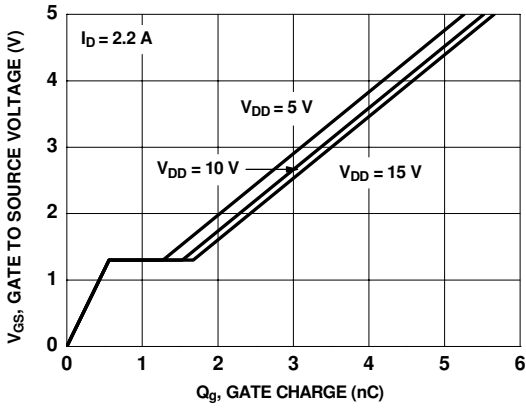


Figure 7. Gate Charge Characteristics

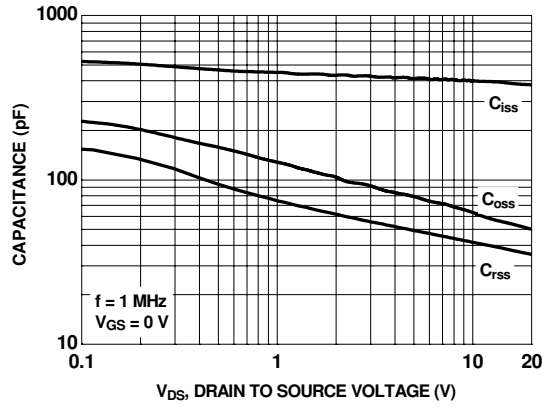


Figure 8. Capacitance vs Drain to Source Voltage

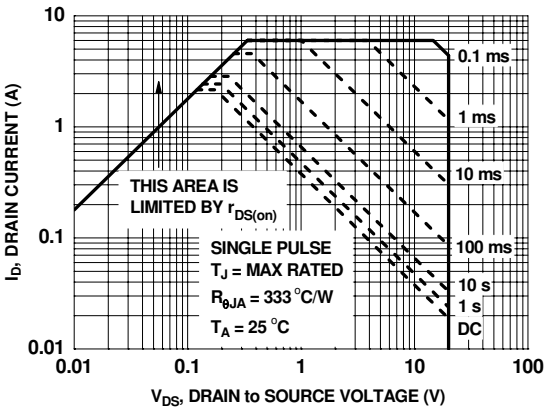


Figure 9. Forward Bias Safe Operating Area

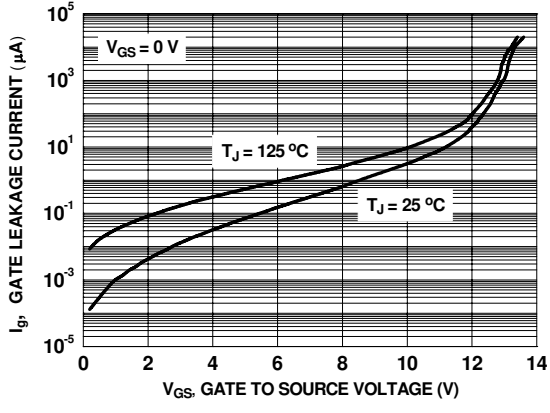


Figure 10. Gate Leakage Current vs Gate to Source Voltage

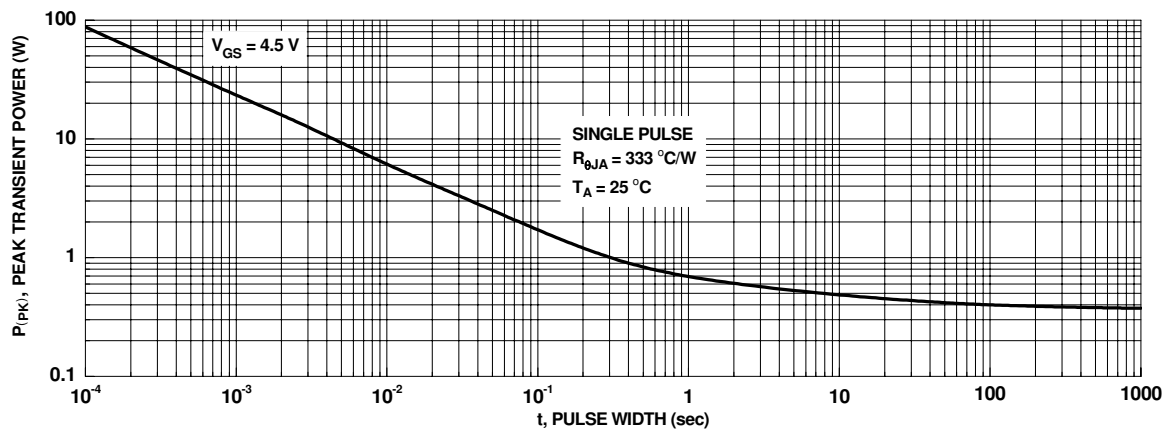
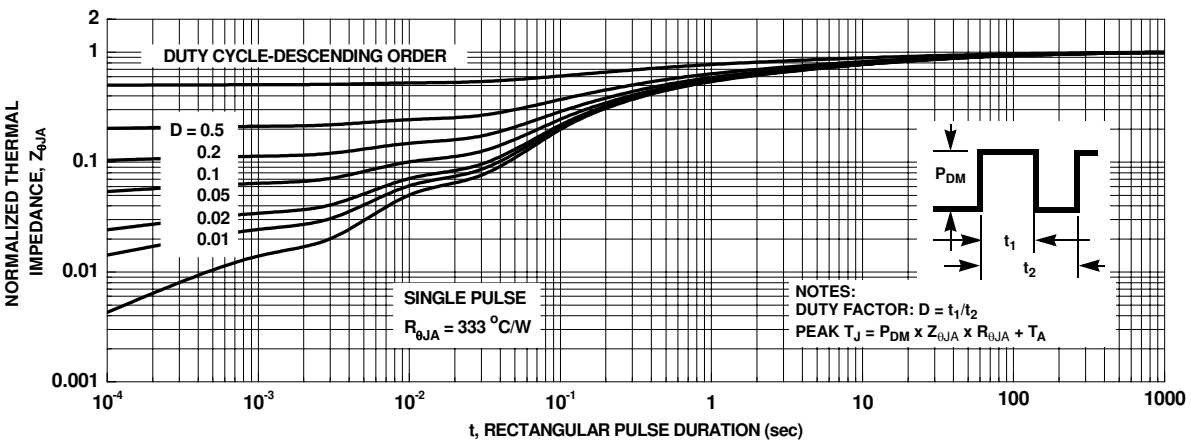
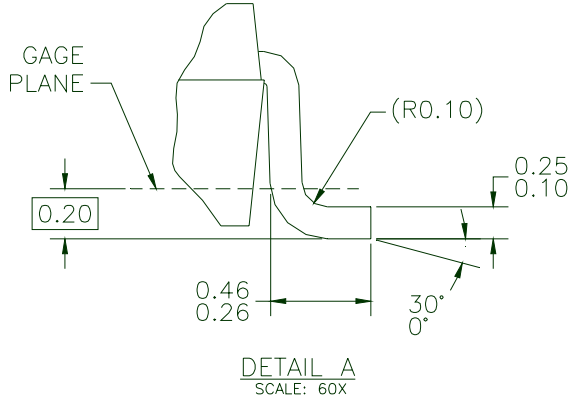
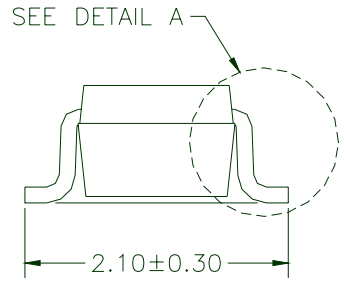
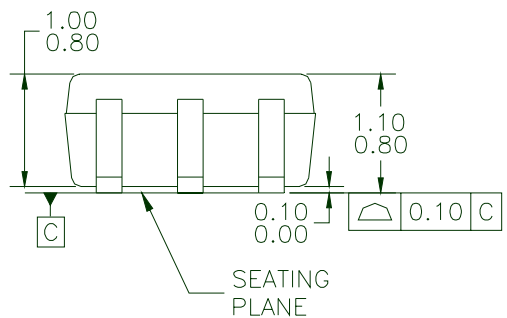
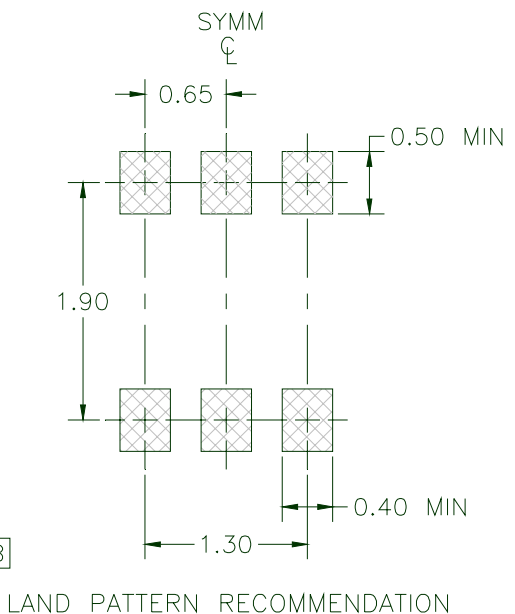
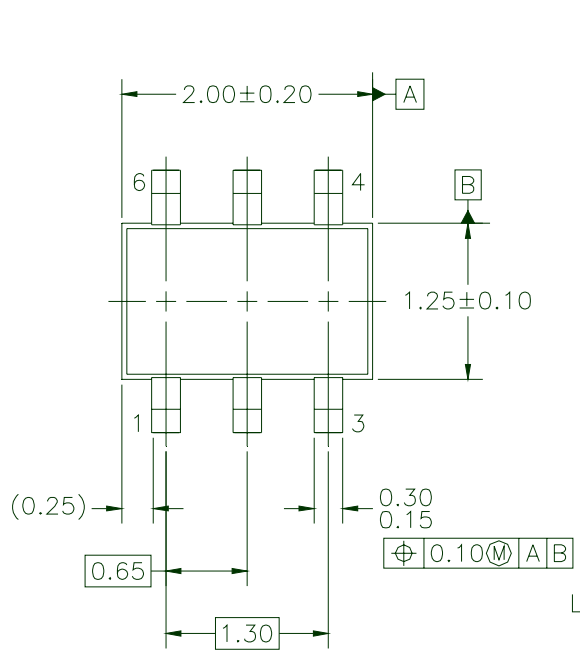


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted



Dimensional Outline and Pad Layout








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 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

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