

TOSHIBA Diode Silicon Epitaxial Planar Type

HN2D01JE

Ultra High Speed Switching Application

- The HN2D01JE is composed of 2 independent diodes.
- Low forward voltage : $V_F(3) = 0.98V$ (typ.)
- Fast reverse recovery time : $t_{rr} = 1.6ns$ (typ.)
- Small total capacitance : $C_T = 0.5pF$ (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ C$) (Note)

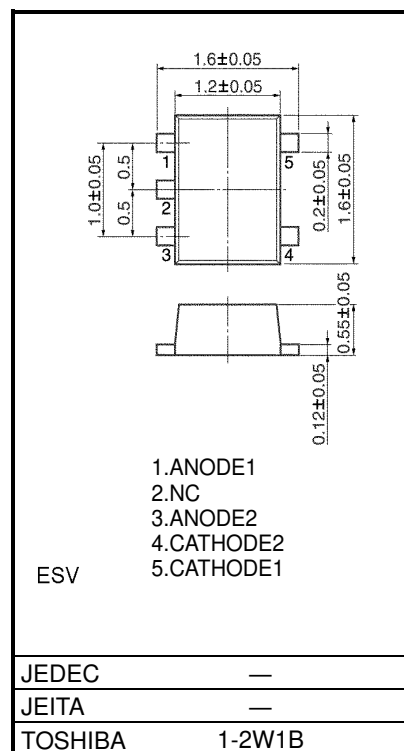
Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current (Notre1)	I_{FM}	200	mA
Average forward current (Notre1)	I_O	100	mA
Surge current (10ms) (Notre1)	I_{FSM}	1	A
Power dissipation (Notre2)	P	100	mW
Junction temperature	T_j	150	$^\circ C$
Storage temperature	T_{stg}	-55 to 150	$^\circ C$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Notre1: Unit rating; total rating = unit rating \times 1.5

Notre2: Total rating.

Unit: mm



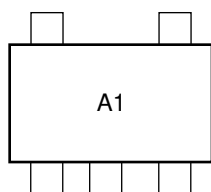
Weight: 0.003 g (typ.)

Electrical Characteristics ($T_a = 25^\circ C$)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	$I_F = 1mA$	—	0.62	—	V
	$V_F(2)$	$I_F = 10mA$	—	0.75	—	
	$V_F(3)$	$I_F = 100mA$	—	0.98	1.20	
Reverse current	$I_R(1)$	$V_R = 30V$	—	—	0.1	μA
	$I_R(2)$	$V_R = 80V$	—	—	0.5	
Total capacitance	C_T	$V_R = 0V, f = 1MHz$	—	0.5	—	pF
Reverse recovery time	t_{rr}	$I_F = 10mA$ (Fig.1)	—	1.6	—	ns

Start of commercial production
2001-10

Marking



Pin Assignment (Top View)

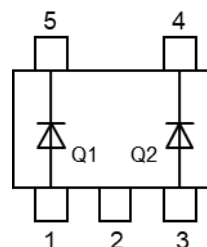
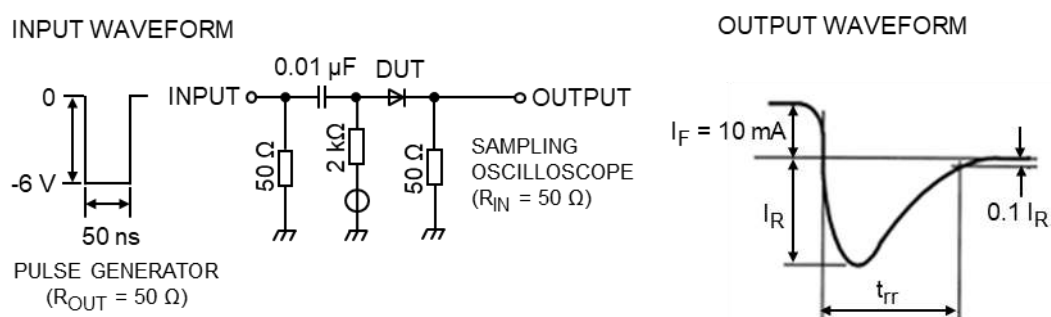
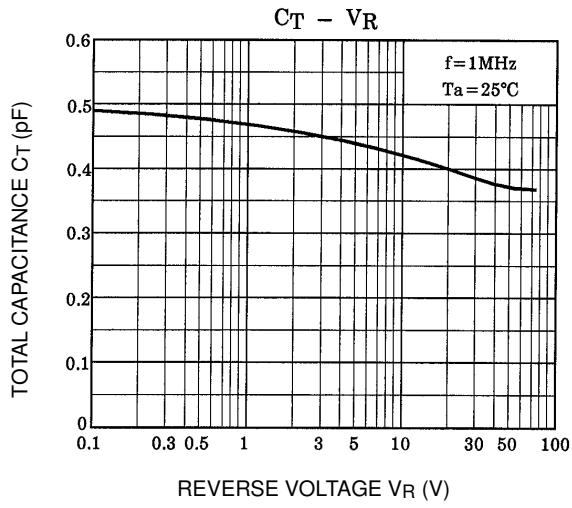
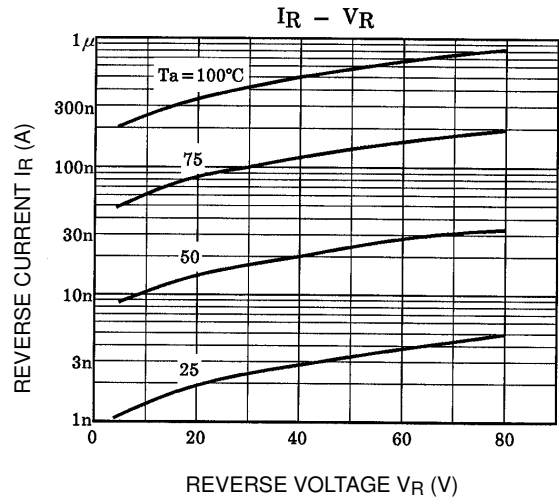
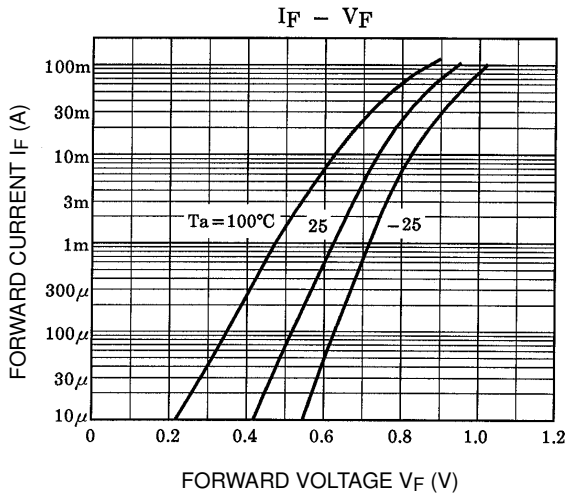


Fig. 1 Reverse Recovery Time (t_{rr}) Test Circuit





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