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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1909

SWITCHING REGULATOR CONTROL IC

DESCRIPTION

The μPC1909 is a switching regulator control IC ideal for primary side control of active-clamp type[Note] DC/DC converters. This IC has 2 outputs employing a totem-pole circuit with peak output current 1.2 A, and is capable of directly driving a power MOS FET. As a result, it has been possible to realize primary side control of an active-clamp type converter on a single chip.

Note It is necessary to obtain license from Vicor Corporation before using the μPC1909 in an active-clamp type circuit.

FEATURES

- 2 on-chip outputs; for Q and $\overline{Q}$
- Capable of directly driving a power MOS FET
- Drive supply voltage range: 7 to 24 V
- On-chip remote control circuit
- On-chip pulse-by-pulse overcurrent protection circuit
- On-chip overvoltage latch circuit

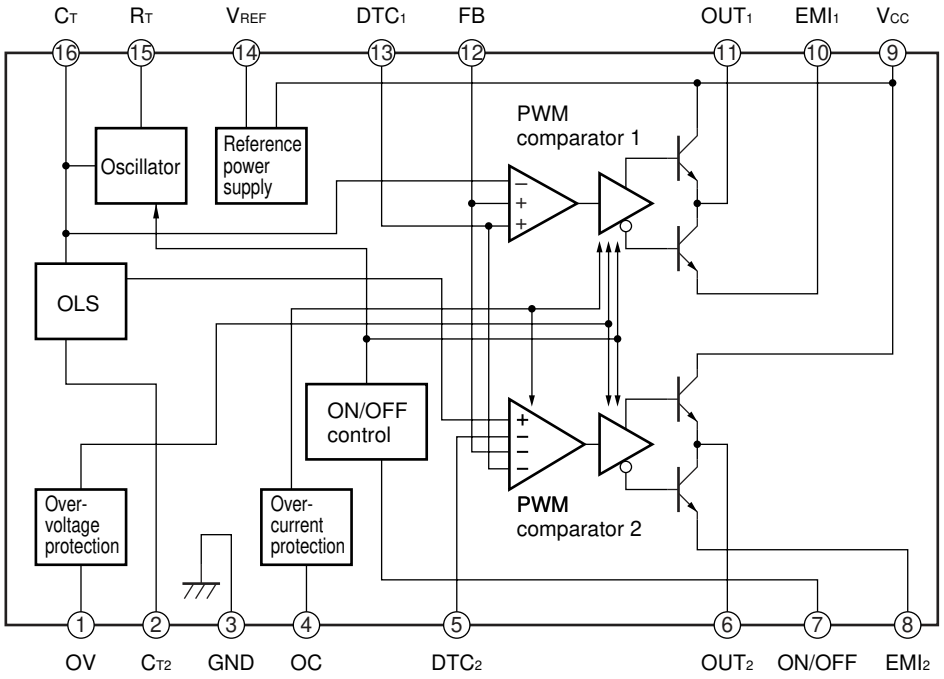
ORDERING INFORMATION

Part Number	Package
μPC1909CX	16-pin plastic DIP (7.62 mm (300))
μPC1909GS	16-pin plastic SOP (7.62 mm (300))

Document No. G14309EJ2V0DS00 (2nd edition)
Date Published November 2000 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

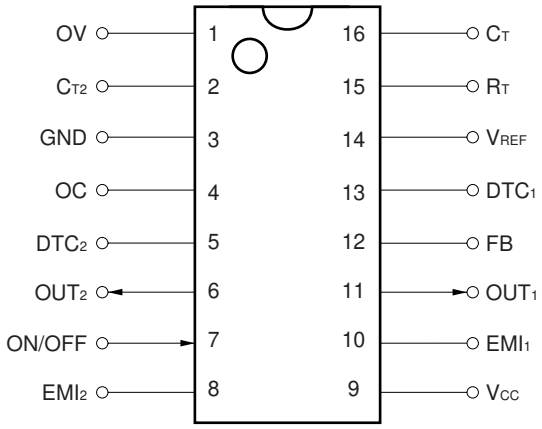
★ BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

16-pin plastic DIP (7.62 mm (300))
μPC1909CX

16-pin plastic SOP (7.62 mm (300))
μPC1909GS



★ **Pin Name**

C_T	: Timing Capacitance
C_{T2}	: OLS Shift Control
DTC_1	: OUT_1 Dead Time Control
DTC_2	: OUT_2 Dead Time Control
EMI_1	: OUT_1 Emitter
EMI_2	: OUT_2 Emitter
FB	: Feedback Input
GND	: Ground
OC	: Over Current Protection
ON/OFF	: ON/OFF Control
OUT_1	: OUT_1 Output
OUT_2	: OUT_2 Output
OV	: Over Voltage Protection
R_T	: Timing Resistance
V_{CC}	: Power Supply
V_{REF}	: Reference Voltage

CONTENTS

★ 1. PIN FUNCTION LIST

Pin No.	Symbol	Function
1	OV	Overvoltage protection This is the input pin of the overvoltage detection comparator. Directly connect this pin to GND when not used.
2	C_{T2}	OLS shift setting The resistor that determines the amount of level shift for dC_T (an internal triangle wave that is a level-shifted C_T) is connected between this pin and the V_{REF} pin.
3	GND	Ground This is the signal ground pin.
4	OC	Overcurrent protection This is the input pin of the overcurrent detection comparator. Directly connect this pin to GND when not used.
5	DTC_2	OUT_2 dead time setting This pins sets the dead time of the OUT_2 output.
6	OUT_2	OUT_2 output This is the subswitch drive output pin.
7	ON/OFF	ON/OFF control The output circuit can be switched on or off by inputting an external signal. Directly connect this pin to V_{REF} when not used.
8	EMI_2	OUT_2 emitter This is a power supply ground pin. This pin must be isolated from the signal ground pin (GND).
9	V_{CC}	Power supply
10	EMI_1	OUT_1 emitter This is a power supply ground pin. This pin must be isolated from the signal ground pin (GND).
11	OUT_1	OUT_1 output This is the main switch drive output pin.
12	FB	Feedback input This is the feedback input pin of PWM comparators 1 and 2.
13	DTC_1	OUT_1 dead time setting This pin sets the maximum duty of the OUT_1 output and determines the minimum duty of the OUT_2 output.
14	V_{REF}	Reference voltage This pin outputs a 4.9-V TYP. reference voltage.
15	R_T	Timing resistance The resistor that determines the oscillation frequency is connected between this pin and GND.
16	C_T	Timing capacitance The capacitor that determines the oscillation frequency is connected between this pin and GND. This pin outputs a triangle wave.

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	μPC1909CX	μPC1909GS	Unit
Power Supply Voltage	V_{CC}	26		V
Output Current (DC, per output)	$I_{C\ (DC)}$	100		mA
Output Current (peak, per output)	$I_{C\ (peak)}$	1.2		A
Total Power Dissipation	P_T	1000	694	mW
Operating Ambient Temperature	T_A	−20 to +85		°C
Operating Junction Temperature	T_J	−20 to +150		°C
Storage Temperature	T_{stg}	−55 to +150		°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V_{CC}	7	10	24	V
Oscillation Frequency	f_{OSC}	50	200	500	kHz
Output Load Capacitance	C_L		2200	3000	pF
★ Timing Resistance	R_T	10			kΩ
Operating Junction Temperature	T_J	−20		+100	°C

★ Caution The recommended operating range may be exceeded without causing any problems provided that the absolute maximum ratings are not exceeded. However, if the device is operated in a way that exceeds the recommended operating conditions, the margin between the actual conditions of use and the absolute maximum ratings is small, and therefore thorough evaluation is necessary. The recommended operating conditions do not imply that the device can be used with all values at their maximum values.

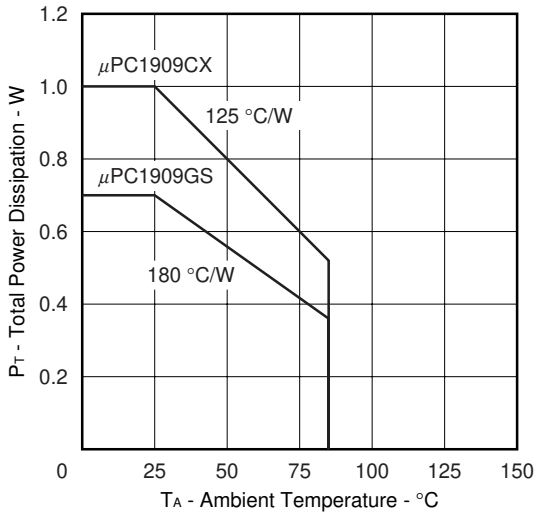
Electrical Characteristics (Unless otherwise specified, T_A = 25°C, V_{CC} = 10 V, R_T = 10 kΩ, fosc = 200 kHz)

Block	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Total	Standby Current	$I_{CC\ (SB)}$	V_{CC} = 7 V		0.1		mA
	Circuit Current	I_{CC}	Without load	6	12	18	mA
Under-Voltage Lockout Circuit	Startup Threshold Voltage	$V_{CC\ (L\ to\ H)}$		8	9	10	V
	Operating Voltage Hysteresis Width	V_H		3	4	5	V
Reference Voltage	Output Voltage	V_{REF}	I_{REF} = 0 A	4.7	4.9	5.1	V
	Line Regulation	REG_{IN}	8 V ≤ V_{CC} ≤ 15 V, I_{REF} = 0 A		1	10	mV
	Load Regulation	REG_L	1 mA ≤ I_{REF} ≤ 4 mA		6	12	mV
	Output Voltage Temperature Coefficient	$\Delta V_{REF}/\Delta T$	−10°C ≤ T_A ≤ +85°C, I_{REF} = 0 A		400	(700)	μV/°C
	Short Circuit Current	$I_{O\ short}$	I_{REF} = 0 A		15		mA
Oscillation	Oscillation Frequency	f_{OSC}		180	200	220	kHz
	Frequency Line Regulation	$\Delta f/\Delta V$	8 V ≤ V_{CC} ≤ 15 V		1		%
	Frequency Temperature Coefficient	$\Delta f/\Delta T$	−10°C ≤ T_A ≤ +85°C		2	(5)	%
PWM Comparator	Input Bias Current	$I_{B\ (COMP1)}$	V_{COMP1} = V_{REF}			10	μA
		$I_{B\ (COMP2)}$	V_{COMP2} = V_{REF}			10	μA
	Low-level Threshold Voltage	$V_{TH\ (L)}$			1.5		V
	High-level Threshold Voltage	$V_{TH\ (H)}$			3.5		V
	Dead time Temperature Coeficient	$\Delta DT/\Delta T$	−10°C ≤ T_A ≤ +85°C, V_D = 0.46 V_{REF}		3		%
Output	Low-level Output Voltage	V_{OL}	I_{SINK} = 3 mA			0.5	V
	High-level Output Voltage	V_{OH}	I_{SOURCE} = 30 mA		V_{CC} − 1.6		V
	Rise Time	t_r	R_L = 15 Ω, C_L = 2200 pF		60		ns
	Fall Time	t_f	R_L = 15 Ω, C_L = 2200 pF		40		ns
Remote Control	Input Voltage at Output ON	$V_{IN\ (ON)}$		2.4	2.6	2.8	V
	Input Voltage at Output OFF	$V_{IN\ (OFF)}$		2.2	2.4	2.6	V
	Hysteresis Width	V_H		0.1	0.2	0.3	V
Overcurrent Latch	Overcurrent Threshold Voltage	$V_{TH\ (OC)}$		190	210	230	mV
	Input Bias Current	$I_{B\ (OC)}$	V_{CC} = 0 V		200		μA
	Delay to Output	$t_{d\ (OC)}$			150		ns
Overvoltage Latch	Overvoltage Threshold Voltage	$V_{TH\ (OV)}$		2	2.4	2.8	V
	Input Bias Current	$I_{B\ (OV)}$	V_{OV} = V_{REF}			4	μA
	OVL Reset Voltage	$V_{R\ (OV)}$			2		V
	Delay to Output	$t_{d\ (OV)}$			750		ns

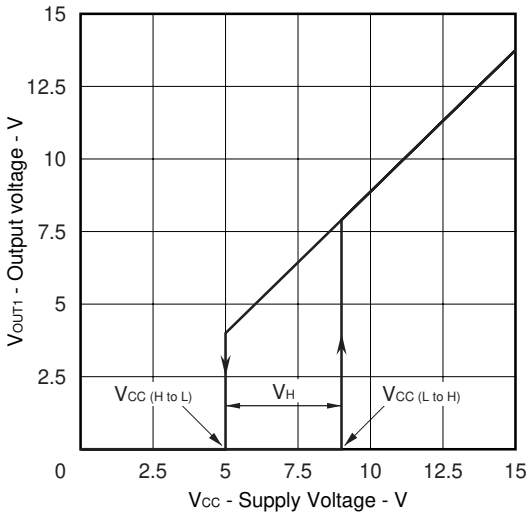
Remark Values in parentheses ( ) represent reference values.

Typical Characteristics Curves (Unless otherwise specified, T_A = 25°C, V_{CC} = 10 V, Reference Values)

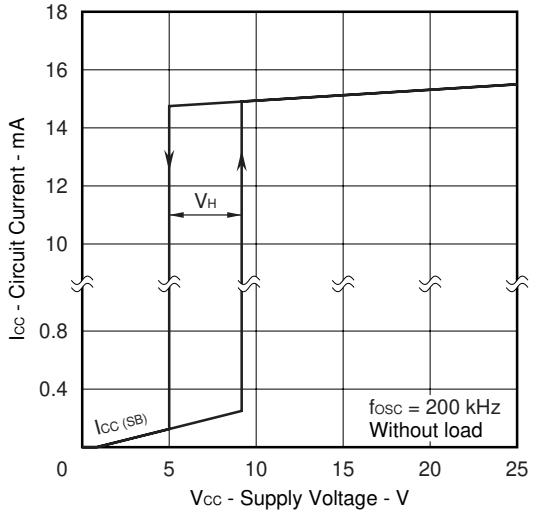
P_T vs. T_A



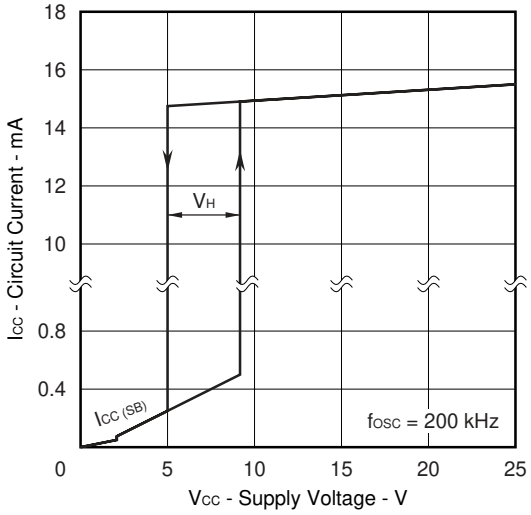
Under-Voltage Lockout Circuit



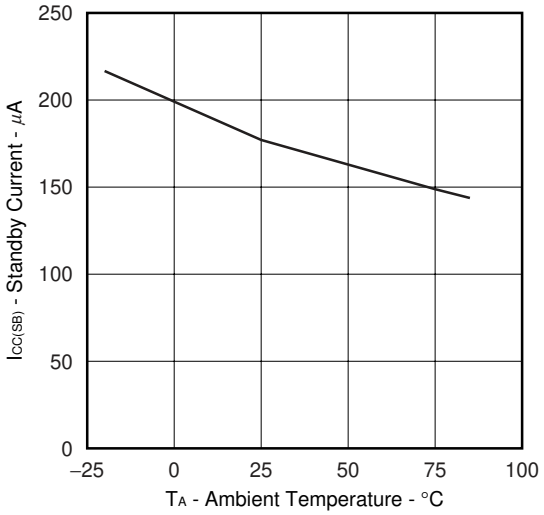
I_{CC} vs. V_{CC}



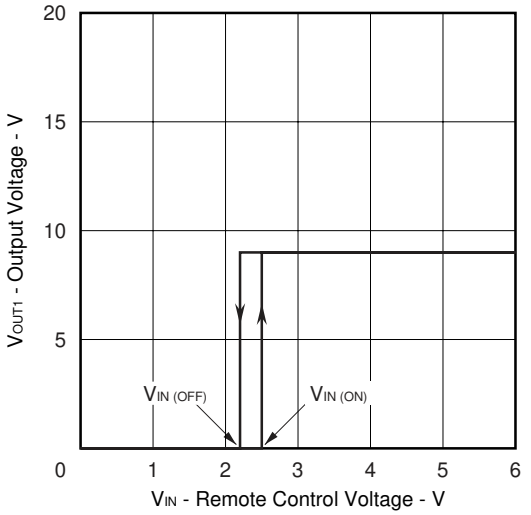
I_{CC} vs. V_{CC} (During OVL Operation)



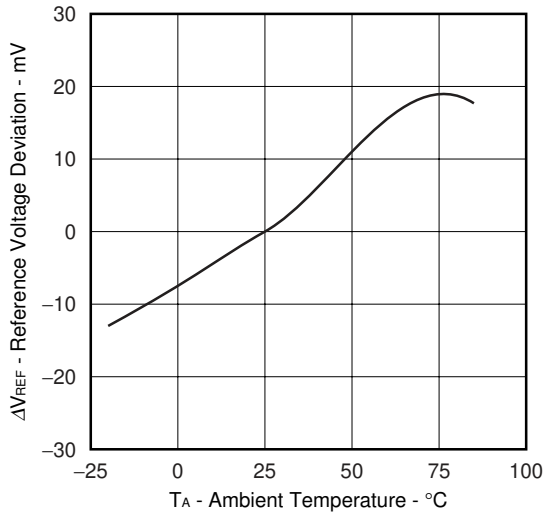
$I_{CC(SB)}$ vs. T_A



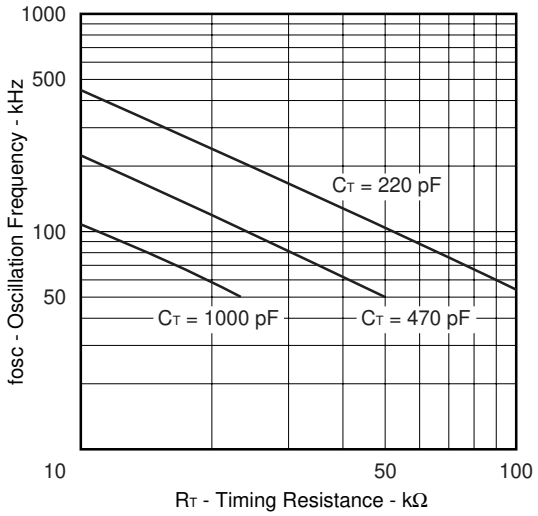
V_{OUT1} vs. V_{IN}



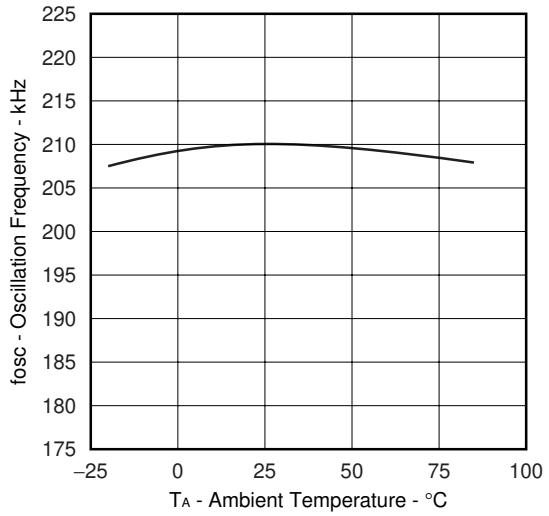
ΔVREF vs. TA



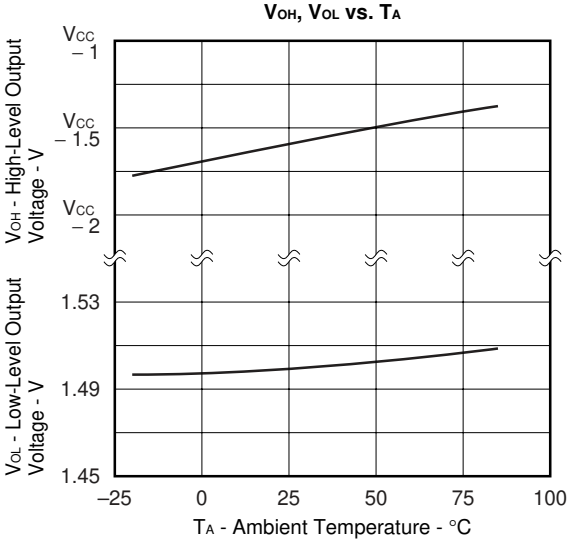
fosc vs. RT, CT



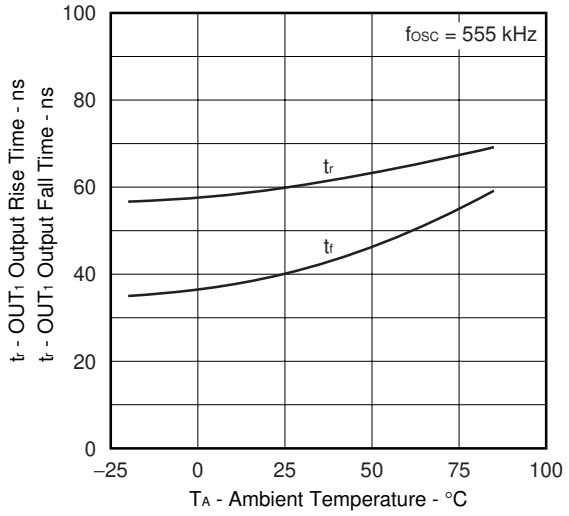
fosc vs. TA



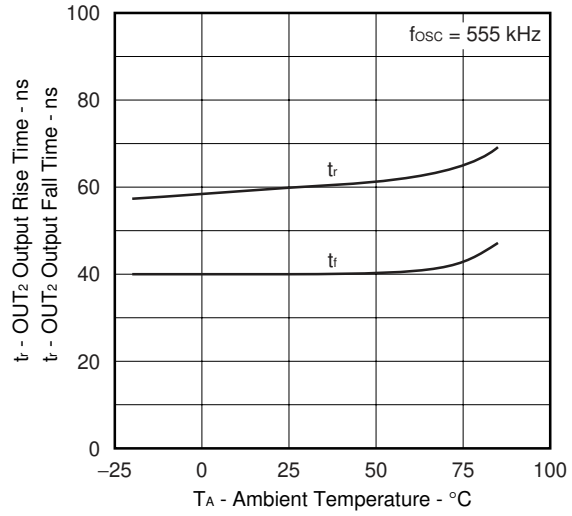
VOH, VOL vs. TA

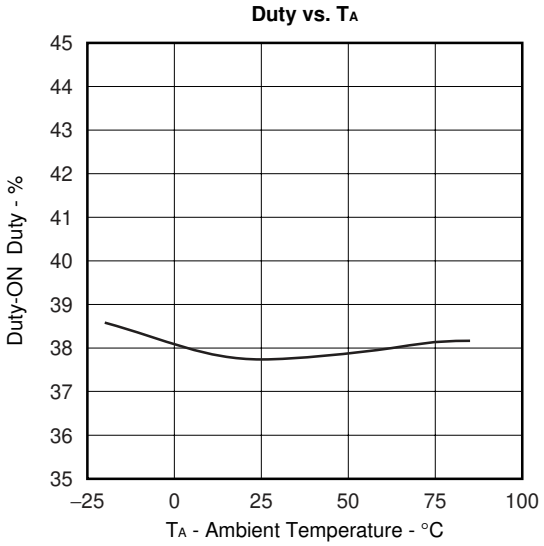


tf, tr vs. TA (OUT1)



tf, tr vs. TA (OUT2)




Duty vs. TA
45
44
43
42
41
40
39
38
37
36
35
Duty-ON Duty - %
–25
0
25
50
75
100
TA - Ambient Temperature - °C

★ 3. OPERATION OVERVIEW

3.1 Startup

The operating waveforms at startup are shown in Figure 3-1 below. The operations at startup are as follows.

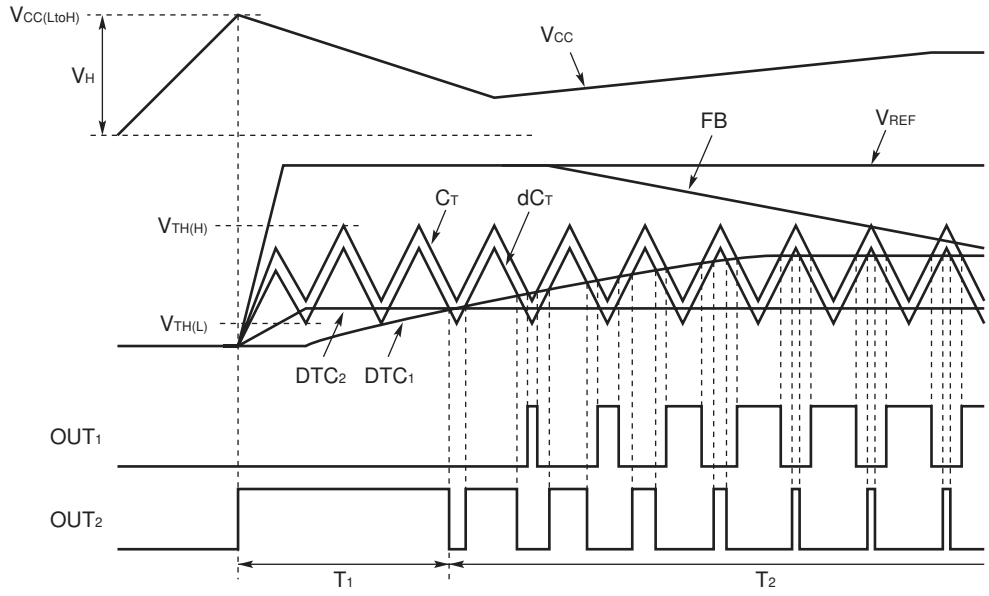
<1> When the power supply voltage (V_{CC}) rises and exceeds the starting voltage ($V_{CC(L\ to\ H)}$), the reference voltage (V_{REF}) rises.

<2> The DTC_1 voltage is boosted as the soft start capacitor is charged (refer to **4.5.3 Soft start**).

<3> Because the DTC_1 voltage is at a lower potential than other voltages, OUT_1 and OUT_2 become low and high level respectively during the T_1 period.

<4> If the DTC_1 voltage is further boosted so that there is a period in which it is higher than the dC_T voltage in the T_2 period, OUT_2 becomes low level. In the period in which the DTC_1 voltage exceeds C_T, OUT_1 and OUT_2 are high and low level respectively. The duty of OUT_1 increases and that of OUT_2 decreases as DTC_1 is boosted.

Figure 3-1. Waveforms at Startup



Signal Name	Function	Signal Name	Function
OUT_1	Output for main switch	OUT_2	Output for subswitch
DTC_1	Voltage for setting maximum duty limit of OUT_1	DTC_2	Voltage for setting maximum duty limit of OUT_2
FB	Feedback voltage of converter output	C_T	Triangle wave generated by oscillator
dC_T	Triangle wave that is C_T level-shifted via the level shift circuit (OLS)		

Remarks 1. The oscillation frequency of C_T is determined by the external capacitor connected to the C_T pin and the external resistor connected to the R_T pin (refer to **3.3 Overcurrent Limitation Operation**). C_T is a symmetrical triangle wave with a trough voltage (low-level threshold voltage $V_{TH(L)}$) of 1.5 V and a crest voltage (high-level threshold voltage $V_{TH(H)}$) of 3.5 V. Note that the dC_T voltage cannot be viewed externally.

2. In the T_1 and T_2 periods in Figure 3-1, the FB voltage level rises as the converter output voltage is boosted, with the result that the converter voltage cannot be controlled by FB.

3.2 Steady Operation

The operating waveforms during steady operation are shown in Figure 3-2 below. Steady operation as used here refers to the state in which the overcurrent and overvoltage latches are not working. The operations that occur during steady operation are as follows.

<1> When the converter is operating at the rated input and output, the FB voltage is between DTC_1 and DTC_2 (in the T_3 period in Figure 3-2).

- The FB voltage and C_T triangle wave are compared by PWM comparator 1. OUT_1 is high level when the FB voltage is higher than the C_T voltage.
- The FB voltage and level-shifted dC_T triangle wave are compared by PWM comparator 2. OUT_2 is high level when the FB voltage is lower than the dC_T voltage.

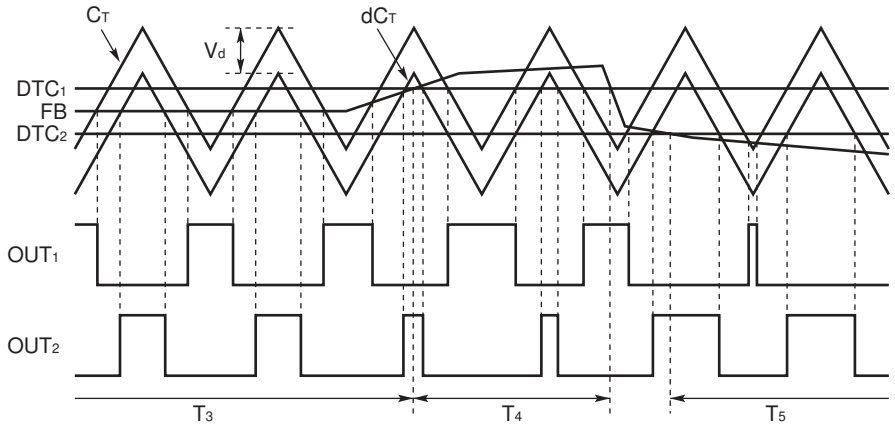
<2> Because the input voltage becomes lower as the load of the converter is increased, there is a period when the FB voltage rises and the OUT_1 duty increases (the T_4 period in Figure 3-2).

When the FB voltage is greater than the DTC_1 voltage, OUT_1 operates at the maximum duty determined by DTC_1. At this time also, OUT_2 operates at the minimum duty determined by DTC_1.

<3> Because the input voltage becomes higher as the load of the converter is decreased, there is a period when the FB voltage falls and the OUT_1 duty decreases (the T_5 period in Figure 3-2).

When the FB voltage is less than the DTC_2 voltage, OUT_2 operates at the maximum duty determined by DTC_2.

Figure 3-2. Waveforms During Steady Operation



For the dC_T level shift amount and the OUT_1 and OUT_2 dead time settings, refer to **4.4 Dead Time Setting**.

The relationship between the FB, DTC_1, and DTC_2 voltages in each operating state and the pins that determine the duty of OUT_1 and OUT_2 are shown in Table 3-1 below. For the duty settings, refer to **4.5 Duty Settings**.

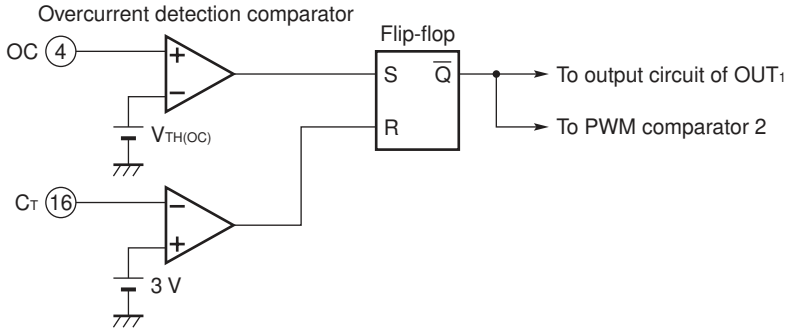
Table 3-1. Relationship Between Pins That Determine Duty During Steady Operation

Operating Status		Voltage Relationship	Pin That Determines OUT_1 Duty	Pin That Determines OUT_2 Duty
Steady operation 1 (rated status)	T_3	$DTC_2 < FB < DTC_1$	FB	FB
Steady operation 2 (heavy load, low input)	T_4	$DTC_2 < DTC_1 < FB$	DTC_1	DTC_1
Steady operation 3 (light load, high input)	T_5	$FB < DTC_2 < DTC_1$	FB	DTC_2

3.3 Overcurrent Limitation Operation

The internal configuration of the overcurrent latch circuit is shown in Figure 3-3 below.

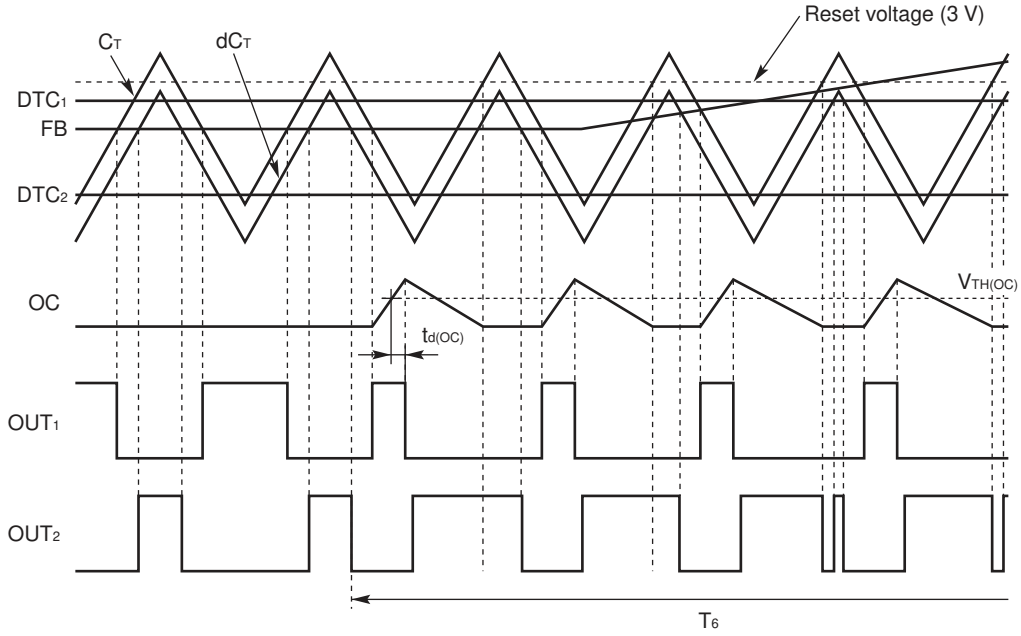
Figure 3-3. μPC1909 Overcurrent Latch Circuit



If a voltage that exceeds the overcurrent detection voltage ($V_{TH(OC)}$ = 210 mV TYP.) is input to the OC pin, OUT_1 is latched to low level, and then OUT_2 is latched to high level. The time between the detection of overcurrent and when OUT_1 becomes low level is the overcurrent detection delay time. Moreover, if the voltage of the C_T pin exceeds 3.0 V, the reset signal will be input to the flip-flop, and the latch status of OUT_1 and OUT_2 will be reset. When the OC pin voltage reaches the overcurrent detection voltage, even in the cycle in which the latch status was reset, the latch and reset operations will be repeated. In other words, the pulse width is limited every cycle (pulse-by-pulse current limitation).

The waveforms when overcurrent limitation is operating are shown in Figure 3-4 below.

Figure 3-4. Waveforms When Overcurrent Limitation Is Operating



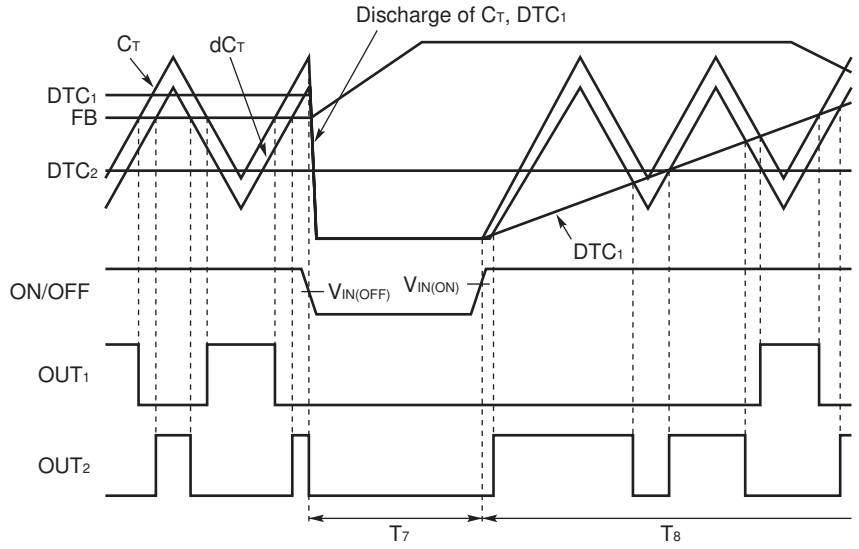
3.4 On/Off Operation

The output of OUT_1 and OUT_2 can be made low level (off) by making the voltage of the ON/OFF pin low level. This also causes discharge of the soft start capacitor externally connected to the DTC_1 pin and the timing capacitor externally connected to the C_T pin.

To prevent chattering when turning on and off slowly, the threshold voltage of the ON/OFF pin has a 0.2-V hysteresis.

The waveforms during the on/off operation are shown in Figure 3-5 below.

Figure 3-5. Waveforms During On/Off Operation

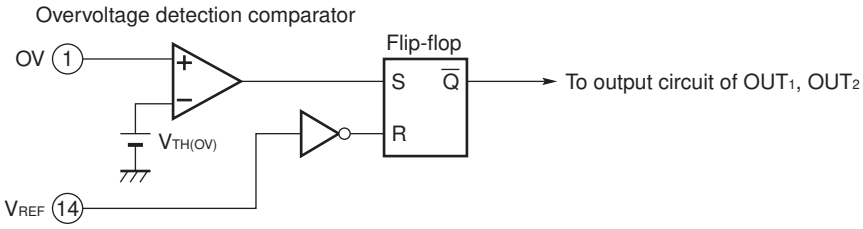


3.5 Overvoltage Protection Operation

The overvoltage latch circuit is a protection circuit that stops the power supply to prevent damage to the load after detection of overvoltage caused by abnormal boosting of the output of the converter.

The internal configuration of the overvoltage latch circuit is shown in Figure 3-6 below.

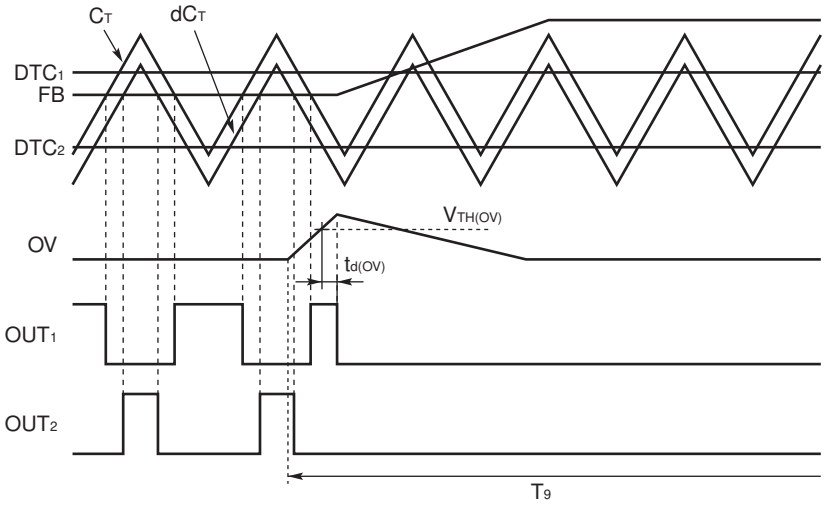
Figure 3-6. μPC1909 Overvoltage Latch Circuit



The threshold voltage ($V_{TH(OV)}$) connected to the overvoltage detection comparator is 2.0 to 2.8 V (2.4 V TYP.). If the voltage of the OV pin exceeds $V_{TH(OV)}$, OUT_1 and OUT_2 are latched to low level. The waveforms when OV (overvoltage) occurs are shown in Figure 3-7 below.

To reset the status of the overvoltage latch, drop the voltage of the V_{CC} pin to below the OVL release voltage ($V_{R(OV)}$ = 2 V TYP.), and drop the voltage of the V_{REF} pin to a sufficiently low level.

Figure 3-7. Waveforms When Overvoltage Latch Is Operating

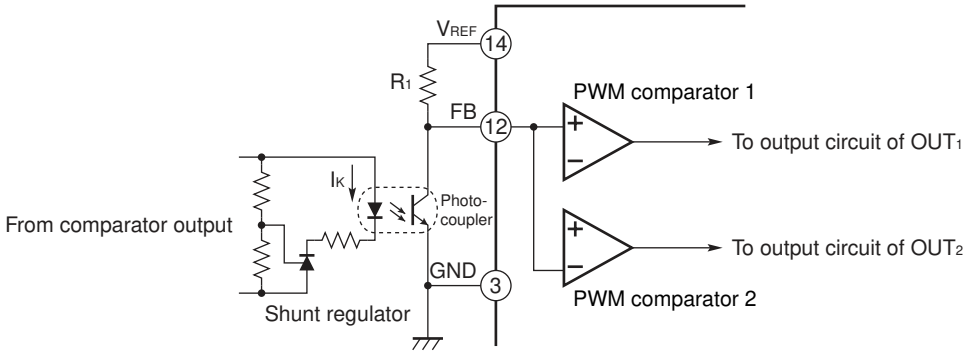


★ 4. SETTINGS

4.1 Controller Settings

The feedback circuit for when the converter output voltage is detected on the secondary side is configured as shown in Figure 4-1 below. The feedback gain is primarily determined by the R_1 resistor.

Figure 4-1. Feedback Circuit Configuration



The voltage of the FB pin is input to PWM comparators 1 and 2.

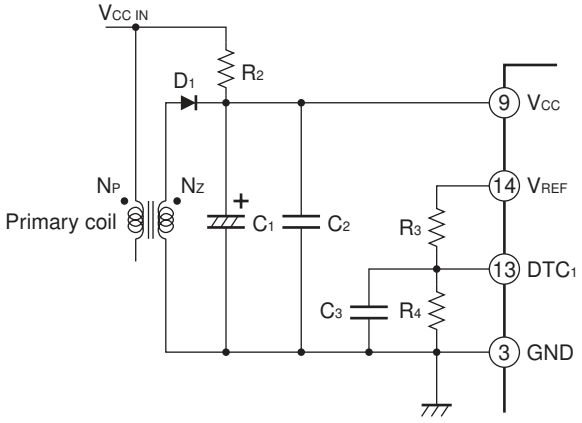
During steady operation (DTC_2 < FB < DTC_1), the duty of OUT_1 and OUT_2 is determined by the slice level of the triangle wave based on the FB pin voltage.

Caution When using a shunt regulator such as the μPC1093 for the secondary-side detector, I_K must be set bearing in mind the variation of the C_{TR} in the photocoupler. Also, be sure to use the photocoupler grounded at the emitter ground.

4.2 Startup Circuit, Low Voltage Malfunction Prevention Circuit Settings

The startup circuit is configured as shown in Figure 4-2 below.

Figure 4-2. Startup Circuit



In the μPC1909, when the power supply voltage (V_{CC}) rises but is less than the operation start voltage ($V_{CC(L\ to\ H)}$), a current of about 100 μA flows as a standby current.

When V_{CC} reaches or exceeds $V_{CC(L\ to\ H)}$, the internal reference voltage (V_{REF}) rises and operating current is supplied to the internal circuits, increasing the circuit current (I_{CC}) to a level of about 12 mA.

In the startup circuit in Figure 4-2, $I_{CC(SB)}$ is supplied via a startup resistor (R_2), and when the power MOS FET is turned on after the μPC1909 is started up, I_{CC} is supplied from a capacitor (C_1) until voltage reaches the auxiliary coil. R_2 is determined using $I_{CC(SB)}$ as follows.

$$R_2 \leq \left\{ \frac{V_{IN(MIN.)} - V_{CC(LtoH)(MAX.)}}{I_{CC(SB)(MAX.)} + I_{REF}} \right\}$$

If R_2 is too small, the loss via R_2 during steady operation will be large. The loss via R_2 during steady operation ($P_{L(MAX.)}$) is shown below. In this equation, N_Z is the number of turns in the power supply auxiliary coil, N_P is the number of turns in the primary coil, and $V_{F(D1)}$ is the forward direction voltage drop in the diode (D_1).

$$P_{L(MAX.)} = \frac{\{(1 - N_Z/N_P) \cdot V_{IN(MAX.)} + V_{F(D1)}\}^2}{R_2}$$

Note that a film or other capacitor (C_2) with good high-frequency characteristics should be connected to prevent a high-frequency current flowing through the V_{CC} line when the power MOS FET is driven.

To apply a soft start, connect a soft start capacitor (C_3) between the DTC_1 pin and GND. Using the overcurrent limitation function of the OC pin allows the duty to be limited on a pulse-by-pulse basis, enabling a more secure soft start.

The time between the startup of the μPC1909 and the first output of OUT_1 (t_1) is expressed as follows.

$$t_1 = - \frac{C_3 \cdot R_3}{1 + R_3 / R_4} \ln \{1 - (1 + R_3 / R_4) \cdot (V_{TH(L)} / V_{REF})\}$$

Although V_{CC} drops in the t_1 period, C_1 is determined so that OUT_1 is output while the drop voltage has not fallen to the operating voltage hysteresis width V_H. At this time, because OUT_2 is output before OUT_1 (refer to **3.1 Startup**), C_1 must be set to compensate for the increase in current caused by the output of OUT_2. Refer to Figure 3-1. Waveforms at Startup for the operating waveforms.

$$C_1 > \frac{I_{CC} + I_{REF} + I_{OUT} - I_{CC(R)}}{V_H} \cdot t_1$$

Here, I_{REF} is the current that flows through the resistor with the maximum duty setting connected to the V_{REF} pin, I_{OUT} is the power MOS FET drive current, and $I_{CC(R)}$ is the current that is supplied from the startup resistor (R_2).

Note that when the rising of V_{REF} is later than the rising of V_{CC} at startup, OUT_1 and OUT_2 become high level simultaneously when V_{REF} is in a range of about 0.45 to 0.5 V, which may result in the external power MOS FET being inadvertently turned on. To prevent this, speed up the rising of V_{REF} by pulling it up to V_{CC} with a resistor. Note, however, that the standby current ($I_{CC(SB)}$) will increase by only the current that flows through the connected resistor.

The pull-up resistance value (R) can be calculated from the following equation.

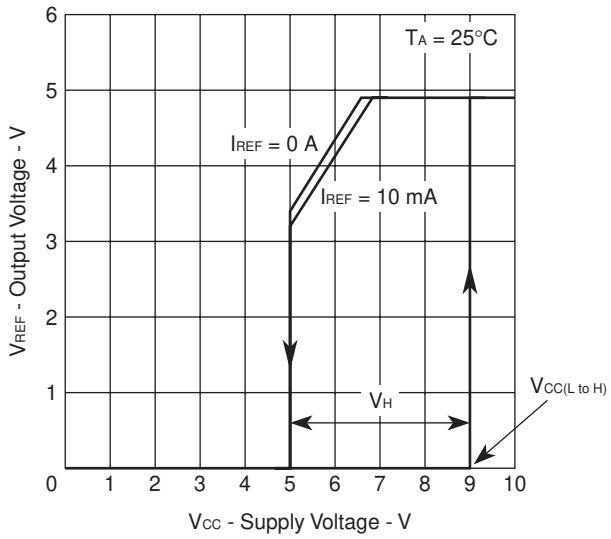
$$R\ [k\Omega] = \frac{V_{CC(MAX.)}\ [V] - 0.5}{0.1\ [mA]}$$

Remark $V_{CC(MAX.)}$: The highest power supply voltage that can be applied at startup without causing malfunction.

For the same reason, if V_{CC} drops below the operation stopped voltage ($V_{CC(L\ to\ H)} - V_H$), V_{REF} and the constant current circuit will be cut-off, which weakens the drive capacity of the OUT_1 and OUT_2 outputs when the power supply is cut-off. If this drive capacity is weakened, the charge that has accumulated at the power MOS FET gates may not be sufficiently discharged, blunting the falling section of the power MOS FET gate drive waveform. In this case, connecting a capacitor of at least 0.47 μF between the V_{REF} pin and GND allows sufficient time and output block drive capacity to discharge the charge accumulated at the gates of the power MOS FET.

Because the operation start and stop voltages in the μPC1909 are 9 V TYP. and 5 V TYP. respectively, V_{REF} is output while operation is stopped until V_{CC} is 5 V or lower. However, when V_{CC} reaches about 6.5 V, V_{REF} falls together with V_{CC}, as can be seen in Figure 4-3. When V_{REF} falls, the constant current value of the triangle wave oscillator decreases, causing the oscillation frequency to drop.

Figure 4-3. V_{REF} vs. V_{CC} Characteristics

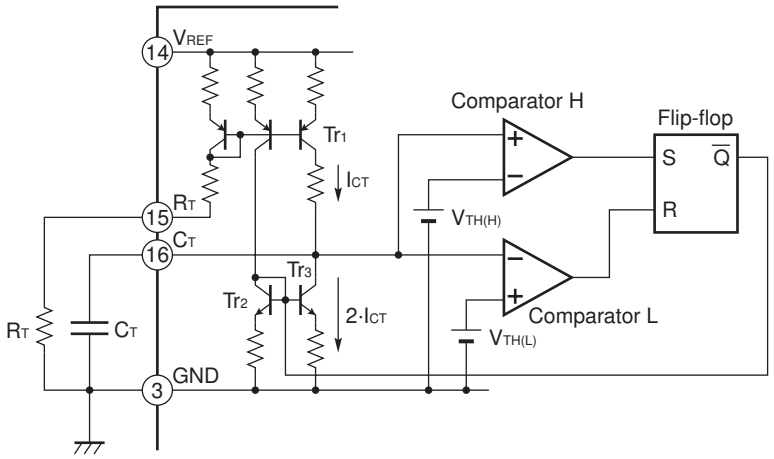


In standard applications, V_{REF} is resistance-divided to create the DTC_1, DTC_2, and FB voltages. In addition, because the levels of the triangle wave (C_T) and internally level-shifted triangle wave (dC_T) are also generated internally by dividing the resistance of V_{REF}, if V_{REF} drops, each of the above will drop in proportion to V_{REF}. As a result, even if the oscillation frequency drops, standard applications are not affected. Further study will be required, however, including for transient states.

4.3 Oscillator Settings

The oscillator circuit is shown in Figure 4-4 below.

Figure 4-4. μPC1909 Oscillator Circuit



A timing resistor (R_T) is connected between the R_T pin and GND, and a timing capacitor (C_T) is connected between the C_T pin and GND. The charge/discharge current of C_T is determined by R_T. The oscillator operates as follows.

<1> If I_{CT} is taken as the current that flows through Tr_1, the current the flows through Tr_3 is set as 2 x I_{CT}. Because the flip-flop ($\overline{Q}$) outputs a high level at startup, Tr_2 is off, and C_T is charged with I_{CT}.

<2> When the C_T voltage reaches $V_{TH(H)}$ = 3.5 V TYP., the output of comparator H is inverted, and Tr_2 is turned on. Due to the discharging of the current set by 2 x I_{CT}, the current flowing through C_T is (I_{CT} – 2 x I_{CT}) = – I_{CT}, so C_T is discharged by I_{CT}.

<3> If the C_T voltage drops to $V_{TH(L)}$ = 1.5 V TYP., the output of comparator L is inverted, the flip-flop is reset, and C_T is recharged because Tr_2 is off.

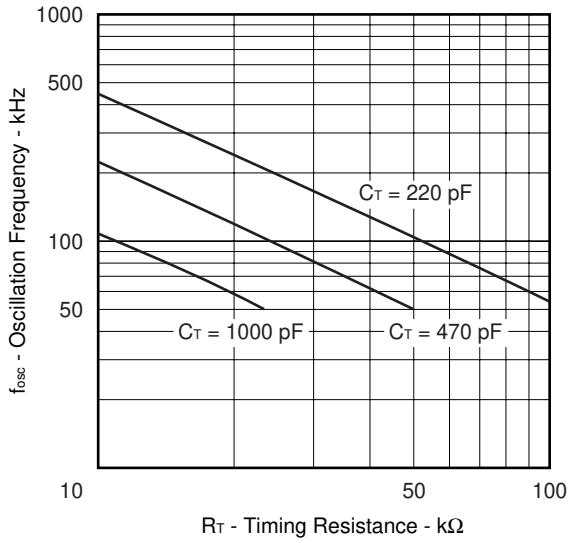
<4> <2> and <3> are repeated, generating a triangle wave with an amplitude of 1.5 to 3.5 V.

The oscillation frequency can be approximated from the following equation.

$$f_{OSC} \cong \frac{1 \times 10^6}{0.8251 \times C_T\,[\mathrm{pF}] \times (R_T\,[\mathrm{k\Omega}] + 0.8) + 320}\ [\mathrm{kHz}]$$

The results of measuring f_{OSC} vs. R_T are shown in Figure 4-5 below, with C_T as the parameter.

Figure 4-5. Relationship Between Oscillation Frequency (f_{OSC}), Timing Capacitor (C_T) and Timing Resistor (R_T)



4.4 Dead Time Setting

The period in which OUT_1 and OUT_2 are simultaneously off is called dead time. This is an important parameter to realize a zero-cross switch when active-clamping. To set the dead time, it is necessary to adjust both the oscillation frequency and level shift parameters (for details of the oscillation frequency setting, refer to **4.3 Oscillator Settings**).

4.4.1 Level shift setting

Whichever is higher of the DTC_2 pin and FB pin voltages is compared with the triangle wave that is the internally level-shifted wave of the C_T pin (dC_T). OUT_2 is high level while dC_T is higher than the DTC_2 and FB voltages.

The triangle wave dC_T, which controls OUT_2, is generated by internally level-shifting the C_T wave on the low potential side. The amount of shift (V_d) is determined using the resistor (R_{CT2}) connected between the C_{T2} and V_{REF} pins.

V_d can be calculated from the following equation.

$$V_d \cong \frac{2 \times 4.2}{R_{CT2}\,[k\Omega] + 10}\,[V]$$

A general diagram of the level shift circuit (OLS) is shown in Figure 4-6, and the relationship between the oscillation frequency (f_{OSC}), the dead time (t_{qd}), and resistor R_{CT2} is shown in Figure 4-7.

Figure 4-6. μPC1909 Level Shift Circuit (OLS)

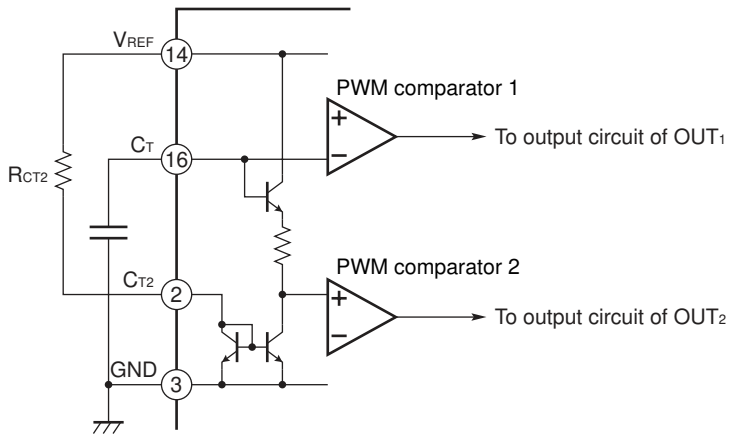
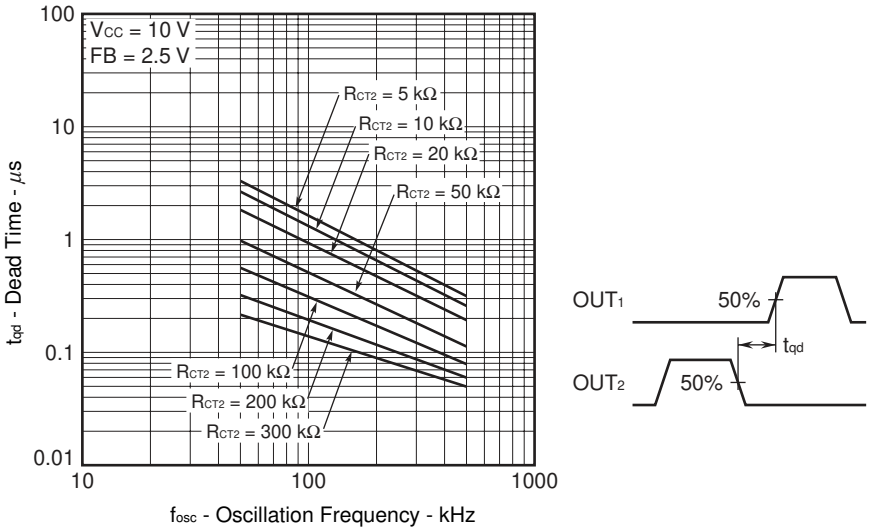


Figure 4-7. Relationship Between fosc, tqd and RCT2

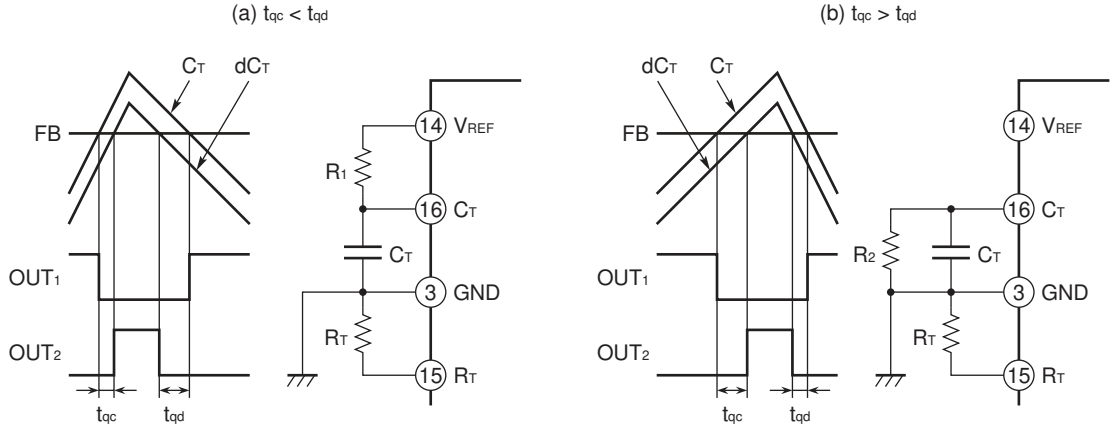


4.4.2 Dead time adjustment

The dead time between the fall of OUT_1 and the rise of OUT_2 (t_{qc}) and the dead time between the fall of OUT_2 and the rise of OUT_1 (t_{qd}) is determined by the oscillation frequency and the amount of level shift of the triangle wave.

Although usually $t_{qc} = t_{qd}$, if these values differ, connect a suitable resistor between the C_T pin and the V_{REF} pin, as well as between the C_T pin and GND, and adjust the dead time by making the oscillation waveform asymmetrical, as shown in Figure 4-8.

Figure 4-8. Dead Time Adjustment



The charge current (I_{CT}) of the timing capacitor (C_T) is expressed as follows.

$$I_{CT}\ [A] = \frac{4.2}{800 + R_T\ [\Omega]}$$

If R_T is taken as 20 kΩ, I_{CT} will be approximately 200 μA.

To reduce t_{qc}, connect a resistor (R_1) between the V_{REF} and C_T pins. If the value of the resistor is set so that the current charged in C_T is about 10% more than I_{CT}, t_{qc} can be reduced and t_{qd} increased by about 10% compared to when R_1 is not connected.

R_1 here can be calculated from the following equation.

$$R_1\ [\Omega] = \frac{V_{REF}\ [V] - V_{OSC}\ [V]}{\Delta I_{CT}\ [A]}$$

Remark V_{OSC} : Central voltage value of triangle wave

ΔI_{CT} : Value of I_{CT} current increased (decreased) by R_1 (R_2)

Note also that connecting a resistor (R_2) between C_T and GND makes it possible to reduce the current charged to C_T. If a resistor is selected that allows about 10% current to flow, t_{qc} can be increased and t_{qd} reduced by about 10% compared to when R_2 is not connected.

R_2 here can be calculated from the following equation.

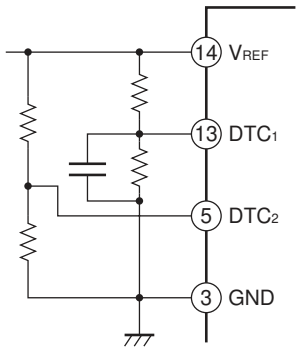
$$R_2\ [\Omega] = \frac{V_{OSC}\ [V]}{\Delta I_{CT}\ [A]}$$

4.5 Duty Settings

4.5.1 Maximum duty setting

In the steady operation state (DTC_2 < FB < DTC_1), the duty during operation at the FB voltage is determined by OUT_1 and OUT_2. To set the duty as an independent FB input at times such as at startup, during low voltage input, and when the current is limited, the OUT_1 and OUT_2 outputs must be set to their maximum duty values. Set the maximum duty for OUT_1 and OUT_2 via the DTC_1 and DTC_2 pins, respectively, as shown in Figure 4-9.

Figure 4-9. Maximum Duty Settings in μPC1909



Note that when pulse-by-pulse current limitation is being applied using the OC pin, the maximum duty of OUT_1 should be set to between 60 and 65%. This is because the duty conversion of OUT_1 sets the reset level of the internal OC circuit to about 75%. For details, refer to **4.7 Overcurrent Limiter Settings**.

There is no limit to the maximum duty of OUT_2.

4.5.2 Minimum duty limit

When OUT_1 is operating at maximum duty, if OUT_2 is not output, it may inadvertently be set to a duty of 0%, depending on the value of "OUT_1 ON time + t_{qc} + t_{qd}". If OUT_2 has 0% duty when active clamping, the transformer will not be able to be reset, and a minimum duty limit will have to be set for OUT_2 at the same time the maximum duty of OUT_1 is determined. Because the DTC_1 pin is also the input of PWM comparator 2 on the OUT_2 side, if the FB voltage is higher than the DTC_1 voltage, the DTC_1 voltage is compared with dC_T and the minimum duty of OUT_2 is limited.

4.5.3 Soft start

This IC incorporates a transistor for discharging the soft start capacitor connected between the DCT_1 pin and GND. If V_{CC} falls below the operation stopped voltage (5 V TYP.) or if the ON/OFF pin becomes low level (off), the DTC_1 pin becomes low level and the soft start capacitor is initialized.

There is no such transistor incorporated on the DTC_2 side.

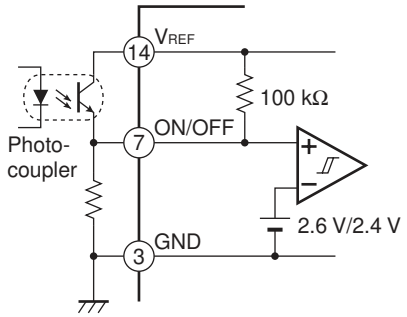
4.6 Remote Control

In the μPC1909, starting up and stopping a converter can be controlled by turning on and off the output circuit using an external signal. When the ON/OFF pin is made low level, the low voltage malfunction protection circuit operates and cuts off OUT_1 and OUT_2, causing the timing capacitor connected between the C_T pin and GND (C_T) and the soft start capacitor connected between the DTC_1 pin and GND to discharge. Because the on/off threshold voltage has 0.2-V hysteresis, the occurrence of chattering can be suppressed, even in slow on/off operations.

The ON/OFF pin is internally pulled up to V_{REF} via a 100 kΩ resistor. When the on/off function is not used, however, be sure to connect the ON/OFF pin directly to the V_{REF} pin in order to prevent the occurrence of noise.

A configuration whereby on/off control is controlled from the primary side by a photocoupler is shown in Figure 4-10 below. Be sure to set the pull-down resistor connected to the ON/OFF pin so that the leakage current between C and E when the photocoupler is off does not cause the ON/OFF pin voltage to be boosted to a level whereby the μPC1909 is turned on.

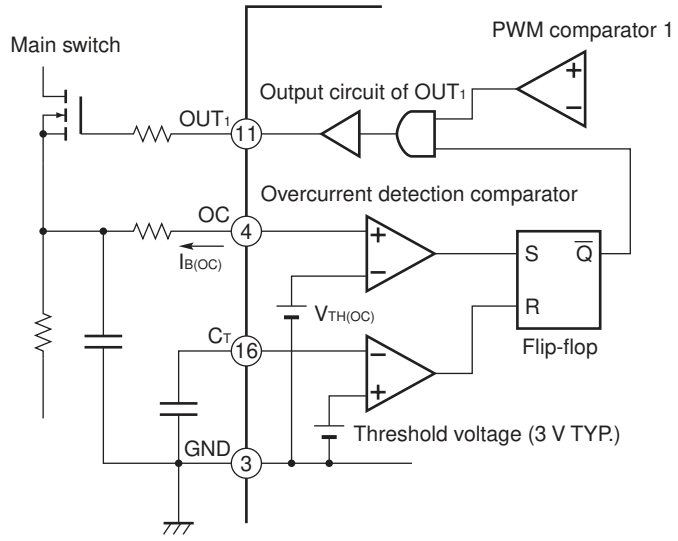
Figure 4-10. ON/OFF Pin Connection



4.7 Overcurrent Limiter Settings

The OC pin in the μPC1909 allows the realization of a pulse-by-pulse overcurrent limiter, whose configuration is shown in Figure 4-11 below.

Figure 4-11. μPC1909 Overcurrent Limiter



If overcurrent is detected by the overcurrent detection comparator, OUT_1 is latched to low level by the flip-flop. Moreover, if the triangle wave generated by the oscillator and a voltage with a threshold value that causes the output latch to be reset are input to the other comparator the flip-flop will be reset at each cycle.

Because the reset threshold voltage is internally set to 3 V TYP. (about 75% V_{REF}), if a maximum duty of 75% or over is set by the DTC_1 pin thus activating overcurrent limitation by the OC pin, two pulses will be inadvertently output in one cycle. To allow for differences in ICs, do not set the maximum duty of DTC_1 (60% or over) to more than 65% when applying overcurrent limitation using the OC pin. Alternatively, do not use OC pin overcurrent limitation if setting the maximum duty (60% or over) to more than 65%. In this case (overcurrent limitation current not used), connect the OC pin directly to GND.

Discharge current flows through the OC pin. This discharge current is expressed as the input bias current of the overcurrent latch block ($I_{B(OC)}$). Although a filter is attached to the OC pin to prevent the overcurrent latch circuit from malfunctioning due to the surge current that flows when the power MOS FET is turned on, be sure to set the resistor to no more than 100 Ω to stop $I_{B(OC)}$ causing a shift in the overcurrent detection point.

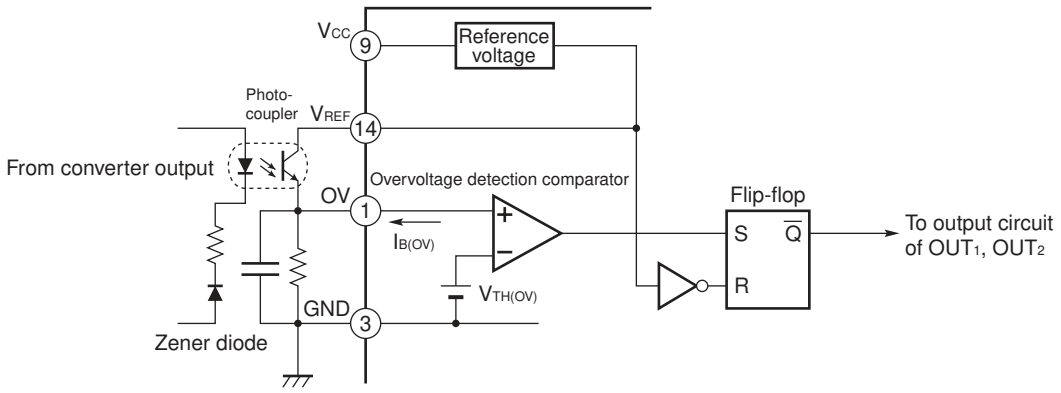
When overcurrent is being limited by the OC pin, OUT_1 operates at the minimum pulse width limitable by the overcurrent latch circuit. The minimum pulse width is the sum of the μPC1909's overcurrent detection delay time ($t_{d(OC)}$), the delay of the filter attached to the OC pin, and the turn-on time of the power MOS FET.

During steady operation (DTC_2 < FB < DTC_1), OUT_2 operates at the duty determined by the FB voltage. Because the FB voltage rises when the output of the converter drops, the duty of the OUT_2 output drops in line with the converter output, until it reaches the minimum duty set by the DTC_1 voltage.

4.8 Overvoltage Protection Circuit Setting

The overvoltage protection circuit based on the overvoltage latch in the μPC1909 is configured as shown in Figure 4-12 below. The threshold voltage connected to the overvoltage detection comparator ($V_{TH(OV)}$) is 2.0 to 2.8 V (2.4 V TYP.). If the input at the OV pin exceeds $V_{TH(OV)}$, the flip-flop in the IC latches OUT_1 and OUT_2 to low level. Once the overvoltage latch circuit is latched, it is not released until the power supply voltage of the IC (V_{CC}) falls below the OVL release voltage (2 V TYP.) (because I_{CC} is higher than $I_{CC(SB)}$ when the circuit is latched, the operation status will not be restored in the steady input state).

Figure 4-12. μPC1909 Overvoltage Protection Circuit



Discharge current flows through the OV pin. This is the input bias current of the overvoltage latch block in the electrical specifications ($I_{B(OV)}$ = 4 μA MAX.). To prevent the detection level fluctuating due to $I_{B(OV)}$, and to allow for the effect of the leakage current between C and E in the photocoupler, be sure to set the overvoltage detection resistor connected to the OV pin to no more than 100 kΩ.

Because the OVL (overvoltage latch) detection delay time is about 750 ns, a capacitor with good frequency characteristics should be connected between the OV pin and GND to prevent malfunction due to noise. However, if the overvoltage latch circuit does malfunction due to electrostatic discharge or other such external noise, an effective countermeasure is to connect a capacitor with good frequency characteristics such as a film capacitor between V_{CC} and GND.

Caution If the power is reapplied immediately after being stopped (V_{REF} drop) while there is charge remaining in the filter's capacitor (such as when V_{CC} (auxiliary coil voltage) is being monitored from V_{REF} without configuring an overvoltage protection circuit such as is shown in Figure 4-12), the overvoltage latch threshold value will be boosted in proportion with the boosting of V_{REF}, possibly causing the overvoltage latch to latch too easily.

4.9 Output Circuit

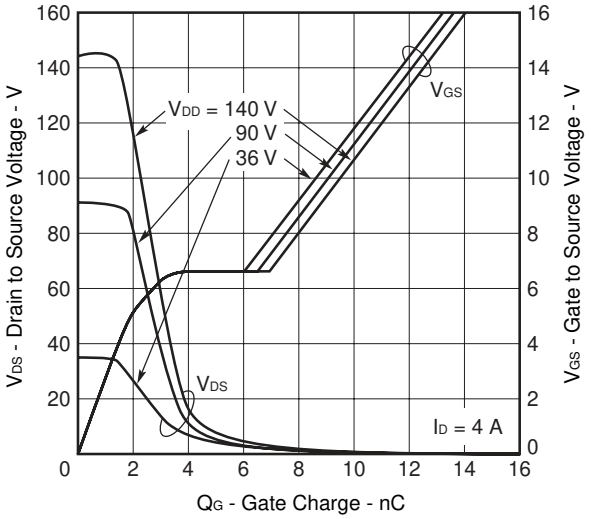
The output circuit is a totem-pole output with a peak output current rating ($I_{C(peak)}$) of 1.2 A. Although a power MOS FET can be driven directly, be careful not to exceed the allowable loss of the μPC1909 when the input capacitance of the power MOS FET is large or the operating frequency is high. The switching speed of the power MOS FET is determined by the charge/discharge current of the gates and the charge of the power MOS FET's gates. Be sure, however, to insert a series resistor at the gates of the power MOS FET to avoid exceeding the peak output current rating of the μPC1909.

Note that the heat generated in the μPC1909 by the output current is determined by the charge at the gates of the power MOS FET, and is not related to the switching speed.

When the 2SK1954 is used, for example, the loss of the μPC1909 (P_d) can be determined as follows,
when the gate drive voltage $V_{GS} \cong VOUT_1$ = 10 V and
the oscillation frequency f_{OSC} = 200 kHz,
as shown in the gate charge graph on the right (Figure 4-13):

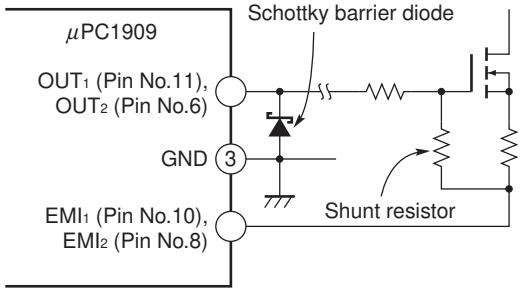
$$P_d = Q_G \cdot V_{GS} \cdot f_{OSC}$$
$$= 10\ [nC] \times 10\ [V] \times 200\ [kHz]$$
$$= 0.02\ [W]$$

Figure 4-13. 2SK1954 Gate Change Characteristics



Moreover, when the μPC1909 and the power MOS FET are separated, the wiring from the OUT_1 and OUT_2 output pins is lengthened, which combined with the parasitic inductance and floating capacitance elements of the power MOS FET causes the voltage of the OUT_1 and OUT_2 pins to fall below that of the GND pin (undershoot). In this case, clamp the undershoot by connecting a Schottky barrier diode as shown in Figure 4-14 to prevent the possibility of malfunction in the μPC1909.

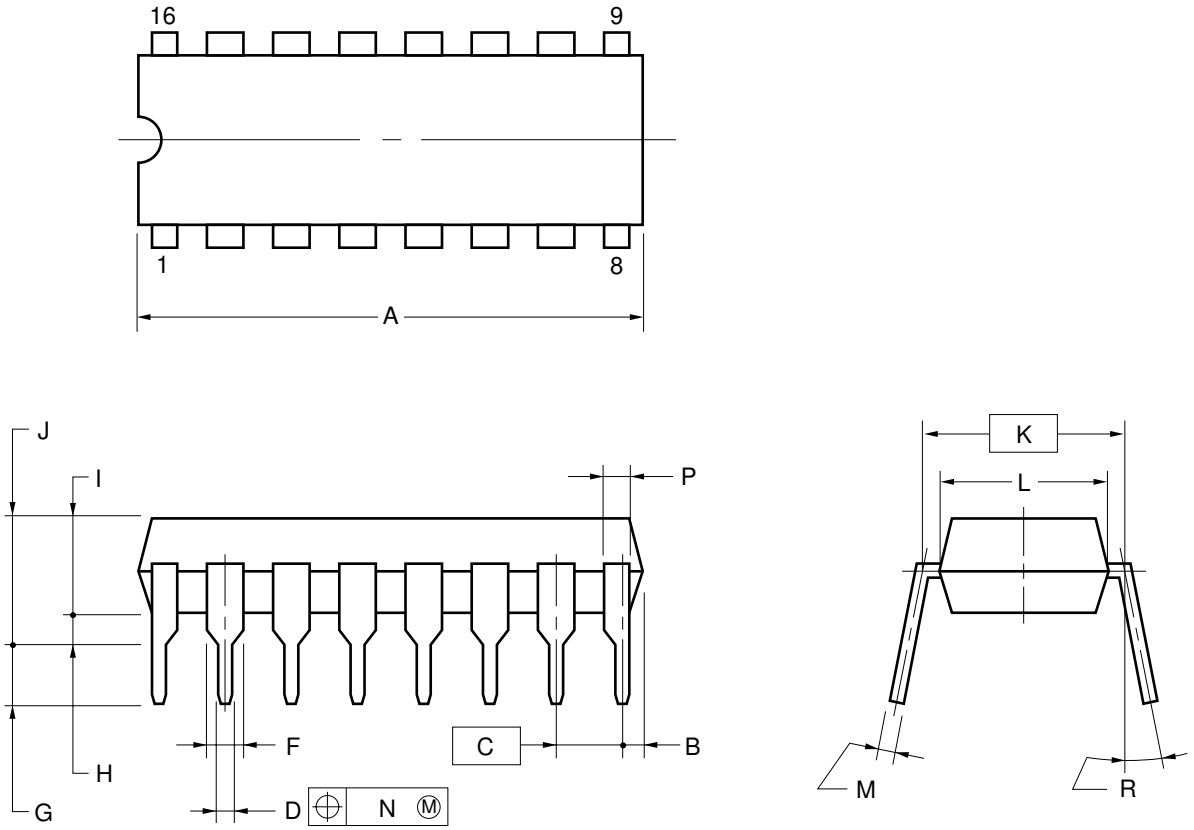
Figure 4-14. Power MOS FET Drive Circuit Block



Note that when active clamping, if the C-cut drive transistor is driven by OUT_2, the voltage of the OUT_2 pin may become higher than V_{CC}. It is therefore vital to observe $VOUT_2 \leq V_{CC}$ + 5 V by taking action such as connecting a diode between OUT_2 and V_{CC}.

★ **5. PACKAGE DRAWINGS**

16-PIN PLASTIC DIP (7.62mm(300))



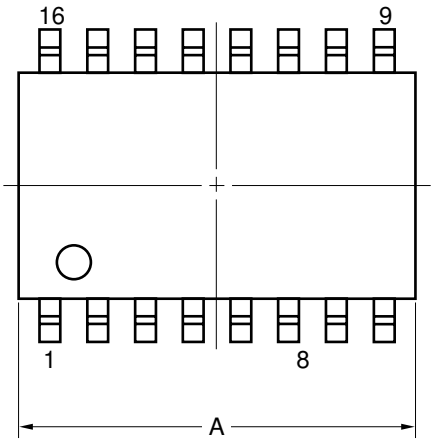
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

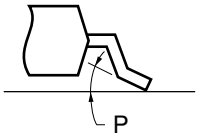
ITEM	MILLIMETERS
A	20.32 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.1 MIN.
G	3.5±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.5
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	1.1 MIN.
R	0~15°

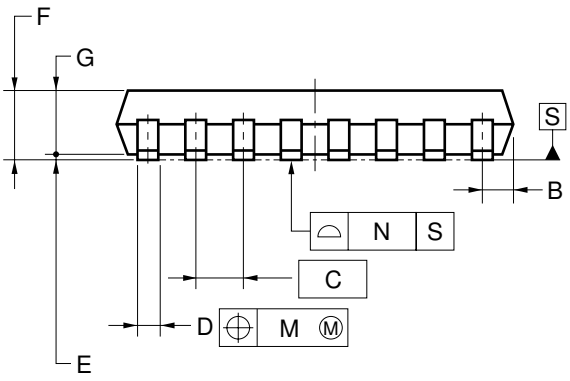
P16C-100-300B-2

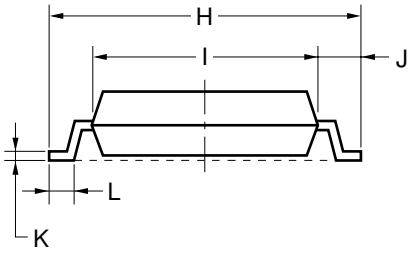
16-PIN PLASTIC SOP (7.62 mm (300))



detail of lead end







NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	10.2±0.2
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.65±0.15
G	1.55
H	7.7±0.3
I	5.6±0.2
J	1.1±0.2
K	$0.22^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P16GM-50-300B-6

6. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"(C10535E)**.

Type of Through-hole Device

μPC1909CX: 16-pin plastic DIP (7.62 mm (300))

Soldering Method	Soldering Conditions
Wave soldering (pins only)	Solder bath temperature : 260°C MAX., Time : 10 seconds MAX.
Partial heating	Pin temperature : 300°C MAX., Time : 3 seconds MAX. (per pin)

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

Type of Surface Mount Device

μPC1909GS: 16-pin plastic SOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition symbol
Infrared reflow	Package peak temperature : 235°C, Time : 30 seconds MAX. (at 210°C or higher), Count : Twice or less	IR35-00-2
VPS	Package peak temperature : 215°C, Time : 40 seconds MAX. (at 200°C or higher), Count : Twice or less	VP15-00-2
Wave soldering	Soldering bath temperature : 260°C or less, Time : 10 seconds MAX., Count : Once, Preheating temperature : 120°C MAX. (package surface temperature)	WS60-00-1

Caution Do not use different soldering methods together.

[MEMO]

[MEMO]

[MEMO]

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