Si53212/Si53208/Si53204 Data Sheet

12/8/4-Output PCI-Express Low Jitter, Low Power Gen 1/2/3/4/5 Clock Buffer

The Si53212, Si53208, and Si53204 are the industry's highest performance, low additive jitter, low power PCIe clock fanout buffer family that can source 12, 8, or 4 clock outputs. All differential clock outputs are compliant to PCIe Gen1/2/3/4/5 common clock and separate reference clock specifications. This family of buffers is spread spectrum tolerant to pass through a spread input clock. Each device has an individual hardware output enable control pin for enabling and disabling each differential output. The device can also support input frequencies from 10 MHz to 200 MHz. All the devices are packaged in small QFN packages. The small footprint and low-power consumption make this family of PCIe clock fanout buffers ideal for industrial and consumer applications. To confirm PCI-Express compliance, the Skyworks PCIe Clock Jitter Tool makes measuring PCIe clock jitter quick and easy. Download it for free at https://www.skyworksinc.com/en/application-pages/pci-express-learning-center.

Applications

- Data Centers
- Servers
- Storage
- PCIe Add-on Cards
- Communications
- Industrial

KEY FEATURES

- 12/8/4-output 100 MHz PCIe Gen1/2/3/4/5-compliant clock fanout buffer
- Low additive jitter: 0.02 ps rms max, Gen 5
- Low-power, push-pull, HCSL compatible differential outputs
- 10 MHz to 200 MHz clock input
- Individual hardware control pins and I^2C controls for Output Enable
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Supports Intel QPI/UPI standards
- Single 1.5 to 1.8 V power supply
- Internal 100 Ω or 85 Ω output impedance matching
- Adjustable output slew rate
- Temperature range: –40 °C to 85 °C
- Package options:
  - 64-pin QFN (9 x 9 mm) : 12-output
  - 48-pin QFN (6 x 6 mm) : 8-output
  - 32-pin QFN (5 x 5 mm) : 4-output
- Small QFN packages
- Pb-free, RoHS-6 compliant

1. Feature List

- 12/8/4-output 100 MHz PCIe Gen1/2/3/4/5 and SRIS compliant clock fanout buffer
- Low-power, push-pull, HCSL compatible differential outputs from 10 MHz to 200 MHz clock input
- Low additive jitter of 0.02 ps rms max to meet PCIe Gen 5 specifications
- Individual hardware control pins and I2C for Output Enable to easily disable unused outputs for power savings
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Supports Intel QPI/UPI jitter requirements with margin
- Internal 100 Ω or 85 Ω output impedance matching
  - Eliminates external termination resistors to reduce board space
- Adjustable slew rate to improve signal quality for different applications and board designs
- Single 1.5–1.8 V power supply
- Temperature range: –40°C to 85°C
- Package options:
  - 64-pin QFN (9 x 9 mm), 12-output
  - 48-pin QFN (6 x 6 mm), 8-output
  - 32-pin QFN (5 x 5 mm), 4-output
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Number of Outputs	Internal Termination	Part Number	Package Type	Temperature
12-output	100 Ω	Si53212-A01AGM	64-QFN	Extended, –40 to 85 °C
		Si53212-A01AGMR	64-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53212-A02AGM	64-QFN	Extended, –40 to 85 °C
		Si53212-A02AGMR	64-QFN, Tape and Reel	Extended, –40 to 85°C
8-output	100 Ω	Si53208-A01AGM	48-QFN	Extended, –40 to 85 °C
		Si53208-A01AGMR	48-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53208-A02AGM	48-QFN	Extended, –40 to 85 °C
		Si53208-A02AGMR	48-QFN, Tape and Reel	Extended, –40 to 85 °C
4-output	100 Ω	Si53204-A01AGM	32-QFN	Extended, –40 to 85 °C
		Si53204-A01AGMR	32-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53204-A02AGM	32-QFN	Extended, –40 to 85 °C
		Si53204-A02AGMR	32-QFN, Tape and Reel	Extended, –40 to 85 °C

2.1 Technical Support

Table 2.1. Technical Support URLs

Frequently Asked Questions	https://www.skyworksinc.com/en/application-pages/pci-express-learning-center
PCIe Clock Jitter Tool	https://www.skyworksinc.com/en/Application-Pages/pcie-clock-jitter-tool
PCIe Learning Center	https://www.skyworksinc.com/en/application-pages/pci-express-learning-center
Development Kit	https://www.skyworksinc.com/en/products/timing/evaluation-kits/clock-buffer/si53208-evaluation-kit

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3. Functional Block Diagrams

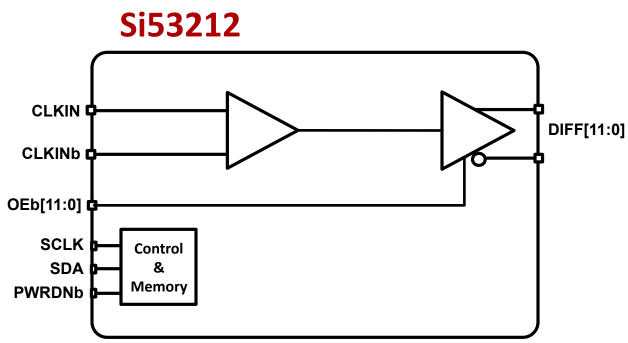


Figure 3.1. Si53212 Block Diagram

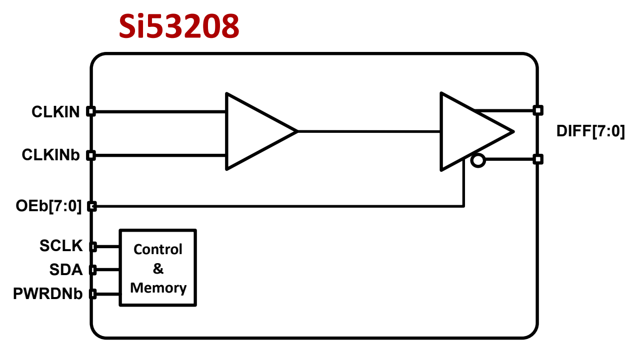


Figure 3.2. Si53208 Block Diagram

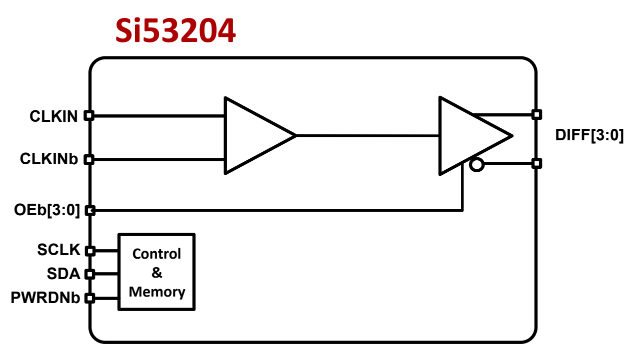


Figure 3.3. Si53204 Block Diagram

4. Electrical Specifications

Table 4.1. DC Electrical Specifications (VDD = VDDA = 1.5 V +/-5%)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.5 V Operating Voltage	VDD	1.5 V ±5%	1.425	1.5	1.575	V
Output Supply Voltage	VDD_IO	Supply voltage for differential Low Power outputs	0.9975	1.05 to 1.5	1.575	V
1.5 V Input High Voltage	V_{IH}	Control input pins	0.75 VDD	—	VDD + 0.3	V
1.5 V Input Low Voltage	V_{IL}	Control input pins	–0.3	—	0.25 VDD	V
Input current	I_{IN}	Single-ended inputs, VIN = GND, VIN = VDD	–5		5	μA
	I_{INP}	Single-ended inputs, VIN = 0 V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200		200	μA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	LIN		—	—	7	nH
Si53212 Current Consumption (VDD = VDDA = 1.5 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$		—	1.3	1.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	0.75	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	60	71.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	12	13	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	46	55.5	mA
Si53208 Current Consumption (VDD = VDDA = 1.5 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$		—	1.3	1.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	0.75	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	42	51.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	10	11	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	30	37.5	mA
Si53204 Current Consumption (VDD = VDDA = 1.5 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$		—	1.3	1.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	0.75	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.5	mA
Dynamic Supply Current	$I_{DD\_1.5V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	26	31.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	8.5	9.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	15.5	19	mA

Table 4.2. DC Electrical Specifications (VDD = VDDA = 1.8 V +/-5%)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.8 V Operating Voltage	VDD	1.8 V ±5%	1.71	1.8	1.89	V
Output Supply Voltage	VDD_IO	Supply voltage for differential Low Power outputs	0.9975	1.05 to 1.8	1.9	V
1.8 V Input High Voltage	V_{IH}	Control input pins	0.75 VDD	—	VDD + 0.3	V
1.8 V Input Low Voltage	V_{IL}	Control input pins	–0.3	—	0.25 VDD	V
Input current	I_{IN}	Single-ended inputs, VIN = GND, VIN = VDD	–5	—	5	μA
	I_{INP}	Single-ended inputs, VIN = 0V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200	—	200	μA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	LIN		—	—	7	nH
Si53212 Current Consumption (VDD = VDDA = 1.8 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$		—	1.4	2.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	61	74	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	12	14.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	47	56.5	mA
Si53208 Current Consumption (VDD = VDDA = 1.8 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$			1.4	2.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	44	53.5	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	10.5	12.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	31	38	mA
Si53204 Current Consumption (VDD = VDDA = 1.8 V +/-5%)						
Power Down Current	$I_{DD\_PD\_total}$		—	1.4	2.7	mA
	I_{DD_PD}	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	I_{DD_APD}	VDDA, all outputs off	—	0.6	0.75	mA
	I_{DD_IOPD}	VDD_IO, all outputs off	—	0.3	0.65	mA
Dynamic Supply Current	$I_{DD\_1.8V\_Total}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	27	33	mA
	I_{DD_OP}	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz		9	10.5	mA
	I_{DD_AOP}	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	I_{DD_IOOP}	VDD_IO, all differential outputs active at 100 MHz	—	16	19.5	mA

Table 4.3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CLKIN Frequency Range			10	—	200	MHz
CLKIN Rising and Falling Slew Rate	$CLKIN\_T_R\_T_F$	Single-ended measurement: VOL = 0.175 to VOH = 0.525 V (Averaged)	0.6	—	4	V/ns
Differential Input High Voltage	V_{IH}		150	—	—	mV
Differential Input Low Voltage	V_{IL}		—	—	-150	mV
Crossing Point Voltage	V_{OX}	Single-ended measurement	250	—	550	mV
Crossing Point Voltage (var)	V_{OX_DELTA}	Single-ended measurement	—	—	140	mV
Differential Ringback Voltage	V_{RB}		–100	—	100	mV
Time before Ringback Voltage	T_{STABLE_RB}		500	—	—	ps
Absolute maximum input voltage	V_{MAX}		—	—	1150	mV
Absolute minimum input voltage	V_{MIN}		–300	—		mV
Duty Cycle for Each Clock Output Signal in a Given Differential Pair	T_{DC}	Measured at crossing point V_{OX}	45	—	55	%
Rise/Fall Matching	T_{FRM}	Determined as a fraction of 2 x $(T_R - T_F)(T_R + T_F)$	—	—	20	%
Control Input Pins						
Trise	T_R	Rise time of single-ended control inputs	—	—	5	ns
Tfall	T_F	Fall time fo single-ended control inputs	—	—	5	ns
DIFF HCSL						
Output-to-Output Skew	T_{SKEW}	Measured at 0 V differential	—	—	50	ps
Additive Cycle to Cycle Jitter	J_{ADD_CCJ}	Measured at 0 V differential	—	14	20	ps
Additive Phase Jitter	J_{ADD}	12 kHz–20 MHz	—	—	0.21	ps (RMS)
PCIe Gen 1 Additive Pk-Pk Jitter[6]	$J_{ADD\_Pk\text{-}Pk}$	PCIe Gen 1	0	10	17	ps
PCIe Gen 2 Additive Phase Jitter[6]	J_{ADD_GEN2}	10 kHz < F < 1.5 MHz	0	0.125	0.2	ps (RMS)
		1.5 MHz < F < Nyquist	0	0.003	0.005	ps (RMS)
PCIe Gen 3 Additive Phase Jitter[6]	J_{ADD_GEN3}	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.04	0.06	ps (RMS)
PCIe Gen 3 SRIS Addtive Phase Jitter[6]	$J_{ADD\_GEN3\_SRIS}$	Includes PLL BW 2-4 MHz, CDR = 10 MHz	—	0.055	0.07	ps (RMS)
PCIe Gen 3 SRNS Additive Phase Jitter[6]	$J_{ADD\_GEN3\_SRNS}$	Includes PLL BW 2-4 MHz, CDR = 10 MHz	—	0.035	0.043	ps (RMS)
PCIe Gen 4 Additive Phase Jitter[6]	J_{ADD_GEN4}	Includes PLL BW 2-4 MHz, CDR = 10 MHz	—	0.04	0.06	ps (RMS)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PCIe Gen 4 SRIS Additive Phase Jitter[6]	$J_{ADD\_GEN4\_SRIS}$	Includes PLL BW 2-4 MHz, CDR = 10 MHz	—	0.055	0.07	ps (RMS)
PCIe Gen 4 SRNS Additive Phase Jitter[6]	$J_{ADD\_GEN4\_SRNS}$	Includes PLL BW 2-4 MHz, CDR = 10 MHz	—	0.035	0.043	ps (RMS)
PCIe Gen 5 Additive Phase Jitter[6, 7]	J_{ADD_GEN5}	Includes PLL BW 500 kHz-1.8 MHz, CDR = 20 MHz	—	0.015	0.021	ps (RMS)
PCIe Gen 5 SRIS Additive Phase Jitter[6, 7]	$J_{ADD\_GEN5\_SRIS}$	Includes PLL BW 500 kHz-1.8 MHz, CDR = 20 MHz	—	0.02	0.03	ps (RMS)
Slew Rate	T_R/T_F	Measured differentially from ±150 mV (fast setting)	—	2.4	3.7	V/ns
		Measured differentially from ±150 mV (slow setting)	—	1.9	2.9	V/ns
Slew Rate Matching	$\Delta T_R/T_F$		—	—	10	%
Voltage High	V_{HIGH}		600	—	850	mV
Voltage Low	V_{LOW}		–150	—	150	mV
Max Voltage	V_{MAX}		—	—	1150	mV
Min Voltage	V_{MIN}		–300	—	—	mV
Enable/Disable and Setup						
Clock Stabilization from Power-up	T_{STABLE}	Minimum ramp rate 200 V/s	—	1	5	ms
OE_b Latency	T_{OEb_LAT}	Differential outputs start after OE_b assertion Differential outputs stop after OE_b deassertion		2	3.5	clocks
PWRDNb Latency to differential outputs enable	T_{PWRDNb}	Differential outputs enable after PWRDNb deassertion	—	490	520	µs
Intel QPI Specifications for 100 MHz and 133 MHz						
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	$J_{ADD\_QPI\_SMI}$	4.8 Gb/s, 133 MHz, 12UI,7.8 M	—	0.16	—	ps (RMS)
		6.4 Gb/s, 133 MHz, 12UI,7.8 M	—	0.12	—	ps (RMS)
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	$J_{ADD\_SQPI\_SMI}$	8 Gb/s, 100 MHz, 12 UI	—	0.09	—	ps (RMS)
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	$J_{ADD\_QPI\_SMI}$	9.6 Gb/s, 100 MHz, 12UI	—	0.07	—	ps (RMS)
Intel UPI Specifications for 100 MHz						
UPI Additive Phase Jitter	J_{ADD_UPI}	Intel UPI 1–10 MHz	—	0.67	1	ps

Note:

1. Skyworks PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt(output jitter^2 - input jitter^2). Input used is 100 MHz from Si5340.
2. Post processed evaluation through Intel supplied Matlab scripts, using Intel PCIe Clock Jitter Tool.
3. Measuring on 100 MHz output using the template file in the Intel PCIe Clock Jitter Tool.
4. Measuring on 100 MHz, 133 MHz outputs using the template file in the Intel PCIe Jitter Tool.
5. Input clock slew rate of 3.0 V/ns used for jitter measurements.
6. Based on PCI Express(R) Base Specification. For complete PCIe specifications, visit www.pcisig.com.
7. Limiting amp is used at the input of the scope.

Table 4.4. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Units
Si53204 - 32-QFN[1]				
Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	50.3	°C/W
		Air Flow 1 m/s	47	
		Air Flow 2 m/s	45.6	
Thermal Resistance, Junction to Case	Θ_{JC}		10.3	°C/W
Thermal Resistance, Junction to Board	Θ_{JB}		30.9	°C/W
Calculation Parameter, Junction to Top Center	Ψ_{JT}		2.3	°C/W
Calculation Parameter, Junction to Board	Ψ_{JB}		30.9	°C/W
Si53208 - 48-QFN[2]				
Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	27.9	°C/W
		Air Flow 1 m/s	24.5	
		Air Flow 2 m/s	23.5	
Thermal Resistance, Junction to Case	Θ_{JC}		17	°C/W
Thermal Resistance, Junction to Board	Θ_{JB}		13.4	°C/W
Calculation Parameter, Junction to Top Center	Ψ_{JT}		0.5	°C/W
Calculation Parameter, Junction to Board	Ψ_{JB}		13.1	°C/W
Si53212 - 64-QFN[3]				
Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	27.2	°C/W
		Air Flow 1 m/s	23.9	
		Air Flow 2 m/s	22.5	
Thermal Resistance, Junction to Case	Θ_{JC}		13.7	°C/W
Thermal Resistance, Junction to Board	Θ_{JB}		14.4	°C/W
Calculation Parameter, Junction to Top Center	Ψ_{JT}		0.5	°C/W
Calculation Parameter, Junction to Board	Ψ_{JB}		14.2	°C/W

Note:

1. Based on a PCB with a dimension of 3" x 4.5", PCB Thickness of 1.6 mm, and PCB Center Land with 4 Via to top plane.
2. Based on 4 layer PCB with a dimension of 3" x 4.5", PCB Thickness of 1.6 mm, and PCB Center Land with 9 Via to top plane.
3. Based on 4 Layer PCB with a dimension of 3" x 4.5", PCB Thickness of 1.6 mm, and PCB Center Land with 25 Via to top plane.

Table 4.5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	VDD_1.8V	Functional	—	—	2.5	V
Input Voltage	VIN	Relative to VSS	–0.5	—	VDD + 0.5	V
Input High Voltage I^2C	VIH_I2C	SDATA and SCLK	—		3.6	V
Temperature, Storage	TS	Non-functional	–65	—	150	Celsius
Temperature, Operating Ambient	T_A	Functional	–40	—	85	Celsius
Temperature, Junction	T_J	Functional	—	—	125	Celsius
ESD Protection (Human Body Model)	ESDHBM	JEDEC (JESD 22-A114)	–2000	—	2000	V
Flammability Rating	UL-94	UL (Class)	V–0			
Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.						

5. Functional Description

5.1 OEb Pin

The OEb pin is an active low input used for synchronous stopping and starting the respective output clock while the rest of the device continues to function. By default, the OEb pin is set to logic low, and I^2C OE bit is set to logic high.There are two methods to disable the output clock: the OEb pin is pulled to a logic high, or the I^2C OE bit is set to a logic low. This pin has a 100 kΩ internal pull-down.

5.2 OEb Assertion

The assertion of the OEb function is achieved by pulling the OEb pin low while the I^2C OE bit is high, which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume.

5.3 OEb Deassertion

The OEb function is deasserted by pulling the pin high or writing the I^2C OE bit to a logic low. The corresponding output is stopped cleanly and the final output state is driven low.

5.4 SA Pin

The SA functionality sets the Slave Address of the part. This address is latched to the value of the pin when the part initially powers up. See Table 8.1 SA State on First Application of PWRDNb on page 24 for the available addresses. By default, the internal 60 kΩ pull-up resistor will set SA to a value of 1. Never directly connect the SA pin to VDD or GND. To drive the pin low or high, use a 10 kΩ resistor.

5.5 PWRDNb (Power Down) Pin

When PWRDNb is pulled low, the device will be placed in power down mode. The assertion and deasertion of PWRDNb is asynchronous. This pin has a 100 kΩ internal pull-up.

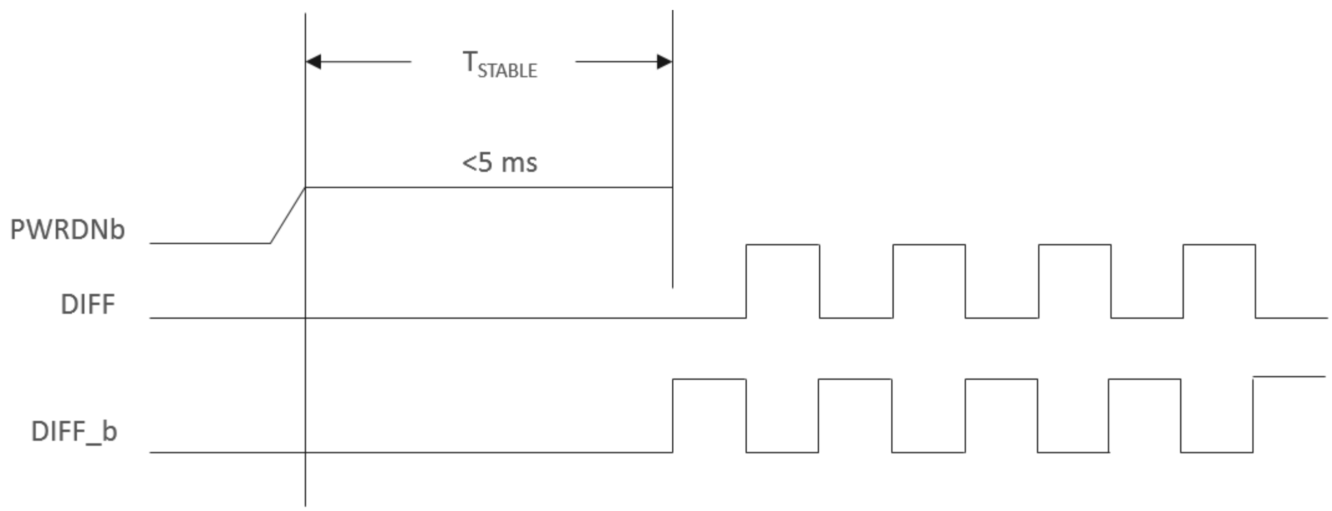


Figure 5.1. Initial Sample High of PWRDNb After Power Up

5.6 PWRDNb (Power Down) Assertion

The PWRDNb pin is an asynchronous active low input used to disable all output clocks in a glitch-free manner. In power down mode, all outputs and the I^2C logic are disabled. All disabled outputs will be driven low.

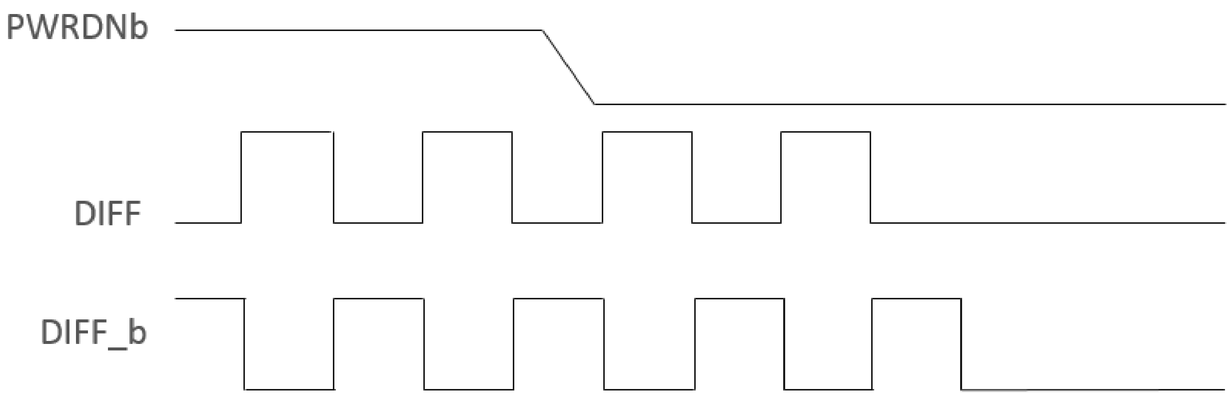


Figure 5.2. PWRDNb Assertion

5.7 PWRDNb (Power Down) Deassertion

When a valid rising edge on PWRDNb pin is applied, all outputs are enabled in a glitch-free manner within 520 µs.

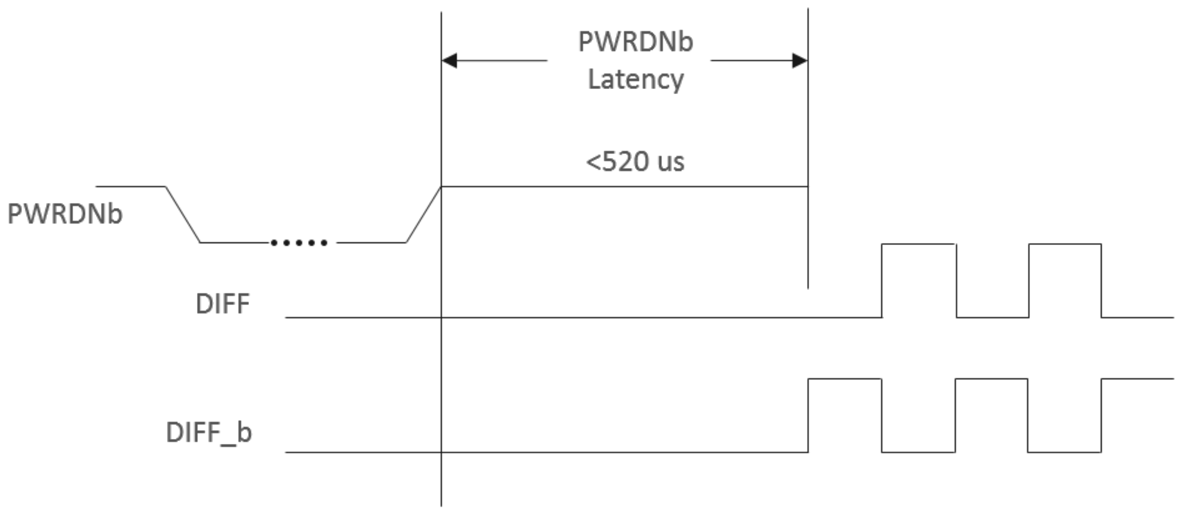


Figure 5.3. Subsequent Deassertion of PWRDNb

5.8 Power Supply Filtering Recommendations

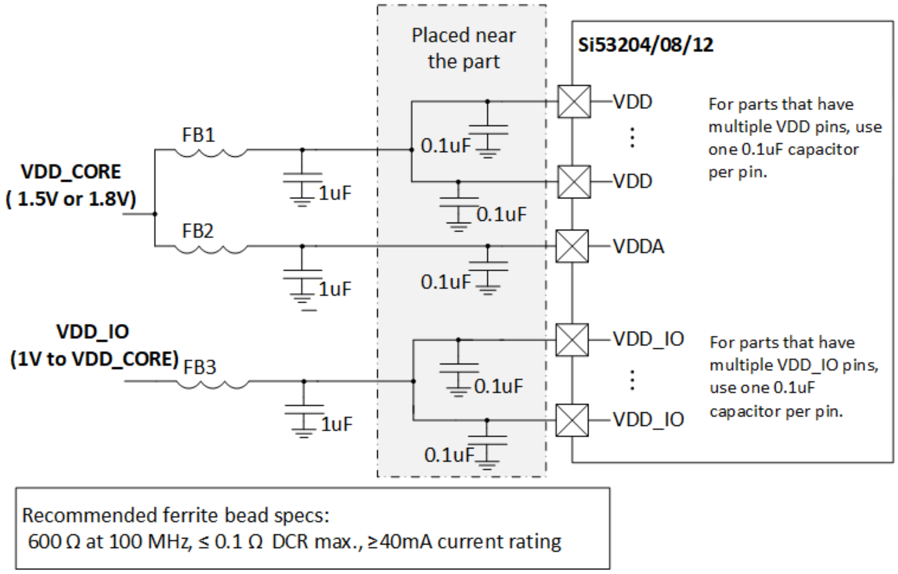


Figure 5.4. Power Supply Filtering

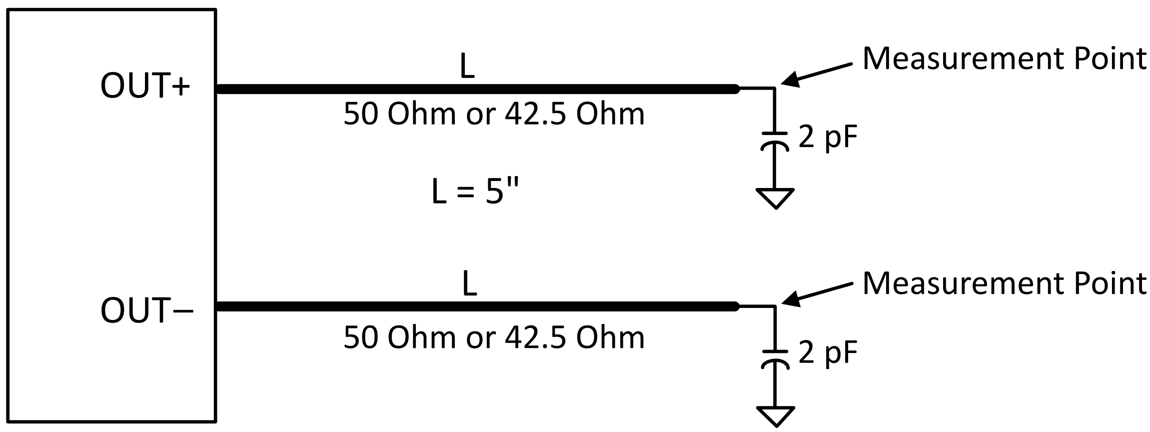
Separate out each type of VDD (VDD, VDDA, and VDD_IO) using ferrite beads. Then, for each VDD type, use one 1 uF bulk capacitor along with an additional 0.1 uF capacitor for each individual VDD pin. All VDD Core (VDD and VDDA) pins should be tied to the same voltage, either 1.8 V or 1.5 V. The VDD_IO pins can be tied to a voltage between 1 V and the selected VDD Core voltage.

Note: The VDD_IO pins must all be tied to the same voltage.

6. Test and Measurement Setup

The figures below show the test load configuration for differential clock signals.

Figure 6.1. 0.7 V Differential Load Configuration



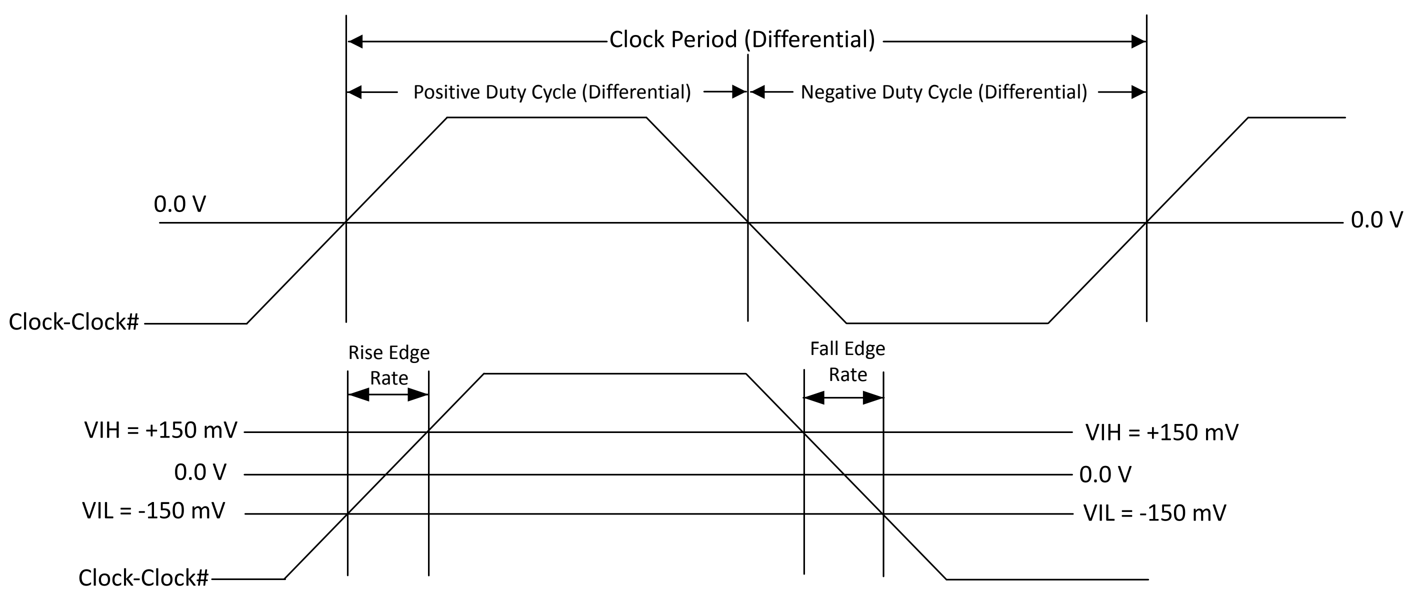


Figure 6.2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

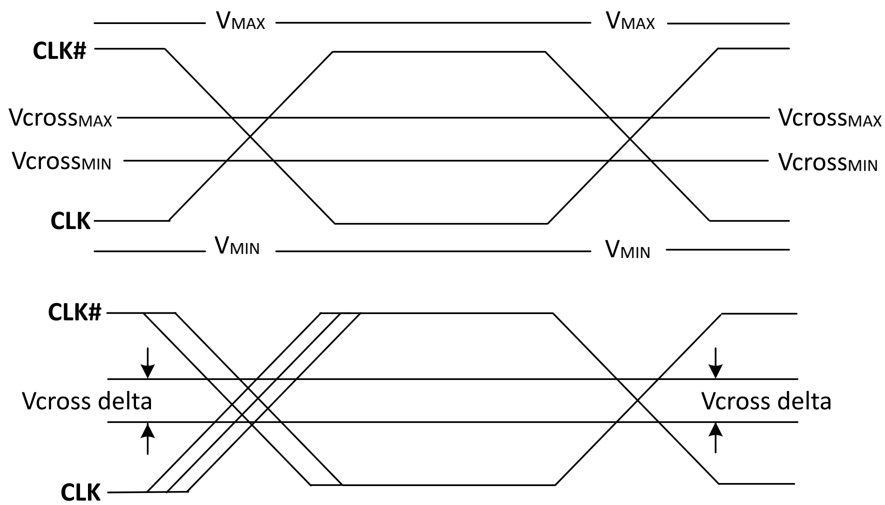


Figure 6.3. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

7. PCIe Clock Jitter Tool

The PCIe Clock Jitter Tool is designed to enable users to quickly and easily take jitter measurements for PCIe Gen1/2/3/4/5 and SRNS/SRIS. This software removes all the guesswork for PCIe Gen1/2/3/4/5 and SRNS/SRIS jitter measurements and margins in board designs.

This software tool will provide accurate results in just a few clicks, and is provided in an executable format to support various common input waveform files, such as .csv, .wfm, and .bin. The easy-to-use GUI and helpful tips guide users through each step. Release notes and other documentation are also included in the software package.

Download it for free https://www.skyworksinc.com/en/application-pages/pci-express-learning-center.

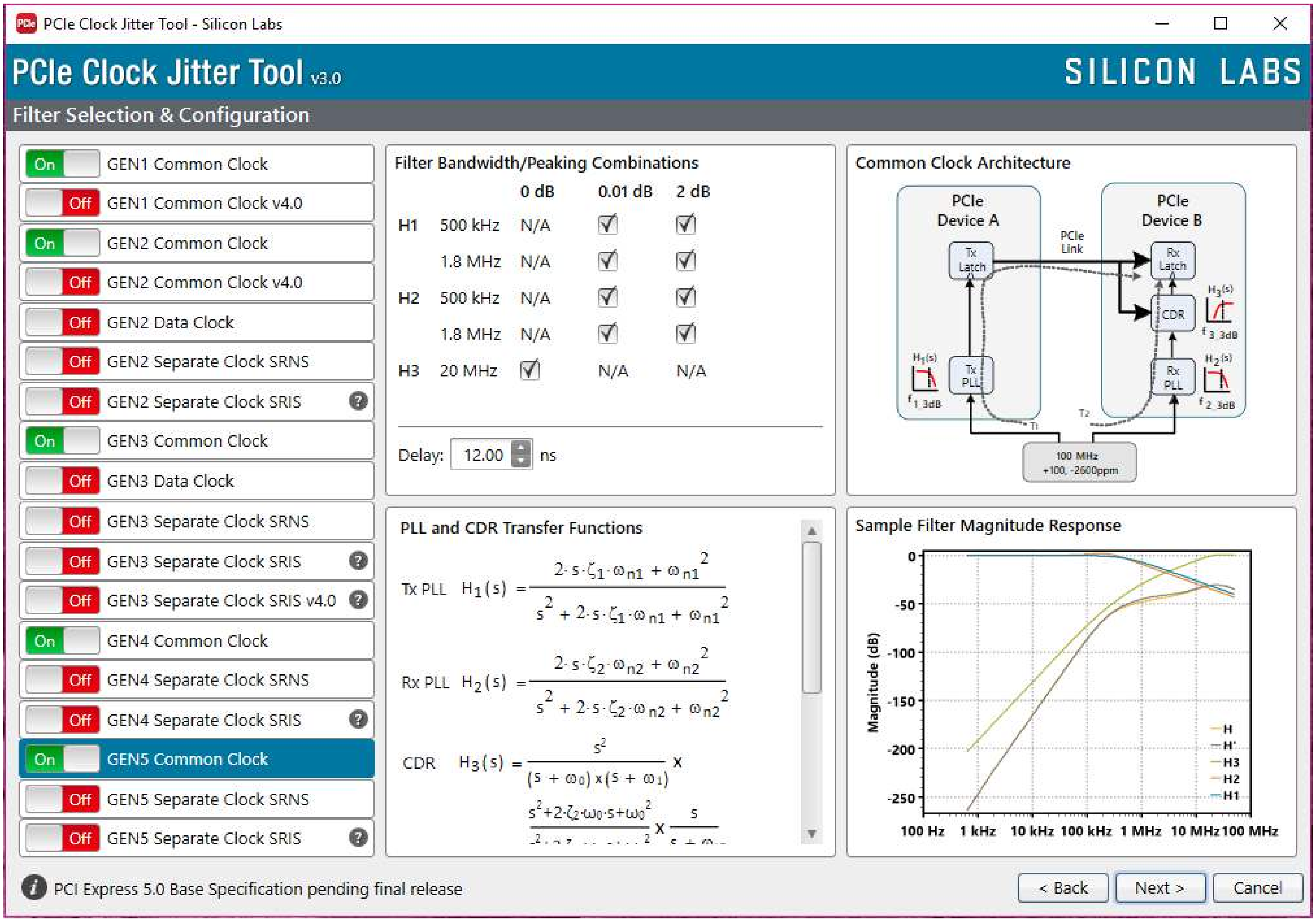


Figure 7.1. PCIe Clock Jittter Tool

8. Control Registers

8.1 I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I²C interface, various device functions, such as individual clock output buffers, are individually enabled or disabled. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

8.2 Block Read/Write

The clock driver I²C protocol accepts block write and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. The block write and block read protocol is outlined in Table 8.2 Block Read and Block Write Protocol on page 24.

8.3 Block Read

After the slave address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The slave acknowledges the register index in the command byte. The master sends a repeat start function. After the slave acknowledges this, the slave sends the number of bytes it wants to transfer (>0 and ≤7). The master acknowledges each byte except the last and sends a stop condition.

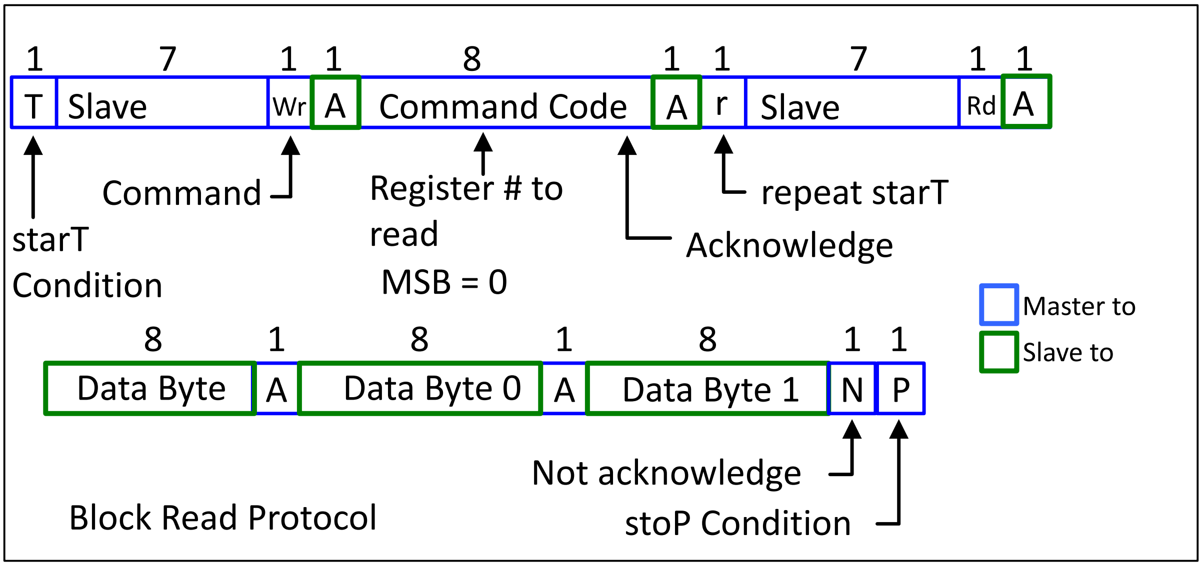


Figure 8.1. Block Read Protocol

8.4 Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a block write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 7. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

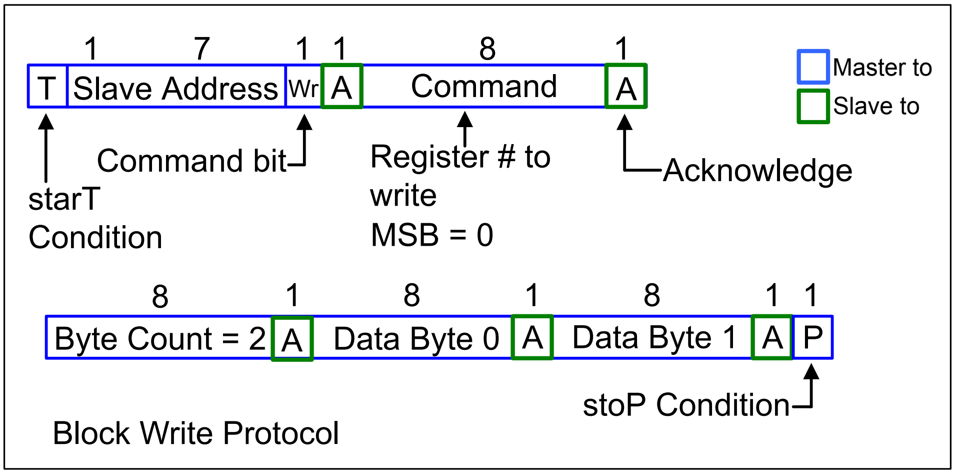


Figure 8.2. Block Write Protocol

8.5 Byte Read/Write

Reading or writing a register in an I^2C slave device in byte mode always involves specifying the register number. Refer to Table 8.3 Byte Read and Byte Write Protocol on page 25 for byte read and byte write protocol.

8.6 Byte Read

The standard byte read is as shown in the figure below. It is an extension of the byte write. The write start condition is repeated; then, the slave device starts sending data, and the master acknowledges it until the last byte is sent. The master terminates the transfer with a Nack, then a stop condition. For byte operation, the MSB bit of the command byte must be set. For block operations, the MSB bit must be set low. If the bit is not set low, the next byte must be the byte transfer count.

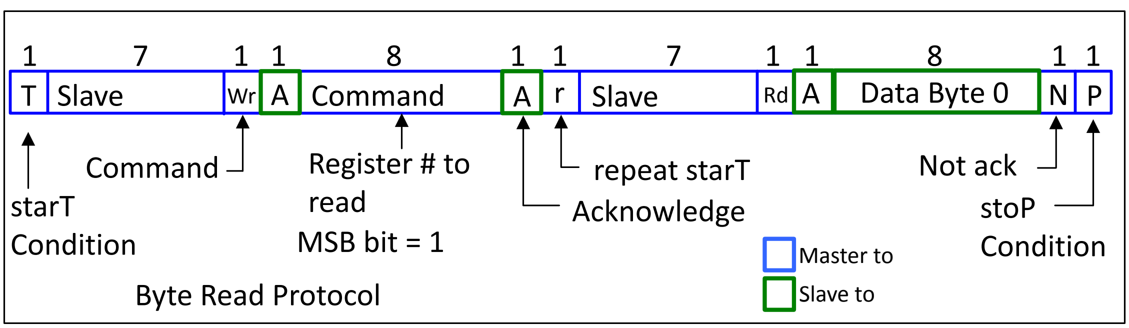


Figure 8.3. Byte Read Protocol

8.7 Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a block write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 7. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

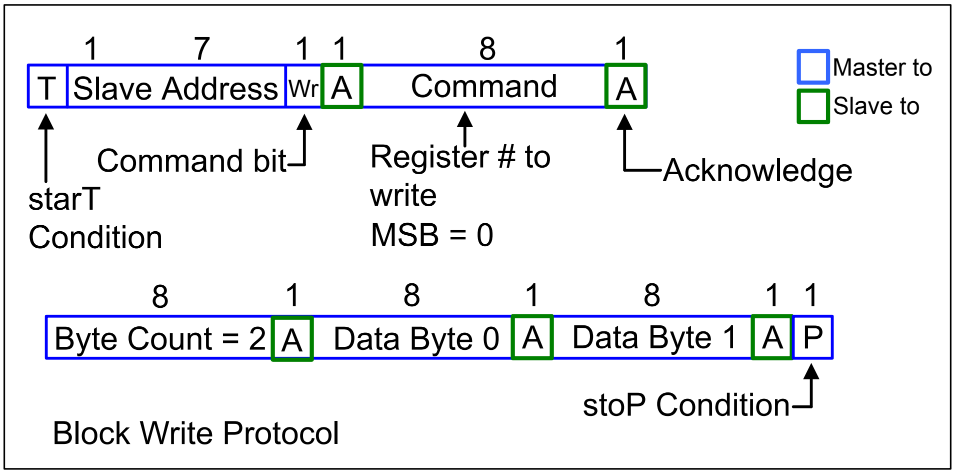


Figure 8.4. Block Write Protocol

8.8 Data Protocol

The clock driver I^2C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operations, the system controller can access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The block write and block read protocol is outlined in Table 8.2 Block Read and Block Write Protocol on page 24 while Table 8.3 Byte Read and Byte Write Protocol on page 25 outlines byte write and byte read protocol. SA is the address select for I^2C. When the part is powered up, SA will be latched to select the I^2C address.

Table 8.1. SA State on First Application of PWRDNb

Description	SA	Address
State of SA on first deassertion of PWRDNb	0	1101001
	1	1101010

Table 8.2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 8.3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

8.9 Register Tables

8.9.1 Si53212 Registers

Table 8.4. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	DIFF7_OE	Disabled	Enabled	RW	1	Output enable for DIFF[7]
6	DIFF6_OE	Disabled	Enabled	RW	1	Output enable for DIFF[6]
5	DIFF5_OE	Disabled	Enabled	RW	1	Output enable for DIFF[5]
4	DIFF4_OE	Disabled	Enabled	RW	1	Output enable for DIFF[4]
3	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF[3]
2	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF[2]
1	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF[1]
0	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF[0]

Table 8.5. Control Register 1. Byte 1

<table>
<tr><th>Bit</th><th>Name</th><th>If Bit = 0</th><th>If Bit = 1</th><th>Type</th><th>Default</th><th>Function</th></tr>
<tr><td>7</td><td>DIFF11_OE</td><td>Disabled</td><td>Enabled</td><td>RW</td><td>1</td><td>Output enable for DIFF[11]</td></tr>
<tr><td>6</td><td>DIFF10_OE</td><td>Disabled</td><td>Enabled</td><td>RW</td><td>1</td><td>Output enable for DIFF[10]</td></tr>
<tr><td>5</td><td>DIFF9_OE</td><td>Disabled</td><td>Enabled</td><td>RW</td><td>1</td><td>Output enable for DIFF[9]</td></tr>
<tr><td>4</td><td>DIFF8_OE</td><td>Disabled</td><td>Enabled</td><td>RW</td><td>1</td><td>Output enable for DIFF[8]</td></tr>
<tr><td>3</td><td colspan="4" rowspan="4">Reserved</td><td>0</td><td rowspan="4">Reserved</td></tr>
<tr><td>2</td><td>0</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td></tr>
</table>

Table 8.6. Control Register 2. Byte 2

Reserved

Table 8.7. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF7	Slow setting	Fast setting	RW	1	Slew rate control for DIFF7
6	SR_SEL_DIFF6	Slow setting	Fast setting	RW	1	Slew rate control for DIFF6
5	SR_SEL_DIFF5	Slow setting	Fast setting	RW	1	Slew rate control for DIFF5
4	SR_SEL_DIFF4	Slow setting	Fast setting	RW	1	Slew rate control for DIFF4
3	SR_SEL_DIFF3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF3
2	SR_SEL_DIFF2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF2
1	SR_SEL_DIFF1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF1
0	SR_SEL_DIFF0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF0

Table 8.8. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF11	Slow setting	Fast setting	RW	1	Slew rate control for DIFF11
6	SR_SEL_DIFF10	Slow setting	Fast setting	RW	1	Slew rate control for DIFF10
5	SR_SEL_DIFF9	Slow setting	Fast setting	RW	1	Slew rate control for DIFF9
4	SR_SEL_DIFF8	Slow setting	Fast setting	RW	1	Slew rate control for DIFF8
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.9. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID [3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.10. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

8.9.2 Si53208 Registers

Table 8.11. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	DIFF4_OE	Disabled	Enabled	RW	1	Output enable for DIFF_4
5	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF_3
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF_2
1	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF_1
0	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF_0

Table 8.12. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	DIFF7_OE	Disabled	Enabled	RW	1	Output enable for DIFF_7
6	DIFF6_OE	Disabled	Enabled	RW	1	Output enable for DIFF_6
5	Reserved				0	Reserved
4	DIFF5_OE	Disabled	Enabled	RW	1	Output enable for DIFF_5
3	Reserved				0	Reserved
2					0	
1					0	
0					0	

Table 8.13. Control Register 2. Byte 2

Reserved

Table 8.14. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	SR_SEL_DIFF_4	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_4
5	SR_SEL_DIFF_3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_3
4	Reserved			RW	1	Reserved
3	Reserved			RW	1	Reserved
2	SR_SEL_DIFF_2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_2
1	SR_SEL_DIFF_1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_1
0	SR_SEL_DIFF_0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_0

Table 8.15. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	SR_SEL_DIFF_7	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_7
6	SR_SEL_DIFF_6	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_6
5	Reserved			RW	1	Reserved
4	SR_SEL_DIFF_5	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_5
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.16. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID [3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.17. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

8.9.3 Si53204 Registers

Table 8.18. Control Register 0. Byte 0

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	DIFF2_OE	Disabled	Enabled	RW	1	Output enable for DIFF_2
5	DIFF1_OE	Disabled	Enabled	RW	1	Output enable for DIFF_1
4	Reserved				0	Reserved
3	Reserved				0	Reserved
2	DIFF0_OE	Disabled	Enabled	RW	1	Output enable for DIFF_0
1	Reserved			RW	0	Reserved
0	Reserved			RW	0	Reserved

Table 8.19. Control Register 1. Byte 1

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved				0	Reserved
6	Reserved				0	Reserved
5	Reserved				0	Reserved
4	DIFF3_OE	Disabled	Enabled	RW	1	Output enable for DIFF_3
3	Reserved				0	Reserved
2					0	
1					0	
0					0	

Table 8.20. Control Register 2. Byte 2

Reserved

Table 8.21. Control Register 3. Byte 3

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	SR_SEL_DIFF_2	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_2
5	SR_SEL_DIFF_1	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_1
4	Reserved			RW	1	Reserved
3	Reserved			RW	1	Reserved
2	SR_SEL_DIFF_0	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_0
1	Reserved			RW	1	Reserved
0	Reserved			RW	1	Reserved

Table 8.22. Control Register 4. Byte 4

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Reserved			RW	1	Reserved
6	Reserved			RW	1	Reserved
5	Reserved			RW	1	Reserved
4	SR_SEL_DIFF_3	Slow setting	Fast setting	RW	1	Slew rate control for DIFF_3
3	AMP			RW	1	DIFF Differential Outputs Amplitude Adjustment. 0110 : 600 mV 0111 : 650 mV 1000 : 700 mV 1001 : 750 mV 1010 : 800 mV 1011 : 850 mV
2	AMP			RW	0	
1	AMP			RW	0	
0	AMP			RW	0	

Table 8.23. Control Register 5. Byte 5

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Rev Code [7:4]			R	0	Revision Code
6				R	0	
5				R	0	
4				R	0	
3	Vendor ID [3:0]			R	1	Vendor Identification Code
2				R	0	
1				R	0	
0				R	0	

Table 8.24. Control Register 6. Byte 6

Bit	Name	If Bit = 0	If Bit = 1	Type	Default	Function
7	Programming ID [7:0]			R	0	Programming ID (Internal Only)
6				R	0	
5				R	0	
4				R	0	
3				R	0	
2				R	0	
1				R	0	
0				R	0	

9. Pin Descriptions

9.1 Si53212 Pin Descriptions

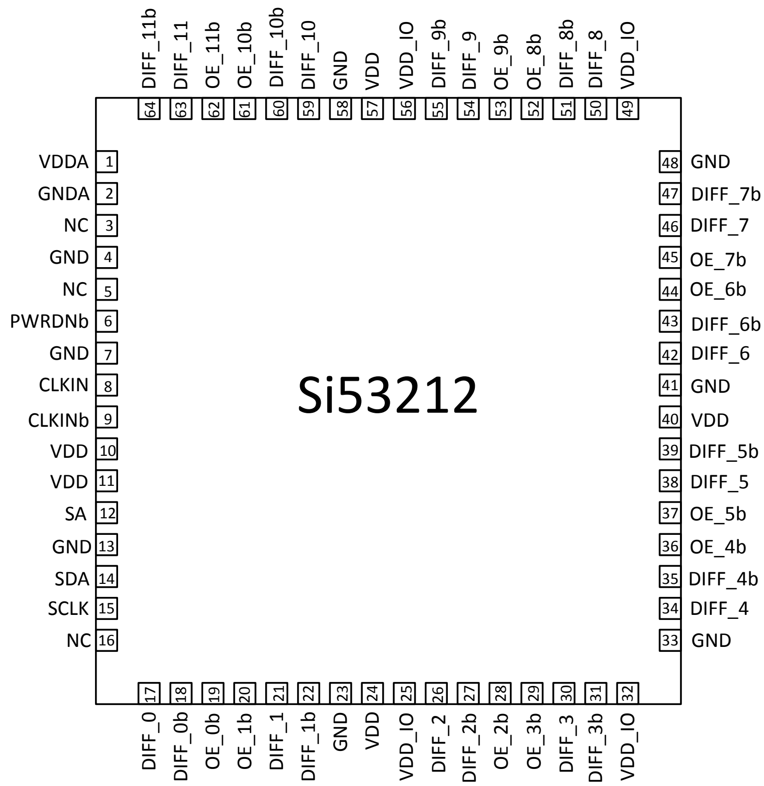


Figure 9.1. 64-Pin QFN

Table 9.1. Si53212 64-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	PWR	Analog Power Supply
2	GNDA	GND	Analog Ground
3	NC	NC	No connect
4	GND	GND	Ground
5	NC	NC	No connect
6	PWRDNb	I	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal 100 kΩ pull-up).
7	GND	GND	Ground
8	CLKIN	I	Clock input
9	CLKINb	I	Complementary clock input
10	VDD	PWR	Power supply
11	VDD	PWR	Power supply
12	SA	I	Address select for I^2C (this pin has an internal 60 kΩ pull-up)

Pin #	Name	Type	Description
13	GND	GND	Ground
14	SDA	I/O	I^2C compatible SDATA
15	SCLK	I	I^2C compatible SCLOCK
16	NC	NC	No connect
17	DIFF_0	O, DIF	HCSL DIFF_0, true
18	DIFF_0b	O, DIF	HCSL DIFF_0, complement
19	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
20	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
21	DIFF_1	O, DIF	HCSL DIFF_1, true
22	DIFF_1b	O, DIF	HCSL DIFF_1, complement
23	GND	GND	Ground
24	VDD	PWR	Power supply
25	VDD_IO	PWR	Output power supply
26	DIFF_2	O, DIF	HCSL DIFF_2, true
27	DIFF_2b	O, DIF	HCSL DIFF_2, complement
28	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
29	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
30	DIFF_3	O, DIF	HCSL DIFF_3, true
31	DIFF_3b	O, DIF	HCSL DIFF_3, complement
32	VDD_IO	PWR	Output power supply
33	GND	GND	Ground
34	DIFF_4	O, DIF	HCSL DIFF_4, true
35	DIFF_4b	O, DIF	HCSL DIFF_4, complement
36	OE_4b	I, PD	Output enable for DIFF_4 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
37	OE_5b	I, PD	Output enable for DIFF_5 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
38	DIFF_5	O, DIF	HCSL DIFF_5, true
39	DIFF_5b	O, DIF	HCSL DIFF_5, complement
40	VDD	PWR	Power supply
41	GND	GND	Ground
42	DIFF_6	O, DIF	HCSL DIFF_6, true
43	DIFF_6b	O, DIF	HCSL DIFF_6, complement
44	OE_6b	I, PD	Output enable for DIFF_6 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs

Pin #	Name	Type	Description
45	OE_7b	I, PD	Output enable for DIFF_7 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
46	DIFF_7	O, DIF	HCSL DIFF_7, true
47	DIFF_7b	O, DIF	HCSL DIFF_7, complement
48	GND	GND	Ground
49	VDD_IO	PWR	Output power supply
50	DIFF_8	O, DIF	HCSL DIFF_8, true
51	DIFF_8b	O, DIF	HCSL DIFF_8, complement
52	OE_8b	I, PD	Output enable for DIFF_8 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
53	OE_9b	I, PD	Output enable for DIFF_9 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
54	DIFF_9	O, DIF	HCSL DIFF_9, true
55	DIFF_9b	O, DIF	HCSL DIFF_9, complement
56	VDD_IO	PWR	Output power supply
57	VDD	PWR	Power supply
58	GND	GND	Ground
59	DIFF_10	O, DIF	HCSL DIFF_10, true
60	DIFF_10b	O, DIF	HCSL DIFF_10, complement
61	OE_10b	I, PD	Output enable for DIFF_10 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
62	OE_11b	I, PD	Output enable for DIFF_11 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
63	DIFF_11	O, DIF	HCSL DIFF_11, true
64	DIFF_11b	O, DIF	HCSL DIFF_11, complement
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

9.2 Si53208 Pin Descriptions

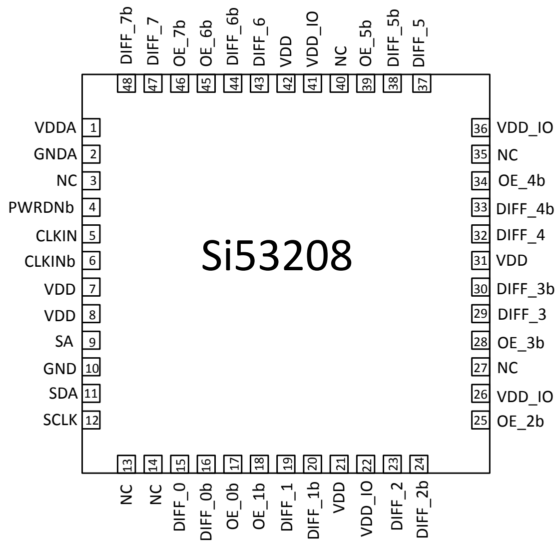


Figure 9.2. 48-pin QFN

Table 9.2. Si53208 48-pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	PWR	Analog Power Supply
2	GNDA	GND	Analog Ground
3	NC	NC	No connect
4	PWRDNb	I	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal 100 kΩ pull-up).
5	CLKIN	I	Clock input.
6	CLKINb	I	Complementary clock input
7	VDD	PWR	Power supply
8	VDD	PWR	Power supply
9	SA	I	Address select for I^2C (this pin has an internal 60 kΩ pull-up)
10	GND	GND	Ground
11	SDA	I/O	I^2C compatible SDATA
12	SCLK	I	I^2C compatible SCLOCK
13	NC	NC	No connect
14	NC	NC	No connect
15	DIFF_0	O, DIF	HCSL DIFF_0, true
16	DIFF_0b	O, DIF	HCSL DIFF_0, complement
17	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs

Pin #	Name	Type	Description
18	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
19	DIFF_1	O, DIF	HCSL DIFF_1, true
20	DIFF_1b	O, DIF	HCSL DIFF_1, complement
21	VDD	PWR	Power supply
22	VDD_IO	PWR	Output power supply
23	DIFF_2	O, DIF	HCSL DIFF_2, true
24	DIFF_2b	O, DIF	HCSL DIFF_2, complement
25	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
26	VDD_IO	PWR	Output power supply
27	NC	NC	No connect
28	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
29	DIFF_3	O, DIF	HCSL DIFF_3, true
30	DIFF_3b	O, DIF	HCSL DIFF_3, complement
31	VDD	PWR	Power supply
32	DIFF_4	O, DIF	HCSL DIFF_4, true
33	DIFF_4b	O, DIF	HCSL DIFF_4, complement
34	OE_4b	I, PD	Output enable for DIFF_4 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
35	NC	NC	No connect
36	VDD_IO	PWR	Output power supply
37	DIFF_5	O, DIF	HCSL DIFF_5, true
38	DIFF_5b	O, DIF	HCSL DIFF_5, complement
39	OE_5b	I, PD	Output enable for DIFF_5 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
40	NC	NC	No connect
41	VDD_IO	PWR	Output power supply
42	VDD	PWR	Power supply
43	DIFF_6	O, DIF	HCSL DIFF_6, true
44	DIFF_6b	O, DIF	HCSL DIFF_6, complement
45	OE_6b	I, PD	Output enable for DIFF_6 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
46	OE_7b	I, PD	Output enable for DIFF_7 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
47	DIFF_7	O, DIF	HCSL DIFF_7, true
48	DIFF_7b	O, DIF	HCSL DIFF_7, complement
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

9.3 Si53204 Pin Descriptions

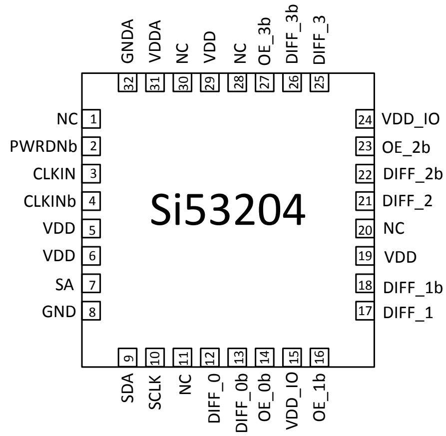


Figure 9.3. 32-pin QFN

Table 9.3. Si53204 32-pin QFN Descriptions

Pin #	Name	Type	Description
1	NC	NC	No connect
2	PWRDNb	I	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal 100 kΩ pull-up).
3	CLKIN	I	Clock input.
4	CLKINb	I	Complementary clock input
5	VDD	PWR	Power supply
6	VDD	PWR	Power supply
7	SA	I	Address select for I^2C (this pin has an internal 60 kΩ pull-up)
8	GND	GND	Ground
9	SDA	I/O	I^2C compatible SDATA
10	SCLK	I	I^2C compatible SCLOCK
11	NC	NC	No connect
12	DIFF_0	O, DIF	HCSL DIFF_0, true
13	DIFF_0b	O, DIF	HCSL DIFF_0, complement
14	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
15	VDD_IO	PWR	Output power supply
16	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
17	DIFF_1	O, DIF	HCSL DIFF_1, true
18	DIFF_1b	O, DIF	HCSL DIFF_1, complement
19	VDD	PWR	Power supply

Pin #	Name	Type	Description
20	NC	NC	No connect
21	DIFF_2	O, DIF	HCSL DIFF_2, true
22	DIFF_2b	O, DIF	HCSL DIFF_2, complement
23	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
24	VDD_IO	PWR	Output power supply
25	DIFF_3	O, DIF	HCSL DIFF_3, true
26	DIFF_3b	O, DIF	HCSL DIFF_3, complement
27	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal 100 kΩ pull-down). 0 = Enable outputs; 1 = Disable outputs
28	NC	NC	No connect
29	VDD	PWR	Power supply
30	NC	NC	No connect
31	VDDA	PWR	Analog Power Supply
32	GNDA	GND	Analog Ground
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

10. Packaging

10.1 Si53212 Package

The figure below illustrates the package details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

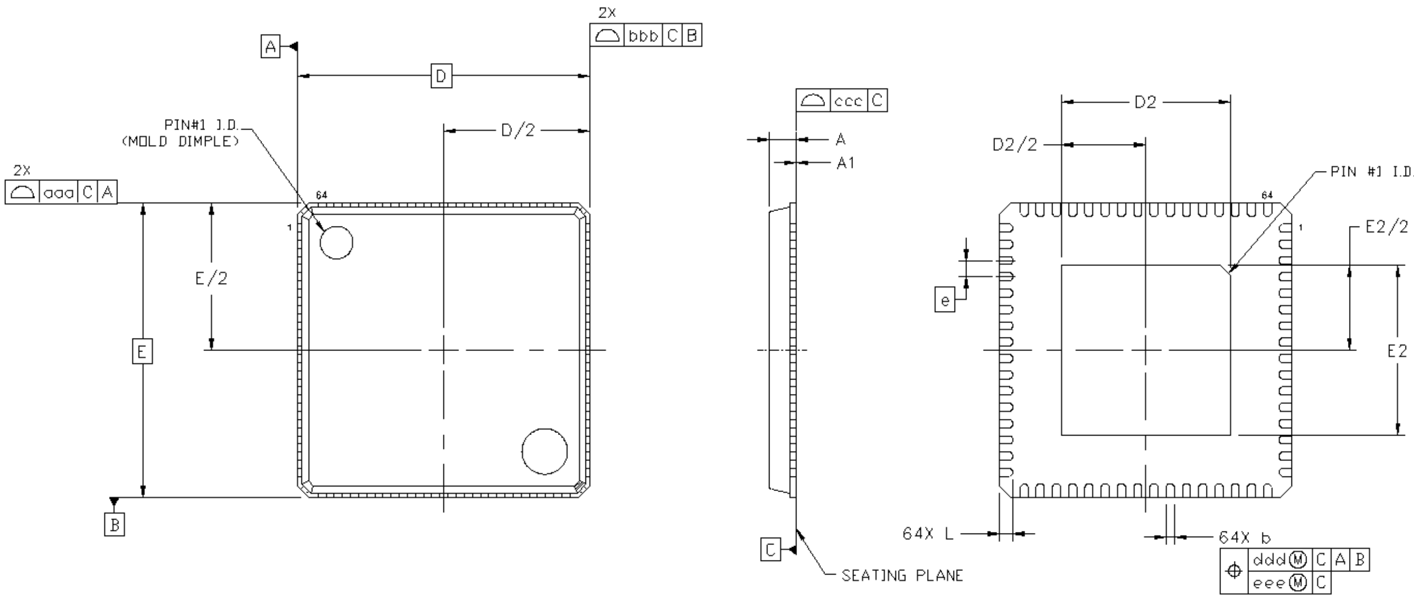


Figure 10.1. 64L 9 x 9 mm QFN Package Diagram

Table 10.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020D specification for Small Body Components.

10.2 Si53212 Land Pattern

The following figure illustrates the land pattern details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

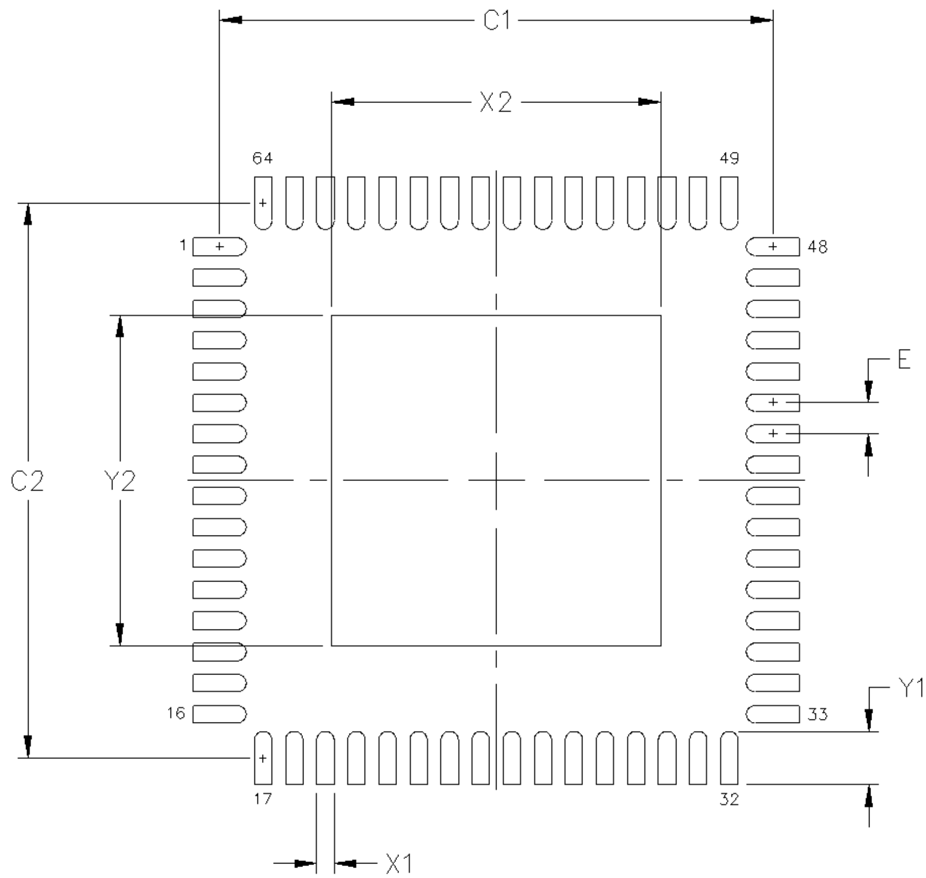


Figure 10.2. 64L 9 x 9 mm QFN Land Pattern

Table 10.2. PCB Land Pattern Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Dimension	mm

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.25 mm square openings on a 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 Si53208 Package

The figure below illustrates the package details for the Si53208 in a 48-Lead 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

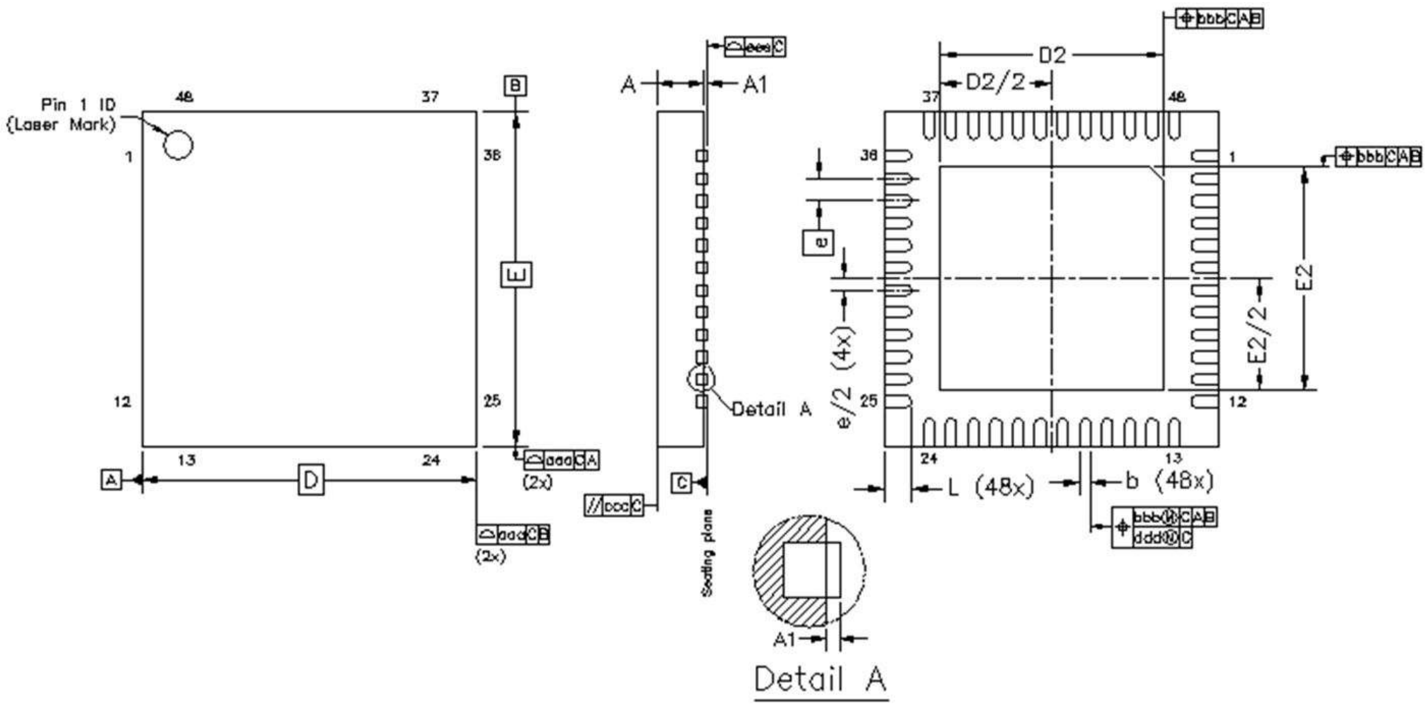


Figure 10.3. 48L 6 x 6 mm QFN Package Diagram

Table 10.3. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		6.00 BSC	
D2	3.5	3.6	3.7
e		0.40 BSC	
E		6.00 BSC	
E2	3.5	3.6	3.7
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

10.4 Si53208 Land Pattern

The figure below illustrates the land pattern details for the Si53208 in a 48-Lead, 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

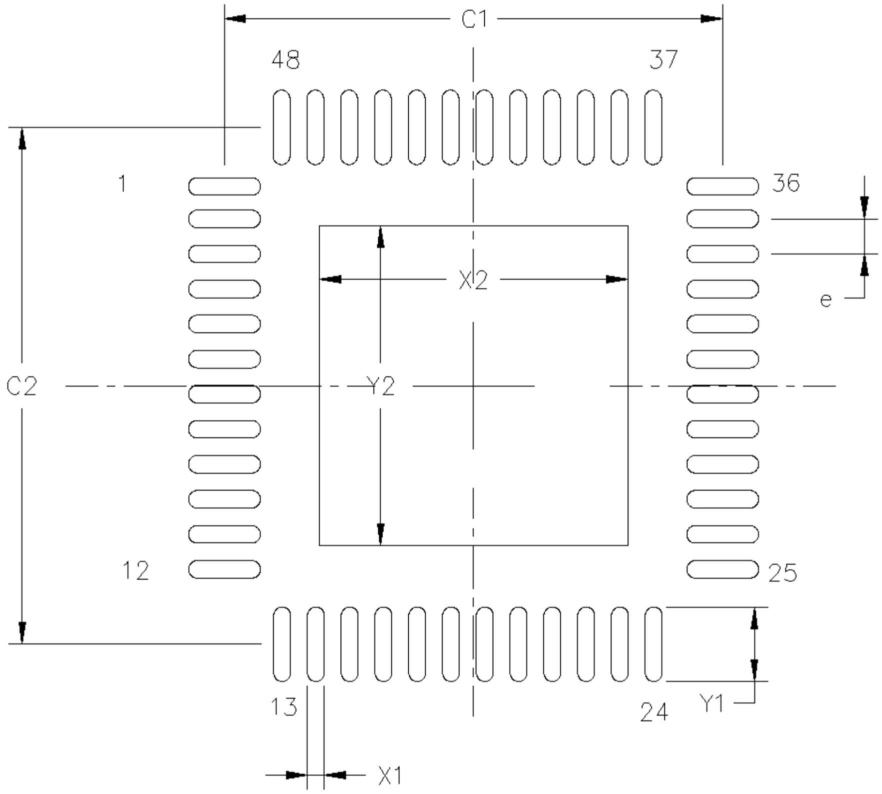


Figure 10.4. 48L 6 x 6 mm QFN Land Pattern

Table 10.4. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
X1	0.20
X2	3.60
Y1	0.85
Y2	3.60
e	0.40 BSC

Dimension	mm
Notes: **General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads. 4. A 3x3 array of 0.90 mm square openings on 1.15mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.	

10.5 Si53204 Package

The figure below illustrates the package details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

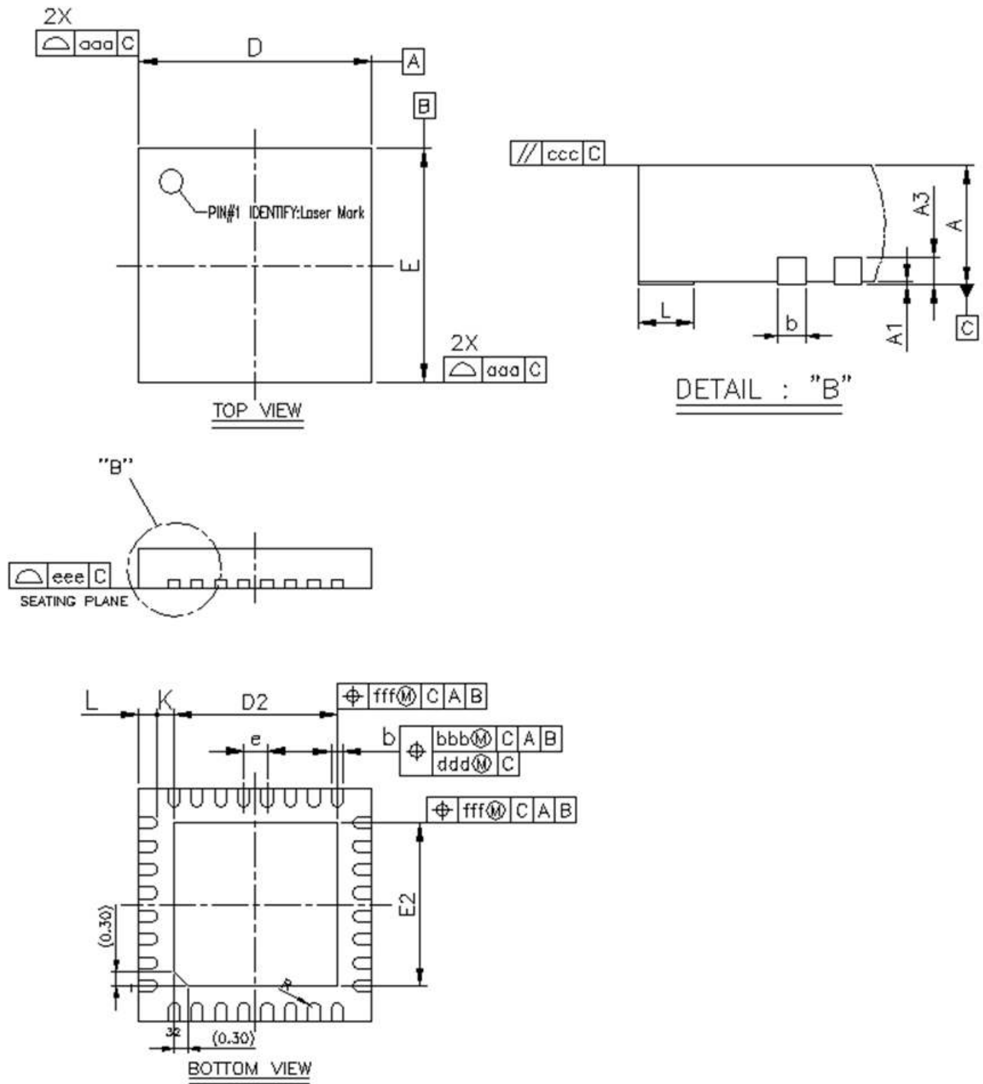


Figure 10.5. 32L 5 x 5 mm QFN Package Diagram

Table 10.5. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
K	0.20	—	—
L	0.30	0.40	0.50

Dimension	Min	Nom	Max
R	0.09	—	0.14
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

10.6 Si53204 Land Pattern

The figure below illustrates the land pattern details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

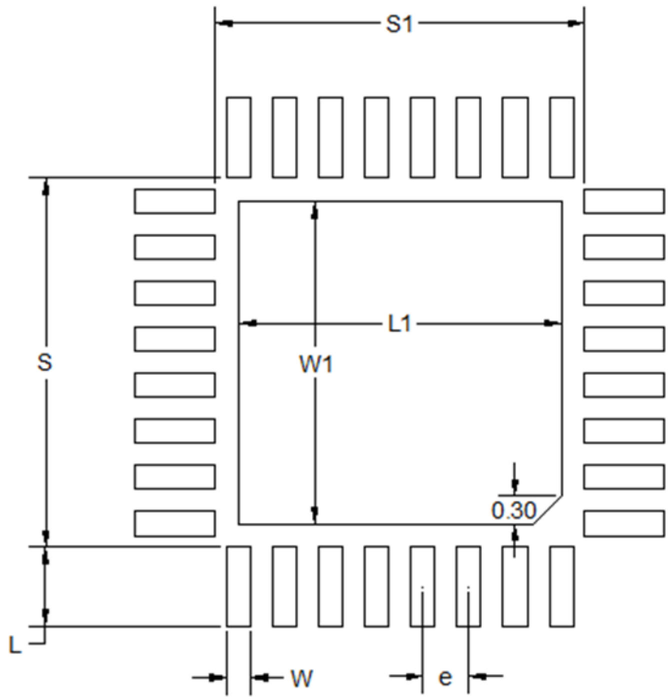


Figure 10.6. 32L 5 x 5 mm QFN Land Pattern

Table 10.6. PCB Land Pattern Dimensions

Dimension	mm
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Dimension	mm

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3x3 array of 0.85 mm square openings on 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.7 Si53212 Top Markings

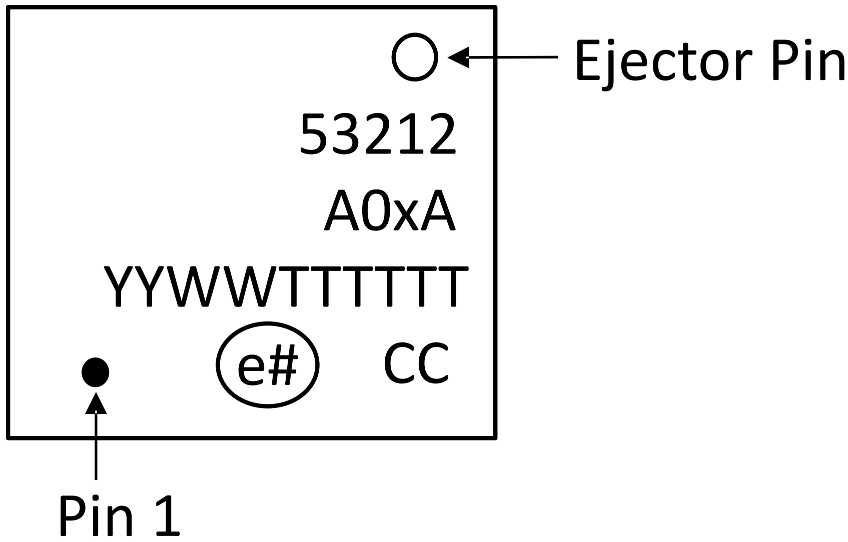


Figure 10.7. Si53212 Top Marking

Table 10.7. Si53212 Top Marking Explanation

Line	Characters	Description
1	53212	Device part number
2	A0xA	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	YYWWTTTTTT	YY = Assembly year WW = Assembly work week TTTTTT = Manufacturing trace code

4	e# CC	e# = Lead-finish symbol. # is a number
		CC = Country of origin (ISO abbreviation)

10.8 Si53208 Top Markings

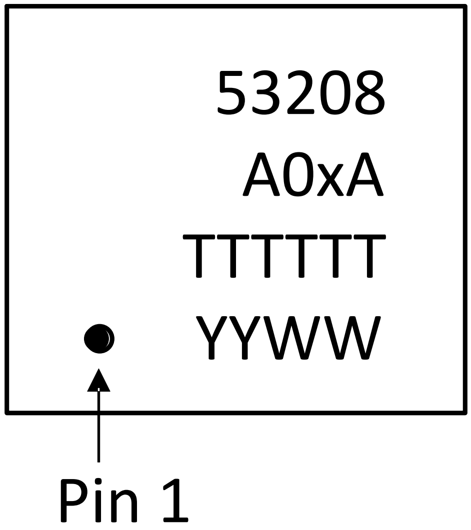


Figure 10.8. Si53208 Top Marking

Table 10.8. Si53208 Top Marking Explanation

Line	Characters	Description
1	53208	Device part number
2	A0xA	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	TTTTTT	Manufacturing trace code
4	YYWW	YY = Assembly year WW = Assembly work week

10.9 Si53204 Top Markings

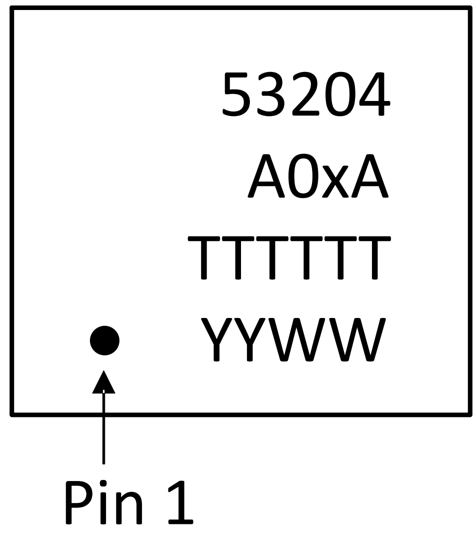


Figure 10.9. Si53204 Top Marking

Table 10.9. Si53204 Top Marking Explanation

Line	Characters	Description
1	53204	Device part number
2	A0xA	Device part number x = 1 = Internal 100 Ω impedance matching x = 2 = Internal 85 Ω impedance matching
3	TTTTTT	Manufacturing trace code
4	YYWW	YY = Assembly year WW = Assembly work week

11. Revision History

Revision 1.0

March, 2019

- Updated Electrical Specifications.
  - Updated Table 4.1 DC Electrical Specifications (VDD = 1.5 V ±5%) on page 7.
  - Updated Table 4.2 DC Electrical Specifications (VDD = 1.8 V ±5%) on page 9.
  - Updated Table 4.3 AC Electrical Specifications on page 11.
- Updated OEb Pin.
- Updated OEb Assertion.
- Updated OEb Deassertion.
- Added SA Pin.
- Added PWRDNb (Power Down) Pin.
- Added PWRDNb (Power Down) Assertion.
- Added PWRDNb (Power Down) Deassertion.
- Added Power Supply Filtering Recommendations.
- Updated Test and Measurement Setup.
- Added Control Registers.
- Updated Pin Descriptions.

Revision 0.7

March, 2018

- Initial release.

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