TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

## SSM6N7002BFE

# High-Speed Switching Applications Analog Switch Applications

Small package

• Low ON-resistance :  $R_{DS(ON)} = 3.3 \Omega \text{ (max) } (@V_{GS} = 4.5 \text{ V})$ 

:  $R_{DS(ON)} = 2.6 \Omega \text{ (max) } (@V_{GS} = 5 \text{ V})$ 

:  $R_{DS(ON)} = 2.1 \Omega \text{ (max) } (@V_{GS} = 10 \text{ V})$ 

#### Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		$V_{DSS}$	60	V	
Gate-source voltage		V <sub>GSS</sub>	±20	V	
Drain current	DC	ID	200	mA	
	Pulse	I <sub>DP</sub>	800		
Power dissipation		P <sub>D</sub> (Note 1)	150	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

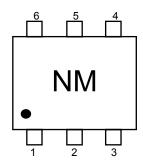
Unit: mm 1.6±0.05 1.2±0.05  $.6\pm0.05$ .0±0.05 4.SOURCE2 1.SOURCE1 5.GATE2 2.GATE1 3.DRAIN2 6.DRAIN1 ES<sub>6</sub> **JEDEC** JEITA **TOSHIBA** 2-2N1D

Weight: 3.0 mg (typ.)

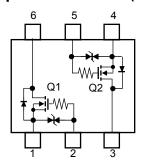
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:Total rating, mounted on FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu Pad: 0.135mm<sup>2</sup>  $\times$  6)

#### Marking



### **Equivalent Circuit (top view)**

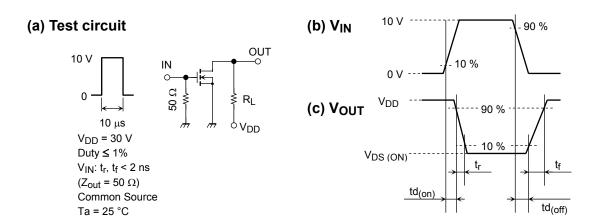


#### Electrical Characteristics (Ta = 25°C)(Q1, Q2 Common)

Char	acteristics	Symbol	Test Condition		Min	Тур	Max	Unit
Gate leakage curr	ent	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±10	μΑ
Drain-source breakdown voltage		V (BR) DSS	$I_D$ = 10 mA, $V_{GS}$ = 0 V $I_D$ = 10 mA, $V_{GS}$ = -10 V		60	_	_	V
		V (BR) DSX			45			
Drain cutoff currer	nt	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$		_		1	μА
Gate threshold vo	Itage	$V_{th}$	$V_{DS}$ = 10 V, $I_{D}$ = 0.25 mA		1.5	_	3.1	٧
Forward transfer a	admittance	Y <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$	(Note 2)	225	_	_	mS
Drain-source ON-resistance		R <sub>DS</sub> (ON)	$I_D = 500 \text{ mA}, V_{GS} = 10 \text{ V}$	(Note 2)	_	1.62	2.1	Ω
			$I_D = 100 \text{ mA}, V_{GS} = 5 \text{ V}$	(Note 2)	_	1.90	2.6	
			$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$	(Note 2)	_	2.10	3.3	
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		_	17.0	_	pF
Reverse transfer capacitance		C <sub>rss</sub>			_	1.9	_	
Output capacitance		Coss			_	3.6	_	
Switching time	Turn-on delay time	td <sub>(on)</sub>	$V_{DD} = 30 \text{ V}$ , $I_D$ = 200 mA, $V_{GS} = 0$ to 10 V		_	3.3	6.6	ns
	Turn-off delay time	td <sub>(off)</sub>			_	14.5	40	115
Drain-source forward voltage		V <sub>DSF</sub>	I <sub>D</sub> = -200 mA, V <sub>GS</sub> = 0 V	(Note 2)	_	-0.84	-1.2	V

Note2: Pulse test

#### **Switching Time Test Circuit**



#### **Precaution**

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current (I<sub>D</sub>) to be low (0.25 mA for the SSM6N7002BFE). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ . Take this into consideration when using the device

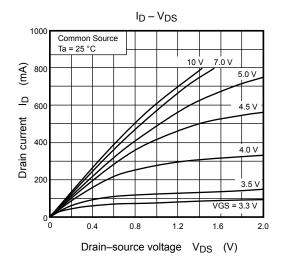
#### **Handling Precaution**

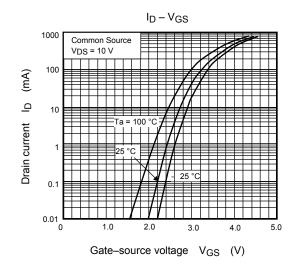
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

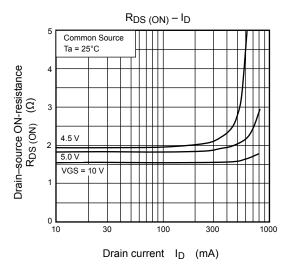
Thermal resistance  $R_{th\ (ch-a)}$  and Power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

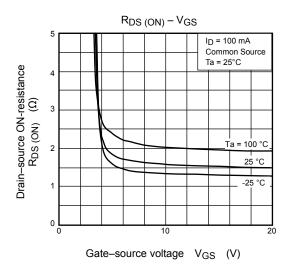
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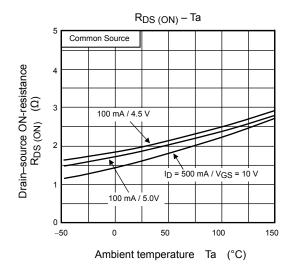
(Q1, Q2 Common)

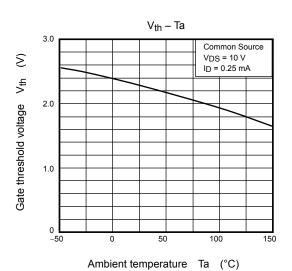






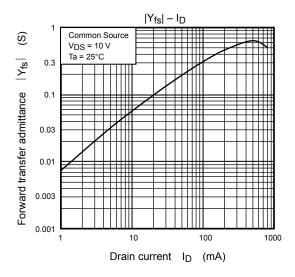


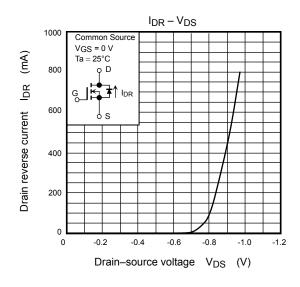


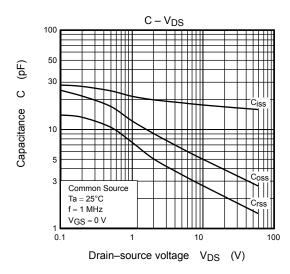


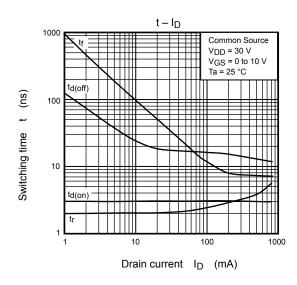
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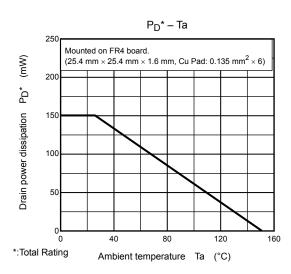
(Q1, Q2 Common)











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