

August 1991

Features

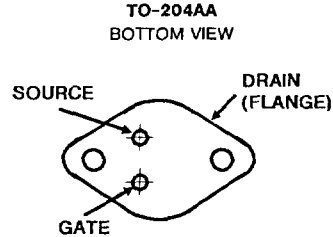
- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)} = 1.0\Omega$ and 1.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

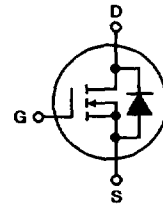
These types are supplied in the JEDEC TO-204AA steel package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

| | 2N6759 | 2N6760 | UNITS |
|--|-------------------|-------------------|---------------------|
| Drain-Source Voltage | 350* | 400* | V |
| Drain-Gate Voltage ($R_{GS} = 20k\Omega$) | 350* | 400* | V |
| Continuous Drain Current | | | |
| $T_C = +25^\circ\text{C}$ | 4.5* | 5.5* | A |
| $T_C = +100^\circ\text{C}$ | 3.0* | 3.5* | A |
| Pulsed Drain Current | 7.0 | 8.0 | A |
| Gate-Source Voltage | ± 20 | ± 20 | V |
| Maximum Power Dissipation | | | |
| $T_C = +25^\circ\text{C}$ (See Figure 11) | 75* | 75* | W |
| $T_C = +100^\circ\text{C}$ (See Figure 11) | 30* | 30* | W |
| Linear Derating Factor (See Figure 11) | 0.6* | 0.6* | W/ $^\circ\text{C}$ |
| Inductive Current, Clamped | 7.0 | 8.0 | A |
| (See Figures 1 and 2, $L = 100\mu\text{H}$) | | | |
| Operating and Storage Junction Temperature Range | -55 to $+150^*$ | -55 to $+150^*$ | $^\circ\text{C}$ |
| Maximum Lead Temperature for Soldering | 300* | 300* | $^\circ\text{C}$ |
| (0.063" (1.6mm) from case for 10s) | | | |

*JEDEC registered values

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N-CHANNEL
POWER MOSFETS

Specifications 2N6759, 2N6760


Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

| Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|--------|------|------|------|----------|--|
| BV _{DSS} Drain - Source Breakdown Voltage | 2N6759 | 350 | - | - | V | $V_{GS} = 0$ $I_D = 1.0 \text{ mA}$ |
| | 2N6760 | 400 | - | - | V | |
| V _{GS(th)} Gate Threshold Voltage | ALL | 2.0* | - | 4.0* | V | $V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$ |
| I _{GSSF} Gate - Body Leakage Forward | ALL | - | - | 100* | nA | $V_{GS} = 20\text{V}$ |
| I _{GSSR} Gate - Body Leakage Reverse | ALL | - | - | 100* | nA | $V_{GS} = -20\text{V}$ |
| I _{DSS} Zero Gate Voltage Drain Current | ALL | - | 0.1 | 1.0* | mA | $V_{DS} = \text{Max. Rating}$, $V_{GS} = 0$ |
| | | - | 0.2 | 4.0* | mA | $V_{DS} = \text{Max. Rating}$, $V_{GS} = 0$, $T_C = 125^\circ\text{C}$ |
| V _{DS(on)} Static Drain-Source On-State Voltage | 2N6759 | - | - | 7.0* | V | $V_{GS} = 10\text{V}$, $I_D = 4.5\text{A}$ |
| | 2N6760 | - | - | 6.7* | V | $V_{GS} = 10\text{V}$, $I_D = 5.5\text{A}$ |
| R _{DS(on)} Static Drain-Source On-State Resistance | 2N6759 | - | 1.0 | 1.5* | Ω | $V_{GS} = 10\text{V}$, $I_D = 3\text{A}$ |
| | 2N6760 | - | 0.8 | 1.0* | Ω | $V_{GS} = 10\text{V}$, $I_D = 3\text{A}$ |
| R _{DS(on)} Static Drain-Source On-State Resistance | 2N6759 | - | - | 3.3* | Ω | $V_{GS} = 10\text{V}$, $I_D = 3\text{A}$, $T_C = 125^\circ\text{C}$ |
| | 2N6760 | - | - | 2.2* | Ω | $V_{GS} = 10\text{V}$, $I_D = 3.5\text{A}$, $T_C = 125^\circ\text{C}$ |
| g _{fs} Forward Transconductance | ALL | 3.0* | 4.5 | 9.0* | S (Ω) | $V_{DS} = 15\text{V}$, $I_D = 3.5\text{A}$ |
| C _{iss} Input Capacitance | ALL | 350* | 600 | 800* | pF | $V_{GS} = 0$, $V_{DS} = 25\text{V}$, $f = 1.0 \text{ MHz}$ See Fig. 10 |
| C _{oss} Output Capacitance | ALL | 50* | 150 | 300* | pF | |
| C _{rss} Reverse Transfer Capacitance | ALL | 20* | 40 | 80* | pF | |
| t _{d(on)} Turn-On Delay Time | ALL | - | - | 30* | ns | $V_{DD} \approx 175\text{V}$, $I_D = 3.5\text{A}$, $Z_{\theta} = 15^\circ\text{C/W}$ |
| t _r Rise Time | ALL | - | - | 35* | ns | (See Figs. 13 and 14) |
| t _{d(off)} Turn-Off Delay Time | ALL | - | - | 55* | ns | (MOSFET switching times are essentially independent of operating temperature.) |
| t _f Fall Time | ALL | - | - | 35* | ns | |

Thermal Resistance

| | | | | | | |
|---------------------------------------|-----|---|-----|-------|--------------------|---|
| R _{thJC} Junction-to-Case | ALL | - | - | 1.67* | $^\circ\text{C/W}$ | |
| R _{thCS} Case-to-Sink | ALL | - | 0.1 | - | $^\circ\text{C/W}$ | Mounting surface flat, smooth, and greased. |
| R _{thJA} Junction-to-Ambient | ALL | - | - | 30 | $^\circ\text{C/W}$ | Free Air Operation |

Body-Drain Diode Ratings and Characteristics

| | | | | | | |
|---|--------|-------|-----|------|---------------|--|
| I _S Continuous Source Current (Body Diode) | 2N6759 | - | - | 4.5* | A | Modified MOSFET symbol showing the integral reverse P-N junction rectifier |
| | 2N6760 | - | - | 5.5* | A | |
| I _{SM} Pulsed Source Current (Body Diode) | 2N6759 | - | - | 7.0 | A |  |
| | 2N6760 | - | - | 8.0 | A | |
| V _{SD} Diode Forward Voltage | 2N6759 | 0.70* | - | 1.4* | V | $T_C = 25^\circ\text{C}$, $I_S = 4.5\text{A}$, $V_{GS} = 0$ |
| | 2N6760 | 0.75* | - | 1.5* | V | $T_C = 25^\circ\text{C}$, $I_S = 5.5\text{A}$, $V_{GS} = 0$ |
| t _{rr} Reverse Recovery Time | ALL | - | 550 | - | ns | $T_J = 150^\circ\text{C}$, $I_F = I_{SM}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$ |
| Q _{RR} Reverse Recovered Charge | ALL | - | 8.0 | - | μC | $T_J = 150^\circ\text{C}$, $I_F = I_{SM}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$ |

*JEDEC registered values Ⓢ Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

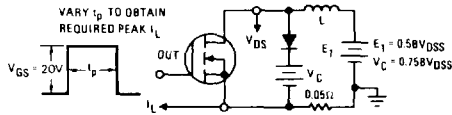


Fig. 1 - Clamped Inductive Test Circuit

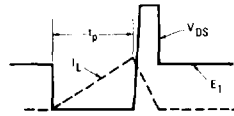


Fig. 2 - Clamped Inductive Waveforms

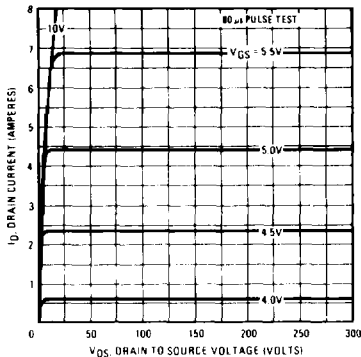


Fig. 3 - Typical Output Characteristics

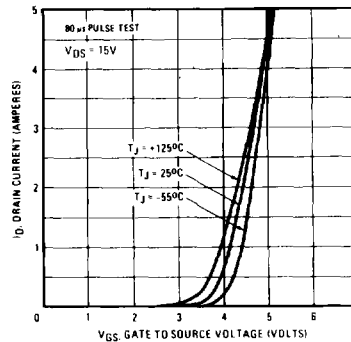


Fig. 4 - Typical Transfer Characteristics

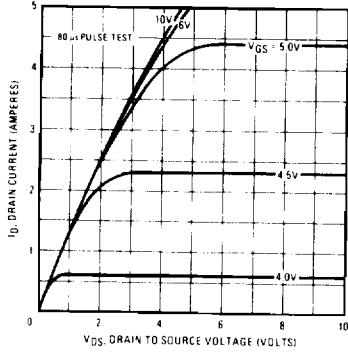


Fig. 5 - Typical Saturation Characteristics (2N6759)

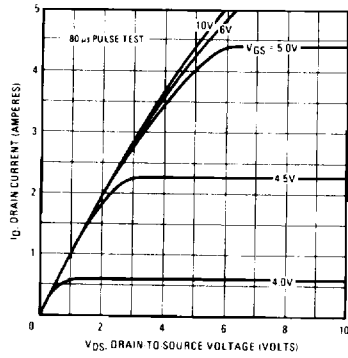


Fig. 6 - Typical Saturation Characteristics (2N6760)

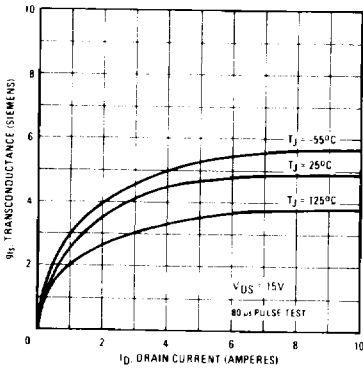


Fig. 7 - Typical Transconductance Vs. Drain Current

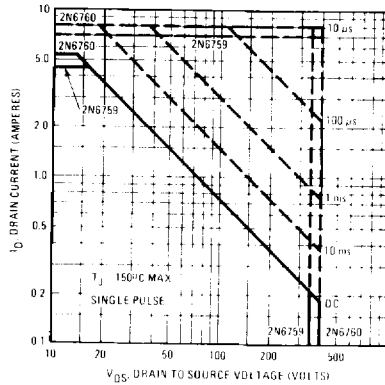


Fig. 8 - Maximum Safe Operating Area

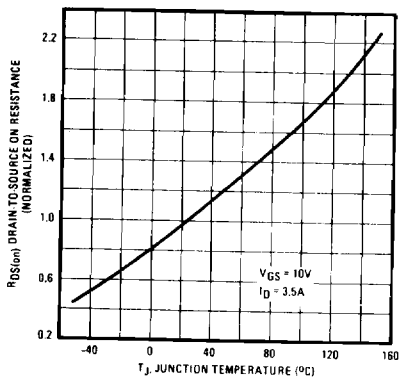


Fig. 9 - Normalized Typical On-Resistance Vs. Temperature

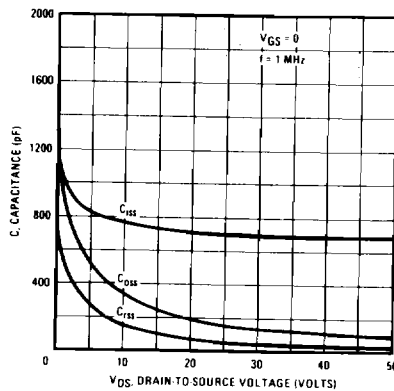


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

2N6759, 2N6760

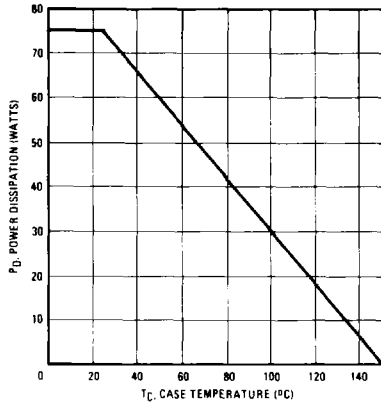


Fig. 11 - Power Vs. Temperature Derating Curve

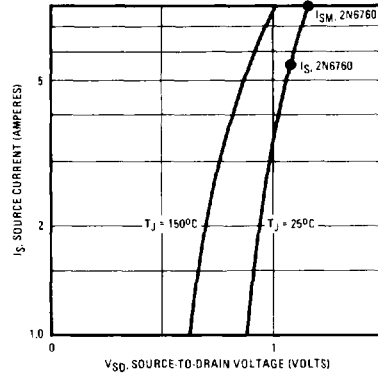


Fig. 12 - Typical Body-Drain Diode Forward Voltage

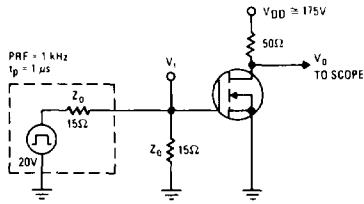


Fig. 13 - Switching Time Test Circuit

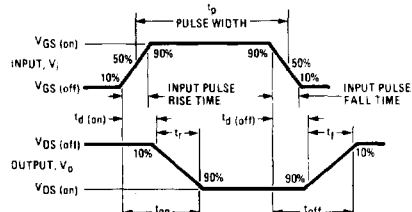


Fig. 14 - Switching Time Waveforms