

Features

- Temperature Ranges
 - Industrial: -40 °C to 85 °C
- Very high speed: 55 ns
 - Wide voltage range: 2.20 V–3.60 V
- Pin-compatible with CY62148CV25, CY62148CV30 and CY62148CV33
- Ultra low active power
 - Typical active current: 1.5 mA at f = 1 MHz
 - Typical active current: 8 mA at f = f_{max} (55-ns speed)
- Ultra low standby power
- Easy memory expansion with \overline{CE} , and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Available in Pb-free 32-pin Small-outline integrated circuit (SOIC package)

Functional Description

The CY62148DV30^[1] is a high-performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected (\overline{CE} HIGH). The eight input and output pins (I/O₀ through I/O₇) are placed in a high-impedance state when:

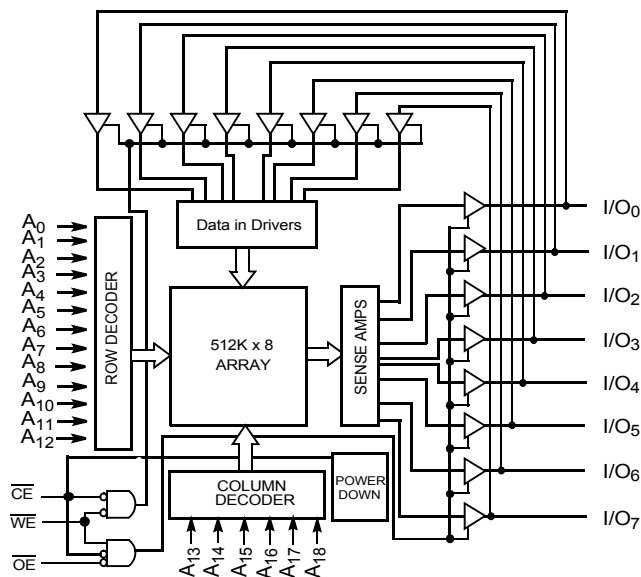
- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- When the write operation is active (\overline{CE} LOW and \overline{WE} LOW)

Write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

Read from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

For a complete list of related documentation, click [here](#).

Logic Block Diagram



Note

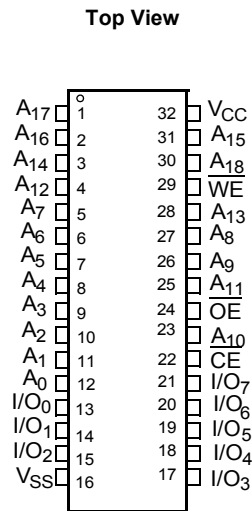
1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

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Pin Configuration

Figure 1. 32-pin SOIC pinout



Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62148DV30LL	Industrial	2.2	3.0	3.6	55	1.5	3	8	10	2	8

Note

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied 55 °C to +125 °C

Supply voltage
to ground potential [3, 4] -0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs
in High Z state [3, 4] -0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] -0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC} [5]
CY62148DV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [2]	Max	
V_{OH}	Output HIGH voltage	$I_{OH} = -0.1$ mA	$V_{CC} = 2.20$ V	2.0	–	–	V
		$I_{OH} = -1.0$ mA	$V_{CC} = 2.70$ V	2.4	–	–	V
V_{OL}	Output LOW voltage	$I_{OL} = 0.1$ mA	$V_{CC} = 2.20$ V	–	–	0.4	V
		$I_{OL} = 2.1$ mA	$V_{CC} = 2.70$ V	–	–	0.4	V
V_{IH}	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V		1.8	–	$V_{CC} + 0.3$	V
		$V_{CC} = 2.7$ V to 3.6 V		2.2	–	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V		-0.3	–	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V		-0.3	–	0.8	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	–	+1	μ A
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, output disabled		-1	–	+1	μ A
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$	–	8	10	mA
		$f = 1$ MHz	$I_{OUT} = 0$ mA CMOS levels	–	1.5	3	mA
I_{SB1}	Automatic CE Power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V), $f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), $V_{CC} = 3.60$ V		–	2	8	μ A
I_{SB2}	Automatic CE Power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.60$ V		–	2	8	μ A

Notes

3. $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.

4. $V_{IH(max)}$ = $V_{CC} + 0.75$ V for pulse durations less than 20 ns.

5. Full device AC operation assumes a 100 μ s ramp time from 0 to $V_{CC(min)}$ and 200 μ s wait time after V_{CC} stabilization.

Capacitance

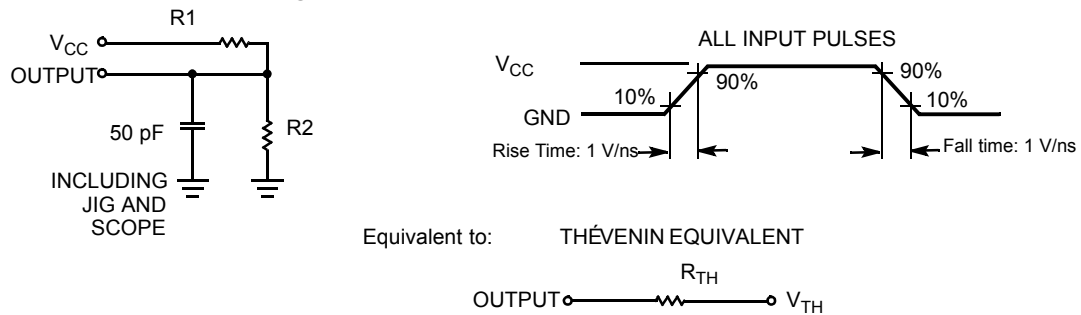
Parameter ^[7]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[7]	Description	Test Conditions	SOIC	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	55	°C/W
Θ _{JC}	Thermal resistance (junction to case)		22	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V – 2.7 V)	3.0 V (2.7 V – 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

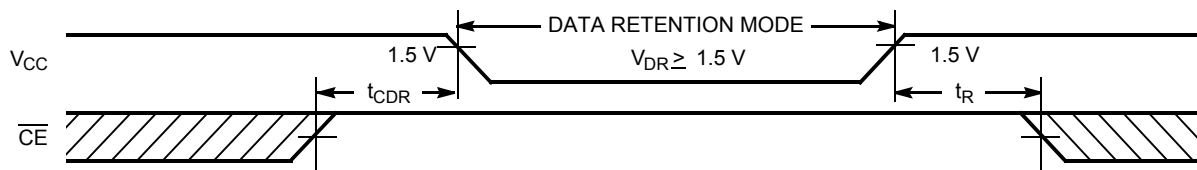
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[6]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–		6	μA
$t_{CDR}^{[7]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[8]}$	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
- Tested initially and after any design or process changes that may affect these parameters.
- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[9]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	55	ns
t_{DOE}	\overline{OE} LOW to data valid	–	25	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[10]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[10, 11]	–	20	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[10]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[10, 11]	–	20	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-up	–	55	ns
Write Cycle ^[12, 13]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	\overline{CE} LOW to write end	40	–	ns
t_{AW}	Address set-up to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	40	–	ns
t_{SD}	Data set-up to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[10, 11]	–	20	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[10]	10	–	ns

Notes

9. Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).

10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

11. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enter a high impedance state.

12. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

13. The minimum write cycle pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

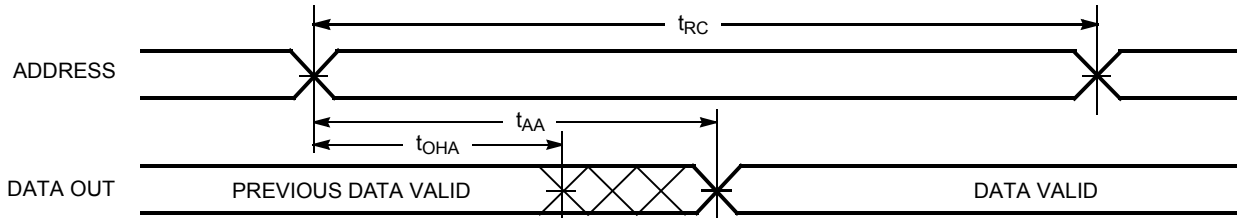
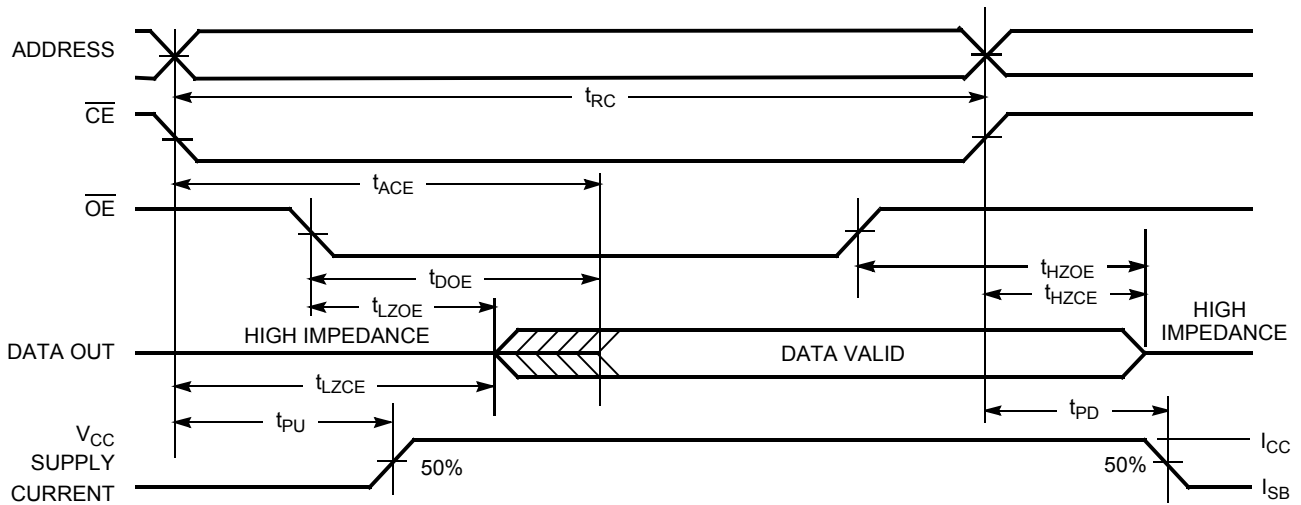


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]

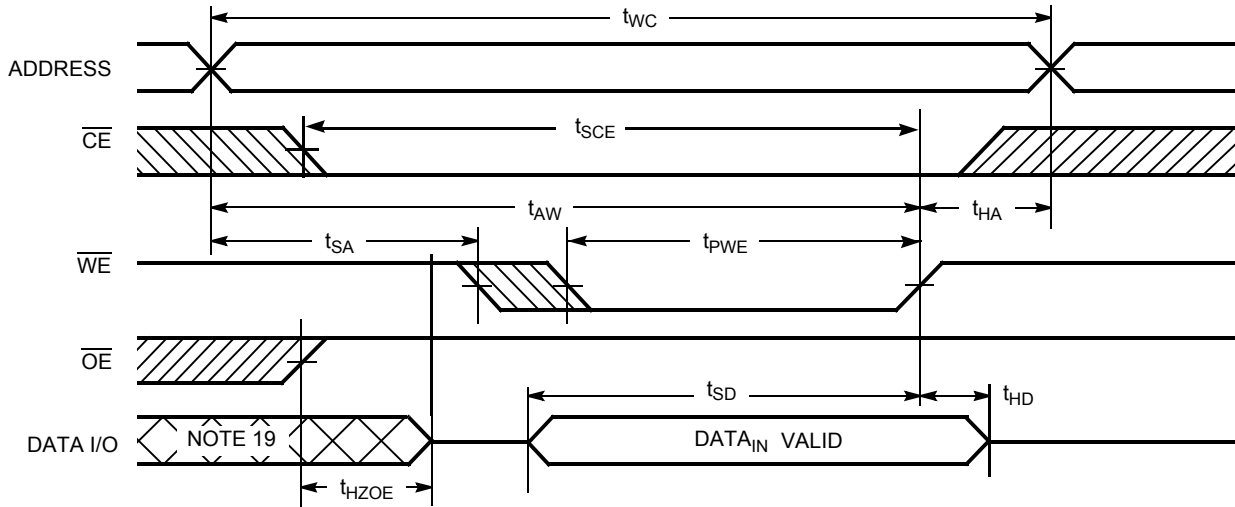


Notes

- 14. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 15. WE is HIGH for read cycle.
- 16. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (\overline{WE} Controlled) [17, 18]



Notes

- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in high-impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [20, 21]

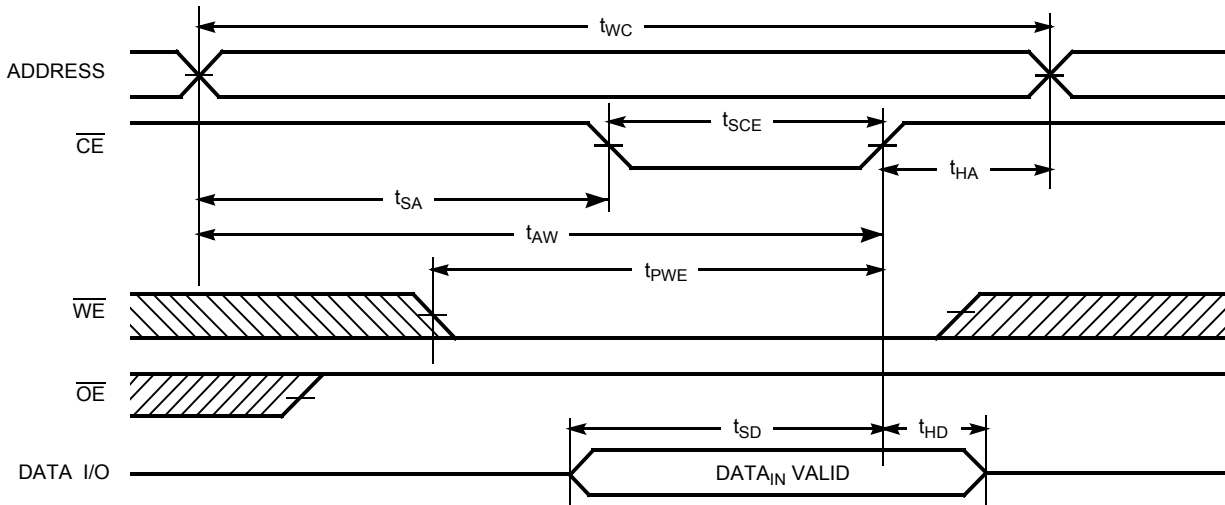
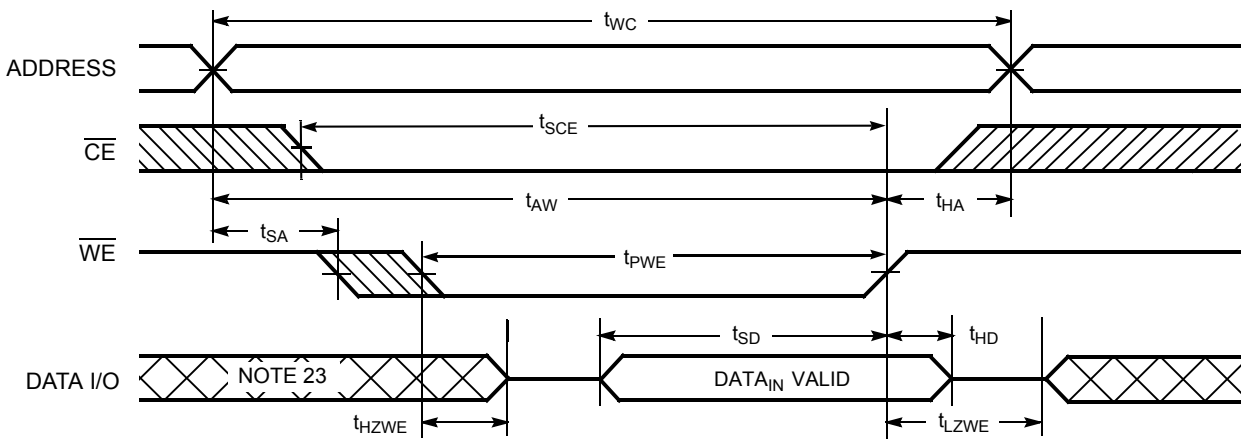


Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [21, 22]



Notes

- 20. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 21. If $\overline{\text{CE}}$ goes HIGH simultaneously with WE HIGH, the output remains in high-impedance state.
- 22. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .
- 23. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

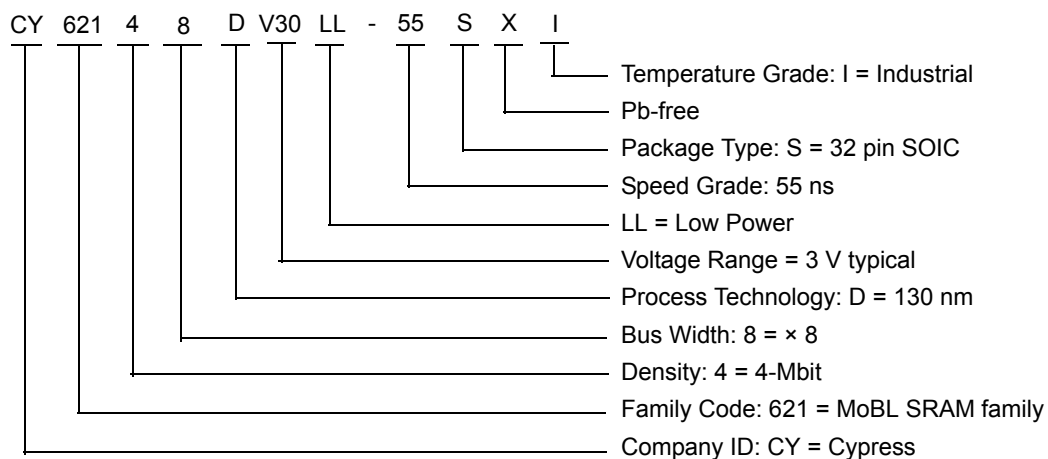
\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data out (I/O_0 - I/O_7)	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in (I/O_0 - I/O_7)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148DV30LL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

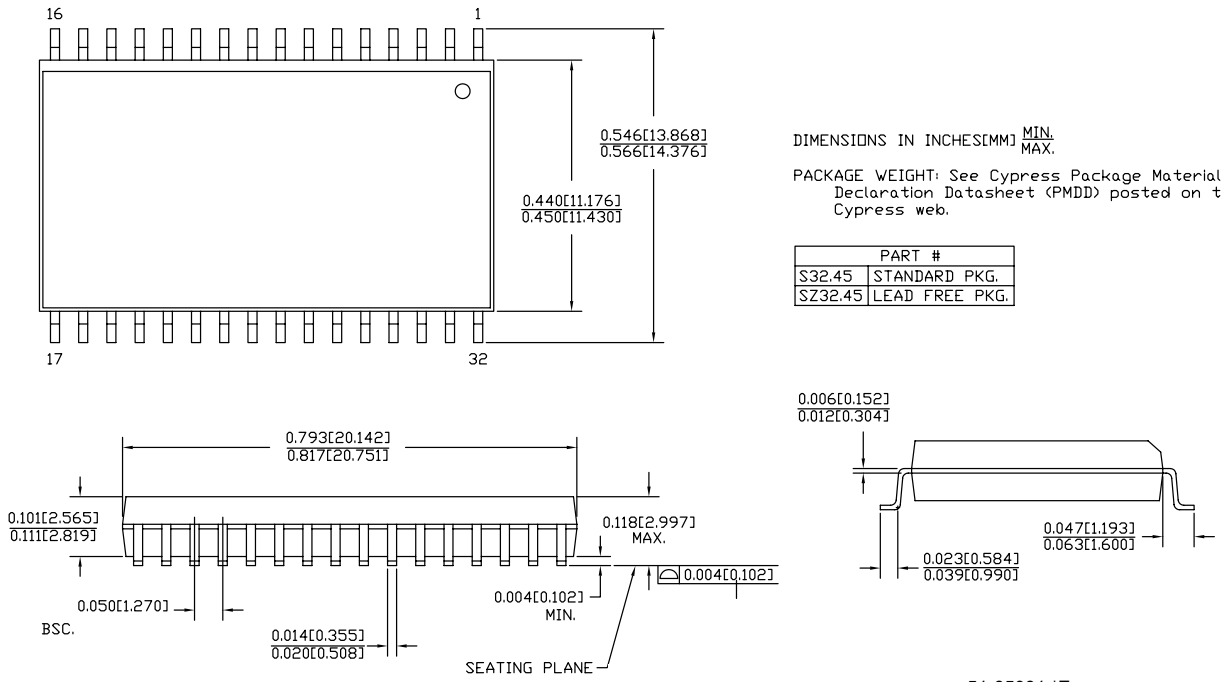
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin SOIC (450 Mils) Package Outline, 51-85081



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
MoBL	More Battery Life
SOIC	Small-Outline Integrated Circuit
SRAM	Static Random Access Memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148DV30, 4-Mbit (512 K × 8) MoBL [®] Static RAM				
Document Number: 38-05341				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	127480	06/17/03	HRT	Created new data sheet
*A	131041	01/23/04	CBD	Changed from Advance to Preliminary
*B	222180	See ECN	AJU	Changed from Preliminary to Final Added 70 ns speed bin Modified footnote #6 and #12 Removed MAX value for V _{DR} on "Data Retention Characteristics" table Modified input and output capacitance values Added Pb-free ordering information Removed 32-pin STSOP package
*C	498575	See ECN	NXR	Added Automotive-A Operating Range Removed SOIC package from Product Offering Updated Ordering Information Table
*D	729917	See ECN	VKN	Added SOIC package and its related information Updated Ordering Information Table
*E	2896036	03/19/10	AJU	Added Table of Contents. Removed inactive parts from Ordering Information. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.
*F	3166059	02/08/2011	RAME	Removed Automotive related info Removed 70 ns speed bin related info Remove TSOP and VFBGA package related info Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template.
*G	4315741	03/20/2014	VINI	Updated Package Diagrams : spec 51-85081 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*H	4576406	01/16/2015	VINI	Added related documentation hyperlink in page 1. Updated Switching Characteristics : Added Note 13 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 22 and referred the same note in Figure 8 .
*I	4702987	03/27/2015	VINI	Updated Maximum Ratings : Referred Notes 3, 4 in "Supply voltage to ground potential". Completing Sunset Review.
*K	5975781	11/24/2017	AESATMP8	Updated logo and Copyright.

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