Introduction

The evaluation board is designed to help the customer evaluate the 5P49V60, 5P49V6965 and 5P49V6975 devices. When the board is connected to a PC running IDT Timing Commander™ software through USB, the device can be configured and programmed to generate different combinations of frequencies. The 5P49V60 and 5P49V6965 use an external crystal, and the 5P49V6975 has an integrated crystal. The devices are pin-compatible and can use the same board.

Board Overview

Use Figure 1 and Table 1 to identify: power supply jacks, USB connector, input and output frequency SMA connectors.

Figure 1. Evaluation Board Overview

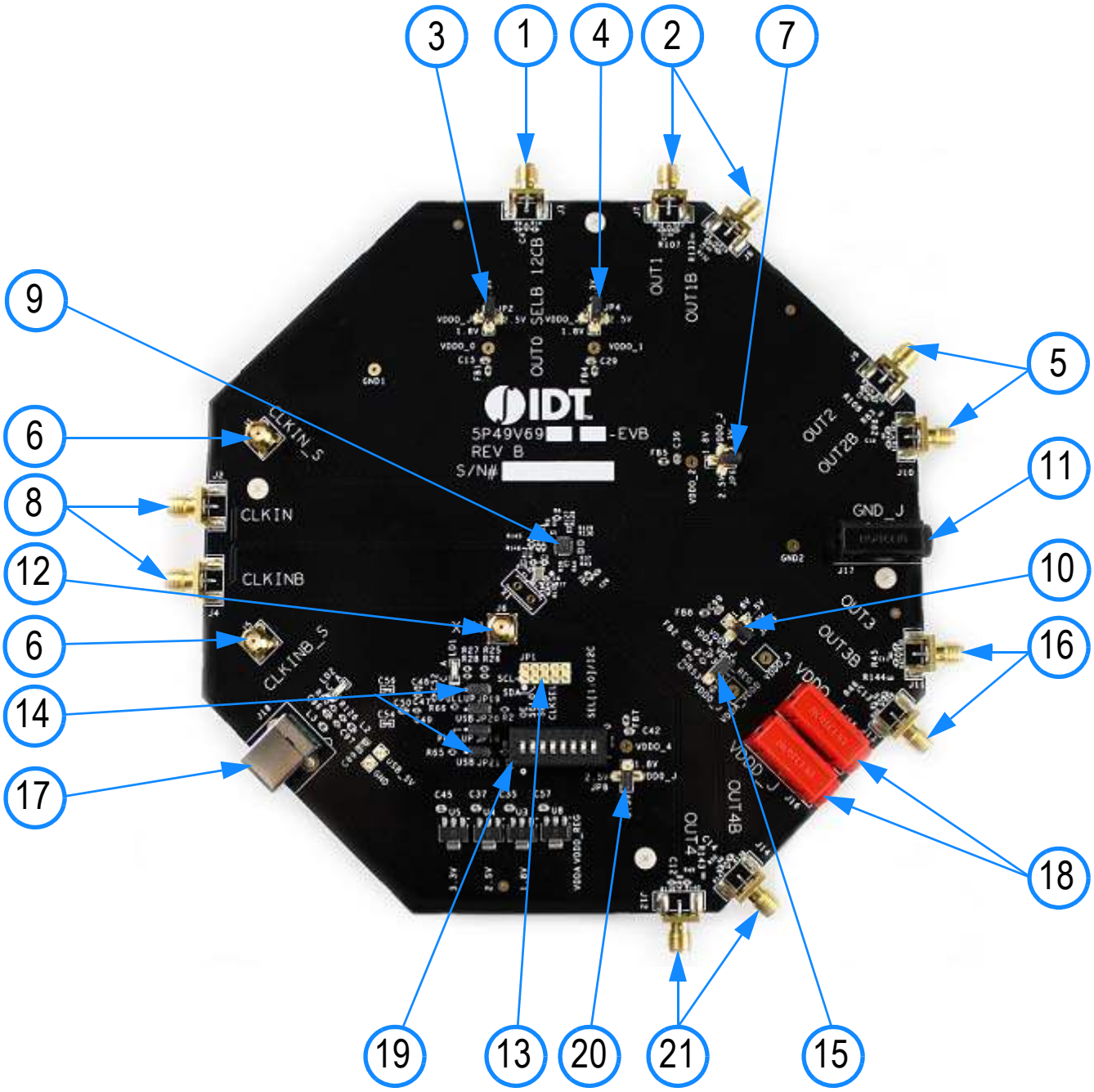


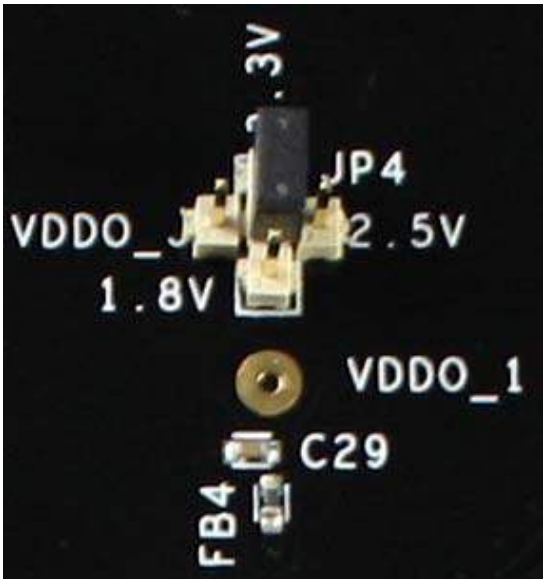
Table 1. Evaluation Board Pins and Functions

Label Number	Name	On-board Connector Label	Function
1	Output 0	J3	Single-ended LVCMOS clock output.
2	Output 1	J6, J7	Differential clock output.
3	VDDO_0	JP2	Power supply voltage selector for Output 0.
4	VDDO_1	JP4	Power supply voltage selector for Output 1.
5	Output 2	J9, J10	Differential clock output.
6	CLKIN Sens	J1, J5	Differential input clock, Sens output.
7	VDDO_2	JP6	Power supply voltage selector for Output 2.
8	CLKIN Input	J2, J4	Differential clock output.
9	5P49V60/6965/6975	U1	Evaluation device.
10	VDDO_3	JP13	Power supply voltage selector for Output 3.
11	Ground Jack	J17	Ground jack for external power supply.
12	XIN	J6	Input for overdriving XIN pin.
13	Aardvark Connector	JP1	For Aardvark connection.
14	I^2C Control Jumpers	J18, J19, J20, J21	4 Jumpers to configure source of I^2C: ▪ Use on-board USB to I^2C bridge. ▪ Use Aardvark adapter. ▪ Disconnect I^2C to allow SEL0/1 switching.
15	VDDA/D	JP3	Power supply selector for VDDA and VDDD.
16	Output 3	J11, J13	Differential clock output.
17	USB Interface	J18	Used for connection with a PC and for interaction with the IDT Timing Commander software.
18	VDD Jacks	J15, J16	VDD jacks for external power supply.
19	DIP Switch	U2	S1: Output Enable (OE/SD). S2: SEL0. S3: SEL1. S8: SEL [1:0]; default: I^2C mode.
20	VDDO_4	JP8	Power supply voltage selector for Output 4.
21	Output 4	J12, J14	Differential clock output.

Board Power Supply

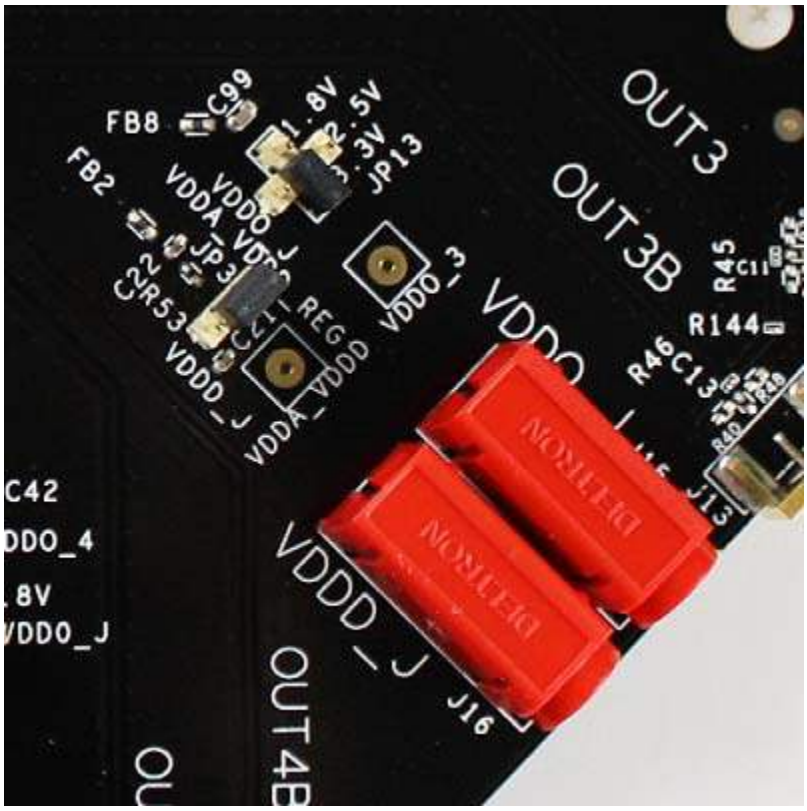
The voltage for each of the four V_{DDO} pins can be selected with jumpers. In the 5-pin configuration, the center pin is connected to the V_{DDO} pin on the device. The four pins around it are connected to different power sources. A jumper connects the V_{DDO} pin to a power source of choice.

Figure 2. VDDO_1 Voltage Selector



In Figure 2, the voltage for VDDO_1 is chosen to be 3.3V. Move the jumper to the right side to select 2.5V, to the bottom to select 1.8V or to the left to select the VDDO_J Jack. The 3.3V, 2.5V and 1.8V are from on-board regulators that get their power from the USB connector. The VDD jacks are for connecting to a bench power supply.

Figure 3. VDDA/D Power Source Selector



JP3 selects the power source for the V_{DDD} and V_{DDO} pins between an on-board 3.3V regulator and the VDDD_J Jack for a bench power supply. In Figure 3, the source for V_{DDD} and V_{DDO} is chosen to be the on-board 3.3V regulator.

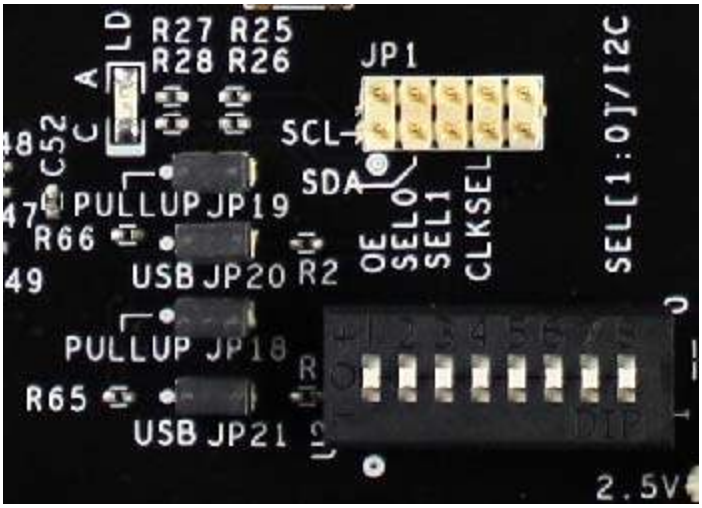
Connecting the Board to a Computer

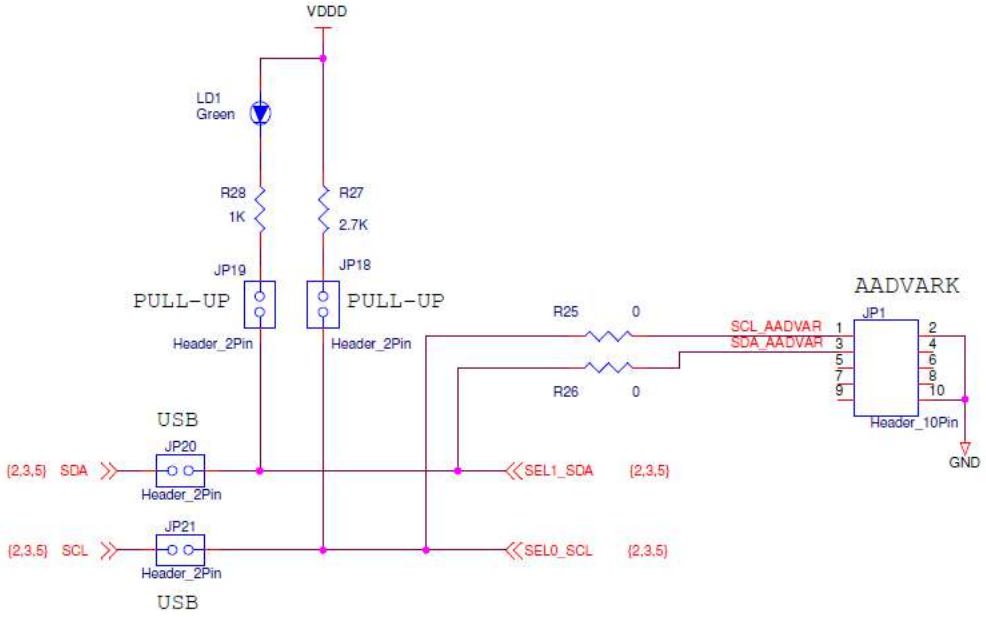
The evaluation board can be connected to a computer with the USB connector. The on-board USB-to-I^{2}C bridge (FTDI chip) does the data communication and the +5V in the USB bus powers the on-board regulators. Using a bench power supply with the V_{DD} jacks is optional. The board can fully function with just the USB cable to a computer.

IDT's Timing Commander software can control the VersaClock 6E device on the board. Timing Commander is compatible with both the on-board USB-to-I^{2}C bridge and the Aardvark adapter. Timing Commander displays a block diagram where you can enter the configuration. You can then program that configuration into the VersaClock 6E device on the board where Timing Commander defines the proper hex-code sequence to program into the device.

The jumpers J18, J19, J20 and J21 configure the I^{2}C configuration.

Figure 4. Configure I^{2}C Operation





Labels “SDA” and “SCL” to the left in the schematic connect to the USB-to-I^{2}C bridge chip. When using an Aardvark or when operating the SEL0/1 switches, jumpers JP20 and JP21 need to be removed to disconnect the USB-to-I^{2}C bridge. Labels “SEL1_SDA” and “SEL0_SCL” to the right in the schematic are the SEL1/SDA and SEL0/SCL pins on the VersaClock 6E device.

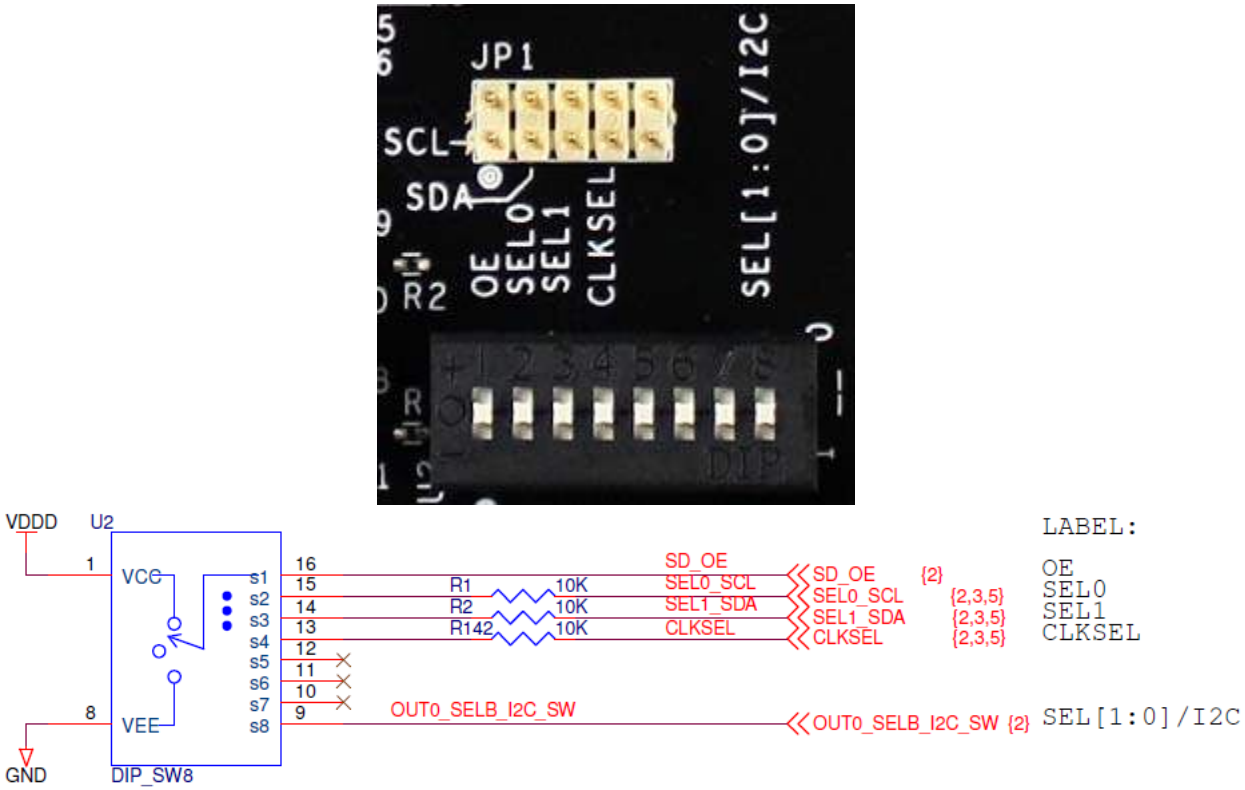
Table 2. Configure I2C Operation

Function	JP18	JP19	JP20	JP21
Uses on-board USB-to-I2C bridge.	Yes	Yes	Yes	Yes
Uses Aardvark or other adapter connected to JP1. The adapter has its own pull-ups enabled.	No	No	No	No
Uses Aardvark or other adapter connected to JP1. The adapter does not have pull-ups, or, has them disabled.	Yes	Yes	No	No
Operates the SEL0 and SEL1 switches.	No	No	No	No

U2 Switch Operation

The DIP switch block U2 has 8 switches, of which 5 are used.

Figure 5. U2 Switches



The switches connect to pins on the VersaClock 6E devices. The middle position leaves the pin open. This is the default for each switch. Move to the "+" side to pull the pin high and move to the "-" side to pull the pin low.

- **Switch 1 = OE**: Connects to the SD/OE pin for output enable or shut-down operation.
- **Switch 2 = SEL0**: Connects to the SEL0/SCL pin. The main purpose of this switch is to operate SEL0 when the device has started in hardware select mode. This switch can also be used to add an extra pull-up (10kΩ) on the SCL line for I2C operation.
- **Switch 3 = SEL1**: Connects to the SEL1/SDA pin. The main purpose of this switch is to operate SEL1 when the device has started in hardware select mode. This switch can also be used to add an extra pull-up (10kΩ) on the SDA line for I2C operation.
- **Switch 4 = CLKSEL**: Connects to the CLKSEL pin for selecting between crystal input or CLKIN differential clock input.

– **Switch 8**: Pulls on the OUT0_SELB_I2C pin on the device to select the operation mode at power-up. The state of the OUT0_SELB_I2C pin is latched at power-up. The operation mode effectively sets the function of the SEL0/SCL and SEL1/SDA pins. The OUT0_SELB_I2C pin has an on-chip pull-down so switch 8 in the center or "-" position has the same effect and results in startup with the I^2C mode. In I^2C mode, the two pins have the SDA and SCL function for I^2C operation. With the switch in the "+" position, the device will start in Hardware Select mode. In Hardware Select mode, the two pins have the SEL0 and SEL1 function for selecting a preprogrammed configuration.

Operating Modes

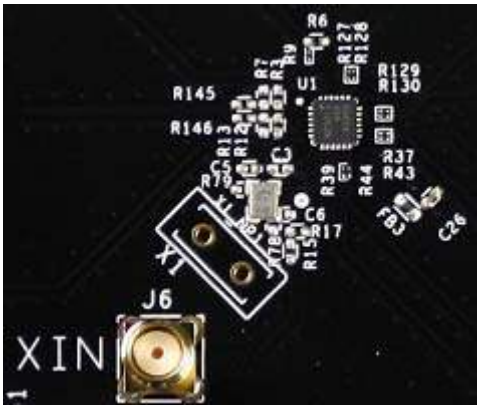
As explained above at switch 8, the VersaClock 6E device can start up in two different operating modes: I^2C mode or Hardware Select mode. The evaluation board is shipped with a "blank" VersaClock 6E device, without configurations pre-programmed into OTP. Without configurations pre-programmed, the Hardware Select mode cannot be used. The "blank" device will start with a default or "test" configuration where output 0 and output 1 are enabled. Output 0 will be 25MHz and output 1 will be 100MHz with LVCMOSD logic. You can then program a configuration into the device into volatile registers with Timing Commander to test a configuration. This works without "burning" the permanent OTP memory and most users of this evaluation board will never burn OTP. This way the board can be used again and again to test configurations. Burning configurations into OTP is only useful when studying the Hardware Select mode and the transition from one configuration to another.

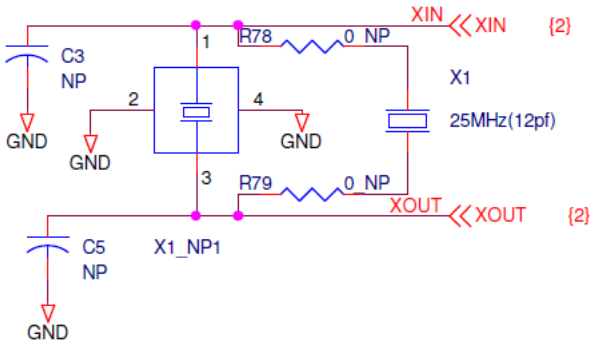
Note: Burning configurations into OTP is permanent and cannot be undone.

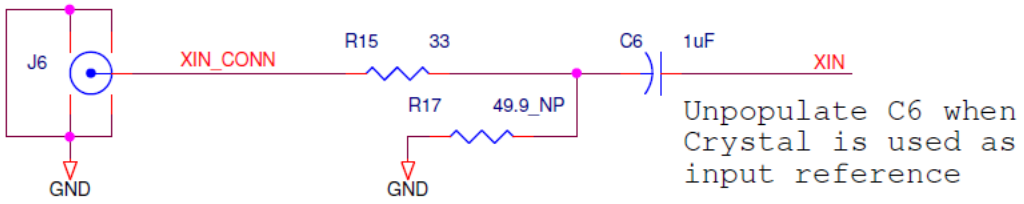
On-board Crystal

A 25MHz crystal is installed on the board with the 5P49V60 and 5P49V6965. If the evaluation board is assembled with a 5P49V6975, no crystal is assembled because the crystal is integrated in the device. The crystal pins on the 5P49V6975 are NC (no connect).

Figure 6. Crystal Circuit







The board is shipped with a small 25MHz SMD crystal installed. The crystal can be replaced with a different frequency if needed. Note that Output 1 with the default or “test” mode will only work when using a 25MHz crystal.

A thru-hole crystal can be assembled in the X1 position. Remove the small 25MHz crystal and also assemble the resistors R78 and R79 to connect the thru-hole crystal.

Another useful modification can be to remove the 25MHz crystal and assemble C6 to connect the SMA connector J6. Now a clock from a generator or other source can be used to drive the XIN pin. Also assemble R17 when termination of the external clock is needed. Please look up the requirements for the XIN amplitude in the device datasheet. Essentially, the amplitude on XIN should not exceed 1.2Vpp and we recommend using 1.0Vpp for most tests. When doing phase noise measurements of the output clocks, use a very low noise clock for XIN. The best phase noise at the outputs is achieved when using a crystal. Only the very best of low noise RF signal generators connected to XIN can result in the same phase noise performance.

Configuration and Setup

1. Set SEL pin (pin 8) of DIP switch (U2) to “O” to select I^2C mode.
2. Connect J18 to a USB port of the PC, using the supplied I^2C cable.
3. Launch VersaClock 6E Timing Commander software (refer to VersaClock 6E Timing Commander User Guide).
4. Following the Getting Started steps in the Timing Commander software, an I^2C connection is established between the GUI software and the VersaClock 6E chip.
5. Select “Open Settings File” if you have existing settings or “New Settings File” and select the VersaClock 6E device depending on your evaluation board. In the same screen, browse for a personality file, by clicking on the button at the bottom right, to be used with the evaluation board.
6. Connect to the EVB by clicking on the microchip icon located at the top right of the Timing Commander screen.

7. Once connected, new options will be available on a green background indicating that the EVB has successfully connected with the board. Write settings to the chip by clicking on the write all registers to the chip option.

8. All intended outputs should now be available for measurement.

Schematics

Evaluation board schematics are shown on the following pages.

Figure 7. VersaClock 6E Evaluation Board Schematics – page 1

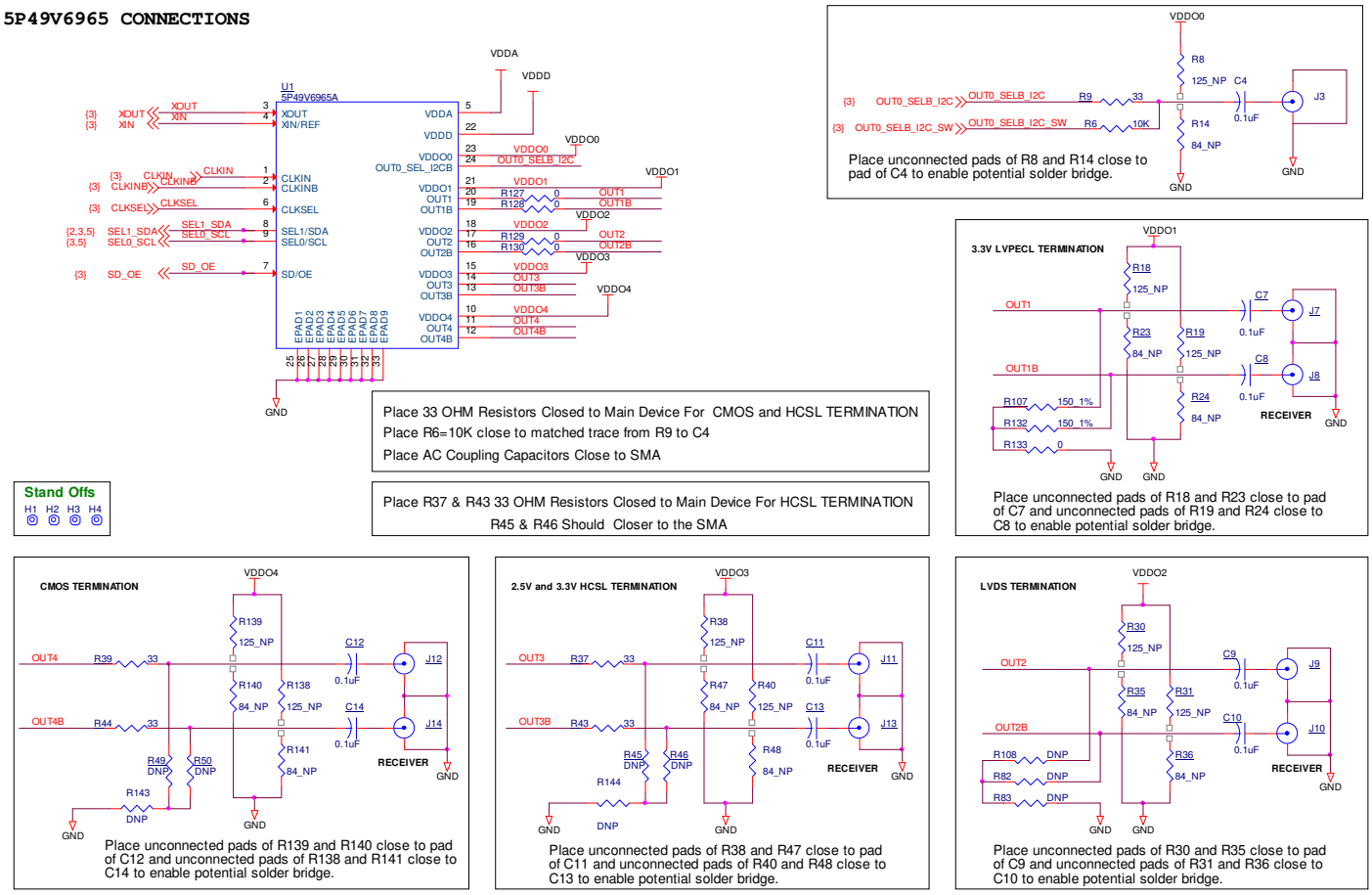


Figure 8. VersaClock 6E Evaluation Board Schematics – page 2

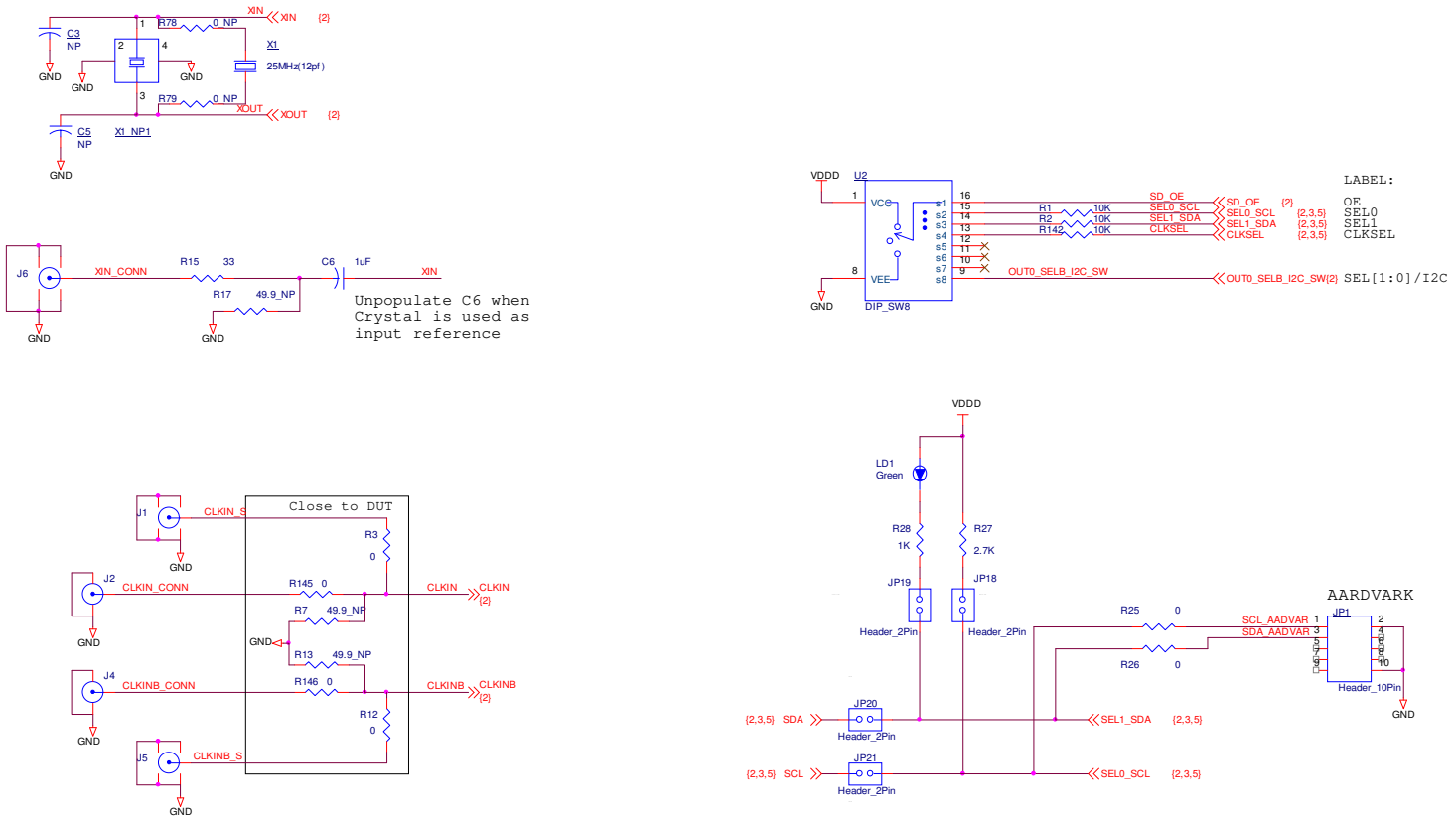


Figure 9. VersaClock 6E Evaluation Board Schematics – page 3

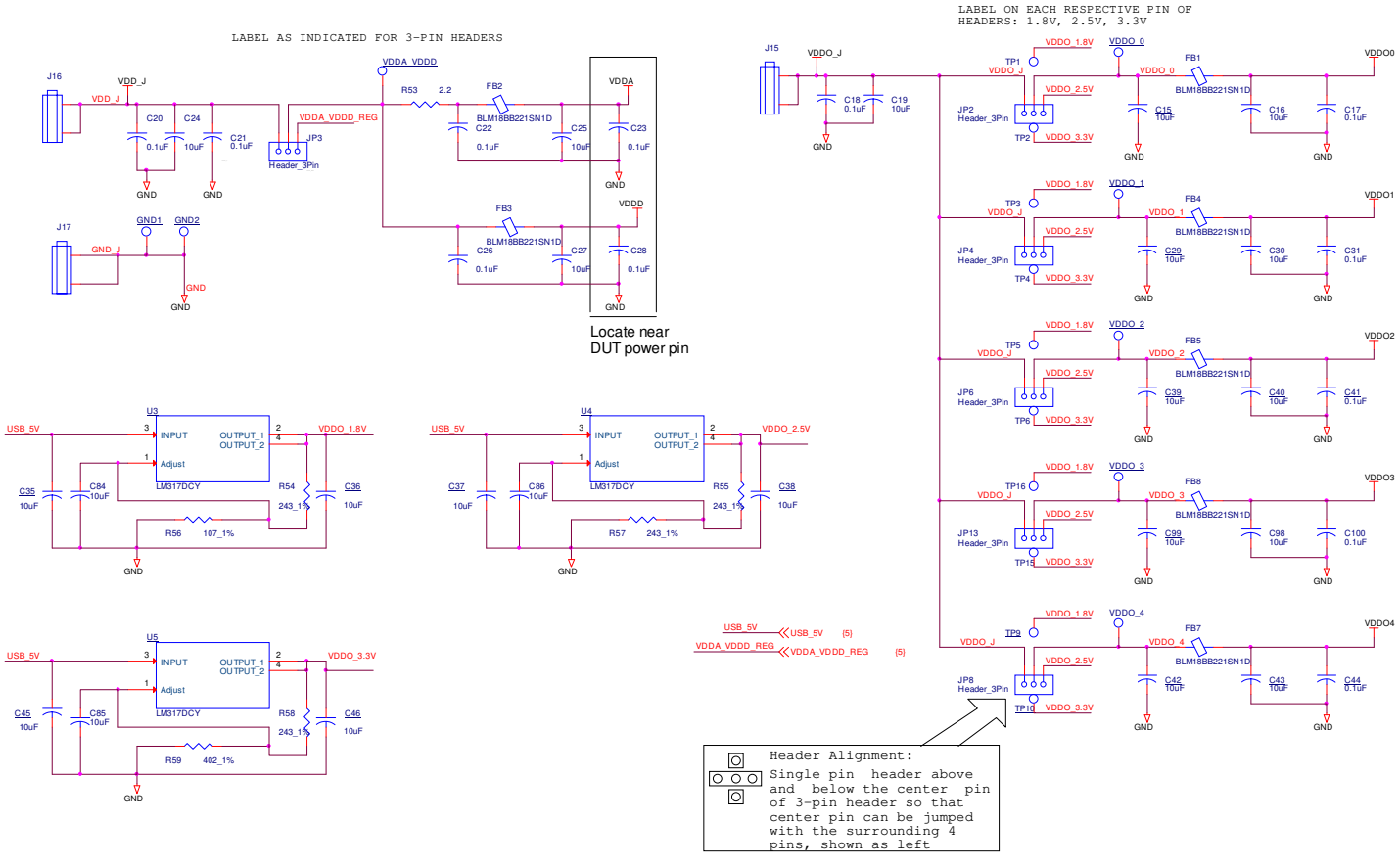
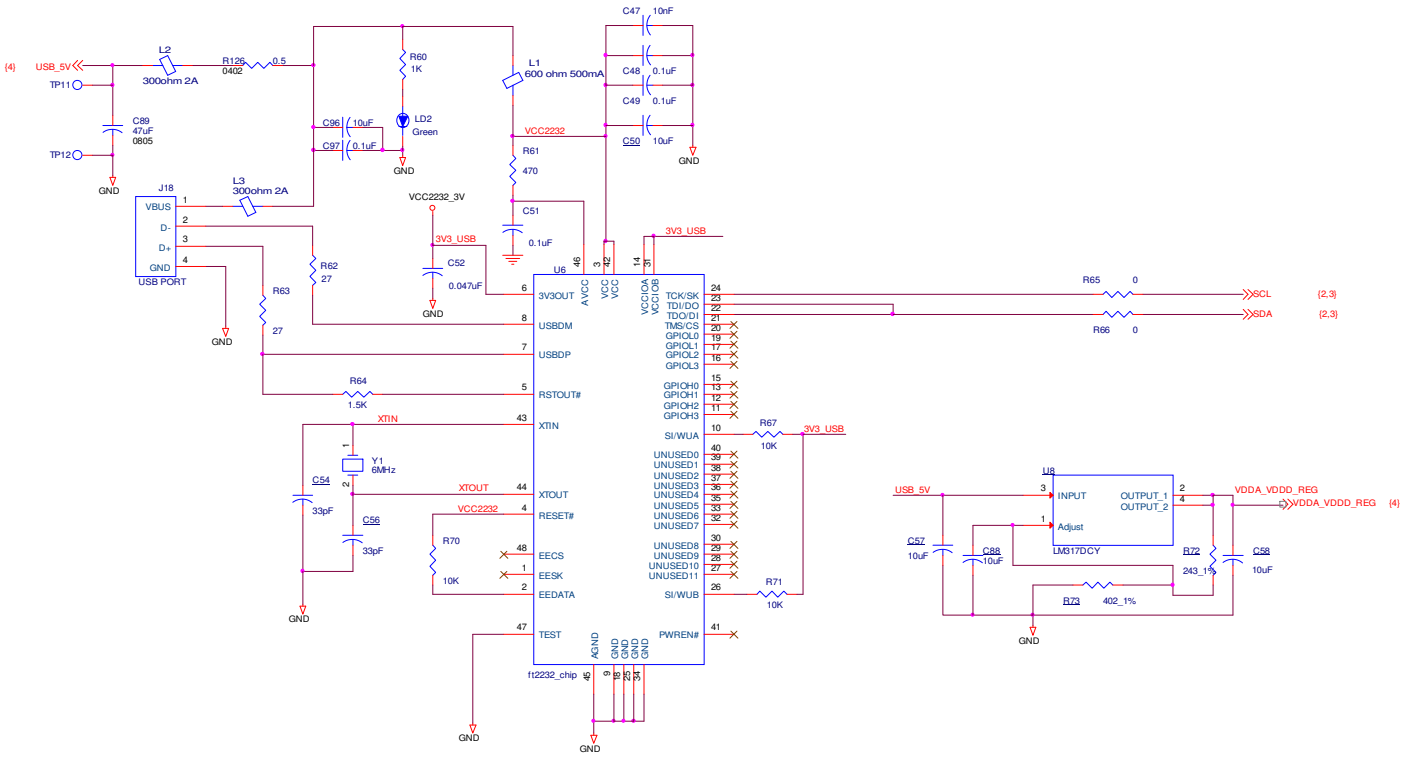


Figure 10. VersaClock 6E Evaluation Board Schematics – page 4



Signal Termination Options

Termination options for OUT1–4 for the VersaClock 6E evaluation board are displayed in Figure 11. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not populating) some resistors. DC or AC coupling of these outputs is also supported.

Table 3 through Table 6 tabulate component installations to support LVPECL, HCSL, LVCMOS and LVDS signal types for OUT1–4 on the VersaClock 6E evaluation board. Note that by doing so, the output signals will be measured and terminated by test equipment with a 50Ω internal termination.

Figure 11. VersaClock 6E Output Termination Options

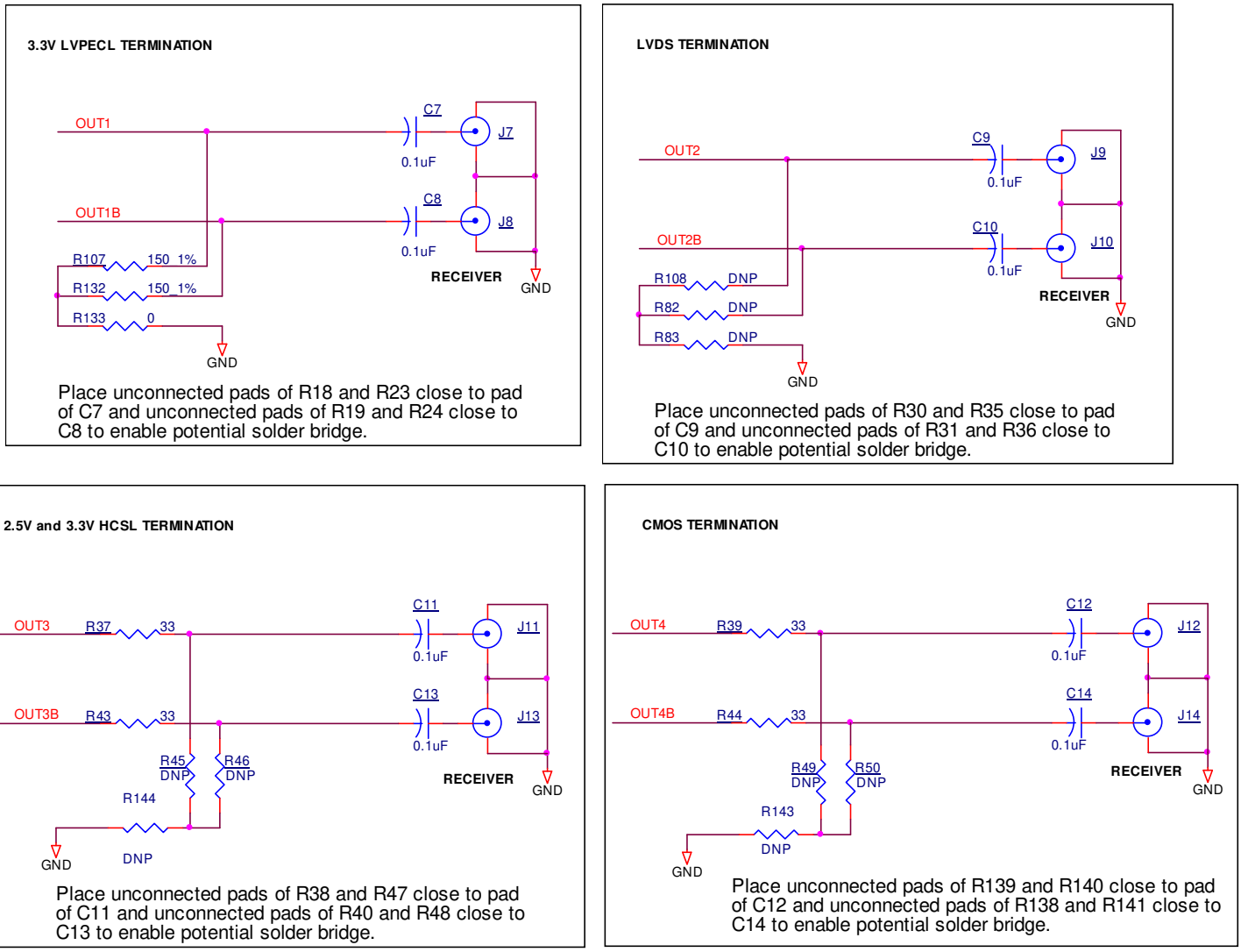


Table 3. Termination Options for Output 1

Signal Type	Series Resistors: R127, R128	150Ω Pull-down: R107, R132, R133	Series Capacitor: C7, C8
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL[1]	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 4. Termination Options for Output 2

Signal Type	Series Resistors: R129, R130	150Ω Pull-down: R108, R82, R83	Series Capacitor: C9, C10
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL[1]	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 5. Termination Options for Output 3

Signal Type	Series Resistors: R37, R43	150Ω Pull-down: R45, R46, R144	Series Capacitor: C11, C13
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL[1]	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 6. Termination Options for Output 4

Signal Type	Series Resistors: R39, R44	150Ω Pull-down: R49, R50, R143	Series Capacitor: C12, C14
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL[1]	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

1. The default configuration of the evaluation board is the HCSL termination scheme. This scheme allows for quick measurements of every logic type without modification of the evaluation board. When using the unmodified board with equipment that has AC coupled inputs, like a spectrum analyzer or phase noise test set, use a 3dB or 6dB attenuator to facilitate a DC path to ground and to allow the output driver to toggle. This is only needed with LVPECL and HCSL logic.

Ordering Information

Orderable Part Number	Description
5P49V60-EVK	5P49V60 evaluation board.
5P49V6965-EVK	5P49V6965 evaluation board.
5P49V6975-EVK	5P49V6975 evaluation board.

Revision History

Revision Date	Description of Change
February 12, 2018	Added references to 5P49V60.
December 15, 2017	Initial release.

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