

Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

MC74HCT573A

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

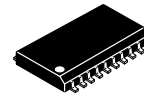
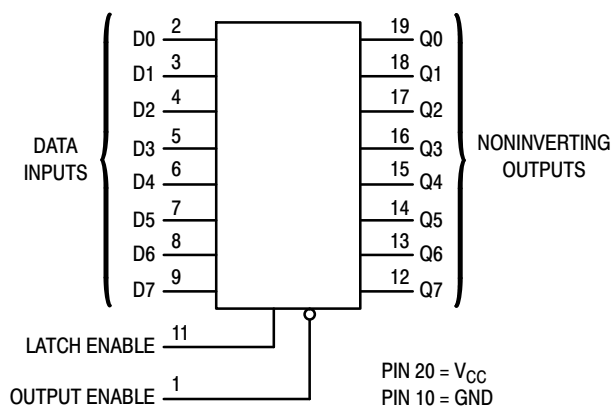
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
 - ◆ Improved Propagation Delays
 - ◆ 50% Lower Quiescent Power
- These Devices are Pb-Free and are RoHS Compliant

LOGIC DIAGRAM

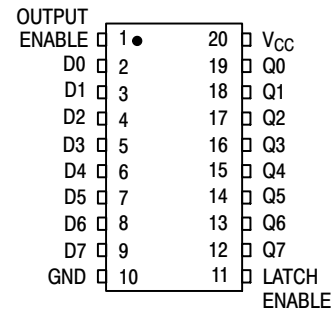


SOIC-20
DW SUFFIX
CASE 751D

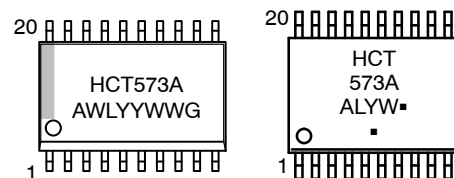


TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-20

TSSOP-20

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|--------------------|--------------------|
| MC74HCT573ADWR2G | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |
| MC74HCT573ADTR2G | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |
| MC74HCT573ADWG | SOIC-20 (Pb-Free) | 38 Units / Rail |
| NLV74HCT573ADTRG | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HCT573ADWG | SOIC-20 (Pb-Free) | 38 Units / Rail |
| NLV74HCT573ADWRG | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MC74HCT573A

FUNCTION TABLE

| Inputs | | | Output |
|---------------|--------------|---|-----------|
| Output Enable | Latch Enable | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | No Change |
| H | X | X | Z |

X = Don't Care

Z = High Impedance

| Design Criteria | Value | Units |
|---------------------------------|--------|---------|
| Internal Gate Count* | 58.5 | ea |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | 0.0075 | pJ |

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|--------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}$ C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (TSSOP or SOIC Package) | 260 | $^{\circ}$ C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/ $^{\circ}$ C from 65 $^{\circ}$ to 125 $^{\circ}$ C
TSSOP Package: -6.1 mW/ $^{\circ}$ C from 65 $^{\circ}$ to 125 $^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|-----|----------|--------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | +125 | $^{\circ}$ C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74HCT573A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------|--|---|----------------------|------------------|---------------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| | | | | | | | |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 5.5 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} ≤ 0 μA | 5.5 | 4.0 | 40 | 160 | μA |
| ΔI _{CC} | Additional Quiescent Supply Current | V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA | 5.5 | ≥ -55°C | 25°C to 125°C | | mA |
| | | | | 2.9 | 2.4 | | |

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|--|--|---|--------|---------|------|
| | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5) | 30 | 38 | 45 | ns |
| t _{PLH} t _{PHL} | Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5) | 30 | 38 | 45 | ns |
| T _{PLZ} , T _{PHZ} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 28 | 35 | 42 | ns |
| t _{TZL} , t _{TZH} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 28 | 35 | 42 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, any Output (Figures 1 and 5) | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
| | | 48 | | | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

TIMING REQUIREMENTS (V_{CC} = 5.0 V ±10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | Fig. | Guaranteed Limit | | | | | | Unit |
|---------------------------------|---|------|------------------|-----|--------|-----|---------|-----|------|
| | | | -55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t _{su} | Minimum Setup Time, Input D to Latch Enable | 4 | 10 | | 13 | | 15 | | ns |
| t _h | Minimum Hold Time, Latch Enable to Input D | 4 | 5.0 | | 5.0 | | 5.0 | | ns |
| t _w | Minimum Pulse Width, Latch Enable | 2 | 15 | | 19 | | 22 | | ns |
| t _r , t _f | Maximum Input Rise and Fall Times | 1 | | 500 | | 500 | | 500 | ns |

MC74HCT573A

SWITCHING WAVEFORMS

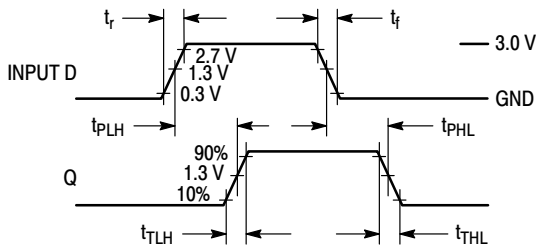


Figure 1.

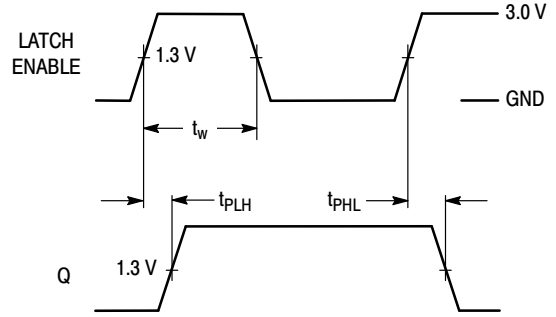


Figure 2.

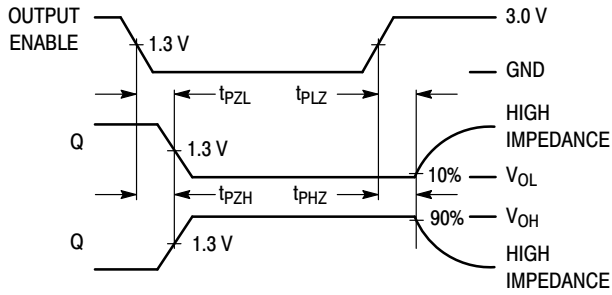


Figure 3.

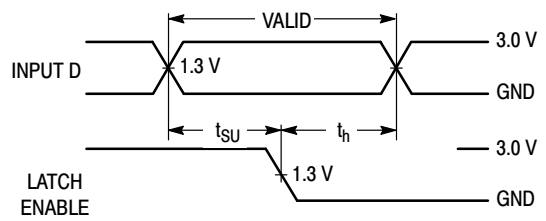
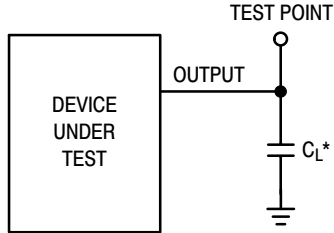
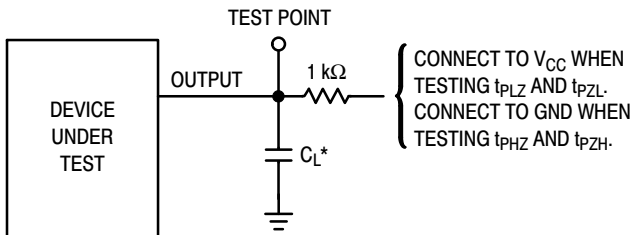


Figure 4.



*Includes all probe and jig capacitance

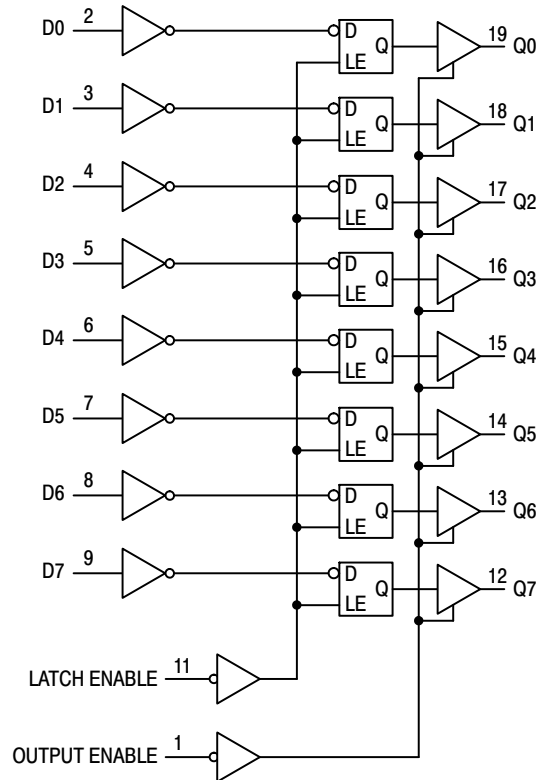
Figure 5. Test Circuit



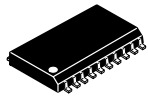
*Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



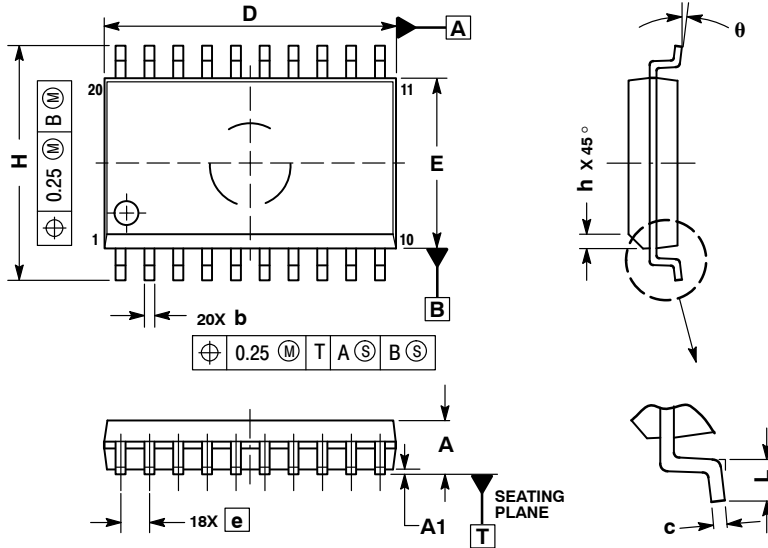
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

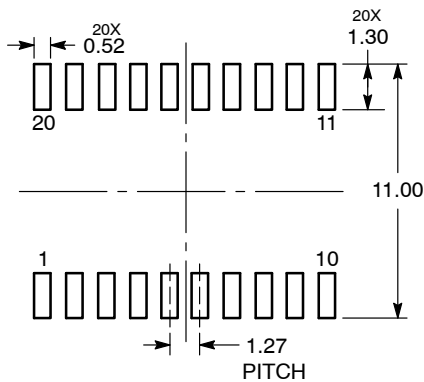


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

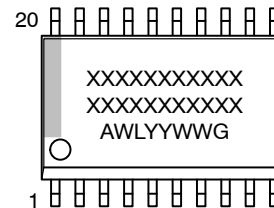
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

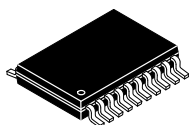
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

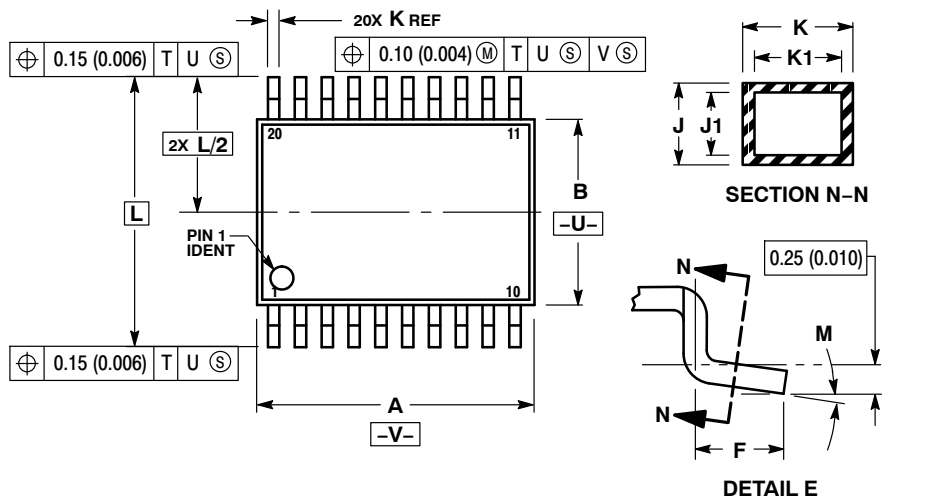
ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

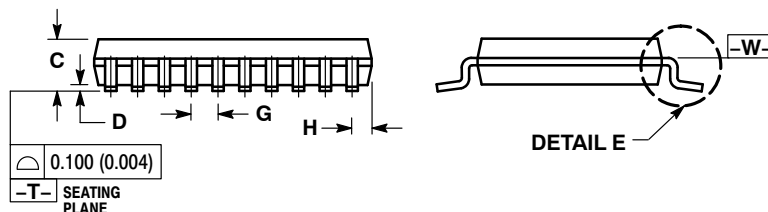
DATE 17 FEB 2016

SCALE 2:1

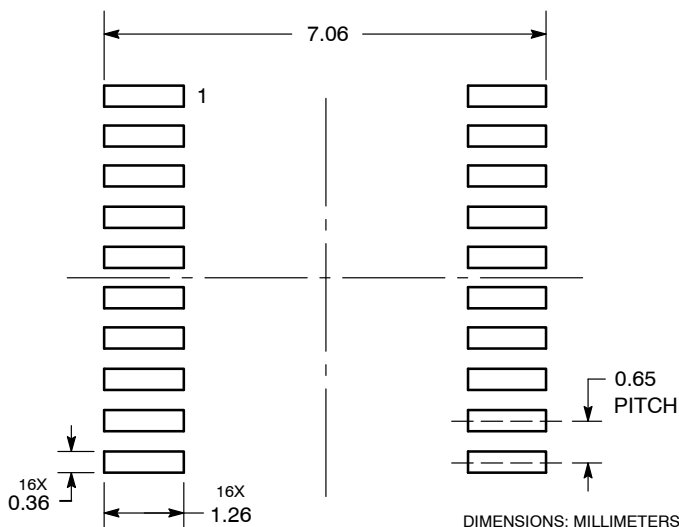


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

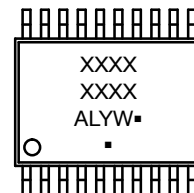
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
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