

SDI-FMC

USER MANUAL

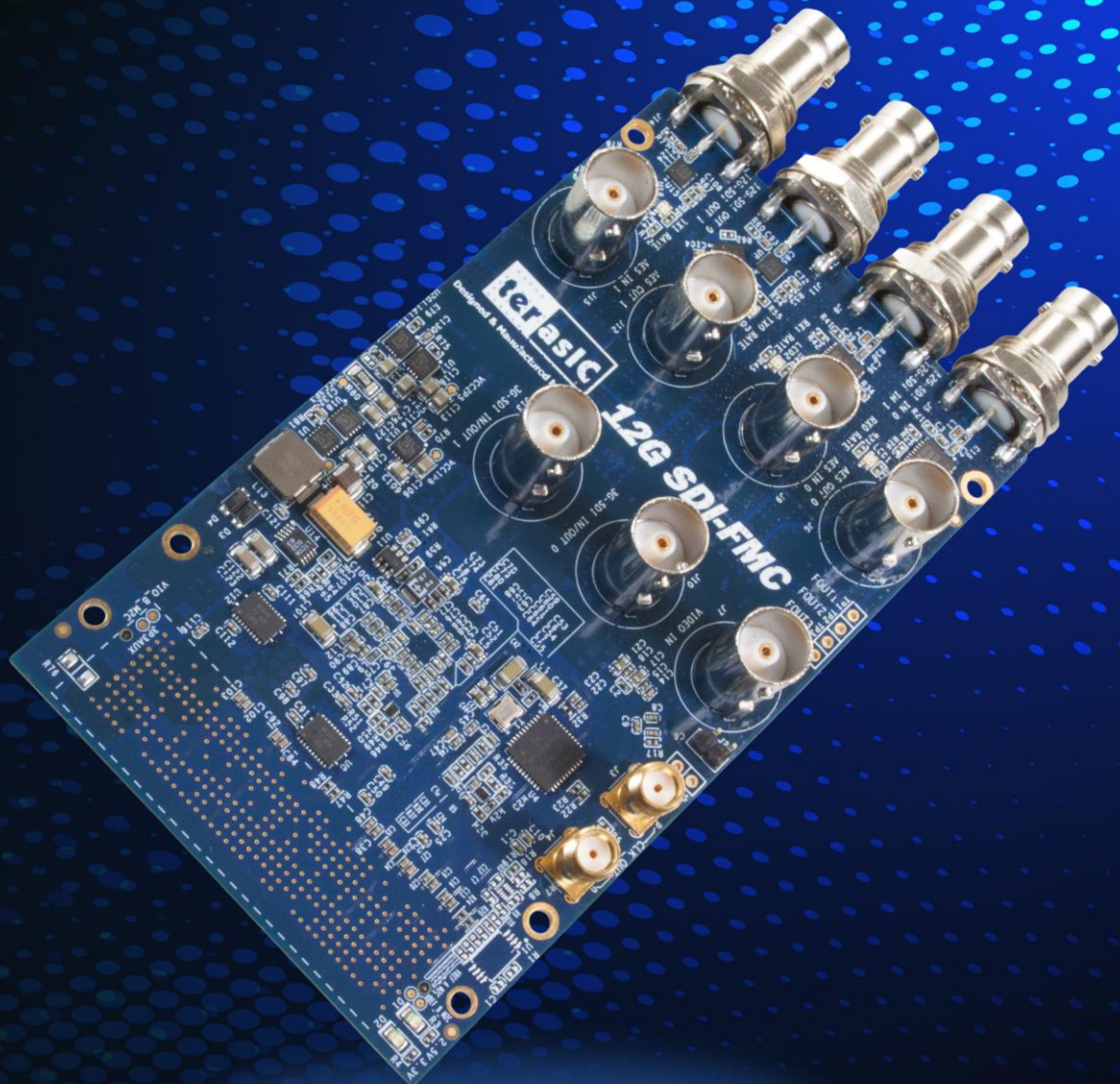


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The Terasic SDI-FMC is a 12G SDI daughter card. It enables users to design and verify their 12G SDI product. The board includes 12G SDI, 3G SDI, AES, and Clock Generators. It uses an FMC expansion connector to interface to the FPGA boards which can support 12G SPI IP, e.g. Intel Arria 10 GX FPGA Development Kit (A10GFP) and Arria 10 SoC Development Kit (A10SoC).

1.1 The Package Contents

The SDI-FMC kit comes with the following items:

- SDI-FMC Daughter Card
- CD Download Guide
- Supporting Package

The system CD contains technical documents of the SDI-FMC kit, which include component datasheets, demonstrations, schematic and user manual. Users can download the CD from the link below:

<http://sdi-fmc.terasic.com/cd>

Figure 1-1 shows the contents of the SDI-FMC kit.



Figure 1-1 Contents of the SDI-FMC Kit

1.2 Assemble SDI-FMC with FPGA Mainboard

In order to make the SDI-FMC daughter card and the FMC connector on the FMC card with more secure hookup, the FMC side of the SDI-FMC daughter card has reserved two screw holes, as shown in **Figure 1-2**. Users can use the screws, copper pillars, and nuts that come with the SDI-FMC, to secure the SDI-FMC on the FPGA mainboard, as shown in **Figure 1-3**. In order to use the 12G SDI high-speed transmission in normal operation, we strongly recommend that users use the screws to secure the connection between the mainboard and the SDI-FMC card.



Figure 1-2 Two screw holes on the FMC side of the SDI-FMC

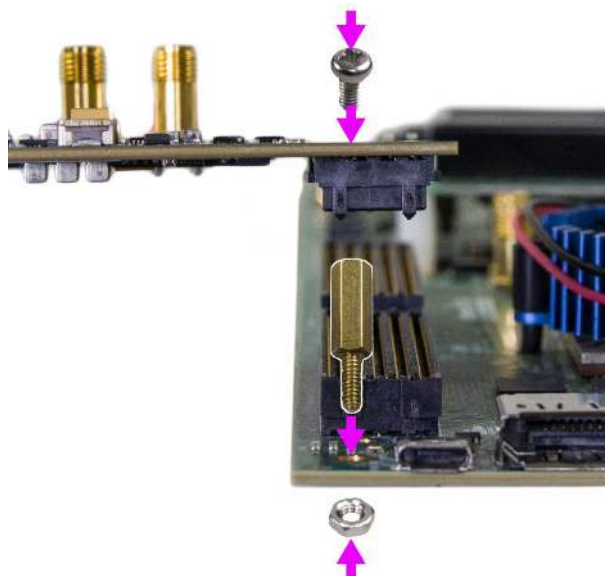


Figure 1-3 Use the screws, copper pillars, and nuts to secure the connection between the SDI-FMC and the FPGA mainboard

In addition to the screws, the SDI-FMC Kit also provides copper pillars and silicon brackets. Users can reference **Figure 1-4** for installation of the brackets for the SDI-FMC. Note: The height of these brackets is designed specifically for the Intel A10SoC and A10GFP. These brackets may not be suitable for other FPGA mainboards.

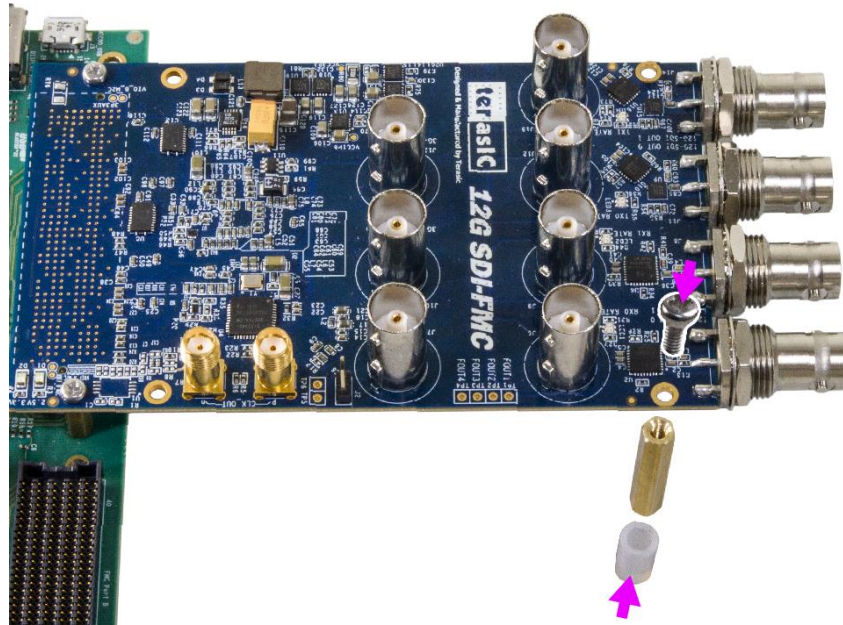


Figure 1-4 Installation of the SDI-FMC brackets

Figure 1-5 shows the completion of the connection assembly on the SDI-FMC and A10SoC

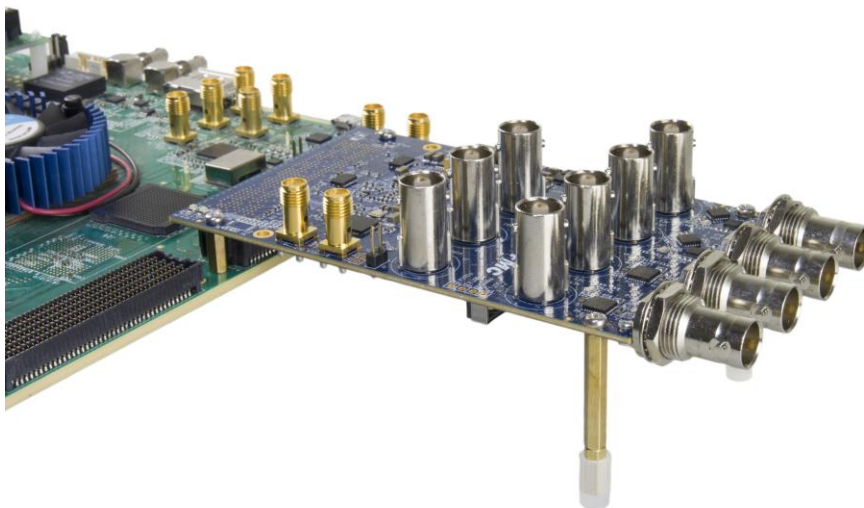


Figure 1-5 SDI-FMC Assembled with A10SoC

1.3 Connectivity

Figure 1-6 and Figure 1-7 below show the connectivity of the SDI-FMC to the A10SoC and A10GFP FPGA boards. The SDI-FMC is powered from FPGA mainboard. It is not necessary to connect a power adapter to the SDI-FMC.

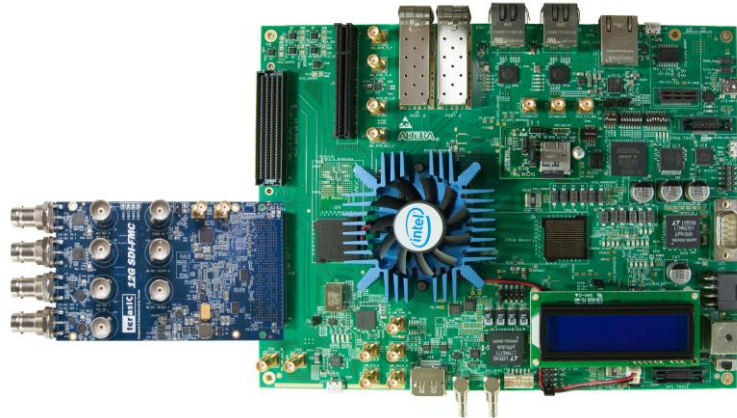


Figure 1-6 SDI-FMC with A10SoC



Figure 1-7 SDI-FMC with A10GFP

1.4 Getting Help

For Technical Support, Terasic's Contact Information is listed below:

- Office Hours: 9:00 a.m. to 6:00 p.m. (GMT +8)
- Telephone: +886-3-575-0880
- Email: support@terasic.com

Chapter 2

Architecture of SDI-FMC

This chapter lists the features and describes the architecture of SDI-FMC daughter card.

2.1 Features

The key features of this module are listed below:

- Two 12G SDI inputs and outputs (Connected to 4 75 Ohm BNC connector)
- Two 3G SDI inputs or outputs (Connected to 2 75 Ohm BNC connector)
- Two AES inputs and outputs (Connected to 2 75 Ohm BNC connector)
- Clock Generator
- FMC interface

2.2 Layout and Block Diagram

■ Component and Layout

The top view of the SDI-FMC is shown in **Figure 2-1**.

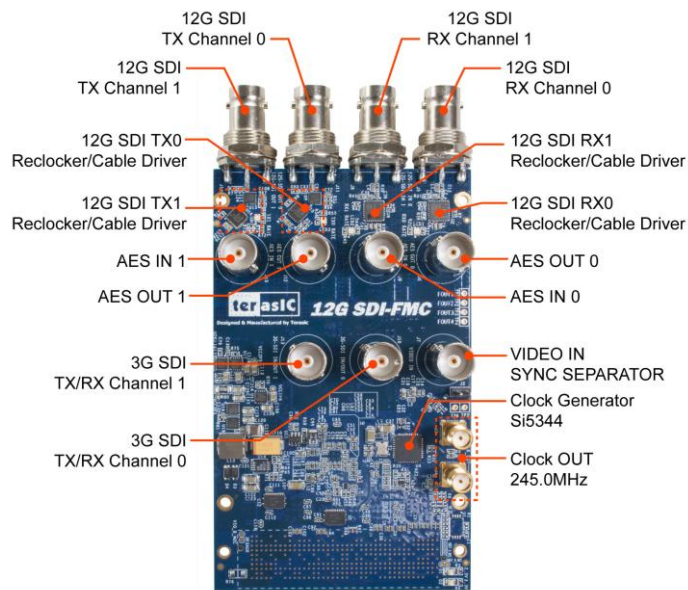


Figure 2-1 Top view of the SDI-FMC Daughter Card

The bottom view of the SDI-FMC is shown in **Figure 2-2**. It depicts the layout and indicates the locations of connectors and key components.

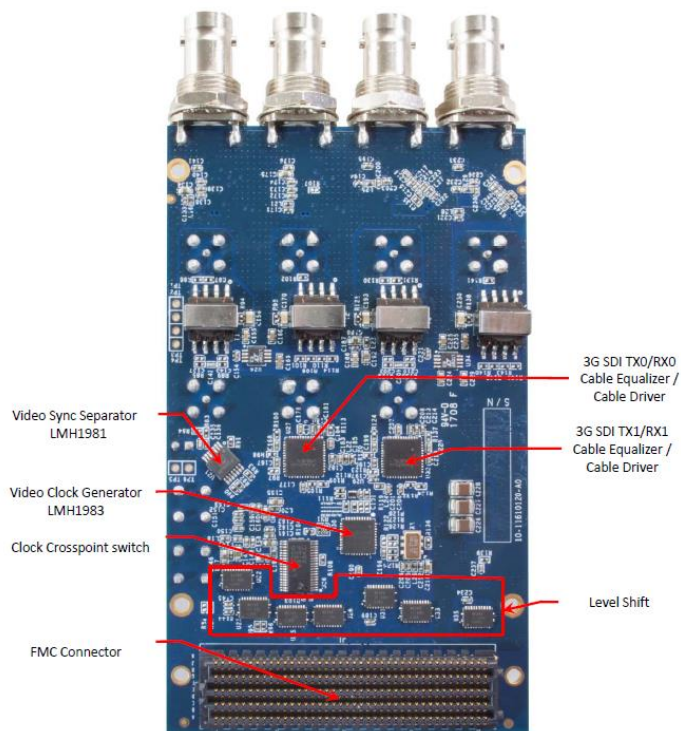


Figure 2-2 Bottom view of the SDI-FMC Daughter Card

■ Block Diagram

Figure 2-3, Figure 2-4 and Figure 2-5 show the block diagrams of the SDI-FMC. The diagrams contain SDI, AES and clock generators three parts. Figure 2-3 shows the SDI function. There are two independent 12G SDI channels in the boards. Each channel contains one transmitter port and one receiving port connected to the BNC connectors. The six 12G SDI chips can be configured through the SPI chain. There are also two independent 3G SDI channels in the boards. Each channel can be configured as either input channel or output channel. The 3G SDI is connected to the BNC connectors. The 3G SDI chips can be configured through their SPI interface.

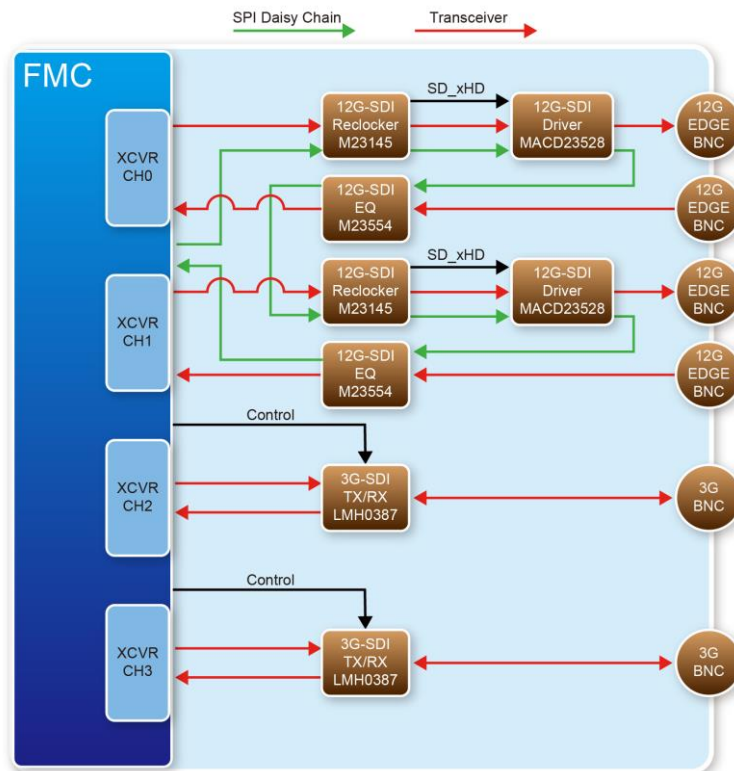


Figure 2-3 SDI Function in the Block Diagram

Figure 2-4 shows the AES audio function. There are two independent AES channels in the boards. Each channel contains one transmitter port and one receiving port connected to the BNC connectors.

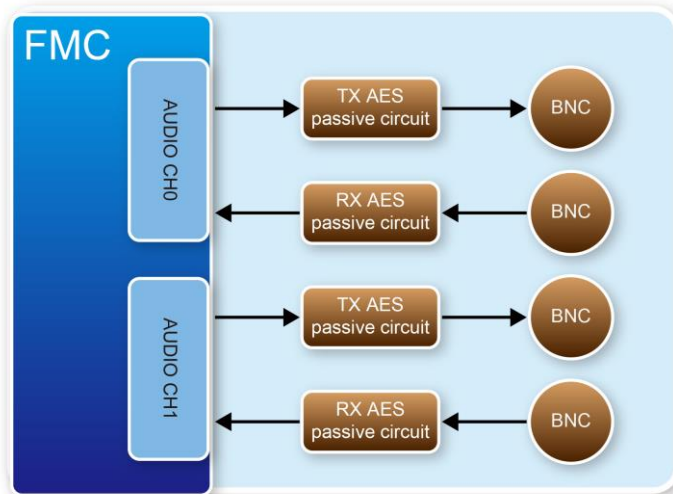


Figure 2-4 AES Function in the Block diagram

Figure 2-5 shows the clock functions. The Si5344, LMH1981 and LMH1983 can provide required clock sources for SDI application.

Please note, when users connect the SDI-FMC card to FPGA main board and power on it, the FPGA should reset the clock generator Si5344 first to output the correct frequency. The output frequency of Si5344 without reset action will be significantly different from the expected output frequency, which will cause the SDI signal synchronization failure.

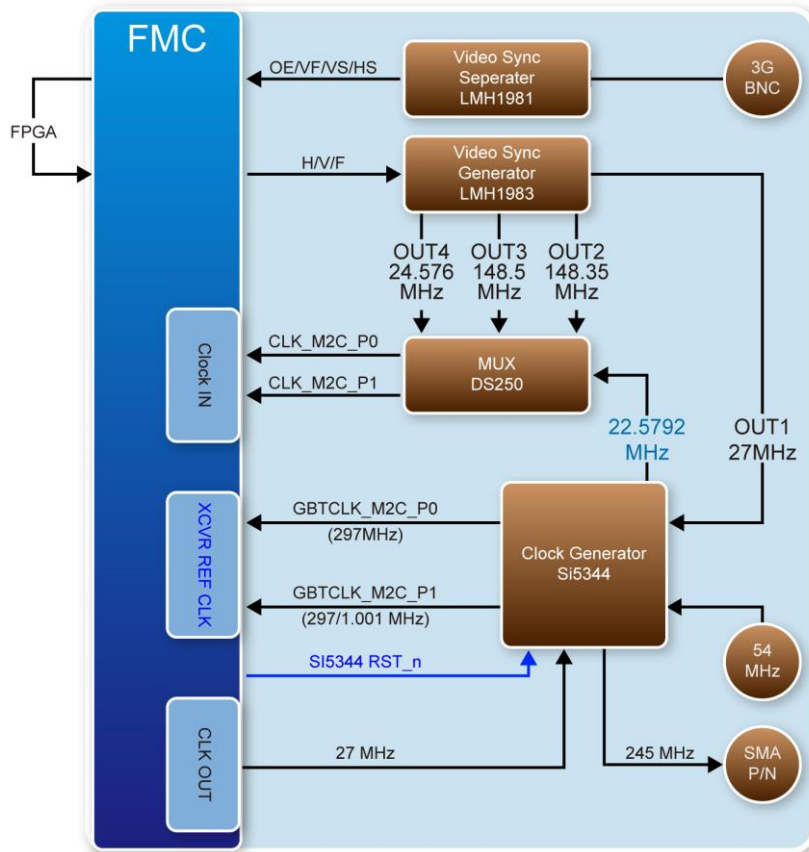


Figure 2-5 Clock Functions in the Block diagram

Using the SDI-FMC

This chapter provides information on how to control the hardware of the SDI-FMC. It includes the definition of the FMC interface and how to use the 12G SDI, 3G SDI, AES and clock generator hardware in the board.

3.1 Pin Definition of FMC Connector

The FMC connector on the SDI-FMC daughter card connects directly to the FMC connector on the FPGA board. **Figure 3-1**, **Figure 3-2** and **Figure 3-3** illustrates the signal names of the FMC connector.

J1A			
D8	LA_TX_CLK_P0	LA_RX_CLK_P	G6
D9	LA_TX_CLK_N0	LA_RX_CLK_N	G7
VCG_H	H7	LA_RX_P0	G9 VCG_NO_LOCK
VCG_V	H8	LA_RX_N0	G10 VCG_NO_ALIGN
VCG_F	H10	LA_RX_P1	C10 VCG_INIT
	H11	LA_RX_N1	C11 FMC_SDI_12G_RC_ALARM_n0
	D11	LA_RX_P2	G12 FMC_SDI_12G_RC_LOS1
	D12	LA_RX_N2	G13 FMC_SDI_12G_RC_ALARM_n1
FPGA_CLK_p	H13	LA_RX_P3	C14 FMC_SDI_12G_RC_LOS0
FPGA_CLK_n	H14	LA_RX_N3	C15 FMC_SDI_12G_RX_LOS0
VSS_OE	D14	LA_RX_P4	G15 FMC_SDI_12G_RX_ALARM_n0
VSS_VF	D15	LA_RX_N4	G16 FMC_SDI_12G_RX_SD_xHD0
VSS_VS	H16	LA_RX_P5	C18 FMC_SDI_12G_RX_LOS1
VSS_HS	H17	LA_RX_N5	C19 FMC_SDI_12G_RX_ALARM_n1
FMC_S15344_IN_SEL1	D17	LA_RX_P6	G18
FMC_S15344_INTR_n	D18	LA_RX_N6	G19 FMC_SDI_12G_RX_SD_xHD1
FMC_S15344_LOL_n	H19	LA_RX_P7	C22 FMC_AES_IN0
FMC_S15344_LOL_XTAL_n	H20	LA_RX_N7	C23 FMC_AES_IN1
FMC_SDI_12G_SPI_SCLK	D20	LA_RX_P8	G21 FMC_SDI_3G_SPI_SS_n0
FMC_SDI_12G_SPI_CS_n	D21	LA_RX_N8	G22 FMC_SDI_3G_TX_EN0
FMC_SDI_12G_SPI_SDO	H22	LA_RX_P9	G24 FMC_SDI_3G_TX_RATE_SELO
FMC_SDI_12G_SPI_SDI	H23	LA_RX_N9	G25 FMC_SDI_3G_SPI_SS_n1
FMC_CLKSEL_S10	H25	LA_RX_P10	G27 FMC_SDI_3G_TX_EN1
FMC_CLKSEL_S11	H26	LA_RX_N10	G28 FMC_SDI_3G_TX_RATE_SEL1
FMC_CLKSEL_S20	D23	LA_RX_P11	C26 FMC_AES_OUT0
FMC_CLKSEL_S21	D24	LA_RX_N11	C27 FMC_AES_OUT1
VCG_NO_REF	H28	LA_RX_P12	G30 FMC_S15344_I2C_SEL
FMC_SDI_3G_SPI_MOSI	H29	LA_RX_N12	G31 FMC_S15344_A1_SDO
FMC_SDI_3G_SPI_SCK	D26	LA_RX_P13	G33 FMC_S15344_A0_CS_n
FMC_SDI_3G_SPI_MISO	D27	LA_RX_N13	G34 FMC_S15344_RST_n
FMC_SDI_3G_CD_n0	H31	LA_RX_P14	G36 FMC_S15344_OE_n
FMC_SDI_3G_CD_n1	H32	LA_RX_N14	G37 FMC_S15344_IN_SELO
VCG_I2C_SDA	H34	LA_TX_P15	
VCG_I2C_SCL	H35	LA_TX_N15	
CLK_I2C_SDA	H37	LA_TX_P16	
CLK_I2C_SCL	H38	LA_TX_N16	

FMC_10x40_Altera

Figure 3-1 Signal names of FMC connector part 1

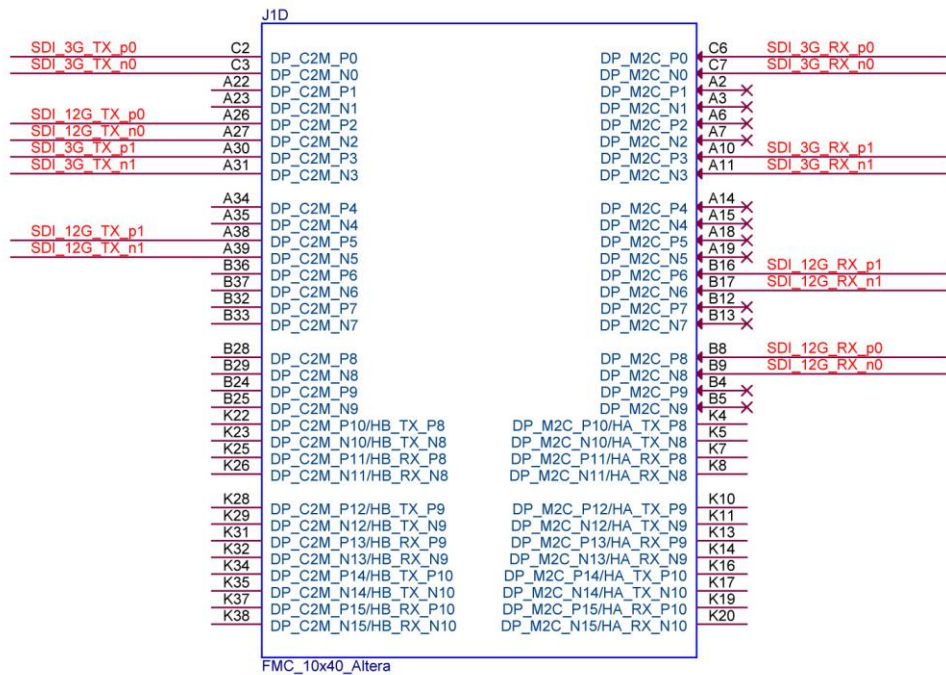


Figure 3-2 Signal names of FMC connector part 2

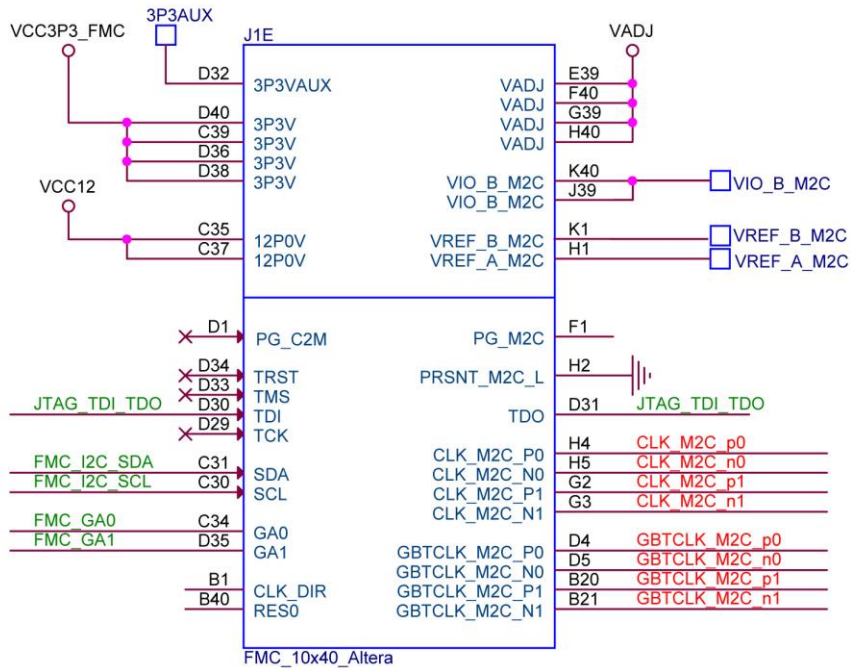


Figure 3-3 Signal names of FMC connector part 3

Table 3-1 shows the SDI-FMC pin assignments for the SDI-FMC pins in Quartus Prime.

Table 3-1 SDI-FMC Pin Assignments of FMC in Quartus Prime

<i>Signal Name</i>	<i>FMC Pin No.</i>	<i>Description</i>	<i>Direction</i>	<i>IO Standard</i>
VCG_H	H7	LMH1983 Horizontal sync reference signal	Output	VCCADJ
VCG_V	H8	LMH1983 Vertical sync reference signal	Output	VCCADJ
VCG_F	H11	LMH1983 Field sync (odd/even) reference signal	Output	VCCADJ
VCG_INIT	C10	LMH1983 Reset signal for audio-video phase alignment (rising edge triggered)	Output	VCCADJ
VCG_NO_LOCK	G9	LMH1983 Loss of lock status flag for PLLs 1-4 (active high)	Input	VCCADJ
VCG_NO_ALIGN	G10	LMH1983 Loss of alignment status flag for OUTs 1-4 (active high)	Input	VCCADJ
VCG_NO_REF	H28	Loss of reference status flag (active high)	Input	VCCADJ
VCG_I2C_SDA	H34	LMH1983 I2C Data signal	Input/ Output	VCCADJ
VCG_I2C_SCL	H35	LMH1983 I2C Clock signal	Output	VCCADJ

VSS_HS	H17	LMH1981 Horizontal Sync Output	Input	VCCADJ
VSS_VS	H16	LMH1981 Vertical Sync Output	Input	VCCADJ
VSS_VF	D15	LMH1981 Video Format Output	Input	VCCADJ
VSS_OE	D14	LMH1981 Odd/Even Field Output	Input	VCCADJ
FMC_CLKSEL_S10	H25	Select Reference Clock 0 input source, bit 0	Output	VCCADJ
FMC_CLKSEL_S11	H26	Select Reference Clock 0 input source, bit 1	Output	VCCADJ
FMC_CLKSEL_S20	D23	Select Reference Clock 1 input source, bit 0	Output	VCCADJ
FMC_CLKSEL_S21	D24	Select Reference Clock 1 input source, bit 1	Output	VCCADJ
CLK_I2C_SDA	H37	Serial Data Signal	Input/ Output	VCCADJ
CLK_I2C_SCL	H38	Serial Clock Signal	Output	VCCADJ
FMC_SI5344_I2C_SEL	G30	Serial interface select, FMC_SI5344_I2C_SEL = 0 is SPI Mode. FMC_SI5344_I2C_SEL = 1 is I2C mode. Please setting high for I2C Interface.	Output	VCCADJ
FMC_SI5344_A1_SDO	G31	I2C Interface Address Select 1	Input/ Output	VCCADJ

FMC_SI5344_A0_CS_n	G33	I2C Interface Address Select 0	Output	VCCADJ
FMC_SI5344_RST_n	G34	Si5344 Device Reset. Active low input that performs power-on reset (POR) of the device. Clock outputs are disabled during reset.	Output	VCCADJ
FMC_SI5344_OE_n	G36	Si5344 Device Output Enable. Disables all outputs when held high.	Output	VCCADJ
FMC_SI5344_IN_SEL0	G37	Input Reference Select, bit0.	Output	VCCADJ
FMC_SI5344_IN_SEL1	D17	Input Reference Select, bit1.	Output	VCCADJ
FMC_SI5344_INTR_n	D18	Interrupt output. This pin is asserted low when a change in device status has occurred.	Input	VCCADJ
FMC_SI5344_LOL_n	H19	Loss Of Lock This output pin indicates when the DSPLL is locked (high) or out-of-lock (low).	Input	VCCADJ
FMC_SI5344_LOL_XTAL_n	H20	Loss Of Signal on XA/XB Pins.	Input	VCCADJ

		This pin indicates a loss of signal at the XA/XB pins when low.		
FMC_SDI_12G_SPI_SCLK	D20	SDI 12G SPI interface, Slave clock input signal.	Output	VCCADJ
FMC_SDI_12G_SPI_CS_n	D21	SDI 12G SPI interface, Chip select signal, Low active.	Output	VCCADJ
FMC_SDI_12G_SPI_SDI	H23	SDI 12G SPI interface, Slave data input signal	Output	VCCADJ
FMC_SDI_12G_SPI_SDO	H22	SDI 12G SPI interface, Slave data output signal	Input	VCCADJ
FMC_SDI_12G_RX_LOS0	C15	SDI 12G RX 0 LOS signal, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold	Input	VCCADJ
FMC_SDI_12G_RX_ALARM_n0	G15	SDI 12G RX 0 ALARM signal,	Input	VCCADJ

		Active low (open drain) H: Normal operation L: Alarm asserted		
FMC_SDI_12G_RX_SD_xHD0	G16	SDI 12G RX 0 SD Data Rate H: SD data rate detected L: HD/3G/6G/12G data rate detected	Input	VCCADJ
FMC_SDI_12G_RX_LOS1	C18	SDI 12G RX 1 LOS signal, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold	Input	VCCADJ
FMC_SDI_12G_RX_ALARM_n1	C19	SDI 12G RX 0 ALARM signal, Active low (open drain) H: Normal operation L: Alarm asserted	Input	VCCADJ
FMC_SDI_12G_RX_SD_xHD1	G19	SDI 12G RX 1 SD Data Rate H: SD data rate	Input	VCCADJ

		detected L: HD/3G/6G/12G data rate detected		
FMC_SDI_12G_RC_LOS0	C14	SDI 12G TX 0 Reclocker LOS signal, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold	Input	VCCADJ
FMC_SDI_12G_RC_ALARM_n0	C11	SDI 12G TX 0 Reclocker ALARM signal, Active low (open drain) H: Normal operation L: Alarm asserted	Input	VCCADJ
FMC_SDI_12G_RC_LOS1	C12	SDI 12G TX 1 Reclocker LOS signal, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is	Input	VCCADJ

		present and cable length is below the MUTEREF threshold		
FMC_SDI_12G_RC_ALARM_n1	C13	SDI 12G TX 1 Reclocker ALARM signal, Active low (open drain) H: Normal operation L: Alarm asserted	Input	VCCADJ
FMC_SDI_3G_SPI_MISO	D27	SDI 3G SPI Interface Data. Master Input, Slave Output.	Input	VCCADJ
FMC_SDI_3G_SPI_MOSI	H29	SDI 3G SPI Interface Data. Master Output, Slave Input.	Output	VCCADJ
FMC_SDI_3G_SPI_SCK	D26	SDI 3G SPI Interface, Serial clock.	Output	VCCADJ
FMC_SDI_3G_SPI_SS_n0	G21	SDI 3G SPI Interface, Slave Select for device 0. Low active.	Output	VCCADJ
FMC_SDI_3G_SPI_SS_n1	G25	SDI 3G SPI Interface, Slave Select for device 1. Low active.	Output	VCCADJ
FMC_SDI_3G_CD_n0	H31	SDI 3G Channel 0 Carrier detect, H = No input signal	Input	VCCADJ

		detected. L = Input signal detected.		
FMC_SDI_3G_CD_n1	H32	SDI 3G Channel 1 Carrier detect, H = No input signal detected. L = Input signal detected.	Input	VCCADJ
FMC_SDI_3G_TX_EN0	G22	SDI 3G Channel 0 Transmitter output driver enable. Internal pullup. H = output driver is enabled. L = output driver is powered off.	Output	VCCADJ
FMC_SDI_3G_TX_EN1	G27	SDI 3G Channel 1 Transmitter output driver enable. Internal pullup. H = output driver is enabled. L = output driver is powered off.	Output	VCCADJ
FMC_SDI_3G_TX_RATE_SEL0	G24	SDI 3G Channel 0 output slew rate control. Internal pulldown. H = Output rise/fall time complies with SMPTE 259M (SD).	Output	VCCADJ

		L = Output rise/fall time complies with SMPTE 424M / 292M (3G/HD).		
FMC_SDI_3G_TX_RATE_SEL1	G28	SDI 3G Channel 1 output slew rate control. Internal pulldown. H = Output rise/fall time complies with SMPTE 259M (SD). L = Output rise/fall time complies with SMPTE 424M / 292M (3G/HD).	Output	VCCADJ
FPGA_CLK_p	H13	For Si5344 input reference clock 1.	Output	VCCADJ
FPGA_CLK_n	H14	For Si5344 input reference clock 1.	Output	VCCADJ
FMC_AES_IN0	C22	AES Channel 0 input.	Input	VCCADJ
FMC_AES_IN1	C23	AES Channel 1 input.	Input	VCCADJ
FMC_AES_OUT0	C26	AES Channel 0 output.	Output	VCCADJ
FMC_AES_OUT1	C27	AES Channel 0 output.	Output	VCCADJ
CLK_M2C_p0	H4	Reference Clock 0 for FPGA.	Input	VCCADJ
CLK_M2C_n0	H5	Reference Clock 0 for FPGA.	Input	VCCADJ
CLK_M2C_p1	G2	Reference Clock 1 for	Input	VCCADJ

		FPGA.		
CLK_M2C_n1	G3	Reference Clock 1 for FPGA.	Input	VCCADJ
GBTCLK_M2C_p0	D4	Transceiver Reference clock 0, 297MHz input.	Input	VCCADJ
GBTCLK_M2C_n0	D5	Transceiver Reference clock 0, 297MHz input.	Input	VCCADJ
GBTCLK_M2C_p1	B20	Transceiver Reference clock 0, 297.0/1.001MHz input.	Input	VCCADJ
GBTCLK_M2C_n1	B21	Transceiver Reference clock 0, 297.0/1.001MHz input.	Input	VCCADJ
SDI_12G_TX_p0	A26	SDI 12G Transmitter Channel 0	Output	VCCADJ
SDI_12G_TX_n0	A27	SDI 12G Transmitter Channel 0	Output	VCCADJ
SDI_12G_TX_p1	A38	SDI 12G Transmitter Channel 1	Output	VCCADJ
SDI_12G_TX_n1	A39	SDI 12G Transmitter Channel 1	Output	VCCADJ
SDI_12G_RX_p0	B8	SDI 12G Receiver Channel 0	Input	VCCADJ
SDI_12G_RX_n0	B9	SDI 12G Receiver Channel 0	Input	VCCADJ
SDI_12G_RX_p1	B16	SDI 12G Receiver Channel 1	Input	VCCADJ
SDI_12G_RX_n1	B17	SDI 12G Receiver Channel 1	Input	VCCADJ

SDI_3G_TX_p0	C2	SDI 3G Transmitter Channel 0	Output	VCCADJ
SDI_3G_TX_n0	C3	SDI 3G Transmitter Channel 0	Output	VCCADJ
SDI_3G_TX_p1	A30	SDI 3G Transmitter Channel 1	Output	VCCADJ
SDI_3G_TX_n1	A31	SDI 3G Transmitter Channel 1	Output	VCCADJ
SDI_3G_RX_p0	C6	SDI 3G Receiver Channel 0	Input	VCCADJ
SDI_3G_RX_n0	C7	SDI 3G Receiver Channel 0	Input	VCCADJ
SDI_3G_RX_p1	A10	SDI 3G Receiver Channel 1	Input	VCCADJ
SDI_3G_RX_n1	A11	SDI 3G Receiver Channel 1	Input	VCCADJ

3.2 Using the 12G SDI

Figure 3-4 shows the system block diagram of the 12G SDI. The M23145 Reclocker chips and MACD23528 Cable Driver chips are used to transmit the 12G SDI signal and the M23554 Cable Equalizer chips are used to receive the 12G SDI signal. The M23145 and M23554 are directly connected to the FPGA transceiver pins. The BNC connectors are used as an interface to connect the external 12G SDI signals. Besides the 12G SDI signal, these chips also support the 6G/3G/HD/SD SDI signals.

The six 12G-SDI chips are connected through an SPI daisy chain (seeing green line in **Figure 3-4**). Developers can communicate with these chips through the SPI interface. Due to the NDA limitation (for detail information about how to control the 12G SDI chips) please contact the chip vender **MACOM** Company.

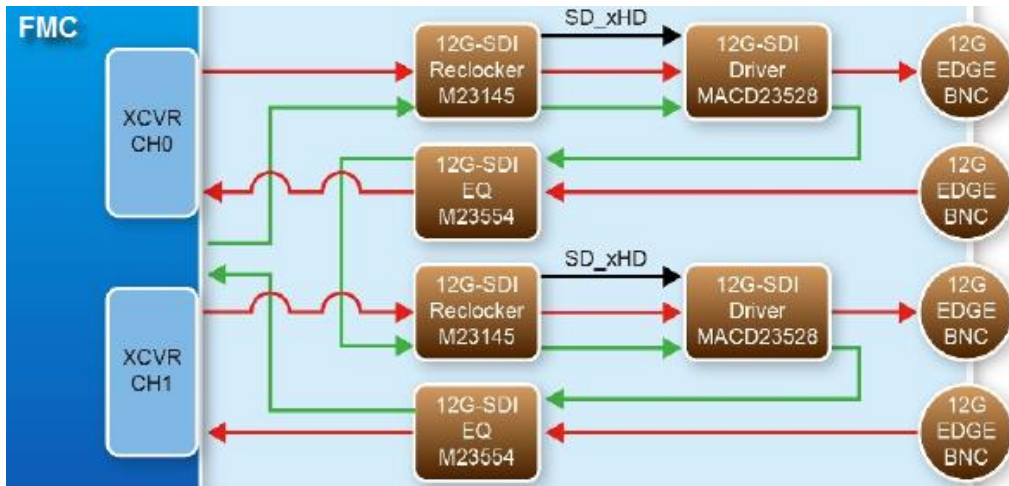


Figure 3-4 12G SDI System Block Diagram

3.3 Using the 3G SDI

Figure 3-5 shows the system block diagram of the 3G SDI. The LMH0387 chips are used to either transmit or receive a 3G SDI signal. The LMH0387 is directly connected to the FPGA transceiver pins. The BNC connectors are used as an interface to connect external 3G SDI signals. The LMH0387 chips can be configured either in the input mode as an equalizer to receiver data over coaxial cable, or in the output mode as a cable driver to transmit data over coaxial cable. Developers can configure the chips through the chips' SPI interface. For detailed information about how to control the SDI chips, please refer to the chips' datasheet included in the SDI-FMC CD-ROM.

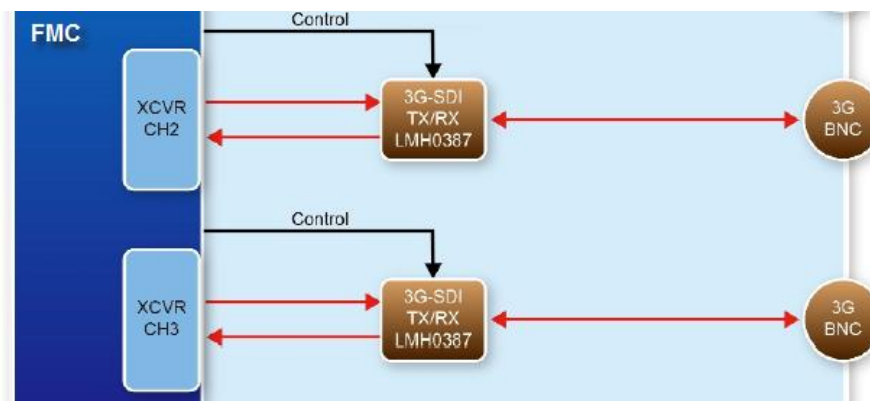


Figure 3-5 3G SDI System Blok Diagram

3.4 Using the AES

Figure 3-6 shows the system block diagram of the AES. There are two AES channels on the SDI-FMC Board. Each contains one TX channel and one RX Channel.

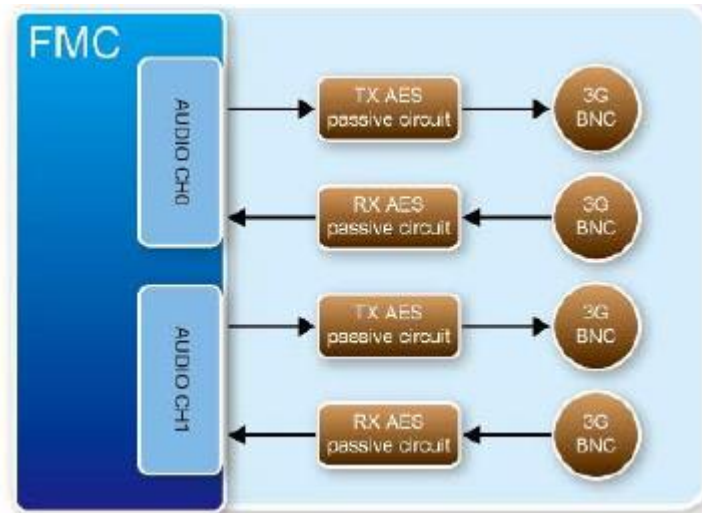


Figure 3-6 AES System Blok Diagram

The AES3 RX channel delivers a 75-Ω load termination with a return loss of 25 dB or more. The signal is inputted through a 75-Ω BNC and terminated with a 75-Ω resistor to ground. The unbalanced signal is then balanced through an isolation transformer. The differential signal output from the transformer is biased and input to a RS422 transceiver. The output of the RS422 transceiver is a single-ended LVCMOS signal which is driven to the host board through the HSMC connector.

Figure 3-7 shows the AES3 RX Channel block diagram.

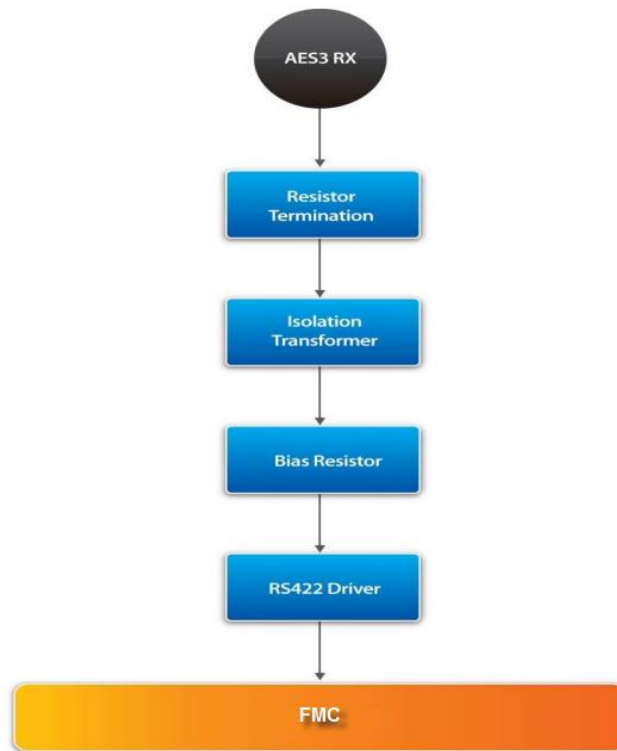


Figure 3-7 AES RX Channel Block Diagram

The AES3 TX channel is designed to have a balanced signal driver next to or on the isolation transformer. The output of the RS422 transceiver has an RX network to limit the output slew rate, thus limiting the bandwidth of AES3 output. The AES3 channel is designed to support 192-kHz to 24-kHz sample rates. The output is unbalanced with a source impedance of 75 Ω and a return loss of 25 dB or more. The peak-to-peak output voltage is 1.0V centered around the ground the transmitter.

Figure 3-8 shows the AES3 TX Channel block diagram.

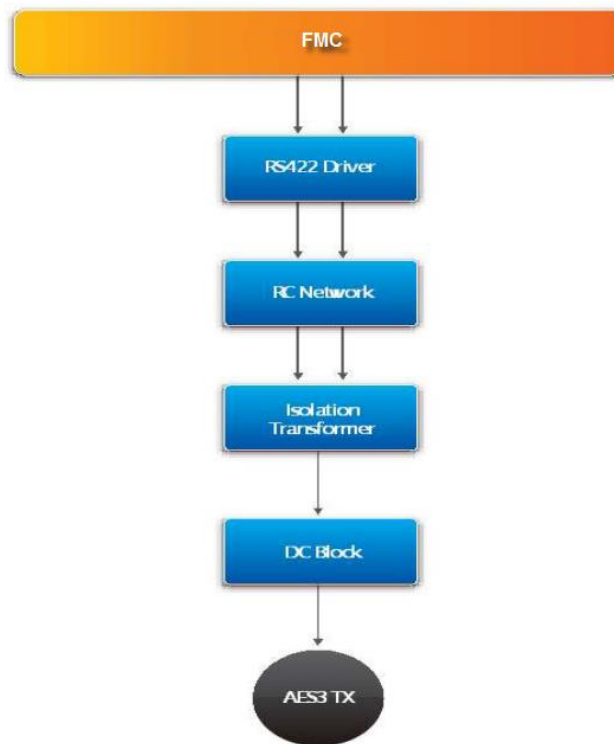


Figure 3-8 AES TX Channel Block Diagram

3.5 Using the Clock Generators

Figure 3-9 shows the block diagram of clock generators on the SDI-FMC. The Si5344 is designed to generate 270.0 and 270.0/1.001 clocks for the transceiver based SDI IP in FPGA. The LMH1983 provides 27MHz as a reference clock for Si5344 chip. In the demonstration project, Terasic provides the Si5344 and LMH1983 configure IP so developers can easily configure these clock generator chips to generate the required clock frequency/ies.

Please note, when users connect the SDI-FMC card to FPGA main board and power on it, the FPGA should reset the clock generator Si5344 first to output the correct frequency. The output frequency of Si5344 without reset action will be significantly different from the expected output frequency, which will cause the SDI signal synchronization failure.

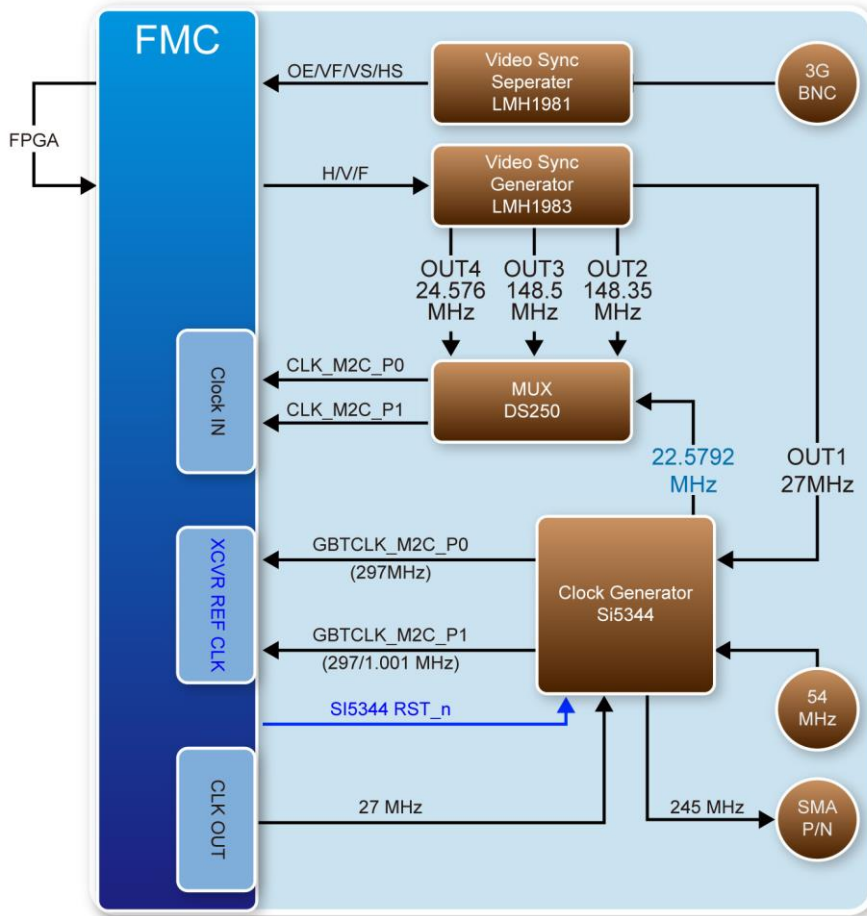


Figure 3-9 Clock Generator System Block Diagram

Chapter 4

SDI Demonstrations

This chapter shows how to use Quartus SDI II IP to generate SDI video pattern and perform loopback test for 12G SDI chips and 3G SDI chips. For 12G SDI chips, the multi rate video standard is selected in SDI II IP to support SD-SDI, HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI. For 3G SDI chips, the triple rate video standard is selected in SD II IP to support SD-SDI, HD-SDI, and 3G-SDI. This demo requires the following hardwares:

- A10SoC or A10GFP FPGA Mainboard
- SDI-FMC Daughter Card
- 12G SDI BNC to BNC Cable x2
- 3G SDI BNC to BNC Cable x1

4.1 Demo Description

Figure 4-1 shows the data path of the loopback test for the 12G SDI signals. There are two 12G SDI loopback tests in the demo. For each 12G SDI loopback test, there is a 12G SDI Pattern Generator module in the FPGA to generate a 12G SDI video pattern. The video pattern is transmitted through the 12G SDI reclocker and driver chips. It will be looped back externally via a BNC-to-BNC cable after it reaches the 1st BNC connector. The incoming 12G SDI video pattern from the 2nd BNC connector goes into the 12G SDI EQ chip and then is sent to the Pattern Checker Module in FPGA.

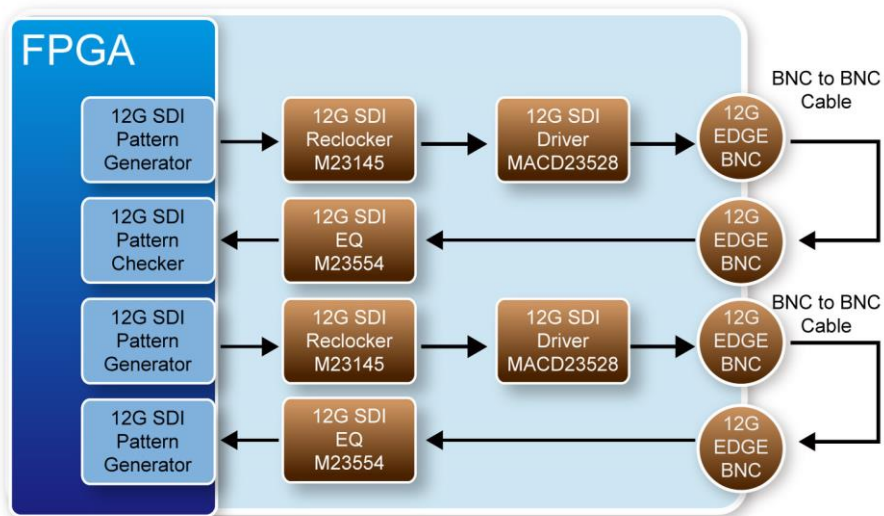


Figure 4-1 Data path for 12G SDI loopback test

For 3G SDI loopback test, there are two test cases because the SDI chips are bi-direction chips. shows the data path for CASE 1 loopback test. In this case, the first 3G-SDI chip is configured as output mode and the second SDI chip is configured as input mode. A BNC to BNC cable is used to loopback the SDI signal from one BNC connector to another. **Figure 4-3** shows the data path for CASE 2 loopback test. It is the complete reverse of CASE1 where the first 3G-SDI chip is configured as input mode and the second SDI chip is configured as output mode.

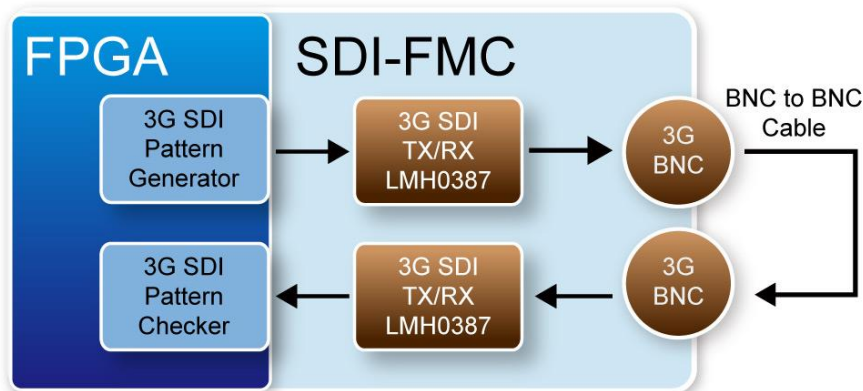


Figure 4-2 Data path for 3G SDI loopback test -CASE1

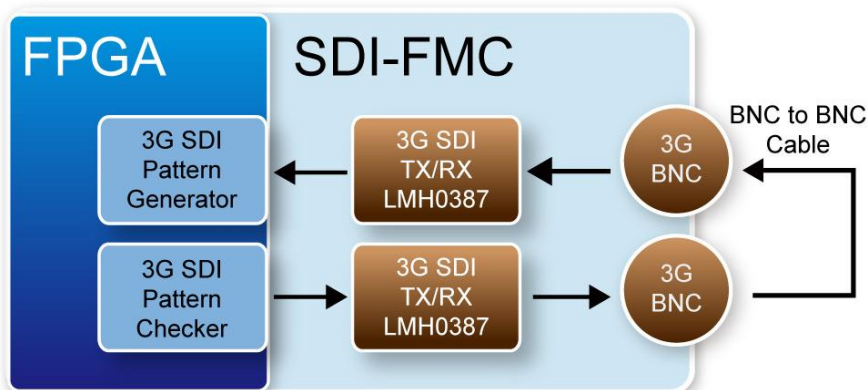


Figure 4-3 Data path for 3G SDI loopback test – CASE2

4.2 System Block Diagram

Figure 4-4 shows the system block diagram of the 12G/3G SDI loopback test. The **TWO_CH_12G** block contains two channels of 12G pattern generator and checker to perform two 12G SDI loopback tests. Each pattern generator and checker is created based on Quartus SDI II IP. The LED0 and LED1 are used by the pattern checkers to report whether they receive a valid SDI pattern. The TRS and Aligns pins of the SDI II controller are used to check whether a valid SDI pattern is received.

When the LED lights up, it means a valid pattern is received. The block requires a 297MHz reference clock for the pattern generator and 148.5MHz reference clock for the pattern checker. The 297 MHz comes from the Si5344 clock generator on the SDI-FMC board and 148.5MHz comes from the FPGA mainboard. The **SI5344_CONFIG** block is used to configure Si5344 chip through I2C interface to generate the required 297MHz clock. The Si5344 required 27MHz reference which can come from either LMH1983 chip on the SDI-FMC board or from FPGA mainboard. The **PLL_27MF** block is used to generate the 27MHz clock. The **SWITCH1** is used to specify whether the 27MHz clock source is form the mainboard or Si5344 chip. The **LMH1983_CONFIG** block is used to configure LMH1983 chip to generator 27MHz clock for Si5344 chip via I2C interface. Please refer to the section **4.7 LMH1983 Configuration IP** in this document for more details.

There are two configuration modes --- AV-Sync and Free-Run, used in this demonstration. **SWITCH2** is used to select which configuration mode is chosen. When AV-Sync mode is selected, the video signal coming from the VIDEO-IN BNC connector J7 is used to synchronize the generated 27MHz. The **SPI_12G_2CH** block is a SPI-Daisy Chain controller. It is used to access the six SDI chips on the SDI-FMC board. **BUTTON1** can be used to toggle the mute function of 12G SDI Driver chips. When **BUTTON1** is pressed, the **SPI_12G_2CH** block will mute SDI TX chips. The SDI TX chips will be unmuted when **BUTTON1** is released. The **BUTTON2** can be

used to adjust the video standard. When **BUTTON2** is pressed, SD SDI video standard is used. When **BUTTON2** is released, 12G SDI video standard is used.

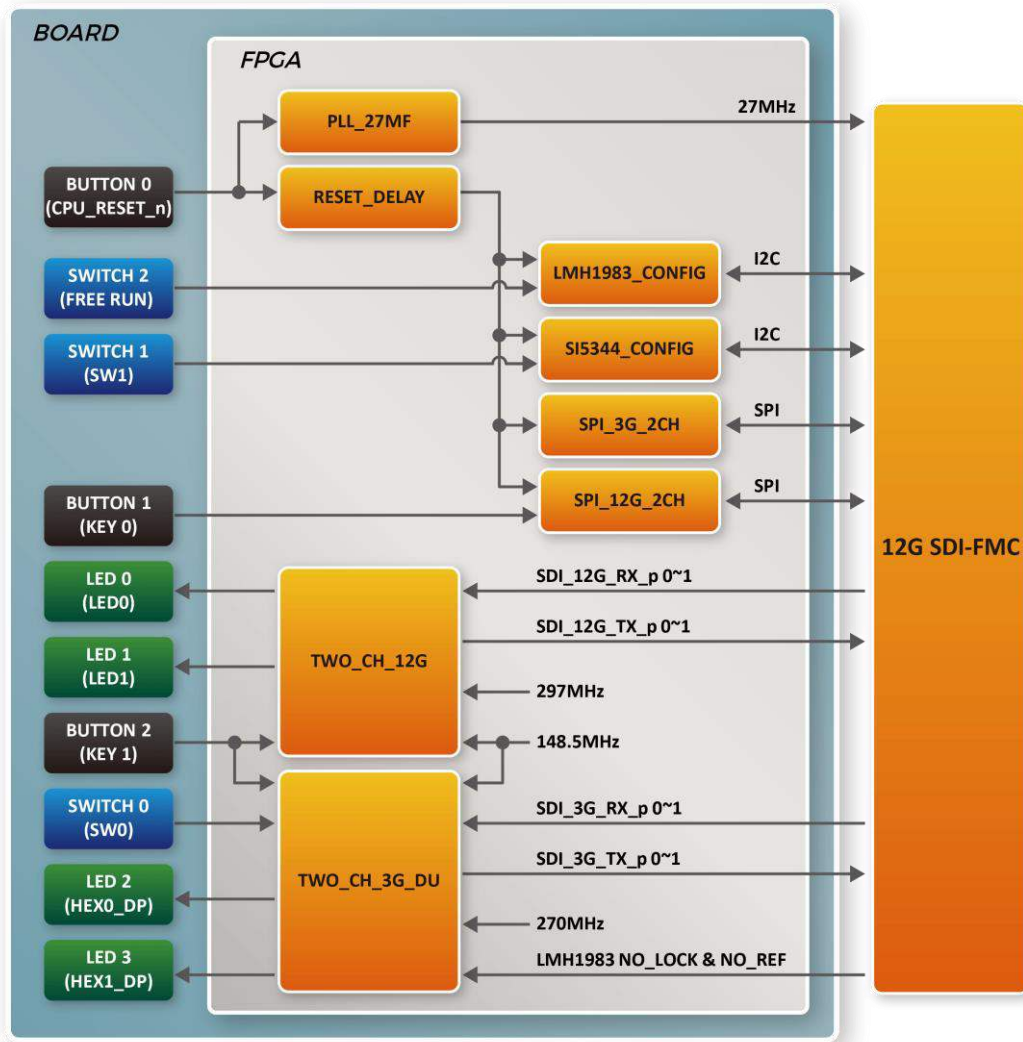


Figure 4-4 Block Diagram of 12G/3G SDI Loopback Test

The **TWO_CH_3G_DU** block contains two channels of 3G pattern generator and checker to perform a 3G SDI loopback test. Only one direction 3G SDI loopback is performed because the 3G SDI chip is a bi-direction chip. The **SWICH0** is used to switch the direction. Each pattern generator and checker is created based on Quartus SDI II IP. The LED2 and LED3 are used by pattern checker to report whether they receive a valid SDI pattern. The TRS and Aligns pins of the SDI II controller are used to check whether a valid SDI pattern is received. When LED is lit, it means a valid pattern is received. The block requires a 148.5 MHz reference clock for the pattern generator and a 270 MHz reference clock for the pattern checker. Both of the clocks are coming from the

FPGA mainboard. The **SPI_3G_2CH** block is a SPI controller. It is used to configure the SDI signal direction of the two 3G SDI chips on the SDI-FMC board. **BUTTON2** can be used to adjust the video standard. When **BUTTON2** is pressed, SD SDI video standard is used. When **BUTTON2** is released, 3G SDI video standard is used. **BUTTON0** is used to reset whole system.

4.3 Demo on A10SoC FPGA Mainboard

This section shows how to setup the demo on the A10SoC Arria 10 FPGA Board.

■ Hardware Setup

Figure 4-5 shows the demo setup of SDI-FMC with A10SoC FPGA mainboard. The SDI-FMC should be installed on the FMC-A expansion header of the A10SoC. Use one BNC to BNC 3G SDI Cable to connect the BNC port J10 and BNC port J13. Use one BNC to BNC 12G SDI Cable to connect the BNC port J11 and the BNC port 15, and use another BNC to BNC 12G SDI Cable to connect the BNC port J14 and the BNC port 8.



Figure 4-5 Hardware setup of SDI-FMC with A10SoC

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the A10SoC.
2. Make sure the SDI-FMC is installed as shown in **Figure 4-5**.
3. Make sure the FMC_A VADJ is set to 1.8V by shorting J42.9 and J42.10 as shown in **Figure 4-6**.
4. Connect the USB-Blaster USB port J22 of the A10SoC to the USB port of host PC with a Mini USB cable.
5. Power on the A10SoC FPGA board.
6. Make sure Quartus Prime and USB-Blaster II driver have been installed on the host PC.

7. Copy the folder Demonstrations/A10SoC_12G_SDI/demo_batch from the SDI-FMC System CD to the host PC and execute “test.bat” to configure the FPGA.
8. Observe LED0 and LED1 as shown in **Figure 4-7**. If two LEDs are lit, it means the two channel 12G SDI loopback test passed.
9. Set the SW2.5 dip switch to down as shown in **Figure 4-8** and observe LED2. If the LED is lit, it means the 3G SDI Loopback test passed. Then, set SW2.5 dip switch to up position, and observe the LED3 to check whether 3G SDI loopback test passed in another direction.
10. **Table 4-1** summarized the functional keys and details of each LED status.

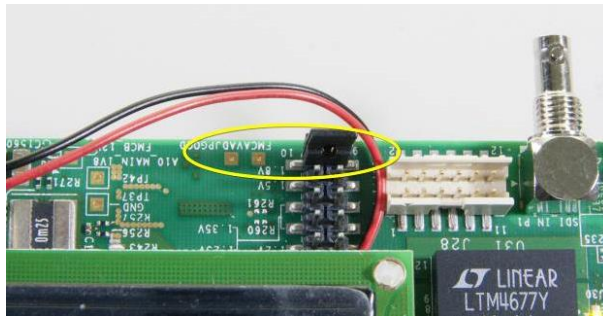


Figure 4-6 Short J42.9 and J42.10

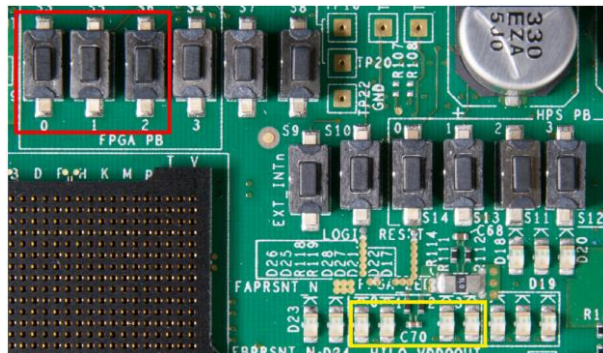


Figure 4-7 BUTTONs and LEDs on A10SoC

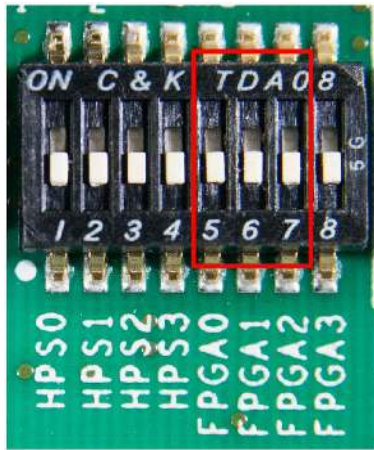


Figure 4-8 SWITCH on A10SoC

Table 4-1 Functional keys of the A10SoC 12G-3G SDI RX/TX demonstration

Name	Description
LED0(D26)	Lighten when 12G Channel 0 receives a valid SDI pattern
LED1(D25)	Lighten when 12G Channel 1 receives a valid SDI pattern
LED2(D28)	<p>Case 1</p> <p>When SWITCH0(SW2.5) is 0 (Up Position):</p> <p>Lighten when 3G Channel 0 receives a valid SDI pattern</p> <p>Case 2</p> <p>When SWITCH0(SW2.5) is 1 (Down Position):</p> <p>Lighten when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p>
LED3(D27)	Case 1

	<p>When SWITCH0(SW2.5) is 0 (Up Position):</p> <p>Lighten when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p> <p>Case 2</p> <p>When SWITCH0(SW2.5) is 1 (Down Position):</p> <p>Lighten when 3G Channel 1 receives a valid SDI pattern</p>
BUTTON0(S3)	SYSTEM reset
BUTTON1(S5)	<p>12G cable driver IC mute control</p> <p>Button Pressed: MUTE</p> <p>Button Released: UNMUTE</p>
BUTTON2(S6)	<p>Video Standard Selection,</p> <p>For 12G-SDI Loopback Test</p> <p>Button Pressed: SD SDI</p> <p>Button Released: 12G SDI</p> <p>For 3G-SDI Loopback Test</p> <p>Button Pressed: SD SDI</p> <p>Button Released: 3G SDI</p>
SWITCH0(SW2.5)	<p>3G SDI Loopback direction control.</p> <p>1 (Down): CH0 TX / CH1 RX,</p>

	0 (Up) : CH0 RX / CH1 TX
SWITCH1(SW2.6)	Si5344 27Mhz Reference Clock Selection 1 (Down): From LMH1983 0 (Up): From FPGA
SWITCH2(SW2.7)	LMH1983 Mode Selection 1 (Down): Select Mode 0, AV-Sync Mode 0 (Up): Select Mode 3, Free-Run Mode

■ Project Source Code

The source code of Quartus project for the loopback demo with the A10SoC board is available in the “Demonstrations\A10SoC_12G_SDI” folder from the SDI-FMC System CD.

4.4 Demo on A10GFP FPGA Mainboard

This section shows how to setup the demo on the A10GFP Arria 10 FPGA Board.

■ Hardware Setup

Figure 4-9 shows the demo setup of SDI-FMC with A10GFP FPGA mainboard. The SDI-FMC should be installed on the FMC-A expansion header of A10GFP. Use one BNC to BNC 3G SDI Cable to connect BNC port J10 and the BNC port J13. Use one BNC to BNC 12G SDI Cable to connect the BNC port J11 and BNC port 15, and use another BNC to BNC 12G SDI Cable to connect the BNC port J14 and BNC port 8.

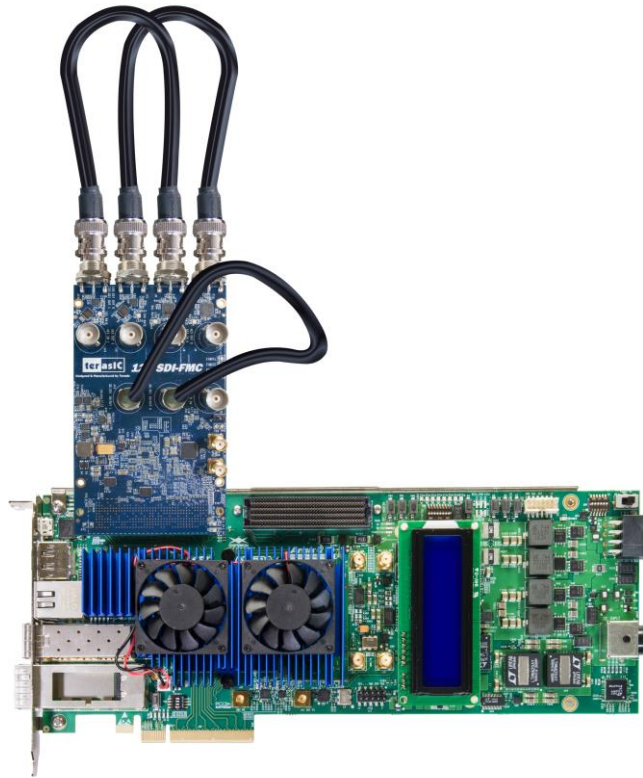


Figure 4-9 Hardware setup of SDI-FMC with A10GFP

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the A10GFP board.
2. Make sure the SDI-FMC is installed as shown in **Figure 4-9**.
3. Mount the SDI-FMC onto the FMC-A expansion header of the A10GFP board.
4. Connect the USB-Blaster USB port J3 of the A10GFP board to the USB port of the host PC with a Mini USB cable.
5. Power on the FPGA A10GFP board.
6. Make sure the Quartus Prime and the USB-Blaster II driver have been installed on the host PC.
7. Copy the folder Demonstrations/A10GFP_12G_SDI/demo_batch from the SDI-FMC System CD to the host PC and execute “test.bat”.
8. Observe LED0 and LED1 as shown in **Figure 4-11**. If two LEDs are lit, it means the two channel 12G SDI loopback test passed.
9. Set the SW2.1 dip switch to down as shown in **Figure 4-11** and observe LED2. If the LED is lit, it means the 3G SDI Loopback test passed. Then, set the SW2.1 dip switch to the up position, and observe the LED3 to check whether the 3G SDI loopback test passed in

another direction.

10. **Table 4-2** summarized the functional keys and details of each LED status.

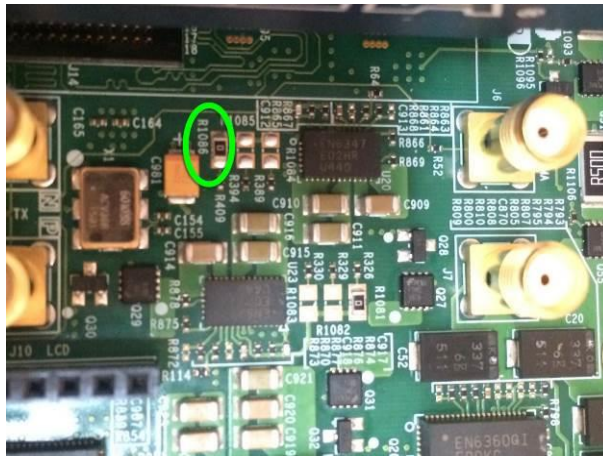


Figure 4-10 Make sure R1086 is installed (default for 1.8V)

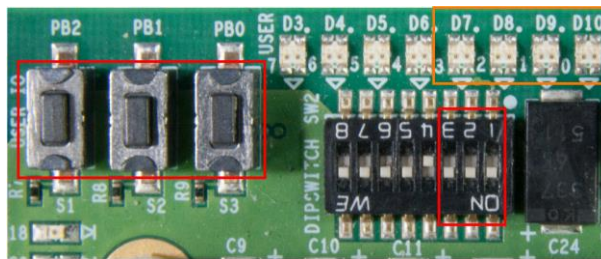


Figure 4-11 BUTTON/SWITCH/LED on A10GFP

Table 4-2 Functional keys of the A10GFP 12G-3G SDI RX/TX demonstration

Name	Description
LED0(D10)	Lighten when 12G Channel 0 receives a valid SDI pattern
LED1(D9)	Lighten when 12G Channel 1 receives a valid SDI pattern
LED2(D8)	Case 1 When SWITCH0(SW2.5) is 0 (Down Position):

	<p>Lighten when 3G Channel 0 receives a valid SDI pattern</p> <p>Case 2</p> <p>When SWITCH0(SW2.5) is 1 (Up Position):</p> <p>Lighten when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p>
LED3(D7)	<p>Case 1</p> <p>When SWITCH0(SW2.5) is 0 (Down Position):</p> <p>Lighten when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p> <p>Case 2</p> <p>When SWITCH0(SW2.5) is 1 (Up Position):</p> <p>Lighten when 3G Channel 1 receives a valid SDI pattern</p>
BUTTON0(PB0)	SYSTEM reset
BUTTON1(PB1)	<p>12G cable driver IC mute control</p> <p>Button Pressed: MUTE</p> <p>Button Released: UNMUTE</p>
BUTTON2(PB2)	<p>Video Standard Selection,</p> <p>For 12G-SDI Loopback Test</p> <p>Button Pressed: SD SDI</p>

	<p>Button Released: 12G SDI</p> <p>For 3G-SDI Loopback Test</p> <p>Button Pressed: SD SDI</p> <p>Button Released: 3G SDI</p>
SWITCH0(SW2.1)	<p>3G SDI Loopback direction control.</p> <p>1 (Up) : CH0 TX / CH1 RX,</p> <p>0 (Down): CH0 RX / CH1 TX</p>
SWITCH1(SW2.2)	<p>Si5344 27Mhz Reference Clock Selection</p> <p>1 (Up): From LMH1983</p> <p>0 (Down): From FPGA</p>
SWITCH2(SW2.3)	<p>LMH1983 Mode Selection</p> <p>1 (Up): Select Mode 0, AV-Sync Mode</p> <p>0 (Down): Select Mode 3, Free-Run Mode</p>

■ Project Source Code

The source code of Quartus project for the loopback demo with the A10GFP board is available in the “Demonstrations\A10GFP_12G_SDI” folder from the SDI-FMC System CD.

4.5 Demo on HAN Pilot Platform

This section will demonstrate connect the SDI-FMC daughter card to the HAN pilot platform and perform loopback test of 12G and 3G SDI image data. This demonstration has built-in 12G and 3G SDI pattern generator IP in the HAN pilot platform FPGA. It is used to output the color bar pattern through the TX port of the SDI FMC daughter card.

In this demonstration, use the BNC cables to connect the image data output by the TX port back to

the RX port of the SDI FMC card. Users can check whether the receiver IP receives the correct SDI pattern by observing the LED on the HAN pilot platform. In addition, users can also connect the 12G or 3G TX ports to the SDI to HDMI device and connect to the LCD monitor to display the color bar.

■ Hardware Setup

Figure 4-12 shows the setup of SDI-FMC with the HAN pilot platform. The SDI-FMC should be installed on the FMC expansion header of HAN pilot platform. Use an BNC to BNC 3G SDI Cable to connect BNC port J10 and the BNC port J13. Use an BNC to BNC 12G SDI Cable to connect the BNC port J11 and BNC port 15, and use another BNC to BNC 12G SDI Cable to connect the BNC port J14 and BNC port 8.

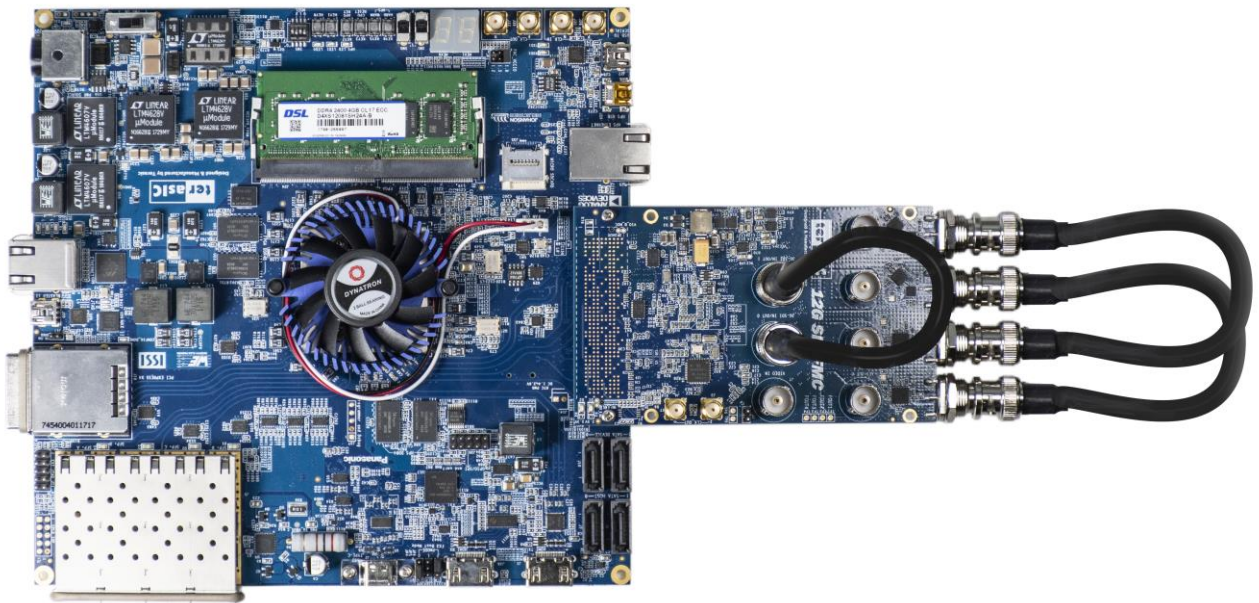


Figure 4-12 Hardware setup of SDI-FMC with HAN pilot platform

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the HAN pilot platform.
2. Make sure the SDI-FMC is installed on the HAN pilot platform as shown in **Figure 4-12**.
3. Set the VCCIO of the FMC connector to 1.8V by shorting J2.5 and J2.6 as shown in the **Figure 4-13**.
4. Connect the USB-Blaster USB port J20 of the HAN pilot platform to the USB port of the

- host PC with a Mini USB cable.
5. Power on the HAN pilot platform.
 6. Make sure the Quartus Prime and the USB-Blaster II driver has been installed on the host PC.
 7. Copy the folder Demonstrations/HAN_12G_SDI/demo_batch from the SDI-FMC System CD to the host PC and execute “test.bat”.
 8. Observe LED0 and LED1 as shown in **Figure 4-14**. If two LEDs light up, it means the two channels 12G SDI loopback test are pass.
 9. Set the SW0 switch to Down as shown in **Figure 4-14** and observe HEX0_DP (dot point). If the dot point lights up, it means the 3G SDI Loopback test is pass. Then, set the SW0 switch to the Up position, and observe the HEX1_DP to check whether the 3G SDI loopback test is pass in another direction.
 10. **Table 4-3** summarized the functional keys and details of each LED status.

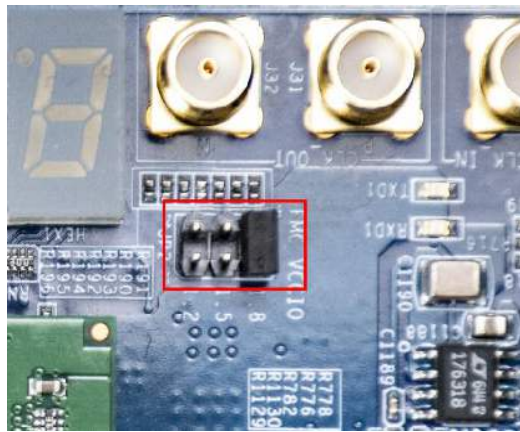


Figure 4-13 Make sure FMC_VCCIO(JP2) is set to 1.8V

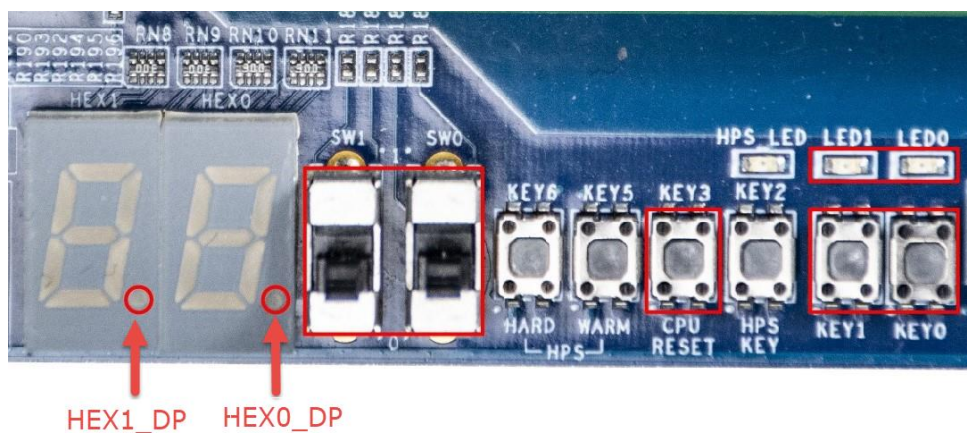


Figure 4-14 KEY/SW/LED on HAN

Table 4-3 Functional keys of the HAN 12G-3G SDI RX/TX demonstration

Name	Description
LED0	Lights up when 12G Channel 0 receives a valid SDI pattern
LED1	Lights up when 12G Channel 1 receives a valid SDI pattern
HEX0_DP	<p>Case 1</p> <p>When set SW0 to logic 0(Down Position):</p> <p>Lights up when 3G Channel 0 receives a valid SDI pattern</p> <p>Case 2</p> <p>When set SW0 to logic 1 (Up Position):</p> <p>Lights up when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p>
HEX1_DP	<p>Case 1</p> <p>When set SW0 to logic 0 (Down Position):</p> <p>Lighten when LMH1983 detects an expected video signal coming from the J7 Video-in BCN connector.</p> <p>Case 2</p> <p>When set SW0 to logic 1 (Up Position):</p> <p>Lighten when 3G Channel 1 receives a valid SDI pattern</p>

CPU_RESET_n	SYSTEM reset
KEY0	12G cable driver IC mute control Button Pressed: MUTE Button Released: UNMUTE
KEY1	Video Standard Selection, For 12G-SDI Loopback Test Button Pressed: SD SDI Button Released: 12G SDI For 3G-SDI Loopback Test Button Pressed: SD SDI Button Released: 3G SDI
SW0	3G SDI Loopback direction control. 1(Up) : CH0 TX / CH1 RX, 0 (Down): CH0 RX / CH1 TX
SW1	Si5344 27Mhz Reference Clock Selection 1 (Up): From LMH1983 0 (Down): From FPGA
Default 0	LMH1983 Mode Selection 1 : Select Mode 0, AV-Sync Mode 0 : Select Mode 3, Free-Run Mode

■ Project Source Code

The source code of this Quartus project for the loopback demo with the HAN board is available in the “Demonstrations\HAN_12G_SDI” folder from the SDI-FMC System CD.

4.6 Si5344 Configuration IP

The reference clock of SDI IP comes from the Si5344 clock generator chip on the SDI-FMC. Terasic provides a Si5344 configure IP for developers to configure Si5344 to generate the required reference clock. The IP can be used to configure Si5344 to generate the following clock setting:

- OUT0: 297.0 MHz clock which is connected to GBTCLK_M2C_P0
- OUT1: 22.5792 MHz clock which is connect co MUX DS250
- OUT2: 254 MHz clock which is connected to SMA connector
- OUT3: 297.0/1.001 MHz clock which is connect to GBTCLK_M2C_P1

The OUT0 and the OUT3 clock can be used as a reference clock of SDI IP. The IP also allow users to select the 27MHz clock source for Si5344 through the 1 pin interface **MODE**. When the MODE is set to low, the 27MHz comes from the LMH1938 chip is used. When the MOD E is set to lit, the 27MHz comes from FPGA mainboard is used. In this case, developers need to generate the required 27MHz clock. The IP is defined below.

```
`define SI5344_27M_FROM_LMH1983 1'd0
`define SI5344_27M_FROM_MAINBOARD 1'd1

module SI5344_CONFIG(
    //mode selection
    input MODE,    //

    //interface to si5344
    output I2C_SEL,
    output A0_CS_n,
    inout A1_SDO,
    inout I2C_SCL,
    inout I2C_SDA,

    output IN_SEL0,
    output IN_SEL1,

    input iCLK,
    input iRST_n,
    input iStart,
    output oCONFIG_DONE
);
```

4.7 LMH1983 Configuration IP

The LMH1983 is designed to generate a 27MHz clock for the Si5344. Terasic provides a LMH1983 configuration IP for developers to configure LMH1983 to generate the required reference clock. The IP can be used to configure LMH1983 to generate the following clock setting in our application:

- OUT0: 27.0 MHz clock which is connected to Si5344
- OUT1: 148.5 or 74.25 MHz clock which is connect co MUX DS250
- OUT2: 148.35 or 74.176 MHz clock which is connected to MUX DS250
- OUT3: 24.579 or 98.304 MHz clock which is connect to MUX DS250

The OUT0 clock can be used as a reference clock for the Si5344 clock generator. The LMH1983 Configuration IP provides 4 configuration modes for users to configure the LMH1983. **Figure 4-15**, **Figure 4-16**, **Figure 4-17** and **Figure 4-18** show the four configuration modes provided by the LMH1983 Configuration IP.

In MODE0, the FPGA would loopback the three H/V/F sync signals from LMH1981 to LMH1983. Users need to provide a video signal to the VIDEO-IN BNC connector J7 on the SDI-FMC board. For supported video formats, please refer to the datasheet of LMH1981.

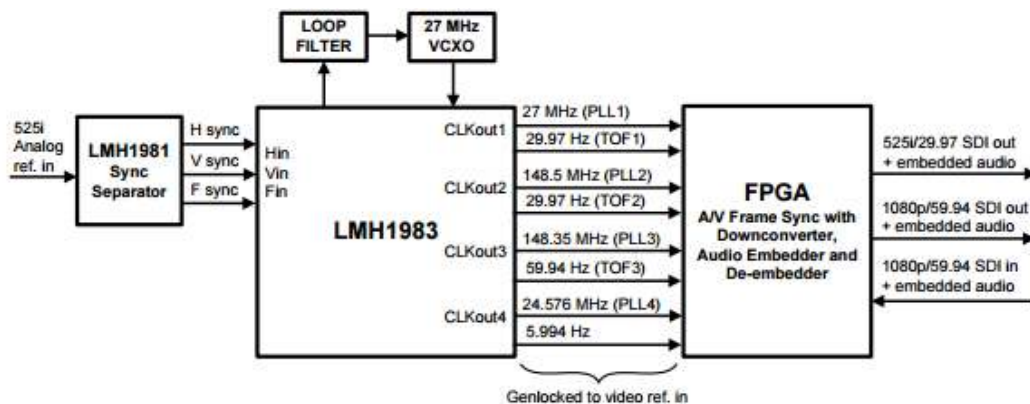


Figure 4-15 MODE0: Video Genlock Timing Generation for A/V Frame Synchronizer

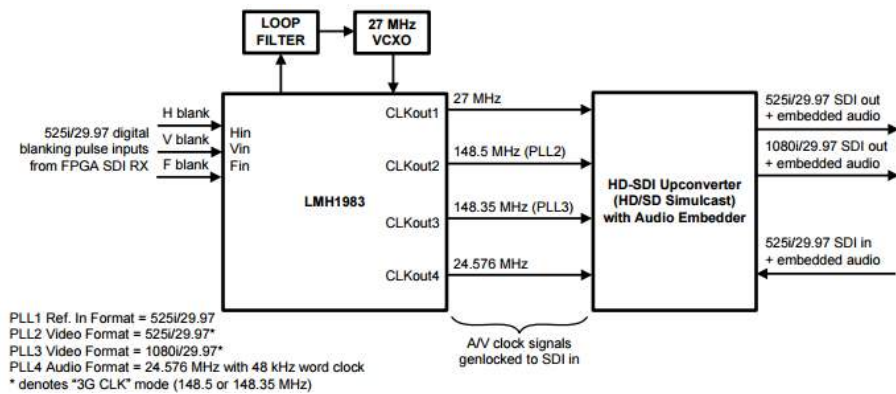


Figure 4-16 MODE1: Video Timing Generation for HD-SDI Up-Conversion

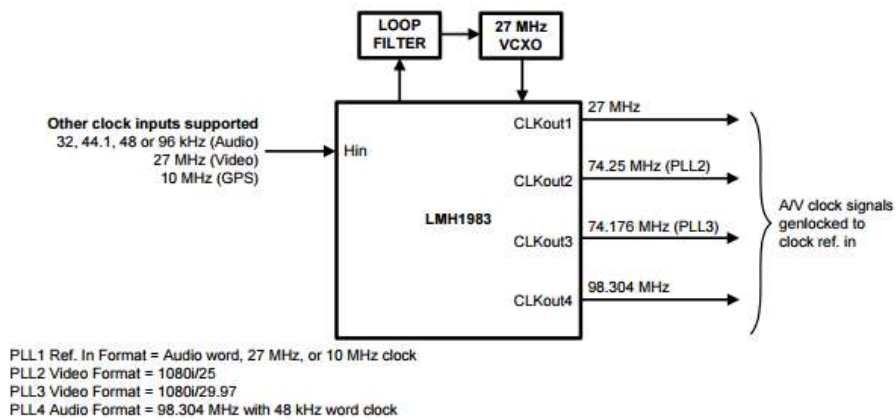


Figure 4-17 MODE2: A/V Clock Generation with Recognized Clock-Base Input Reference

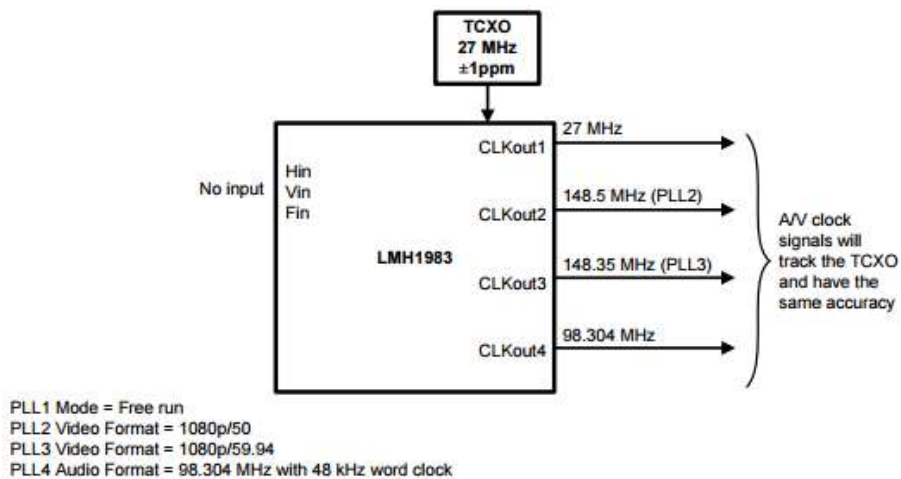


Figure 4-18 MODE3: A/V Clock Generation Using Free-Run

The IP named as LMH1983_CONFIG is defined below. In this demonstration, MODE0 and MODE3 are used.

```
`define LMH1983_AV          2'd0 // datasheet figure 22
`define LMH1983_SD_SDI     2'd1 // datasheet figure 23
`define LMH1983_NON_FORMAT 2'd2 // datasheet figure 28
`define LMH1983_FREE_RUN   2'd3 // datasheet figure 30

module LMH1983_CONFIG(
  //mode selection
  input [1:0] MODE,

  //interface to lmh1983
  inout      SDA,
  inout      SCL,

  input      iCLK,
  input      iRST_n,
  input      iStart,
  output     oCONFIG_DONE
);
```

5.1 Revision History

<i>Version</i>	<i>Date</i>	<i>Change Log</i>
V1.0	6/22, 2017	Initial Version (Preliminary)
V1.1	10/26, 2018	Add Note for section 2.2 and 3.5, modify Figure 2-5 and Figure 3-9
V1.2	04/11,2019	Add section 4.5 12G SDI demo for HAN Pilot Platform

5.2 Copyright Statement

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