PRELIMINARY

CYP15G0401RB

Quad HOTLink II™ Receiver

Features

- Quad receiver for 195 to 1500 MBaud serial signaling rate
  - Aggregate throughput of 6 GBits/second
- Second-generation HOTLink® technology
- Compliant to multiple standards
  - ESCON, DVB-ASI, Fibre Channel and Gigabit Ethernet (IEEE802.3z)
  - 8B/10B encoded or 10-bit unencoded data
- Selectable parity generate
- Selectable output clocking options
- MultiFrame™ Receive Framer
  - Bit and Byte alignment
  - Comma or full K28.5 detect
  - Single- or multi-byte framer for byte alignment
  - Low-latency option
- Synchronous LVTTL parallel interface
- Optional Elasticity Buffer in Receive Path
- Internal Clock/Data Recovery (CDR) PLLs with no external PLL components
- Dual differential PECL-compatible serial inputs per channel
  - Internal DC-restoration
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Per-channel Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
- Low power 2.1W @ 3.3V typical
- Single 3.3V supply
- 256-ball thermally enhanced BGA
- Pb free package available
- 0.25µ BiCMOS technology

Functional Description

The CYP15G0401RB Quad HOTLink II™ Receiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195-to-1500 MBaud per serial link.

Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an Output Register. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP15G0401TB and CYP15G0401RB parts.

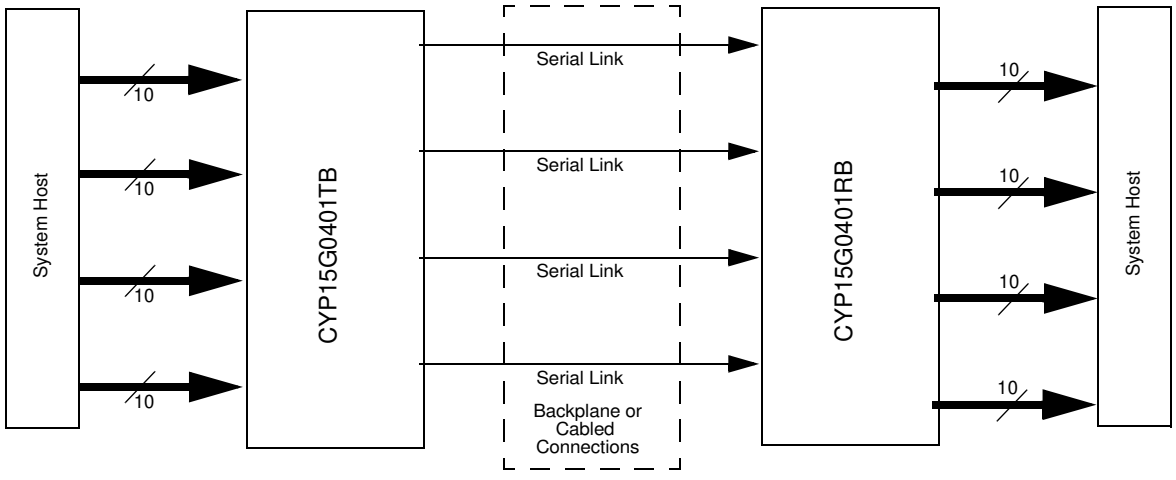


Figure 1. HOTLink II System Connections

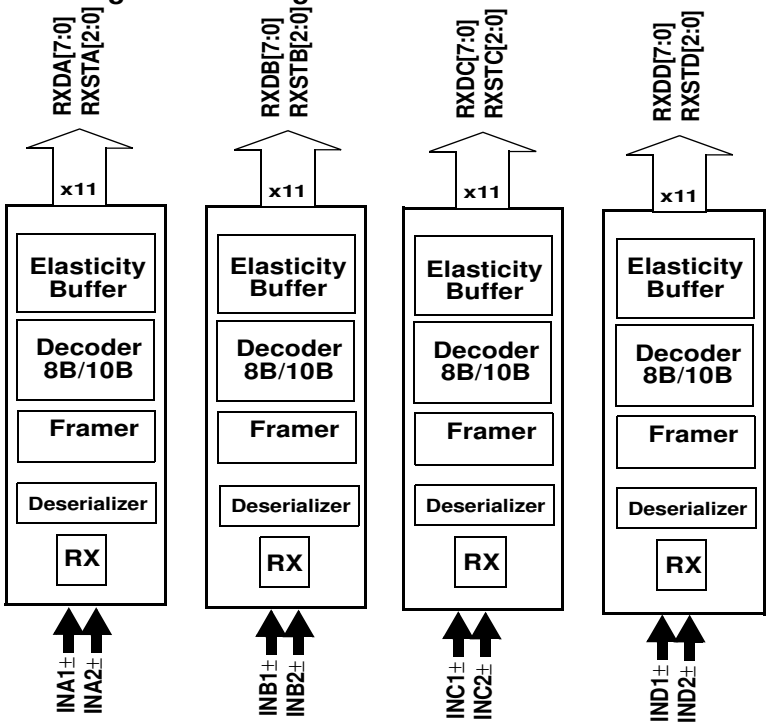
As a second-generation HOTLink device, the CYP15G0401RB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices. The receivers (RX) of the CYP15G0401RB Quad HOTLink II consist of four byte-wide channels. Each channel accepts a serial bit-stream from one of two PECL-compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered serial stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B Decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. The receive interface may be configured to present data relative to a recovered clock or to a local training clock.

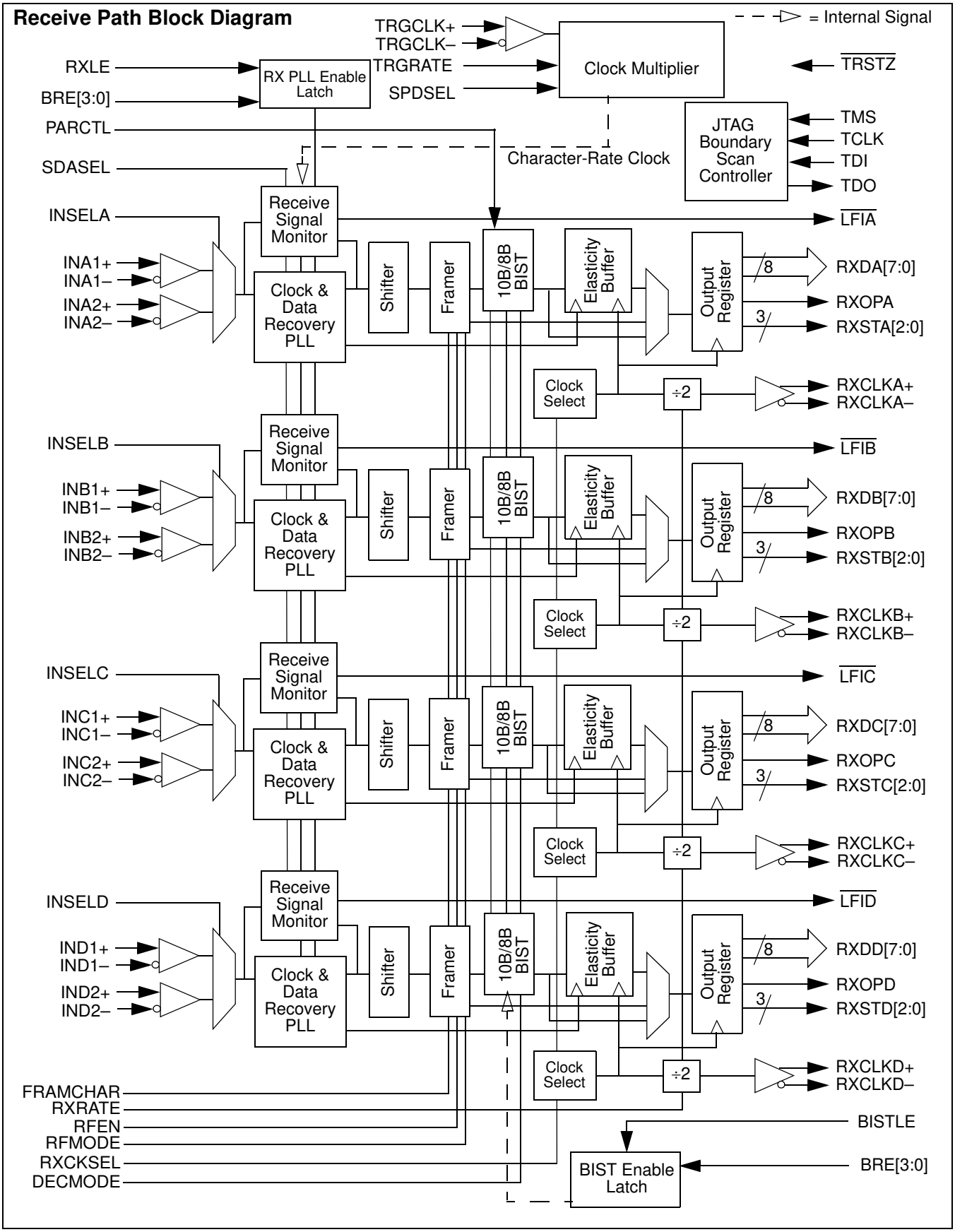
Each receive channel contains an independent BIST pattern checker. This BIST hardware allows at-speed testing of the high-speed serial data paths in each receive section, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, servers and video transmission systems.

CYP15G0401RB Receiver Logic Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC1-	N/C	INC2-	N/C	V_{CC}	IND1-	N/C	GND	IND2-	N/C	INA1-	N/C	GND	INA2-	N/C	V_{CC}	INB1-	N/C	INB2-	N/C
B	INC1+	N/C	INC2+	N/C	V_{CC}	IND1+	N/C	GND	IND2+	N/C	INA1+	N/C	GND	INA2+	N/C	V_{CC}	INB1+	N/C	INB2+	N/C
C	TDI	TMS	INSELC	INSELB	V_{CC}	PAR CTL	SDA SEL	GND	N/C	N/C	N/C	N/C	GND	N/C	GND	V_{CC}	TRG RATE	RX RATE	GND	TDO
D	TCLK	$\overline{TRSTZ}$	INSELD	INSELA	V_{CC}	RF MODE	SPD SEL	GND	BRE[3]	BRE[2]	BRE[1]	BRE[0]	GND	N/C	GND	V_{CC}	V_{CC}	RXLE	RFEN	N/C
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	N/C	V_{CC}	V_{CC}	RXCK SEL													BISTLE	RXSTB [1]	RXOPB	RXSTB [0]
G	GND	GND	GND	GND													DEC MODE	GND	FRAM CHAR	RXDB [1]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	GND	GND	GND	GND													RXSTB [2]	RXDB [0]	RXDB [5]	RXDB [2]
K	RXDC [2]	RXCLK C–	GND	$\overline{LFIC}$													RXDB [3]	RXDB [4]	RXDB [7]	RXCLK B+
L	RXDC [3]	RXCLK C+	GND	GND													RXDB [6]	$\overline{LFIB}$	RXCLK B–	GND
M	RXDC [4]	RXDC [5]	RXDC [7]	RXDC [6]													GND	GND	GND	GND
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RXDC [1]	RXDC [0]	RXSTC [0]	RXSTC [1]													GND	GND	GND	GND
R	RXSTC [2]	RXOP C	N/C	V_{CC}													V_{CC}	V_{CC}	V_{CC}	N/C
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	RXDD [2]	RXDD [1]	GND	RX OPD	N/C	TRG CLK-	GND	GND	GND	V_{CC}	V_{CC}	RXDA [2]	RXOPA	RXSTA [2]	RXSTA [1]
V	V_{CC}	V_{CC}	V_{CC}	RXDD [6]	V_{CC}	RXDD [3]	RXSTD [0]	GND	RXSTD [2]	N/C	TRG CLK+	N/C	GND	GND	V_{CC}	V_{CC}	RXDA [7]	RXDA [3]	RXDA [0]	RXSTA [0]
W	V_{CC}	V_{CC}	$\overline{LFID}$	RXCLK D–	V_{CC}	RXDD [4]	RXSTD [1]	GND	N/C	GND	GND	GND	GND	GND	V_{CC}	V_{CC}	$\overline{LFIA}$	RXCLK A-	RXDA [4]	RXDA [1]
Y	V_{CC}	V_{CC}	RXDD [7]	RXCLK D+	V_{CC}	RXDD [5]	RXDD [0]	GND	N/C	N/C	GND	N/C	GND	GND	V_{CC}	V_{CC}	V_{CC}	RXCLK A+	RXDA [6]	RXDA[5]

Note:
1. N/C = Do Not Connect

Pin Configuration (Bottom View)[1]

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
N/C	INB2-	N/C	INB1-	V_{CC}	N/C	INA2-	GND	N/C	INA1-	N/C	IND2-	GND	N/C	IND1-	V_{CC}	N/C	INC2-	N/C	INC1-	A
N/C	INB2+	N/C	INB1+	V_{CC}	N/C	INA2+	GND	N/C	INA1+	N/C	IND2+	GND	N/C	IND1+	V_{CC}	N/C	INC2+	N/C	INC1+	B
TDO	GND	RX RATE	TRG RATE	V_{CC}	GND	N/C	GND	N/C	N/C	N/C	N/C	GND	SDA SEL	PAR CTL	V_{CC}	INSELB	INSELC	TMS	TDI	C
N/C	RFEN	RXLE	V_{CC}	V_{CC}	GND	N/C	GND	BRE[0]	BRE[1]	BRE[2]	BRE[3]	GND	SPD SEL	RF MODE	V_{CC}	INSELA	INSELD	$\overline{\text{TRSTZ}}$	TCLK	D
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	E
RXSTB [0]	RXOP B	RXSTB [1]	BISTLE													RXCK SEL	V_{CC}	V_{CC}	N/C	F
RXDB [1]	FRAM CHAR	GND	DEC MODE													GND	GND	GND	GND	G
GND	GND	GND	GND													GND	GND	GND	GND	H
RXDB [2]	RXDB [5]	RXDB [0]	RXSTB [2]													GND	GND	GND	GND	J
RXCLK B+	RXDB [7]	RXDB [4]	RXDB [3]													$\overline{\text{LFIC}}$	GND	RXCLK C-	RXDC [2]	K
GND	RXCLK B-	$\overline{\text{LFIB}}$	RXDB [6]													GND	GND	RXCLK C+	RXDC [3]	L
GND	GND	GND	GND													RXDC [6]	RXDC [7]	RXDC [5]	RXDC [4]	M
GND	GND	GND	GND													GND	GND	GND	GND	N
GND	GND	GND	GND													RXSTC [1]	RXSTC [0]	RXDC [0]	RXDC [1]	P
N/C	V_{CC}	V_{CC}	V_{CC}													V_{CC}	N/C	RXOP C	RXSTC [2]	R
V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}	T
RXSTA [1]	RXSTA [2]	RXOPA	RXDA [2]	V_{CC}	V_{CC}	GND	GND	GND	TRG CLK-	N/C	RXOP D	GND	RXDD [1]	RXDD [2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	U
RXSTA [0]	RXDA [0]	RXDA [3]	RXDA [7]	V_{CC}	V_{CC}	GND	GND	N/C	TRG CLK+	N/C	RXSTD [2]	GND	RXSTD [0]	RXDD [3]	V_{CC}	RXDD [6]	V_{CC}	V_{CC}	V_{CC}	V
RXDA [1]	RXDA [4]	RXCLK A-	$\overline{\text{LFIA}}$	V_{CC}	V_{CC}	GND	GND	GND	GND	GND	N/C	GND	RXSTD [1]	RXDD [4]	V_{CC}	RXCLK D–	$\overline{\text{LFID}}$	V_{CC}	V_{CC}	W
RXDA [5]	RXDA [6]	RXCLK A+	V_{CC}	V_{CC}	V_{CC}	GND	GND	N/C	GND	N/C	N/C	GND	RXDD [0]	RXDD [5]	V_{CC}	RXCLK D+	RXDD [7]	V_{CC}	V_{CC}	Y

Pin Descriptions

CYP15G0401RB Quad HOTLink II Receiver

Pin Name	I/O Characteristics	Signal Description
Receive Path Data Signals		
RXDA[7:0] RXDB[7:0] RXDC[7:0] RXDD[7:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output (or TRGCLK↑ input[2] when RXCKSEL = LOW)	**Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is enabled (DECMODE = HIGH or MID), these outputs represent either received data or special characters. The status of the received data is represented by the values of RXSTx[2:0]. When the Decoder is bypassed (DECMODE = LOW), RXDx[7:0] become the higher order bits of the 10-bit received character. See *Table 7* for details.
RXSTA[2:0] RXSTB[2:0] RXSTC[2:0] RXSTD[2:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output (or TRGCLK↑ input[2] when RXCKSEL = LOW)	**Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is bypassed (DECMODE = LOW), RXSTx[1:0] become the two low-order bits of the 10-bit received character, while RXSTx[2] = HIGH indicates the presence of a Comma character in the Output Register. See *Table 7* for details. When the Decoder is enabled (DECMODE = HIGH or MID), RXSTx[2:0] provide status of the received signal. See *Table 9* and *Table 10* for a list of Receive Character status.
RXOPA RXOPB RXOPC RXOPD	Three-state, LVTTL Output, synchronous to the selected RXCLKx↑ output (or TRGCLK↑ input[2] when RXCKSEL = LOW)	**Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z).
Receive Path Clock and Clock Control		
RXRATE	LVTTL Input, static control input, internal pull-down	**Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When TRGCLK± is selected to clock the output registers (RXCKSELx = LOW), RXRATEx is not interpreted. The RXCLKA± and RXCLKC± output clocks will follow the frequency and duty cycle of TRGCLK±.
TRGRATE	LVTTL Input, static control input, internal pull-down	**Training Clock Rate Select**. When TRGCLK is selected to clock the receive parallel interfaces (RXCKSEL = LOW), the TRGRATE input also determines if the clocks on the RXCLKA± and RXCLKC± outputs are full or half-rate. When TRGRATE = HIGH (TRGCLK is half-rate) and RXCKSEL = LOW, the RXCLKA± and RXCLKC± output clocks are also half-rate clocks and follow the frequency and duty cycle of the TRGCLK input. When TRGRATE = LOW (TRGCLK is full-rate) and RXCKSEL = LOW, the RXCLKA± and RXCLKC± output clocks are full-rate clocks and follow the frequency and duty cycle of the TRGCLK input.
FRAMCHAR	Three-level Select [3], static control input	**Framing Character Select**. Used to select the character or portion of a character used for character framing of the received data streams. When MID, the Framer looks for both positive and negative disparity versions of the eight-bit Comma character. When HIGH, the Framer looks for both positive and negative disparity versions of the K28.5 character. Configuring FRAMCHAR to LOW is reserved for component test.
RFEN	LVTTL Input, asynchronous, internal pull-down	**Reframe Enable for All Channels**. Active HIGH. When HIGH, the framers in all four channels are enabled to frame per the presently enabled framing mode as selected by RFMODE and selected framing character as selected by FRAMCHAR.

Notes:
2. When TRGCLK is configured for half-rate operation (TRGRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of TRGCLK.
3. Three-level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a Three-level select input will self-bias to the MID level.

Pin Descriptions (continued)

CYP15G0401RB Quad HOTLink II Receiver

Pin Name	I/O Characteristics	Signal Description
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	Three-state, LVTTL Output clock or static control input	**Receive Character Clock Output or Clock Select Input**. When configured such that all output data paths are clocked by the recovered clock (RXCKSEL = MID), these true and complement clocks are the receive interface clocks which are used to control timing of output data (RXDx[7:0], RXSTx[2:0] and RXOPx). These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE. When configured such that all output data paths are clocked by TRGCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLKA± and RXCLKC± output drivers present a buffered and delayed form of TRGCLK. RXCLKA± and RXCLKC± are buffered forms of TRGCLK that are slightly different in phase. This phase difference allows the user to select the optimal setup/hold timing for their specific interface.
RXCKSEL	Three-level Select [3], static control input	**Receive Clock Mode**. Selects the receive clock source used to transfer data to the Output Registers. When LOW, all four Output Registers are clocked by TRGCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present buffered and delayed forms of TRGCLK. When MID, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE. When the 10B/8B Decoder and Elasticity Buffer are bypassed (DECMODE = LOW), RXCKSEL must be MID. When HIGH and the receive channels are operated in independent mode (RX modes 0 and 2), RXCLKA± and RXCLKC± output the recovered clock from receive channel A, B, C, or D, as selected by RXCLKB+ and RXCLKD+. This output clock may operate at the character-rate or half the character-rate as selected by RXRATE.
DECMODE	Three-level Select [3], static control input	**Decoder Mode Select**. This input selects the behavior of the Decoder block. When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When the Decoder is bypassed, RXCKSEL must be MID. When MID, the Decoder is enabled and the Cypress decoder table for Special Code characters is used. When HIGH, the Decoder is enabled and the alternate decoder table for Special Code characters is used. See *Table 15* for a list of the Special Codes supported in both encoded modes.
RFMODE	Three-level Select [3], static control input	**Reframe Mode Select**. Used to select the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the received serial bit stream). This signal operates with the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered character-rate clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode Multi-Byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phase regardless of character offset. When HIGH, the alternate mode Multi-Byte parallel Framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received serial bit stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phase regardless of character offset.

Pin Descriptions (continued)

CYP15G0401RB Quad HOTLink II Receiver

Pin Name	I/O Characteristics	Signal Description
Device Control Signals		
PARCTL	Three-level Select [3], static control input	**Parity Generate Control**. Used to control the different parity generate functions. When LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z). When MID, and the 10B/8B Decoder is enabled (DECMODE ≠ LOW), ODD parity is generated for the RXDx[7:0] outputs and presented on RXOPx. When the Decoder is disabled (DECMODE = LOW), ODD parity is generated for the RXDx[7:0] and RXSTx[1:0] outputs and presented on RXOPx. When HIGH, parity generation is enabled. ODD parity is generated for the RXDx[7:0] and RXSTx[2:0] outputs and presented on RXOPx. See *Table 8* for details.
SPDSEL	Three-level Select [3] static control input	**Serial Rate Select**. This input specifies the operating bit-rate range of the receive PLLs. LOW = 195–400 MBd, MID = 400–800 MBd, HIGH = 800–1500 MBd. When SPDSEL is LOW, setting TRGRATE = HIGH (Half-rate Training Clock) is invalid.
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of TRGCLK↑, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by TRGCLK↑), the status and data outputs will become deterministic in less than 16 TRGCLK cycles. The BISTLE and RXLE latches are reset by TRSTZ. If the Elasticity Buffer is used, TRSTZ should be applied after power up to initialize the internal pointers into these memory arrays.
TRGCLK±	Differential LVPECL or single-ended LVTTL Input Clock	**Training Clock**. This clock is used as the centering frequency of the Range Controller block of the Receive CDR PLLs, via the Clock Multiplier. This input clock may also be selected to clock the receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement TRGCLK input, and leave the alternate TRGCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When RXCKSEL = LOW, the Elasticity Buffer is enabled and TRGCLK is used as the clock for the parallel receive data (output) interface. If the Elasticity Buffer is used, framing characters will be inserted or deleted to/from the data stream to compensate for frequency differences between the training clock and recovered clock. When an addition happens, a K28.5 will be appended immediately after a framing character is detected in the Elasticity Buffer. When deletion happens, a framing character will be removed from the data stream when detected in the Elasticity Buffer.
Analog I/O and Control		
INA1± INB1± INC1± IND1±	LVPECL Differential Input	**Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx1± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = HIGH.
INA2± INB2± INC2± IND2±	LVPECL Differential Input	**Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx2± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = LOW.
INSELA INSELB INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. Determines which external serial bit stream is passed to the receiver Clock and Data Recovery circuit. When HIGH, the INx1± input is selected. When LOW, the INx2± input is selected.
SDASEL	Three-level Select [3] static configuration input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 1*.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BRE[3:0] inputs directly control the receive BIST enables. When the BRE[x] input is LOW, the associated receive channel is configured to compare the BIST sequence. When the BRE[x] input is HIGH, the associated receive channel is configured for normal data reception. The specific mapping of BRE[3:0] signals to receive BIST enables is listed in *Table 2*. When BISTLE returns LOW, the last values present on BRE[3:0] are captured in the internal BIST Enable Latch. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all receive channels.

Pin Descriptions (continued)

CYP15G0401RB Quad HOTLink II Receiver

Pin Name	I/O Characteristics	Signal Description
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-control Latch Enable**. Active HIGH. When RXLE = HIGH, the signals on the BRE[3:0] inputs directly control the power enables for the receive PLLs and analog circuitry. When the BRE[3:0] input is HIGH, the associated receive channel A through D PLL and analog circuitry are active. When the BRE[3:0] input is LOW, the associated receive channel A through D PLL and analog circuitry are powered down. The specific mapping of BRE[3:0] signals to the associated receive channel enables is listed in *Table 2*. When RXLE returns LOW, the last values present on BRE[3:0] are captured in the internal RX PLL Enable Latch. When the device is reset ($\overline{TRSTZ}$ = LOW), the latch is reset to disable all receive channels.
BRE[3:0]	LVTTL Input, asynchronous, internal pull-up	**BIST and Receive Channel Enables**. These inputs are passed to and through the BIST Enable Latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel Enable Latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
$\overline{LFIA}$ $\overline{LFIB}$ $\overline{LFIC}$ $\overline{LFID}$	LVTTL Output, Asynchronous	**Link Fault Indication Output**. Active LOW. $\overline{LFIx}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	Three-state LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		**+3.3V Power**
GND		**Signal and power ground for all internal circuits**.

CYP15G0401RB HOTLink II Operation

The CYP15G0401RB is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to one destination. This device supports four single-byte or single-character channels.

CYP15G0401RB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude above limit specified by SDASEL
- transition density greater than specified limit
- range controller reports the received data stream within normal frequency range (±1500 ppm)[4]
- receive channel enabled

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the $\overline{LFIx}$ (Link Fault Indicator) output associated with each receive channel.

Table 1. Analog Amplitude Detect Valid Signal Levels[5]

SDASEL	Typical signal with peak amplitudes above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable. This allows operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a three-level select[3] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 1*. This control input affects the analog monitors for all receive channels.

The Analog Signal Detect Monitors are active for the Line Receiver selected by the associated INSELx input.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received on a channel, the Transition Detection logic for that channel will assert LFIx. The LFIx output remains asserted until at least one transition is detected in each of three adjacent received characters.

Range Controls

The Clock/Data Recovery (CDR) circuit includes logic to monitor the frequency of the Phase Locked Loop (PLL) Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been “missing”
- when the incoming data stream is outside the acceptable frequency range

To perform this function, the frequency of the VCO is periodically sampled and compared to the frequency of the TRGCLK input. If the VCO is running at a frequency beyond ±1500 ppm[4] as defined by the training clock frequency, it is periodically forced to the correct frequency (as defined by TRGCLK, SPDSEL, and TRGRATE) and then released in an attempt to lock to the input data stream. The sampling and relock period of the Range Control is calculated as follows: RANGE CONTROL SAMPLING PERIOD = (TRGCLK-PERIOD) * (16000).

During the time that the Range Control forces the PLL VCO to run at TRGCLK*10 (or TRGCLK*20 when TRGRATE = HIGH) rate, the LFIx output will be asserted LOW. While the PLL is attempting to re-lock to the incoming data stream, LFIx may be either HIGH or LOW (depending on other factors such as transition density and amplitude detection) and the recovered byte clock (RXCLKx) may run at an incorrect rate (depending on the quality or existence of the input serial data stream). After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Receive Channel Enabled

The CYP15G0401RB contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BRE[3:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BRE[3:0] inputs are passed through the Receive Channel Enable Latch to control the PLLs and logic of the associated receive channel. The BRE[3:0] input associated with a specific receive channel is listed in *Table 2*.

Table 2. BIST and Receive Channel Enable Signal Map

BRE Input	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BRE[3]	Receive D	Receive D
BRE[2]	Receive C	Receive C
BRE[1]	Receive B	Receive B
BRE[0]	Receive A	Receive A

When RXLE is HIGH and BRE[x] is HIGH, the associated receive channel is enabled to receive and recover a serial stream. When RXLE is HIGH and BRE[x] is LOW, the associated receive channel is disabled and powered down. Any disabled channel indicates an asserted LFIx output. When RXLE returns LOW, the values present on the BRE[3:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to open the latch again.[6]

Clock Multiplier

The Clock Multiplier accepts a character-rate or half-character-rate external clock at the TRGCLK input, to generate a character-rate clock for use by the Clock/Data Recovery (CDR) blocks.

This clock multiplier can accept a TRGCLK input between 20 MHz and 150 MHz (providing the user with the option to use a TRGCLK frequency at 1/10 or 1/20 the serial bit rate), however, this clock range is limited by the operating mode of the CYP15G0401RB clock multiplier (controlled by TRGRATE) and by the level on the SPDSEL input.

SPDSEL is a static three-level select [3] (ternary) input that selects one of three operating ranges for the serial data inputs. The operating serial signaling-rate and allowable range of TRGCLK frequencies are listed in *Table 3*.

Notes:

4. TRGCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLK must be within ±1500 ppm (±0.15%) of the remote transmitter’s PLL reference (REFCLK) frequency. Although transmitting to a HOTLink II receiver necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-ppm, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard. For example, to be IEEE 802.3z Gigabit Ethernet compliant, the frequency stability of the crystal needs to be within ±100 ppm.
5. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sine-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.
6. When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Table 3. Operating Speed Settings

SPDSEL	TRGRATE	TRGCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The TRGCLK± input is a differential input with each input internally biased to 1.4V. If the TRGCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, TRGCLK– can be left floating and the input signal is recognized when it passes through the internally biased reference point.

When both the TRGCLK+ and TRGCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the TRGCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the TRGCLK+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each receive channel. The clock extraction function is performed by embedded phase-locked loops (PLLs) that track the frequency of the transitions in the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) training clock from the TRGCLK input. This TRGCLK input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency.
- to reduce PLL acquisition time
- and to limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits of the range control monitor, the CDR will switch to track TRGCLK instead of the data stream. Once the CDR output (RXCLKx) frequency returns back close to TRGCLK frequency, the CDR input will be switched back to track the input data stream. In case no data is present at the input this switching behavior may result in brief RXCLKx frequency excursions from TRGCLK. However, the validity of the input data stream is indicated by the LFIx output. The frequency of TRGCLK is required to be within ±1500 ppm[4] of the frequency of the clock that drives the TRGCLK input of the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± inputs through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream and frame to the incoming character boundaries.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream, looking for one or more Comma or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP15G0401RB allows selection of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in *Table 4*. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Table 4. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
LOW	Reserved for test	
MID (Open)	Comma+ or Comma–	00111110XX [7] or 11000001XX
HIGH	–K28.5 or +K28.5	0011111010 or 1100000101

Framer

The Framer on each channel operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the framers in all four receive paths are disabled, and no combination of bits in a received data stream will alter the character boundaries. When RFEN = HIGH, the Framer selected by RFMODE is enabled on all four channels.

When RFMODE = LOW, the Low-Latency Framer is selected[8]. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode, the Framer starts its alignment process on the first detection of the selected framing

Notes:
7. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the eighth bit as an inversion of the seventh bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.
8. When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which would cause the Receiver to update its character boundaries incorrectly.

character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to fourteen character-clock cycles from the detection of the selected framing character.

When RFMODE = MID (open), the Cypress-mode Multi-Byte Framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased framing characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE = HIGH, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing for all channels is enabled when RFEN = HIGH. If RFEN = LOW, the Framer for each channel is disabled. When the framers are disabled, no changes are made to the recovered character boundaries on any channel, regardless of the presence of framing characters in the data stream.

10B/8B Decoder Block

The Decoder logic block performs three primary functions:

- decoding the received transmission characters back into Data and Special Character codes
- comparing generated BIST patterns with received characters to permit at-speed link and device testing
- generation of ODD parity on the decoded characters.

10B/8B Decoder

The framed parallel output of each Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the 10B/8B Decoder patterns in *Table 14* and *Table 15* of this data sheet. Valid data characters are indicated by a 000b bit-combination on the associated RXSTx[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 10B/8B Decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. In this mode the Receive Elasticity Buffers are bypassed, and RXCKSEL must be MID. This clock mode generates separate RXCLKx± outputs for each receive channel.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using *Table 14* and *Table 15*. Received Special Code characters are decoded using the Cypress column of *Table 15*.

When DECMODE = HIGH, the 10-bit transmission characters are decoded using *Table 14* and *Table 15*. Received Special Code characters are decoded using the Alternate column of *Table 15*.

Receive BIST Operation

The Receiver interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BRE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s), the CYP15G0401TB for example. If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass must be preceded by a 16-character Word Sync Sequence. Please note that BIST cannot be used in a common clock configuration (RXCKSEL ≠ MID) when using the CYP15G0401TB device as the BIST generator, as the 16-character Word Sync Sequence will not be present in the BIST pattern. When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the Output Register. See *Table 10* for details.

When the BISTLE signal is HIGH, any BRE[x] input that is LOW enables the BIST generator/checker in the associated Receive channel. When BISTLE returns LOW, the values of all BRE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This D0.0 character is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXSTx[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values

are presented when the Decoder is bypassed and BIST is enabled on a receive channel.

The status reported on RXSTx[2:0] by the BIST state machine are listed in *Table 10*. When Receive BIST is enabled, the same status is reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP15G0401RB when RXCKSEL = MID is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by sixteen, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for common clock operation (RXCKSEL ≠ MID), each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations (see CYP15G0401TB datasheet for details on how to send a 16-character Word Sync Sequence from the remote transmitter).

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low Latency Framer is enabled (RFMODE = LOW), the Framer will misalign to an aliased framing character within the BIST sequence. If the Alternate Multi-Byte Framer is enabled (RFMODE = HIGH) and the Receiver outputs are clocked relative to a recovered clock, it is necessary to frame the Receiver before BIST is enabled.

Receive Elasticity Buffer

Each receive channel contains an Elasticity Buffer that is designed to support multiple clocking modes. These buffers allow data to be read using an Elasticity Buffer read-clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to use a read clock that is frequency coherent but with uncontrolled phase relative to the Elasticity Buffer write clock.

Each Elasticity Buffer is 10-characters deep, and supports a twelve-bit wide data path. It is capable of supporting a decoded character, three status bits, and a parity bit for each character present in the buffer. The write clock for these buffers is always the recovered clock for the associated read channel.

The read clock for the Elasticity Buffers may come from one of three selectable sources. It may be a

- character-rate TRGCLK (RXCKSEL = LOW and DECMODE ≠ LOW)
- recovered clock from an alternate receive channel (RXCKSEL = HIGH and DECMODE ≠ LOW).

The Elasticity Buffers are bypassed whenever the Decoders are bypassed (DECMODE = LOW). When the Decoders and Elasticity Buffers are bypassed, RXCKSELx must be set to MID.

Receive Normal Data Operation

When RXCKSEL = LOW, all four receive channels are clocked by TRGCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and the RXCLKA± and RXCLKC± outputs present a buffered and delayed form of TRGCLK. In this mode, the Receive Elasticity Buffers are enabled. For TRGCLK clocking, the Elasticity Buffers must be able to insert K28.5 characters and delete framing characters as appropriate.

The insertion of a K28.5 or deletion of a framing character can occur at any time on any channel, however, the actual timing on these insertions and deletions is controlled in part by the how the attached remote transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the Elasticity Buffer. Likewise, to delete a framing character, one must also be present in the Elasticity Buffer. To prevent a receive buffer overflow or underflow on a receive channel, a minimum density of framing characters must be present in the received data streams.

When RXCKSEL = MID (or open), each received channel Output Register is clocked by the recovered clock for that channel. Since no characters may be added or deleted, the receiver Elasticity Buffer is bypassed.

When RXCKSEL = HIGH in independent channel mode, all channels are clocked by the selected recovered clock. This selection is made using the RXCLKB+ and RXCLKD+ signals as inputs per *Table 5*. This selected clock is always output on RXCLKA± and RXCLKC±. In this mode the Receive Elasticity Buffers are enabled. When data is output using a recovered clock (RXCKSEL = HIGH), the receive channels are not allowed to insert and delete characters, except as necessary for Elasticity Buffer alignment.

When the Elasticity Buffer is used, prior to reception of valid data, a Word Sync Sequence (or at least four framing characters) must be received to center the Elasticity Buffers. The Elasticity Buffer may also be centered by a device reset operation initiated by $\overline{\text{TRSTZ}}$ input. However, following such an event, the CYP15G0401RB also requires a framing event before it will correctly decode characters. When RXCKSEL = HIGH, since the Elasticity Buffer is not allowed to insert or delete framing characters, the transmit clocks on all received channels must all be from a common source.

Table 5. Independent Recovered Clock Select

RXCLKB+	RXCLKD+	RXCLKA±/RXCLKC± Clock Source
0	0	RXCLKA
0	1	RXCLKB
1	0	RXCLKC
1	1	RXCLKD

Power Control

The CYP15G0401RB supports user control of the powered up or down state of each receive channel. The receive channels are controlled by the RXLE signal and the values present on the BRE[3:0] bus. Powering down unused channels will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Receive Channels

When RXLE is HIGH, the signals on the BRE[3:0] inputs directly control the power enables for the receive PLLs and analog circuits. When a BRE[3:0] input is HIGH, the associated receive channel [A through D] PLL and analog logic are active. When a BRE[3:0] input is LOW, the

associated receive channel [A through D] PLL and analog circuits are powered down. When RXLE returns LOW, the last values present on the BRE[3:0] inputs are captured in the Receive Channel Enable Latch. The specific BRE[3:0] input signal associated with a receive channel is listed in *Table 2*.

Any disabled receive channel will indicate a constant $\overline{\text{LFIx}}$ output. When a disabled receive channel is re-enabled, the status of the associated $\overline{\text{LFIx}}$ output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Device Reset State

When the CYP15G0401RB is reset by assertion of $\overline{\text{TRSTZ}}$, the Receive Enable Latches are both cleared, and the BIST Enable Latch is preset. In this state, all receive channels are disabled, and BIST is disabled on all channels.

Following a device reset, it is necessary to enable the receive channels used for normal operation. This can be done by sequencing the appropriate values on the BRE[3:0] inputs while the RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the device to power up in a fixed configuration, it is also possible to strap the RXLE control signal HIGH to permanently enable its associated latches. Connection of the associated BRE[3:0] signals to a stable HIGH will then enable the respective receive channels as soon as the $\overline{\text{TRSTZ}}$ signal is deasserted.

Output Bus

Each receive channel presents a 12-signal output bus consisting of

- an eight-bit data bus
- a three-bit status bus
- a parity bit.

The bit assignments of the Data and Status are dependent on the setting of DECMODE. The bits are assigned as per *Table 6*.

Table 6. Output Register Bit Assignments [9]

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXSTx[2] (LSB)	COMDETx	RXSTx[2]
RXSTx[1]	DOUTx[0]	RXSTx[1]
RXSTx[0]	DOUTx[1]	RXSTx[0]
RXDx[0]	DOUTx[2]	RXDx[0]
RXDx[1]	DOUTx[3]	RXDx[1]
RXDx[2]	DOUTx[4]	RXDx[2]
RXDx[3]	DOUTx[5]	RXDx[3]
RXDx[4]	DOUTx[6]	RXDx[4]
RXDx[5]	DOUTx[7]	RXDx[5]
RXDx[6]	DOUTx[8]	RXDx[6]
RXDx[7] (MSB)	DOUTx[9]	RXDx[7]

When the 10B/8B Decoder is bypassed (DECMODE = LOW), the framed 10-bit character and a single status bit (COMDET) are presented at the receiver Output Register. The status output indicates if the character in the Output Register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in *Table 7*.

The COMDETx outputs are HIGH when the character in the Output Register for the associated channel contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the Low-Latency Framer and half-rate receive port clocking are also enabled (RFMODE = LOW, RXRATE = HIGH, and RXCKSEL ≠ LOW), the Framer will stretch the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

Notes:
9. The RXOPx outputs are also driven from the associated Output Register, but their interpretation is under the separate control of PARCTL.

Table 7. Decoder Bypass Mode (DECMODE = LOW)

Signal Name	Bus Weight	10Bit Name
RXSTx[2] (LSB)	COMDETx	
RXSTx[1]	2^0	a
RXSTx[0]	2^1	b
RXDx[0]	2^2	c
RXDx[1]	2^3	d
RXDx[2]	2^4	e
RXDx[3]	2^5	i
RXDx[4]	2^6	f
RXDx[5]	2^7	g
RXDx[6]	2^8	h
RXDx[7] (MSB)	2^9	j

When the Cypress or Alternate Mode Framer is enabled and half-rate receive port clocking is also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the Framer logic such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

This adjustment only occurs when the Framer is enabled (RFEN = HIGH). When the Framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLK– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the eleven data and status bits that are presented by each channel, an RXOPx parity output is also available on each channel. This allows the CYP15G0401RB to support ODD parity generation for each channel. To handle a wide range of system environments, the CYP15G0401RB supports different forms of parity generation, including no parity.

When the decoders are enabled (DECMODE ≠ LOW), parity can be generated on

- the RXDx[7:0] character
- the RXDx[7:0] character and RXSTx[2:0] status.

When the decoders are bypassed (DECMODE = LOW), parity can be generated on

- the RXDx[7:0] and RXSTx[1:0] bits
- the RXDx[7:0] and RXSTx[2:0] bits.

These modes differ in the number of bits which are included in the parity calculation. Only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 8*.

Table 8. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)			
	LOW [10]	MID		HIGH
		DECMODE = LOW	DECMODE ≠ LOW	
RXSTx[2]				X [11]
RXSTx[1]		X		X
RXSTx[0]		X		X
RXDx[0]		X	X	X
RXDx[1]		X	X	X
RXDx[2]		X	X	X
RXDx[3]		X	X	X
RXDx[4]		X	X	X
RXDx[5]		X	X	X
RXDx[6]		X	X	X
RXDx[7]		X	X	X

Parity generation is enabled through the three-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL = MID (open) and the decoders are enabled (DECMODE ≠ LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] signals and is presented on the associated RXOPx output. When PARCTL = MID and the decoders are bypassed (DECMODE = LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] and RXSTx[1:0] bit positions. When PARCTL = HIGH, ODD parity is generated for the RXDx[7:0] and the associated RXSTx[2:0] status bits.

Receive Status Bits

When the 10B/8B Decoder is enabled (DECMODE ≠ LOW), each character presented at the Output Register includes three associated status bits. These bits are used to identify:

- if the contents of the data bus are valid
- the type of character present
- the state of receive BIST operations (regardless of the state of DECMODE)
- character violations.

These conditions normally overlap; e.g., a valid data character received with incorrect running disparity is not reported as a valid data character. It is instead reported as a Decoder violation of some specific type. This implies a hierarchy or priority level to the various status bit combinations. The hierarchy and value of each status is listed in *Table 9*.

The receive status when normal data is received is shown in *Table 9*. The receive status when Receive BIST is enabled is shown in *Table 10*.

Notes:

10. Receive path parity output drivers (RXOPx) are disabled (High-Z) when PARCTL = LOW.
11. When the Decoder is bypassed (DECMODE = LOW) and BIST is not enabled (Receive BIST Latch output is HIGH), RXSTx[2] is driven to a logic-0, except when the character in the output buffer is a framing character.

Table 9. Receive Character Status when Channels are Operated to Receive Normal Data

RXSTx[2:0]	Priority	Status
000	7	**Normal Character Received.** The valid data character with the correct running disparity received
001	7	**Special Code Detected**. Special code other than the selected framing character or decoder violation received
010	2	**Receive Elasticity Buffer underrun/overrun error.** The receive elasticity buffer was not able to add/drop a K28.5 or framing character.
011	5	**Framing Character Detected.** This indicates that a character matching the patterns identified as a framing character was detected. The decoded value of this character is present on the associated output bus.
100	4	**Codeword Violation.** The character on the output bus is a C0.7. This indicates that the received character cannot be decoded into any valid character.
101	1	**PLL Out Of Lock Indication**
110	6	**Running Disparity Error.** The character on the output bus is a C4.7, C1.7 or C2.7
111	3	**INVALID**

Table 10. Receive Character Status when Channels are Operated to Receive BIST Data

RXSTx[2:0]	Priority	Receive BIST Status (Receive BIST = Enabled)
000	7	**BIST Data Compare**. Character compared correctly
001	7	**BIST Command Compare**. Character compared correctly
010	2	**BIST Last Good**. Last Character of BIST sequence detected and valid.
011	5	**RESERVED for TEST**
100	4	**BIST Last Bad**. Last Character of BIST sequence detected invalid.
101	1	**BIST Start**. Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition, and Elasticity Buffer overflow/underflow conditions.
110	6	**BIST Error**. While comparing characters, a mismatch was found in one or more of the decoded character bits.
111	3	**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the RXSTx[2:0] bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 10*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than sixteen, the state machine is forced to the WAIT_FOR_BIST state where it monitors the interface for the first character (D0.0) of the next BIST sequence. Also, if the Elasticity Buffer ever hits an overflow/underflow condition, the status is forced to the BIST_START until the buffer is recentered (approximately nine character periods).

To ensure compatibility between the source and destination systems when operating in BIST modes, the sending and receiving ends of the link must use the same receive clock setup, i.e. RXCKSEL = MID or RXCKSEL ≠ MID. This is applicable when interfacing to a CYP(V)15G0401DXB for example. When interfacing to transmitter only HOTLink II devices such as the CYP15G0401TB it is necessary to have RXCKSEL = MID.

JTAG Support

The CYP15G0401RB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs, LVTTL outputs and the TRGCLK± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0401RB is ‘1C800069’x.

Three-level Select Inputs

Each Three-level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11, respectively.

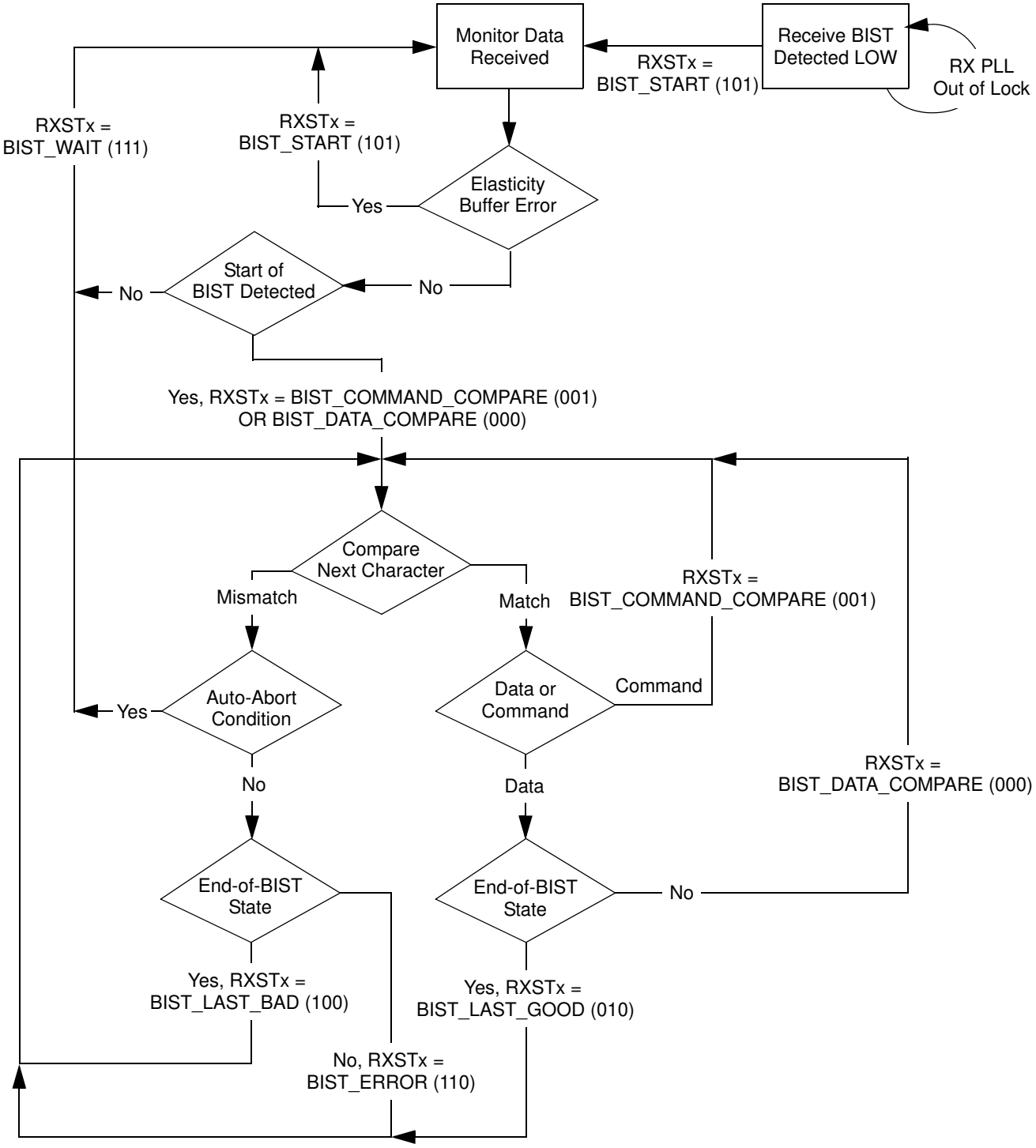


Figure 2. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. User guidelines only, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage.....> 2000V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Power-up Requirements

The CYP15G0401RB requires one power-supply. The voltage on any input or I/O pin cannot exceed the power pin during power-up

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%
Industrial	–40°C to +85°C	+3.3V ±5%

CYP15G0401RB DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[12]	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	TRGCLK Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	TRGCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: TRGCLK±					
V_{DIFF}[13]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	$V_{CC/2}$	V
V_{COMREF}[14]	Common Mode Range		1.0	V_{CC} – 1.2V	V
Three-level Inputs					
V_{IHH}	Three-level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND		–200	µA
Differential Serial Line Receiver Inputs: INA1±, INA2±, INB1±, INB2±, INC1±, INC2±, IND1±, IND2±					
V_{DIFFS}[13]	Input Differential Voltage |(IN+) – (IN–)|		100	1200	mV
V_{IHE}	Highest Input HIGH Voltage			V_{CC}	V

Notes:

12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
14. The common mode range defines the allowable range of TRGCLK+ and TRGCLK– when TRGCLK+ = TRGCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

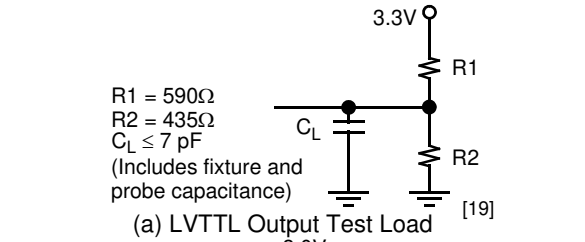
CYP15G0401RB DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{ILE}	Lowest Input LOW Voltage		V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.		1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.	–700		µA
V_{COM} [15, 16]	Common Mode Input Range		V_{CC} – 1.95	V_{CC} – 0.05	V

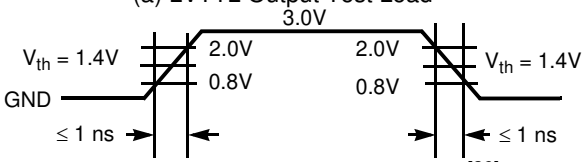
Power Supply

Parameter	Description	Test Conditions	Typ.[17]	Max.[18]	Unit
I_{CC}	Power Supply Current TRGCLK = Max.	Commercial	660	690	mA
		Industrial		740	mA
I_{CC}	Power Supply Current TRGCLK = 125 MHz	Commercial	640	650	mA
		Industrial		700	mA

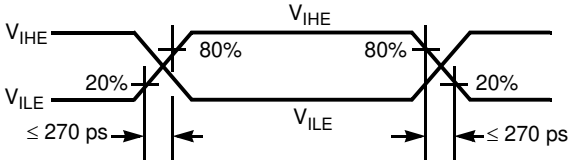
Test Loads and Waveforms



(a) LVTTL Output Test Load



(b) LVTTL Input Test Waveform [20]



(c) CML/LVPECL Input Test Waveform

CYP15G0401RB AC Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
CYP15G0401RB Receiver LVTTL Switching Characteristics Over the Operating Range				
f_{RS}	RXCLKx Clock Output Frequency	9.75	150	MHz
t_{RXCLKP}	RXCLKx Period	6.66	102.56	ns
t_{RXCLKH}	RXCLKx HIGH Time (RXRATE = LOW)	2.33 [21]	26.64	ns
	RXCLKx HIGH Time (RXRATE = HIGH)	5.66	52.28	ns
t_{RXCLKL}	RXCLKx LOW Time (RXRATE = LOW)	2.33 [21]	26.64	ns
	RXCLKx LOW Time (RXRATE = HIGH)	5.66	52.28	ns
t_{RXCLKD}	RXCLKx Duty Cycle centered at 50%	–1.0	+1.0	ns
t_{RXCLKR} [21]	RXCLKx Rise Time	0.3	1.2	ns
t_{RXCLKF} [21]	RXCLKx Fall Time	0.3	1.2	ns

Notes:

15. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
16. Not applicable for AC-coupled interfaces. For AC-coupled interfaces, V_{DIFFS} requirement still needs to be satisfied.
17. Maximum I_{CC} is measured with V_{CC} = MAX, RXCKSEL = LOW, with all TX and RX channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern to the associated receive channel, and outputs unloaded.
18. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, RXCKSEL = LOW, with all RX channels enabled receiving a continuous alternating 01 pattern to the associated receive channel. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
19. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only. 5-pF differential load reflects tester capacitance, and is recommended at low data rates only.
20. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses the threshold voltage.
21. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.

CYP15G0401RB AC Characteristics Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
t_{RXDV-} [24]	Status and Data Valid Time to RXCLKx (RXCKSEL HIGH or MID)	5UI – 1.5		ns
	Status and Data Valid Time to RXCLKx (HALF RATE RECOVERED CLOCK)	5UI – 1.0		ns
t_{RXDV+} [24]	Status and Data Valid Time From RXCLKx (RXCKSEL HIGH or MID)	5UI – 1.8		ns
	Status and Data Valid Time From RXCLKx (HALF RATE RECOVERED CLOCK)	5UI – 2.3		ns

CYP15G0401RB TRGCLK Switching Characteristics Over the Operating Range				
f_{TRG}	TRGCLK Clock Frequency	19.5	150	MHz
t_{TRGCLK}	TRGCLK Period	6.66	51.28	ns
t_{TRGH}	TRGCLK HIGH Time (TRGRATE = HIGH)	5.9		ns
	TRGCLK HIGH Time (TRGRATE = LOW)	2.9 [21]		ns
t_{TRGL}	TRGCLK LOW Time (TRGRATE = HIGH)	5.9		ns
	TRGCLK LOW Time (TRGRATE = LOW)	2.9 [21]		ns
t_{TRGD} [25]	TRGCLK Duty Cycle	30	70	%
t_{TRGR} [21, 22, 23]	TRGCLK Rise Time (20% – 80%)		2	ns
t_{TRGF} [21, 22, 23]	TRGCLK Fall Time (20% – 80%)		2	ns
t_{RTRGDA} [26]	Receive Data Access Time from TRGCLK (RXCKSEL = LOW)		9.5	ns
t_{RTRGDV}	Receive Data Valid Time from TRGCLK (RXCKSEL = LOW)	2.5		ns
$t_{TRGADV-}$	Received Data Valid Time to RXCLKA (RXCKSEL = LOW)	10UI – 4.7		ns
$t_{TRGADV+}$	Received Data Valid Time from RXCLKA (RXCKSEL = LOW)	0.5		ns
$t_{TRGCDV-}$	Received Data Valid Time to RXCLKC (RXCKSEL = LOW)	10UI – 4.3		ns
$t_{TRGCDV+}$	Received Data Valid Time from RXCLKC (RXCKSEL = LOW)	–0.2		ns
t_{TRGRX} [4]	TRGCLK Frequency Referenced to Received Clock Period	–1500	+1500	ppm

CYP15G0401RB Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range					
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)			376K	UI[29]
	Receive PLL lock to input data stream			376K	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate			46	UI
t_{JTOL} [27]	Total Jitter Tolerance	IEEE 802.3z[28]	600		ps
t_{DJTOL} [27]	Deterministic Jitter Tolerance	IEEE 802.3z[28]	370		ps

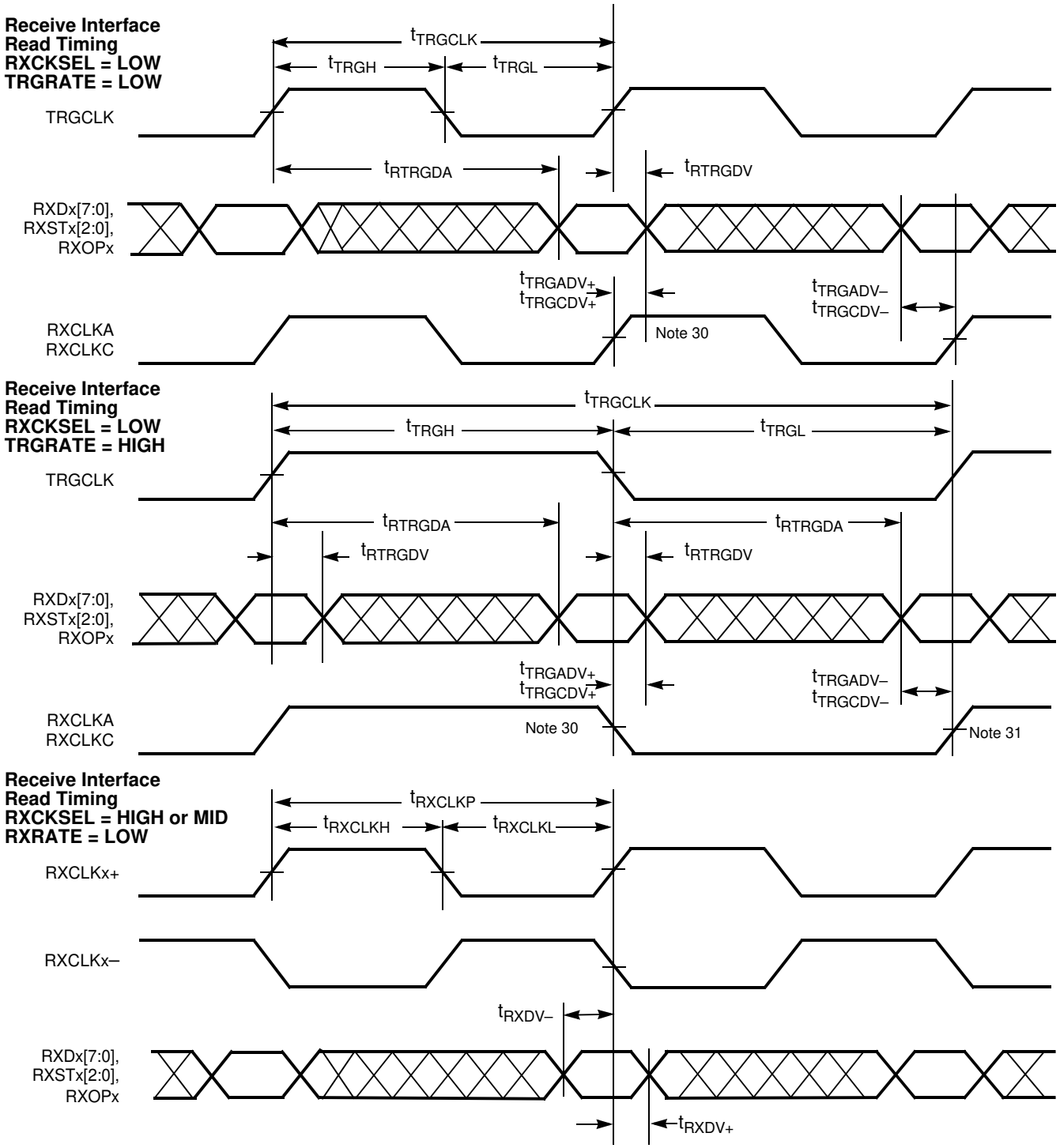
Capacitance [21]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 3.3V$	7	pF
C_{INPECL}	PECL input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 3.3V$	4	pF

Notes:

22. The ratio of rise time to falling time must not vary by greater than 2:1.
23. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
24. Parallel data output specifications are only valid if all inputs or outputs are loaded with similar DC and AC loads.
25. The duty cycle specification is a simultaneous condition with the t_{TRGH} and t_{TRGL} parameters. This means that at faster character rates the TRGCLK duty cycle cannot be as large as 30% – 70%.
26. Since this timing parameter is greater than the minimum time period of TRGCLK it sets an upper limit to the frequency in which TRGCLKx can be used to clock the receive data out of the output register. For predictable timing, users can use this parameter only if TRGCLK period is greater than sum of t_{RTRGDA} and set-up time of the upstream device. When this condition is not true, RXCLKC± or RXCLKA± (a buffered or delayed version of TRGCLK when RXCKSELx = LOW) could be used to clock the receive data out of the device.
27. Total jitter is calculated at an assumed BER of 1E –12. Hence: total jitter (t_J) = (t_{RJ} * 14) + t_{DJ}.
28. Also meets all Jitter Tolerance requirements as specified by OBSAI RP3, CPRI, ESCON, FICON, Fibre Channel and DVB-ASI.
29. Receiver UI (Unit Interval) is calculated as 1/(f_{TRG} * 20) (when RXRATE = HIGH) or 1/(f_{TRG} * 10) (when RXRATE = LOW) if no data is being received, or 1/(f_{TRG} * 20) (when RXRATE = HIGH) or 1/(f_{TRG} * 10) (when RXRATE = LOW) of the remote transmitter if data is being received. In an operating link this is equivalent to t_B.

Switching Waveforms for the CYP15G0401RB HOTLink II Receiver



Notes:

30. RXCLKA and RXCLKC are delayed in phase from TRGCLK, and are different in phase from each other.
31. When operated with a half-rate TRGCLK, the set-up and hold specifications for data relative to RXCLKA and RXCLKC are relative to both rising and falling edges of the respective clock output.

Switching Waveforms for the CYP15G0401RB HOTLink II Receiver (continued)

Receive Interface
Read Timing
RXCKSEL = HIGH or MID
RXRATE = HIGH

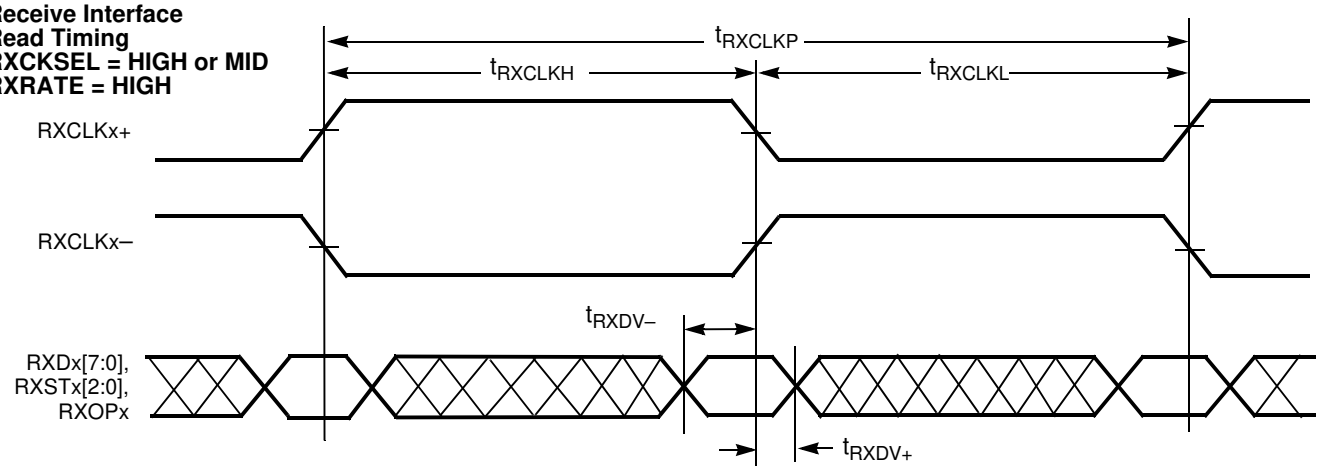


Table 11.Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	INC1–	CML IN	C04	INSELB	LVTTL IN	E19	VCC	POWER
A02	N/C	NO CONNECT	C05	VCC	POWER	E20	VCC	POWER
A03	INC2–	CML IN	C06	PARCTL	3-LEVEL SEL	F01	N/C	NO CONNECT
A04	N/C	NO CONNECT	C07	SDASEL	3-LEVEL SEL	F02	VCC	POWER
A05	VCC	POWER	C08	GND	GROUND	F03	VCC	POWER
A06	IND1–	CML IN	C09	N/C	NO CONNECT	F04	RXCKSEL	3-LEVEL SEL
A07	N/C	NO CONNECT	C10	N/C	NO CONNECT	F17	BISTLE	LVTTL IN PU
A08	GND	GROUND	C11	N/C	NO CONNECT	F18	RXSTB[1]	LVTTL OUT
A09	IND2–	CML IN	C12	N/C	NO CONNECT	F19	RXOPB	LVTTL 3-S OUT
A10	N/C	NO CONNECT	C13	GND	GROUND	F20	RXSTB[0]	LVTTL OUT
A11	INA1–	CML IN	C14	N/C	NO CONNECT	G01	GND	GROUND
A12	N/C	NO CONNECT	C15	GND	GROUND	G02	GND	GROUND
A13	GND	GROUND	C16	VCC	POWER	G03	GND	GROUND
A14	INA2–	CML IN	C17	TRGRATE	LVTTL IN PD	G04	GND	GROUND
A15	N/C	NO CONNECT	C18	RXRATE	LVTTL IN PD	G17	DECMODE	3-LEVEL SEL
A16	VCC	POWER	C19	GND	GROUND	G18	GND	GROUND
A17	INB1–	CML IN	C20	TDO	LVTTL 3-S OUT	G19	FRAMCHAR	3-LEVEL SEL
A18	N/C	NO CONNECT	D01	TCLK	LVTTL IN PD	G20	RXDB[1]	LVTTL OUT
A19	INB2–	CML IN	D02	$\overline{\text{TRSTZ}}$	LVTTL IN PU	H01	GND	GROUND
A20	N/C	NO CONNECT	D03	INSELD	LVTTL IN	H02	GND	GROUND
B01	INC1+	CML IN	D04	INSELA	LVTTL IN	H03	GND	GROUND
B02	N/C	NO CONNECT	D05	VCC	POWER	H04	GND	GROUND
B03	INC2+	CML IN	D06	RFMODE	3-LEVEL SEL	H17	GND	GROUND
B04	N/C	NO CONNECT	D07	SPDSEL	3-LEVEL SEL	H18	GND	GROUND
B05	VCC	POWER	D08	GND	GROUND	H19	GND	GROUND
B06	IND1+	CML IN	D09	BRE[3]	LVTTL IN PU	H20	GND	GROUND
B07	N/C	NO CONNECT	D10	BRE[2]	LVTTL IN PU	J01	GND	GROUND
B08	GND	GROUND	D11	BRE[1]	LVTTL IN PU	J02	GND	GROUND
B09	IND2+	CML IN	D12	BRE[0]	LVTTL IN PU	J03	GND	GROUND
B10	N/C	NO CONNECT	D13	GND	GROUND	J04	GND	GROUND
B11	INA1+	CML IN	D14	N/C	NO CONNECT	J17	RXSTB[2]	LVTTL OUT
B12	N/C	NO CONNECT	D15	GND	GROUND	J18	RXDB[0]	LVTTL OUT
B13	GND	GROUND	D16	VCC	POWER	J19	RXDB[5]	LVTTL OUT
B14	INA2+	CML IN	D17	VCC	POWER	J20	RXDB[2]	LVTTL OUT
B15	N/C	NO CONNECT	D18	RXLE	LVTTL IN PU	K01	RXDC[2]	LVTTL OUT
B16	VCC	POWER	D19	RFEN	LVTTL IN PD	K02	RXCLKC–	LVTTL OUT
B17	INB1+	CML IN	D20	N/C	NO CONNECT	K03	GND	GROUND
B18	N/C	NO CONNECT	E01	VCC	POWER	K04	$\overline{\text{LFIC}}$	LVTTL OUT
B19	INB2+	CML IN	E02	VCC	POWER	K17	RXDB[3]	LVTTL OUT
B20	N/C	NO CONNECT	E03	VCC	POWER	K18	RXDB[4]	LVTTL OUT
C01	TDI	LVTTL IN PU	E04	VCC	POWER	K19	RXDB[7]	LVTTL OUT
C02	TMS	LVTTL IN PU	E17	VCC	POWER	K20	RXCLKB+	LVTTL I/O PD
C03	INSELC	LVTTL IN	E18	VCC	POWER	L01	RXDC[3]	LVTTL OUT

Table 11.Package Coordinate Signal Allocation (continued)

Ball ID	Signal Name	Signal Type
L02	RXCLKC+	LVTTL I/O PD
L03	GND	GROUND
L04	GND	GROUND
L17	RXDB[6]	LVTTL OUT
L18	$\overline{\text{LFIB}}$	LVTTL OUT
L19	RXCLKB–	LVTTL OUT
L20	GND	GROUND
M01	RXDC[4]	LVTTL OUT
M02	RXDC[5]	LVTTL OUT
M03	RXDC[7]	LVTTL OUT
M04	RXDC[6]	LVTTL OUT
M17	GND	GROUND
M18	GND	GROUND
M19	GND	GROUND
M20	GND	GROUND
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	RXDC[1]	LVTTL OUT
P02	RXDC[0]	LVTTL OUT
P03	RXSTC[0]	LVTTL OUT
P04	RXSTC[1]	LVTTL OUT
P17	GND	GROUND
P18	GND	GROUND
P19	GND	GROUND
P20	GND	GROUND
R01	RXSTC[2]	LVTTL OUT
R02	RXOPC	LVTTL 3-S OUT
R03	N/C	NO CONNECT
R04	VCC	POWER
R17	VCC	POWER
R18	VCC	POWER
R19	VCC	POWER
R20	N/C	NO CONNECT
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	VCC	POWER
U02	VCC	POWER
U03	VCC	POWER
U04	VCC	POWER
U05	VCC	POWER
U06	RXDD[2]	LVTTL OUT
U07	RXDD[1]	LVTTL OUT
U08	GND	GROUND
U09	RXOPD	LVTTL 3-S OUT
U10	N/C	NO CONNECT
U11	TRGCLK–	PECL IN
U12	GND	GROUND
U13	GND	GROUND
U14	GND	GROUND
U15	VCC	POWER
U16	VCC	POWER
U17	RXDA[2]	LVTTL OUT
U18	RXOPA	LVTTL OUT
U19	RXSTA[2]	LVTTL OUT
U20	RXSTA[1]	LVTTL OUT
V01	VCC	POWER
V02	VCC	POWER
V03	VCC	POWER
V04	RXDD[6]	LVTTL OUT
V05	VCC	POWER
V06	RXDD[3]	LVTTL OUT
V07	RXSTD[0]	LVTTL OUT
V08	GND	GROUND
V09	RXSTD[2]	LVTTL OUT
V10	N/C	NO CONNECT
V11	TRGCLK+	PECL IN
V12	N/C	NO CONNECT
V13	GND	GROUND
V14	GND	GROUND
V15	VCC	POWER
V16	VCC	POWER
V17	RXDA[7]	LVTTL OUT
V18	RXDA[3]	LVTTL OUT
V19	RXDA[0]	LVTTL OUT
V20	RXSTA[0]	LVTTL OUT
W01	VCC	POWER
W02	VCC	POWER
W03	$\overline{\text{LFID}}$	LVTTL OUT
W04	RXCLKD–	LVTTL OUT
W05	VCC	POWER
W06	RXDD[4]	LVTTL OUT
W07	RXSTD[1]	LVTTL OUT
W08	GND	GROUND
W09	N/C	NO CONNECT
W10	GND	GROUND
W11	GND	GROUND
W12	GND	GROUND
W13	GND	GROUND
W14	GND	GROUND
W15	VCC	POWER
W16	VCC	POWER
W17	$\overline{\text{LFIA}}$	LVTTL OUT
W18	RXCLKA–	LVTTL OUT
W19	RXDA[4]	LVTTL OUT
W20	RXDA[1]	LVTTL OUT
Y01	VCC	POWER
Y02	VCC	POWER
Y03	RXDD[7]	LVTTL OUT
Y04	RXCLKD+	LVTTL I/O PD
Y05	VCC	POWER
Y06	RXDD[5]	LVTTL OUT
Y07	RXDD[0]	LVTTL OUT
Y08	GND	GROUND
Y09	N/C	NO CONNECT
Y10	N/C	NO CONNECT
Y11	GND	GROUND
Y12	N/C	NO CONNECT
Y13	GND	GROUND
Y14	GND	GROUND
Y15	VCC	POWER
Y16	VCC	POWER
Y17	VCC	POWER
Y18	RXCLKA+	LVTTL I/O PD
Y19	RXDA[6]	LVTTL OUT
Y20	RXDA[5]	LVTTL OUT

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data characters are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 eight-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard contain a distinct and easily recognizable bit pattern that assists the receiver in achieving character alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an eight-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the eight-bit byte for the raw eight-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

```
FC-2 bit designation—   7  6  5  4  3  2  1  0
HOTLink D/Q designation—7  6  5  4  3  2  1  0
8B/10B bit designation— H  G  F  E  D  C  B  A
```

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character.

```
FC-2  45H
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation, note that the order of bits has been reversed):

```
Data Byte Name  D5.2
      Bits: ABCDE FGH
            10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
      Bits: abcdei fghj
            101001 0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and SC/D = LOW) or a Special Character (c is set to K, and SC/D = HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7). This definition of the 10-bit Transmission Code is based on the following references.

A.X. Widmer and P.A. Franaszek. “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code” IBM Journal of Research and Development, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. “Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code” (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230-1994 ANSI FC-PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22-7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within any higher-level constructs specified by a standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit “a” is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order.

Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters and checking the validity of received Transmission Characters. In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two Transmission Characters. The two columns correspond to the current value of the running disparity. Running disparity is a binary parameter with either a negative (–) or positive (+) value.

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Trans-

mitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted and received.

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the six-bit sub-block if the four-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in *Table 14* for the Valid Data byte or *Table 15* for Special Character byte identify which Transmission Character is to be generated. The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 12* shows naming notations and examples of valid transmission characters.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.

Table 12.Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	00101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 12* shows an example of this behavior.

Table 13.Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 14.Valid Data Characters (RXSTx[2:0] = 000)

Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011
D1.0	000 00001	011101 0100	100010 1011
D2.0	000 00010	101101 0100	010010 1011
D3.0	000 00011	110001 1011	110001 0100
D4.0	000 00100	110101 0100	001010 1011
D5.0	000 00101	101001 1011	101001 0100
D6.0	000 00110	011001 1011	011001 0100
D7.0	000 00111	111000 1011	000111 0100
D8.0	000 01000	111001 0100	000110 1011
D9.0	000 01001	100101 1011	100101 0100
D10.0	000 01010	010101 1011	010101 0100
D11.0	000 01011	110100 1011	110100 0100
D12.0	000 01100	001101 1011	001101 0100
D13.0	000 01101	101100 1011	101100 0100
D14.0	000 01110	011100 1011	011100 0100
D15.0	000 01111	010111 0100	101000 1011
D16.0	000 10000	011011 0100	100100 1011
D17.0	000 10001	100011 1011	100011 0100
D18.0	000 10010	010011 1011	010011 0100
D19.0	000 10011	110010 1011	110010 0100
D20.0	000 10100	001011 1011	001011 0100
D21.0	000 10101	101010 1011	101010 0100
D22.0	000 10110	011010 1011	011010 0100
D23.0	000 10111	111010 0100	000101 1011
D24.0	000 11000	110011 0100	001100 1011
D25.0	000 11001	100110 1011	100110 0100
D26.0	000 11010	010110 1011	010110 0100
D27.0	000 11011	110110 0100	001001 1011
D28.0	000 11100	001110 1011	001110 0100
D29.0	000 11101	101110 0100	010001 1011
D30.0	000 11110	011110 0100	100001 1011
D31.0	000 11111	101011 0100	010100 1011

Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj
D0.1	001 00000	100111 1001	011000 1001
D1.1	001 00001	011101 1001	100010 1001
D2.1	001 00010	101101 1001	010010 1001
D3.1	001 00011	110001 1001	110001 1001
D4.1	001 00100	110101 1001	001010 1001
D5.1	001 00101	101001 1001	101001 1001
D6.1	001 00110	011001 1001	011001 1001
D7.1	001 00111	111000 1001	000111 1001
D8.1	001 01000	111001 1001	000110 1001
D9.1	001 01001	100101 1001	100101 1001
D10.1	001 01010	010101 1001	010101 1001
D11.1	001 01011	110100 1001	110100 1001
D12.1	001 01100	001101 1001	001101 1001
D13.1	001 01101	101100 1001	101100 1001
D14.1	001 01110	011100 1001	011100 1001
D15.1	001 01111	010111 1001	101000 1001
D16.1	001 10000	011011 1001	100100 1001
D17.1	001 10001	100011 1001	100011 1001
D18.1	001 10010	010011 1001	010011 1001
D19.1	001 10011	110010 1001	110010 1001
D20.1	001 10100	001011 1001	001011 1001
D21.1	001 10101	101010 1001	101010 1001
D22.1	001 10110	011010 1001	011010 1001
D23.1	001 10111	111010 1001	000101 1001
D24.1	001 11000	110011 1001	001100 1001
D25.1	001 11001	100110 1001	100110 1001
D26.1	001 11010	010110 1001	010110 1001
D27.1	001 11011	110110 1001	001001 1001
D28.1	001 11100	001110 1001	001110 1001
D29.1	001 11101	101110 1001	010001 1001
D30.1	001 11110	011110 1001	100001 1001
D31.1	001 11111	101011 1001	010100 1001

Table 14.Valid Data Characters (RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010

Table 14.Valid Data Characters (RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010

Table 14.Valid Data Characters (RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 15.Valid Special Character Codes and Sequences (RXSTx[2:0] = 001) [32, 33]

S.C. Code Name	S.C. Byte Name						Current RD– abcdei fghj	Current RD+ abcdei fghj
	Cypress			Alternate				
	S.C. Byte Name [34]		Bits HGF EDCBA	S.C. Byte Name [34]		Bits HGF EDCBA		
K28.0	C0.0	(C00)	000 00000	C28.0	(C1C)	000 11100	001111 0100	110000 1011
K28.1 [35]	C1.0	(C01)	000 00001	C28.1	(C3C)	001 11100	001111 1001	110000 0110
K28.2 [35]	C2.0	(C02)	000 00010	C28.2	(C5C)	010 11100	001111 0101	110000 1010
K28.3	C3.0	(C03)	000 00011	C28.3	(C7C)	011 11100	001111 0011	110000 1100
K28.4 [35]	C4.0	(C04)	000 00100	C28.4	(C9C)	100 11100	001111 0010	110000 1101
K28.5 [35, 36]	C5.0	(C05)	000 00101	C28.5	(CBC)	101 11100	001111 1010	110000 0101
K28.6 [35]	C6.0	(C06)	000 00110	C28.6	(CDC)	110 11100	001111 0110	110000 1001
K28.7 [35, 37]	C7.0	(C07)	000 00111	C28.7	(CFC)	111 11100	001111 1000	110000 0111
K23.7	C8.0	(C08)	000 01000	C23.7	(CF7)	111 10111	111010 1000	000101 0111
K27.7	C9.0	(C09)	000 01001	C27.7	(CFB)	111 11011	110110 1000	001001 0111
K29.7	C10.0	(C0A)	000 01010	C29.7	(CFD)	111 11101	101110 1000	010001 0111
K30.7	C11.0	(C0B)	000 01011	C30.7	(CFE)	111 11110	011110 1000	100001 0111
End of Frame Sequence								
EOFxx [39]	C2.1	(C22)	001 00010	C2.1	(C22)	001 00010	–K28.5, Dn.xxx0	+K28.5, Dn.xxx1
Code Rule Violation and SVS Tx Pattern								
Exception[37, 40]	C0.7	(CE0)	111 00000	C0.7	(CE0)	111 00000[43]	100111 1000	011000 0111
–K28.5 [41]	C1.7	(CE1)	111 00001	C1.7	(CE1)	111 00001[43]	001111 1010	001111 1010
+K28.5[42]	C2.7	(CE2)	111 00010	C2.7	(CE2)	111 00010[43]	110000 0101	110000 0101
Running Disparity Violation Pattern								
Exception[42]	C4.7	(CE4)	111 00100	C4.7	(CE4)	111 00100[43]	110111 0101	001000 1010

Notes:

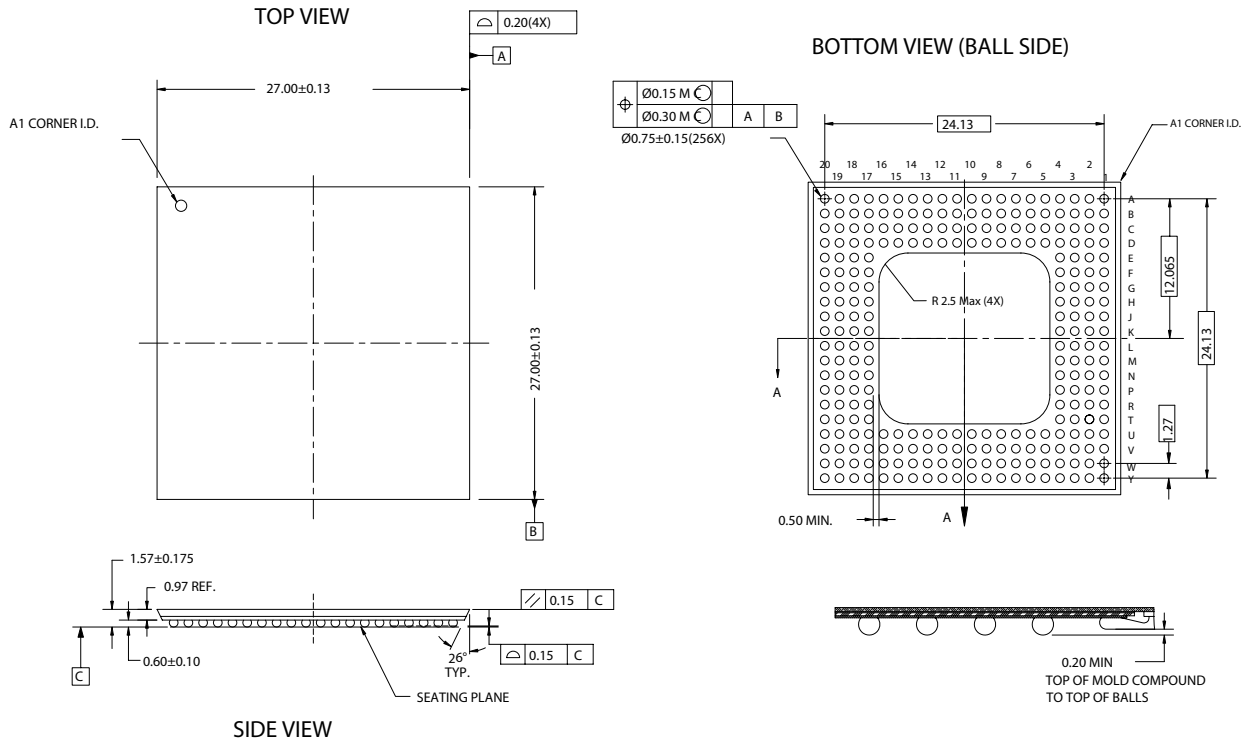
32. All codes not shown are reserved.
33. Notation for Special Character Code Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn = the specified value between 00 and FF).
34. Both the Cypress and alternate encodings may be used for data transmission to generate specific Special Character Codes. The decoding process for received characters generates Cypress codes or Alternate codes as selected by the DECMODE configuration input.
35. These characters are used for control of ESCON interfaces. They can be sent as embedded commands or other markers when not operating using ESCON protocols.
36. The K28.5 character is used for framing operations by the receiver. It is also the pad or fill character transmitted to maintain the serial link when no user data is available.
37. Care must be taken when using this Special Character code. When a K28.7(C7.0) or SVS(C0.7) is followed by a D11.x or D20.x, an alias K28.5 sync character is created. These sequences can cause erroneous framing and should be avoided while RFEN = HIGH.
38. C2.1 = Transmit either –K28.5+ or +K28.5– as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (–) the LSB becomes 1. This modification allows construction of X3.230 “EOF” frame delimiters wherein the second data byte is determined by the Current RD.
For example, to send “EOFdt” the controller could issue the sequence C2.1–D21.4– D21.4–D21.4, and the HOTLink II Transmitter will send either K28.5–D21.4–D21.4–D21.4 or K28.5–D21.5– D21.4–D21.4 based on Current RD. Likewise to send “EOFdti” the controller could issue the sequence C2.1–D10.4–D21.4–D21.4, and the HOTLink II Transmitter will send either K28.5–D10.4–D21.4– D21.4 or K28.5–D10.5–D21.4– D21.4 based on Current RD. The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.
39. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.
40. C1.7 = Transmit Negative K28.5 (–K28.5+) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if –K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.
41. C2.7 = Transmit Positive K28.5 (+K28.5–) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD–, otherwise K28.5 is decoded as C5.0 or C1.7.
42. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation. The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.
43. Supported only for data transmission. The receive status for these conditions will be reported by specific combinations of receive status bits.

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0401RB-BGC	BL256	256-ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP15G0401RB-BGI	BL256	256-ball Thermally Enhanced Ball Grid Array	Industrial
Standard	CYP15G0401RB-BGXC	BL256	Pb Free 256-ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP15G0401RB-BGXI	BL256	Pb Free 256-ball Thermally Enhanced Ball Grid Array	Industrial

Package Diagram

256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



51-85123-*E

Document History Page

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REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	318023	See ECN	REV	New Data Sheet