

August 1997

## 8-Bit, 125 MSPS, Flash A/D Converter

### Features

- Differential Linearity Error  $\pm 0.5$  LSB (Typ) or Less
- Integral Linearity Error  $\pm 0.5$  LSB (Typ) or Less
- Built-in Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 125 MSPS (Min)
- Low Input Capacitance (Typ) .....18pF
- Wide Analog Input Bandwidth (Min for Full Scale Input)..... 200MHz
- Single Power Supply .....-5.2V
- Low Power Consumption (Typ) .....870mW
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50 $\Omega$  Loads
- Direct Replacement for Sony CXA1396

### Applications

- Video Digitizing
- HDTV (High Definition TV)
- Direct RF Down-Conversion
- Communication Systems
- Radar Systems
- Digital Oscilloscopes

### Description

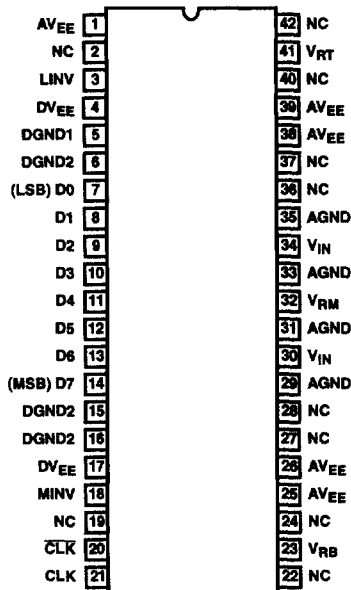
The HI1396 is an 8-bit, ultra high speed flash analog-to-digital converter IC capable of digitizing analog signals at the maximum rate of 125 MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

### Ordering Information

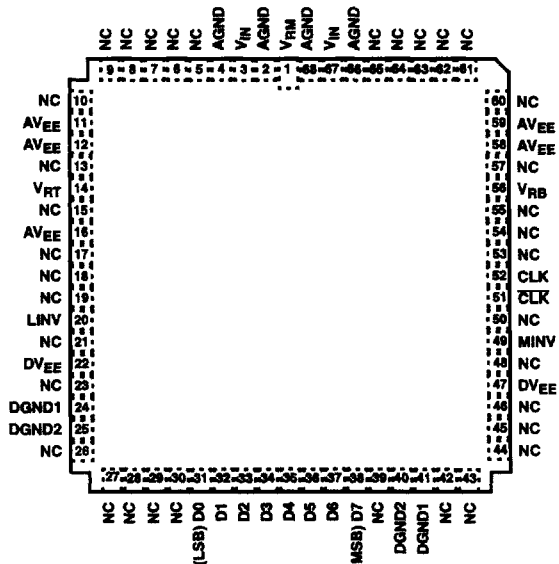
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1396JCJ	-20 to 75	42 Ld SBDIP	D42.6
HI1396AIL	-20 to 100	68 Ld CLCC	J68.A

### Pinouts

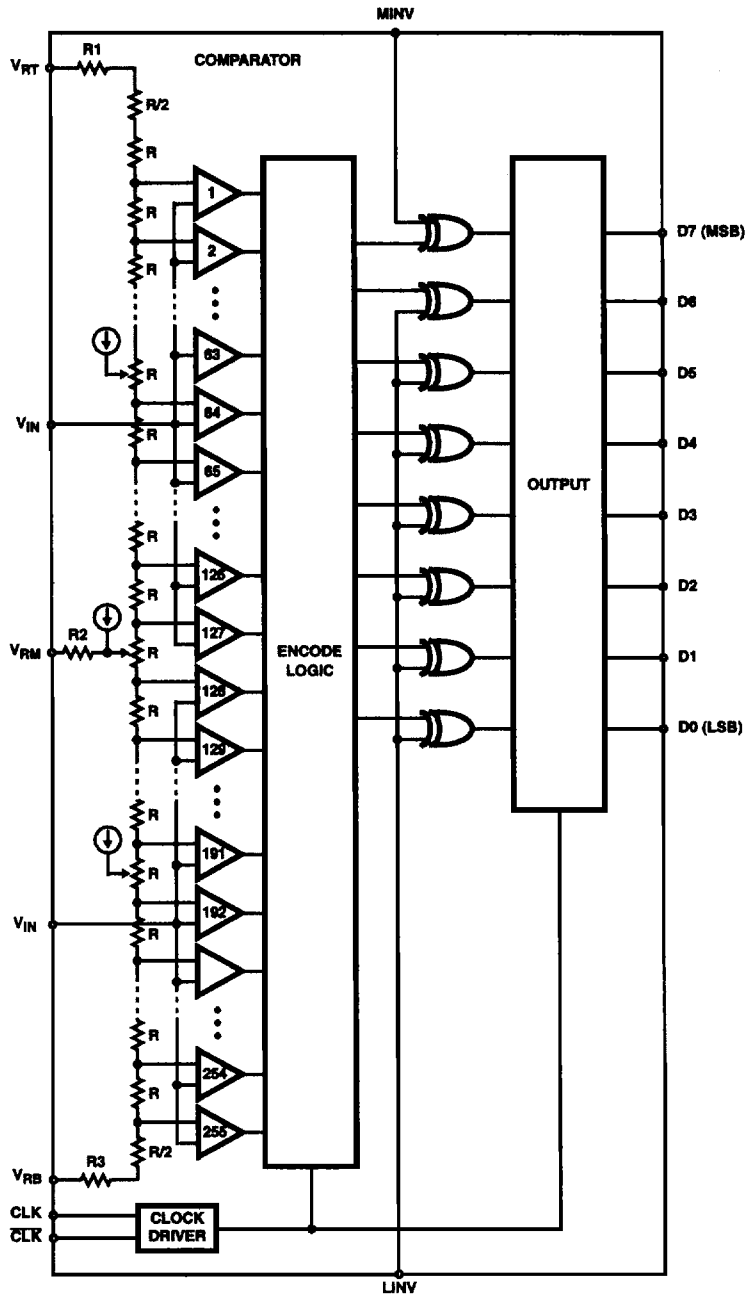
HI1396 (SBDIP)  
TOP VIEW



HI1396 (CLCC)  
TOP VIEW



Functional Block Diagram



**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$

Supply Voltage ( $V_{EE}$ , $DV_{EE}$ )	-7V
Analog Input Voltage ( $V_{IN}$ )	-2.7V to +0.5V
Reference Input Voltage	
$V_{RT}$ , $V_{RB}$ , $V_{RM}$	-2.7V to +0.5V
$I_{VRT} - V_{RB}$	2.5V
Digital Input Voltage	
CLK, $\bar{\text{CLK}}$ , MINV, LINV	-4V to +0.5V
CLK-CLK1	2.7V
$V_{RM}$ Pin Input Current ( $I_{VRM}$ )	-3mA to +3mA
Digital Output Current (ID0 to ID7)	-30mA to 0mA

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}^\circ\text{C/W}$	$\theta_{JC}^\circ\text{C/W}$
SBDIP Package	45	7
CLCC Package	45	8
Maximum Junction Temperature		
Ceramic Packages		175°C
Maximum Storage Temperature Range ( $T_{STG}$ )		-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)		300°C

**Operating Conditions** (Note 1)

Temperature Ranges (Note 4)	
SBDIP Package, $T_A$	-20°C to 75°C
CLCC Package, $T_C$	-20°C to 100°C
Supply Voltage Ranges	
$V_{EE}$ , $DV_{EE}$	-5.5V to -4.95V
$V_{EE} - DV_{EE}$	-0.05V to 0.05V
AGND - DGND	-0.05V to 0.05V
Reference Input Voltage	
$V_{RT}$	-0.1V to 0.1V
$V_{RB}$	-2.2V to -1.8V

Analog Input Voltage, $V_{IN}$	$V_{RB}$ to $V_{RT}$
Pulse Width of Clock	
$t_{PW1}$	4.0ns (Min)
$t_{PW0}$	4.0ns (Min)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ ,  $V_{EE} = DV_{EE} = -5.2\text{V}$ ,  $V_{RT} = 0\text{V}$ ,  $V_{RB} = -2\text{V}$  (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SYSTEM PERFORMANCE</b>					
Resolution		-	8	-	Bits
Integral Linearity Error, INL HI1396JCJ, HI1396AIL	$f_C = 125 \text{ MSPS}$	-	$\pm 0.3$	$\pm 0.5$	LSB
Differential Linearity Error, DNL HI1396JCJ, HI1396AIL	$f_C = 125 \text{ MSPS}$	-	-	$\pm 0.5$	LSB
<b>ANALOG INPUT</b>					
Input Bandwidth	$V_{IN} = 2\text{Vp-p}$	200	-	-	MHz
Analog Input Capacitance, $C_{IN}$	$V_{IN} = 1\text{V} + 0.07\text{V}_{\text{RMS}}$	-	17	-	pF
Analog Input Resistance, $R_{IN}$		50	190	-	k $\Omega$
Input Bias Current, $I_{IN}$	$V_{IN} = -1\text{V}$	20	130	400	$\mu\text{A}$
<b>REFERENCE INPUTS</b>					
Reference Resistance, $R_{REF}$		75	110	155	$\Omega$
Offset Voltage					
$E_{OT}$	$V_{RT}$	8	19	32	mV
$E_{OB}$	$V_{RB}$	0	15	24	mV
<b>DIGITAL INPUTS</b>					
Logic H Level, $V_{IH}$		-1.13	-	-	V
Logic L Level, $V_{IL}$		-	-	-1.50	V
Logic H Current, $I_{IH}$	Input Connected to -0.8V	0	-	50	$\mu\text{A}$
Logic L Current, $I_{IL}$	Input Connected to -1.6V	0	-	50	$\mu\text{A}$
Input Capacitance		-	7	-	pF
<b>DIGITAL OUTPUTS</b>					
Logic H Level, $V_{OH}$	$R_L = 50\Omega$ to -2V	-1.10	-	-	V
Logic L Level, $V_{OL}$	$R_L = 50\Omega$ to -2V	-	-	-1.62	V

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A/D CONVERTERS  
HIGH SPEED

# HI1396

## Electrical Specifications $T_A = 25^\circ\text{C}$ , $AV_{EE} = DV_{EE} = -5.2\text{V}$ , $V_{RT} = 0\text{V}$ , $V_{RB} = -2\text{V}$ (Note 1) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING CHARACTERISTICS</b>					
Output Rise Time, $t_r$	$R_L = 50\Omega$ to $-2\text{V}$ , 20% to 80%	0.5	0.9	1.2	ns
Output Fall Time, $t_f$	$R_L = 50\Omega$ to $-2\text{V}$ , 20% to 80%	0.5	1.0	1.3	ns
Output Delay, $t_{OD}$		3.0	3.6	4.2	ns
H Pulse Width of Clock, $tp_{W1}$		4.0	-	-	ns
L Pulse Width of Clock, $tp_{W0}$		4.0	-	-	ns
<b>DYNAMIC CHARACTERISTICS</b>					
Maximum Conversion Rate, $f_C$	Error Rate $10^{-9}$ TPS (Note 2)	125	-	-	MSPS
Aperture Jitter, $t_{AJ}$		-	10	-	ps
Sampling Delay, $t_{DS}$		-	1.5	-	ns
Signal to Noise Ratio (SINAD)	Input = 1MHz, Full Scale $f_C = 125$ MSPS	-	46	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise} + \text{Distortion}}$	Input = 31.5MHz, Full Scale $f_C = 125$ MSPS	-	40	-	dB
Error Rate	Input = 31.249MHz, Full Scale Error > 16 LSB, $f_C = 125$ MSPS	-	-	$10^{-9}$	TPS (Note 2)
Differential Gain Error, DG	NTSC 40 IRE Mod.	-	1.0	-	%
Differential Phase Error, DP	Ramp, $f_C = 125$ MSPS	-	0.5	-	Degree
<b>POWER SUPPLY CHARACTERISTICS</b>					
Supply Current, $I_{EE}$		-230	-160	-	mA
Power Consumption	Note 3	-	870	-	mW

### NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.

$$3. P_D = I_{EE} \cdot V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$$

4.  $T_A$  specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

### Timing Diagram

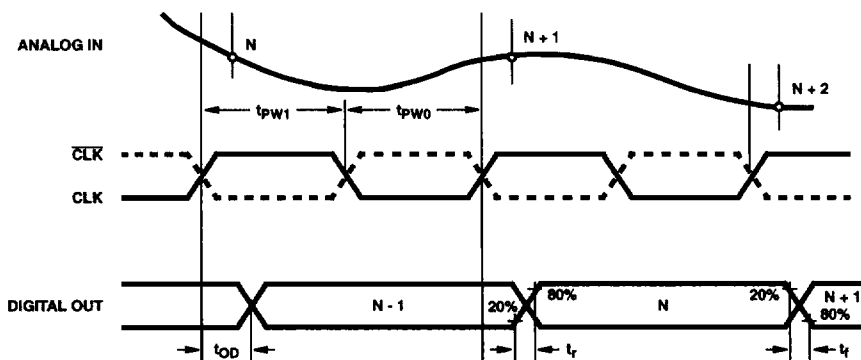


FIGURE 1.

# HI1396

## Pin Descriptions and I/O Pin Equivalent Circuits

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
29, 31, 33, 35	49, 51, 53, 55	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AV <sub>EE</sub>	-	-5.2V		Analog V <sub>EE</sub> -5.2V (Typ). Internally connected to DV <sub>EE</sub> (Resistance: 4Ω to 6Ω). Bypass with 0.1μF to AGND.
21	35	CLK	I	ECL		CLK Input.
20	34	CLK				Input complementary to CLK. When left open pulled down to -1.3V. Device is operable without CLK input, but use of complementary inputs of CLK and CLK is recommended to obtain stable high speed operation.
5, 16	7, 24	DGND1	-	0V		Digital GND for internal circuits.
6, 15	8, 23	DGND2	-	0V		Digital GND for output transistors.
4, 17	5, 30	DV <sub>EE</sub>	-	-5.2V		Digital V <sub>EE</sub> . Internally connected to AV <sub>EE</sub> (resistance: 4Ω to 6Ω). Bypass with 0.1μF to DGND
7	14	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	15	D1				Data outputs. External pull-down resistors are required.
9	16	D2				
10	17	D3				
11	18	D4				
12	19	D5				
13	20	D6				
14	21	D7		MSB of data outputs. External pull-down resistor is required.		

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**A/D CONVERTERS**  
**HIGH SPEED**

**Pin Descriptions and I/O Pin Equivalent Circuits** (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
3	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
18	32	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
30, 34	50, 54	V <sub>IN</sub>	I	V <sub>RT</sub> to V <sub>RB</sub>		<p>Analog input pins. These two pins must be connected externally, since they are not internally connected.</p>
23	39	V <sub>RB</sub>	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1μF and 10μF to AGND.
32	52	V <sub>RM</sub>	I	V <sub>RB</sub> /2		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
41	65	V <sub>RT</sub>	I	0V		Reference voltage (top) typically 0V. When a voltage different from AGND is applied to this pin, bypass with a 0.1μF and 10μF to AGND.

**Pin Descriptions and I/O Pin Equivalent Circuits** (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9-13, 25-29, 31, 33, 36-38, 40, 43-48, 56-61, 64, 66, 68	NC	-	-		Unused pins. No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

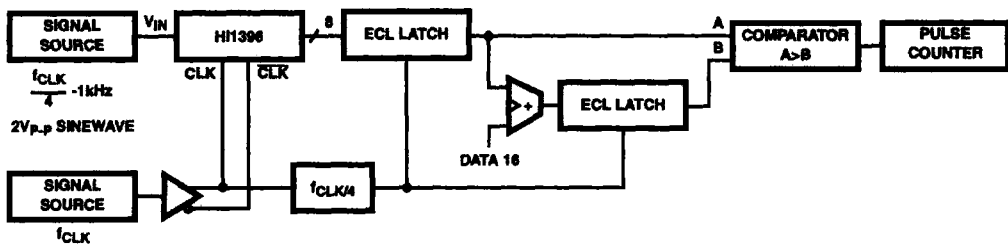
**A/D OUTPUT CODE TABLE**

V <sub>IN</sub> (Note 5)	STEP	MINV 1, LINV 1		0, 1		1, 0		0, 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V	0	000	.....00	100	.....00	011	.....11	111	.....11
		000	.....00	100	.....00	011	.....11	111	.....11
		000	.....01	100	.....01	011	.....10	111	.....10
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
-1V	127	011	.....11	111	.....11	000	.....00	100	.....00
		100	.....00	000	.....00	111	.....11	011	.....11
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		111	.....10	011	.....10	100	.....01	000	.....01
-2V	254	111	.....11	011	.....11	100	.....00	000	.....00
		111	.....11	011	.....11	100	.....00	000	.....00

NOTE:

5. V<sub>RT</sub> = 0V, V<sub>RB</sub> = -2V.

**Test Circuits**



**FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT**

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A/D CONVERTERS  
HIGH SPEED

Test Circuits (Continued)

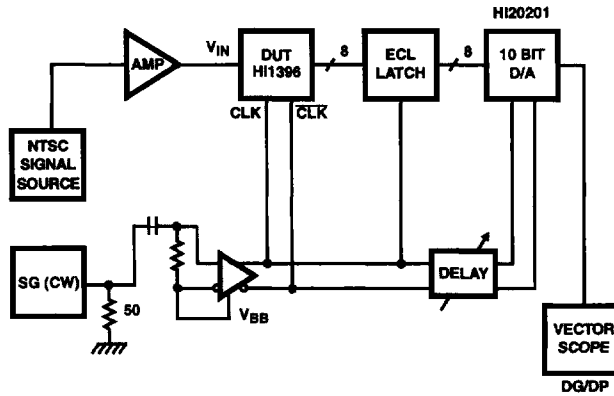


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

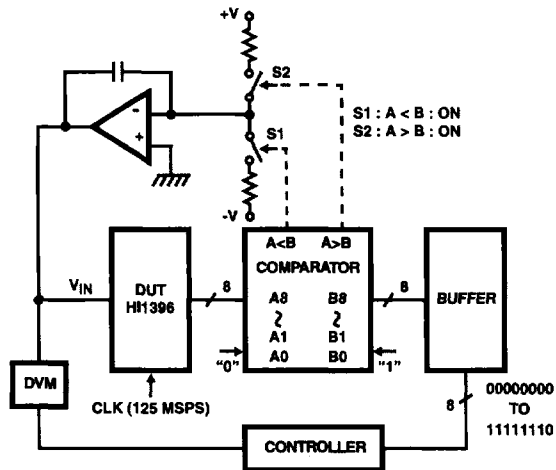


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT



Test Circuits (Continued)

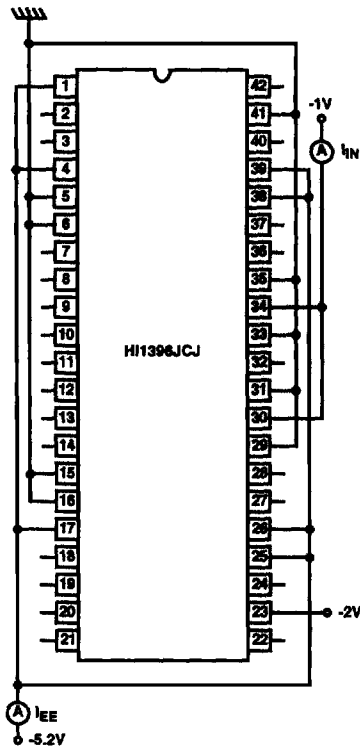


FIGURE 5A.

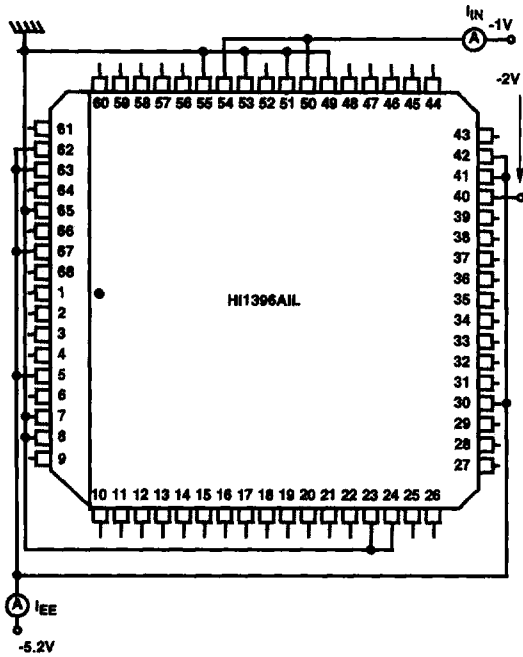


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

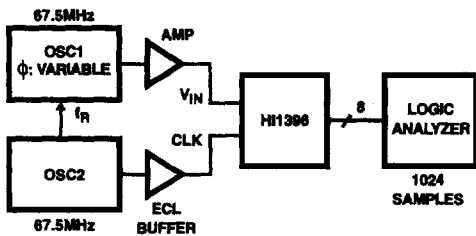
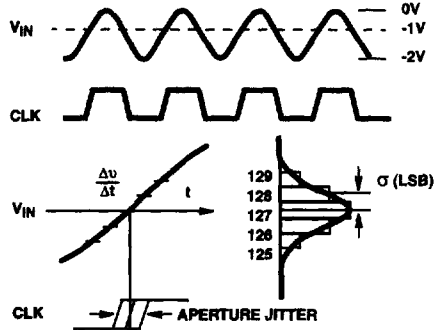


FIGURE 6A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma \frac{\Delta v}{\Delta t} = \sigma \left( \frac{256}{2} \times 2\pi f \right)$$

Where  $\sigma$  (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slow rate point.

FIGURE 6B. APERTURE JITTER TEST METHOD

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT