NUP1105LT1G, SZNUP1105LT1G

ESD Protection Diode

Single Line CAN/LIN Bus Protector

The NUP1105L has been designed to protect LIN and single line CAN transceivers from ESD and other harmful transient voltage events. This device provides bidirectional protection for the data line with a single SOT−23 package, giving the system designer a low cost option for improving system reliability and meeting stringent EMI requirements.

Features

- SOT−23 Package Allows One Separate Bidirectional Configuration
- 350 W Peak Power Dissipation per Line (8 x 20 μsec Waveform)
- Low Reverse Leakage Current (< 100 nA)
- IEC Compatibility: – IEC 61000−4−2 (ESD): Level 4
  – IEC 61000−4−4 (EFT): 40 A – 5/50 ns
  – IEC 61000−4−5 (Lighting) 8.0 A (8/20 μs)
- ISO 7637−1, Nonrepetitive EMI Surge Pulse TBD
- ISO 7637−3, Repetitive Electrical Fast Transient (EFT) TBD EMI Surge Pulses
- Flammability Rating UL 94 V−0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

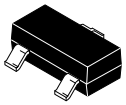
Applications

- Automotive Electronics
  - LIN Bus
  - Single Line CAN
- Industrial Control Networks
  - Smart Distribution Systems (SDS®)
  - DeviceNet™

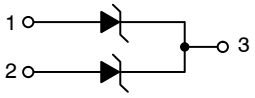
ON Semiconductor®

www.onsemi.com

SOT−23 BIDIRECTIONAL VOLTAGE SUPPRESSOR 350 W PEAK POWER

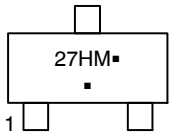


SOT−23
CASE 318
STYLE 27



PIN 1. ANODE
2. ANODE
3. CATHODE

MARKING DIAGRAM



27H = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP1105LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SZNUP1105LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
NUP1105LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

Symbol	Rating	Value	Unit
PPK	Peak Power Dissipation 8 x 20 μs Double Exponential Waveform (Note 1)	 350	W
T_J	Operating Junction Temperature Range	−55 to 150	°C
T_J	Storage Temperature Range	−55 to 150	°C
T_L	Lead Solder Temperature (10 s)	260	°C
ESD	Human Body model (HBM) Machine Model (MM) IEC 61000−4−2 Specification (Contact)	16 400 30	kV V kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non-repetitive current pulse per Figure 1.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)	24			V
V_{BR}	Breakdown Voltage	I_T = 1 mA (Note 3)	25.7		28.4	V
I_R	Reverse Leakage Current	V_{RWM} = 24 V		15	100	nA
V_C	Clamping Voltage	I_{PP} = 5 A (8 x 20 μs Waveform) (Note 4)			40	V
V_C	Clamping Voltage	I_{PP} = 8 A (8 x 20 μs Waveform) (Note 4)			44	V
I_{PP}	Maximum Peak Pulse Current	8 x 20 μs Waveform (Note 4)			8.0	A
CJ	Capacitance	V_R = 0 V, f = 1 MHz (Anode to GND) V_R = 0 V, f = 1 MHz (Anode to Anode)			60 30	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. Pulse waveform per Figure 1.
5. Include SZ-prefix devices where applicable.

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

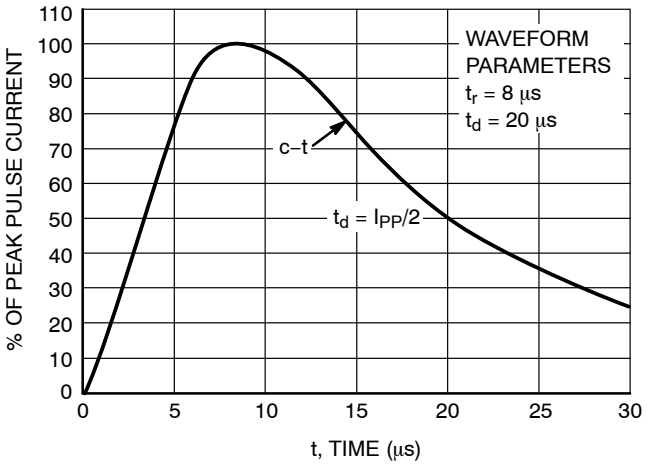


Figure 1. Pulse Waveform, 8 × 20 μs

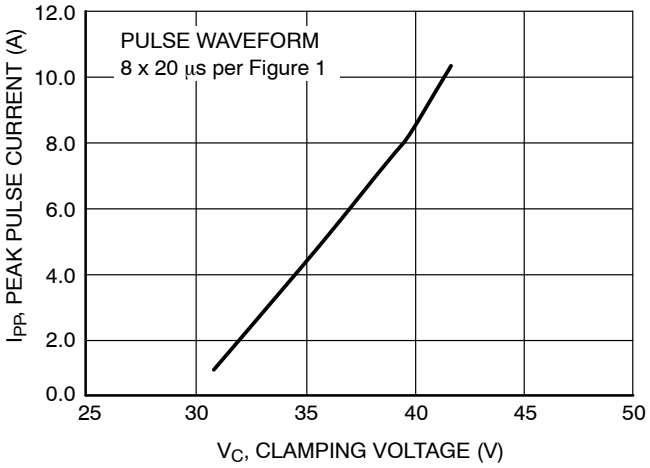


Figure 2. Clamping Voltage vs Peak Pulse Current

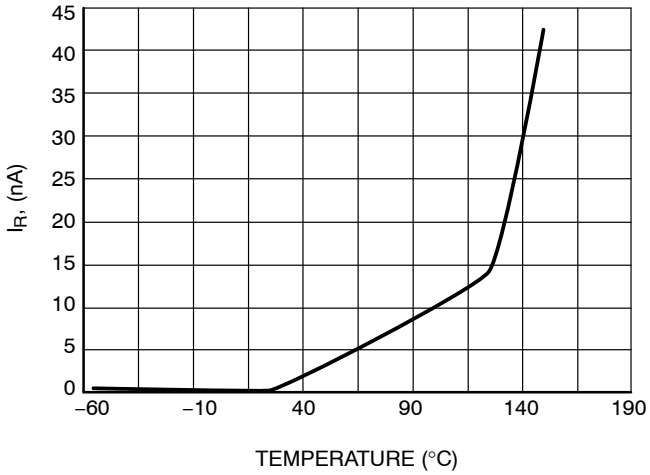


Figure 3. Typical Leakage vs. Temperature

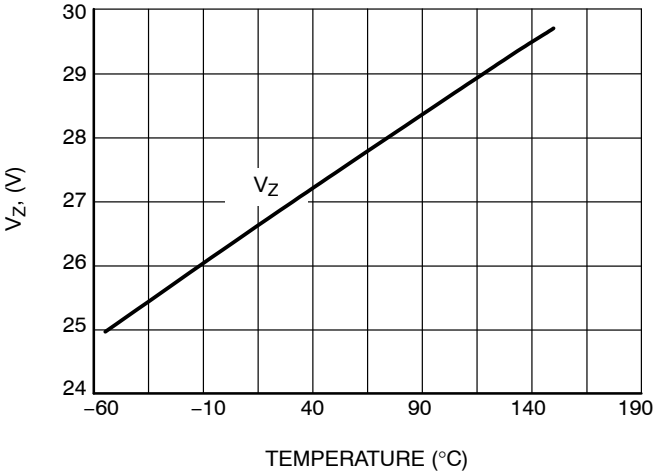


Figure 4. Typical V_Z @ 1.0 mA vs. Temperature

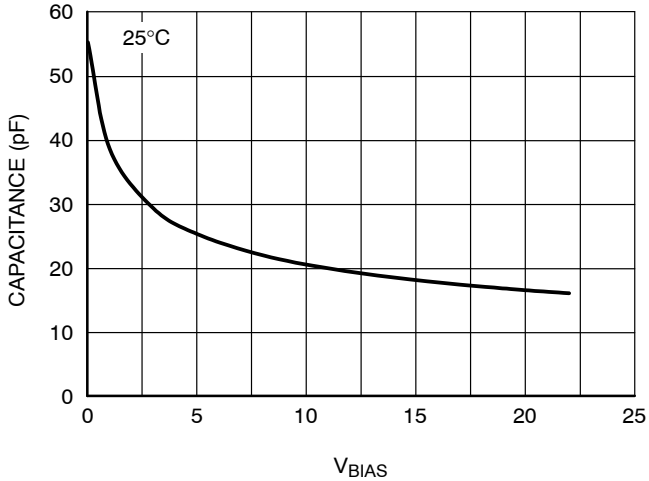


Figure 5. Capacitance vs. V_{BIAS}

APPLICATIONS SECTION

The NUP1105L provides a surge protection solution for the LIN data communication bus. The NUP1105L is a dual bidirectional surge protection device in a compact SOT−23 package. This device is based on Zener technology that optimizes the active area of a PN junction to provide robust protection against transient EMI surge voltage and ESD. The NUP1105L has been tested to EMI and ESD levels that exceed the specifications of popular high speed LIN networks.

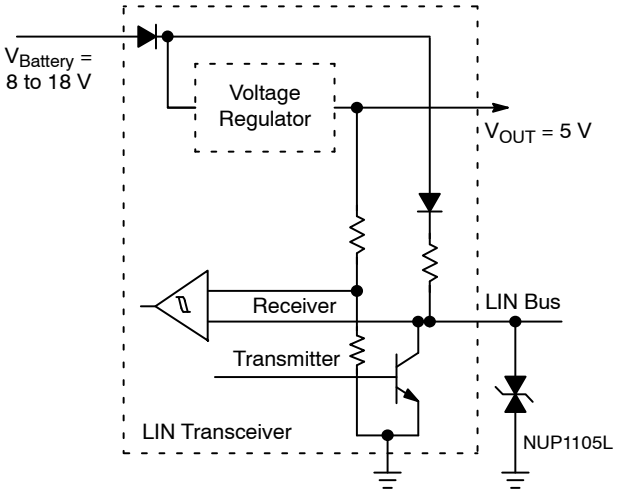


Figure 6. LIN Transceiver

The NUP1105L device can be used to provide transcient voltage suppression for a single data line CAN system. Figure 7 provides an example of a single data line CAN protection circuit.

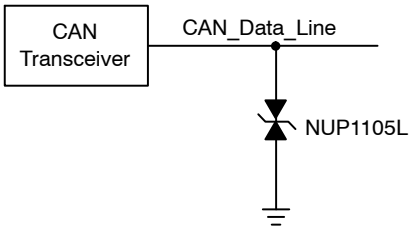
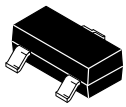


Figure 7. High−Speed and Fault Tolerant CAN Surge Protection Circuit

SDS is a registered trademark of Honeywell International Inc.
DeviceNet is a trademark of Rockwell Automation.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
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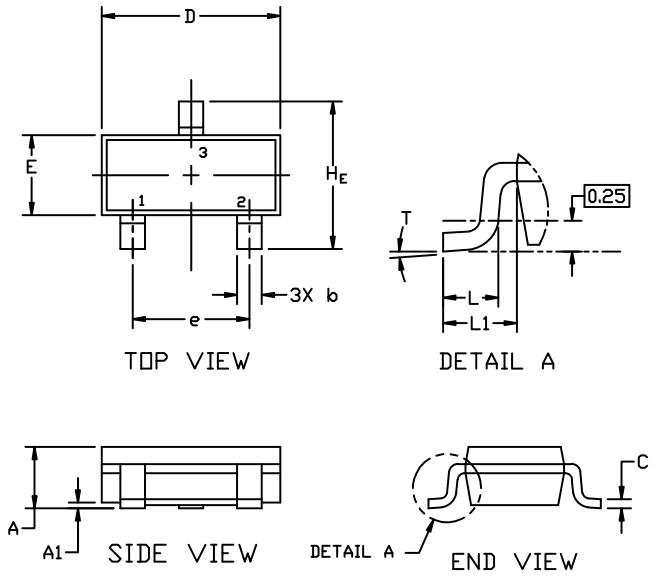
ISSUE AT

DATE 01 MAR 2023

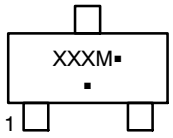


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

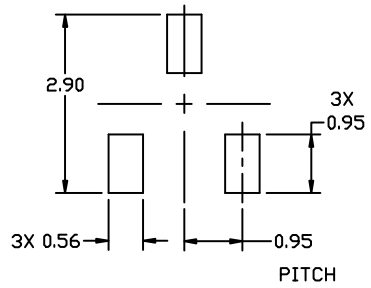
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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