IPS160HF, IPS161HF

Datasheet

60 V, 60 mΩ single high-side switches with short start-up propagation delay

Features

- 8 V to 60 V operating voltage range
- Minimum output current limitation: 0.7 A (IPS161HF) or 2.5 A (IPS160HF)
- Short propagation delay at start-up (≤ 60 µs)
- Fast demagnetization of inductive load
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Ground disconnection protection
- V_{CC} disconnection protection
- Thermal shutdown protection
- Undervoltage lock-out
- Diagnostic signalization for: open load in off-state, cut-off and junction thermal shutdown
- Designed to meet IEC 61131-2
- PowerSSO12 package

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Domotics
- General power supply switch

Product status
IPS160HF
IPS161HF

Product label

SUSTAINABLE TECHNOLOGY

Product summary		
Order code	IPS160HF	IPS160HFTR
	IPS161HF	IPS161HFTR
Package	PowerSSO12	
Packing	Tube	Tape and reel

Description

The IPS160HF (Iout < 2.5 A) and IPS161HF (Iout < 0.7 A) are monolithic devices which can drive capacitive, resistive or inductive loads with one side connected to ground.

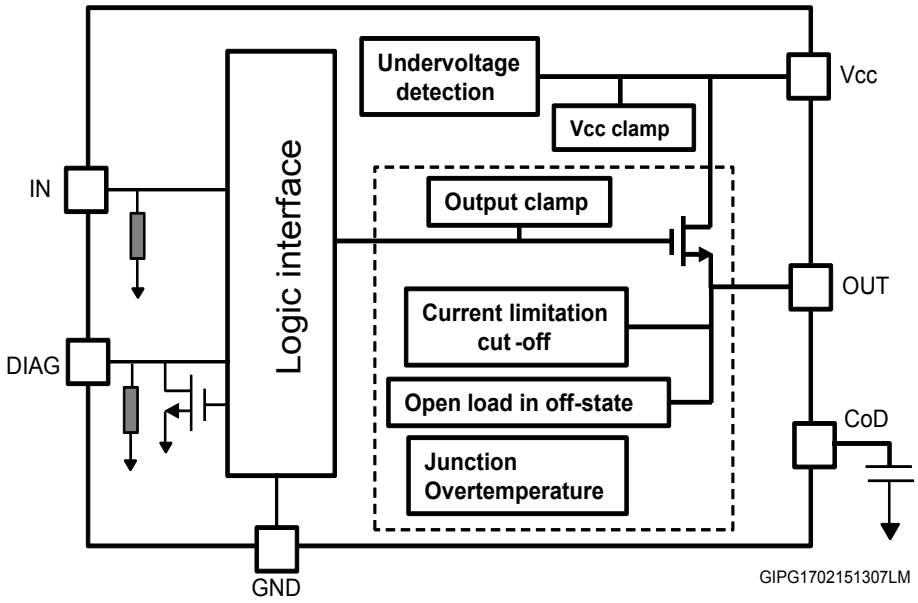
The 60 V operating range and Ron = 60 mΩ, combined with the extended diagnostic (Open Load, Over Load, Overtemperature) and the < 60 us propagation delay time at startup (enabling Class 3 for interface types C and D), make the IC suitable for applications implementing the proper architectures to address higher SIL levels.

The built-in overload and thermal shutdown protections guarantee the ICs, the application and the load against electrical and thermal overstress. Furthermore, in order to minimize the power dissipation when the output is shorted, a low-dissipative short-circuit protection (cut-off) is implemented to limit the output average current value and consequent device overheating. Cut-off delay time can be set by soldering an external capacitor or disabled by a resistor on pin 4 (CoD).

The DIAG common diagnostic open drain pin reports the open load in off-state, cut-off (overload) and thermal shutdown.

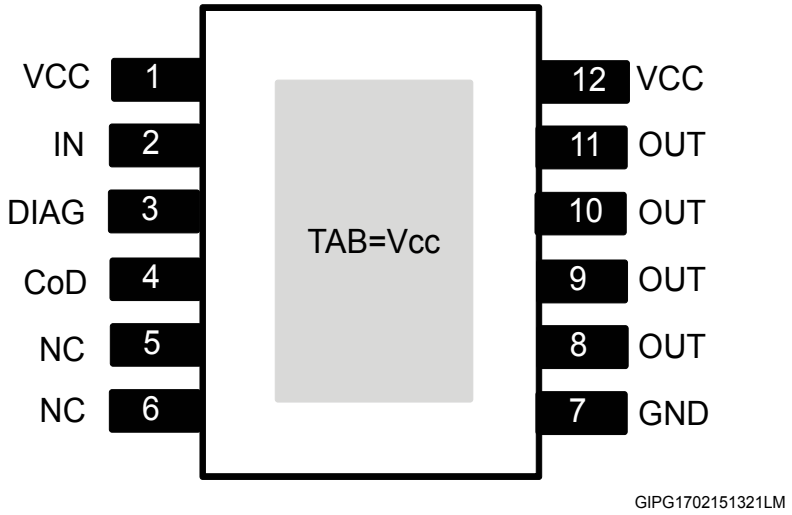
1 Block diagram

Figure 1. **Block diagram**



2 Pin description

Figure 2. **Pin connection (top view)**



GIPG1702151321LM

Table 1. **Pin configuration**

Number	Name	Function	Type
1, 12, TAB	VCC	Device supply voltage	Supply
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Cut-off delay pin, cannot be left floating. Connected to GND by 1 kΩ resistor to disable the cut-off function. Connect to a C_{CoD} capacitor to set the cut-off delay see Table 8. Protection and diagnostic	Input
5, 6	NC	Not connected	
7	GND	Device ground	Ground
8, 9, 10, 11	OUT	Channel power stage output	Output

IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see Table 7. Logic inputs.

OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

DIAG

This pin is used for diagnostic purposes and is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

CoD

This pin cannot be left floating and can be used to program the cut-off delay time t_{coff}, see Table 8. Protection and diagnostic through an external capacitor (C_{CoD}). The cut-off function can be completely disabled by connecting the CoD pin to GND through 1 kΩ resistor: in this condition, the output channel remains in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered.

GND

IC ground.

VCC

IC supply voltage.

Reverse polarity

The IC can be protected against reverse polarity using two different solutions:

1. Placing a resistor R_{GND} between IC GND pin and load connection point to GND (R_{GND} > VCC/Icc, see Table 2. Absolute maximum rating). Note that power dissipated by R_{GND} during reverse polarity condition is Vcc^2/R_{GND}.

2. Placing a diode in parallel to R_{GND}

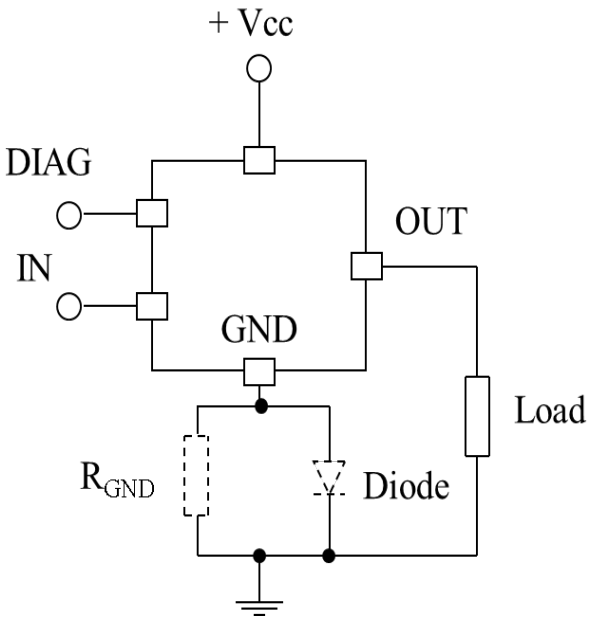
The diode must be selected such that its VRRM > |VCC| and power dissipation capability is higher than VF*I_S (see Table 4).

In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the module.

Using option 1, ΔV = R_{GND} * I_{CC}.

Using option 2, ΔV = $VF_{@(I_S)}$.

Figure 3. Reverse polarity protection schematic



3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 65	V
V_{OUT}	Output channel voltage	V_{cc}-V_{clamp} to V_{cc}+0.3	V
I_{IN}	Input current	-10 to +10	mA
V_{IN}	IN voltage	V_{CC}	V
V_{COD}	Output cut-off voltage pin	5.5	V
I_{COD}	Input current on cut-off pin	-1 to +10	mA
V_{DIAG}	Fault voltage	V_{CC}	V
I_{DIAG}	Fault current	-5 to +10	mA
I_{CC}	Maximum DC reverse current flowing through the IC from GND to V_{CC}	-250	mA
I_{OUT}	Output stage current	Internally limited	A
$-I_{OUT}$ (1)	Maximum DC reverse current flowing through the IC from OUT to V_{CC}	5	
E_{AS} (1)	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{load} = 0.5 A)	3000	mJ
	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{load} = 1 A)	1000	
P_{TOT}	Power dissipation at T_C = 25 °C (2)	Internally limited	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature	-40 to 150	

1. *Verified on X-NUCLEO-OUT08A1 and NUCLEO-OUT10A1 application board*
2. *$(T_{JSD(MAX)}$-$T_C)$/ $R_{th(JA)}$*

Note: Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		1s	2s2p	2s2p (with 4 thermal vias)	
$R_{th(JC)}$	Thermal resistance junction-case	0.4	0.9	0.5	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	117	57	29	

Note: $R_{th(JC)}$ is intended between the die and the bottom case surface measured by cold plate as per JESD51. $R_{th(JA)}$ according JESD51-3 (1s) JESD51-5 (2s2p) and JESD51-7 (2s2p and thermal vias).

4 Electrical characteristics

(8 V < V_{CC} < 60 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		V_{UVON}		60	V
V_{UVON}	Undervoltage on threshold		6.9		8	V
V_{UVOFF}	Undervoltage off threshold		6.5		7.8	V
V_{UVH}	Undervoltage hysteresis		0.15	0.5		V
I_S	Supply current in off-state	V_{CC} = 24 V		300	500	µA
		V_{CC} = 60 V		350	600	
	Supply current in on-state	V_{CC} = 24 V		1	1.4	mA
		V_{CC} = 60 V		1.4	2.1	
I_{LGND}	GND disconnection output current	V_{GND} = V_{IN} = V_{CC}, V_{OUT} = 0 V; T_J = 25°C			0.5	mA
		V_{GND} = V_{IN} = V_{CC}, V_{OUT} = 0 V; T_J = 125°C			0.55	

Table 5. Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	On-state resistance	V_{CC} = 24 V I_{OUT} =0.5 A (IPS161HF), 1 A (IPS160HF) @ T_J = 25 °C		60	80	mΩ
		V_{CC} = 24 V I_{OUT} =0.5 A (IPS161HF), 1 A (IPS160HF) @ T_J = 125 °C			120	
$V_{OUT(OFF)}$	Off-state output voltage	V_{IN} = 0 V and I_{OUT} = 0 A			2	V
$I_{OUT(OFF)}$	Off-state output current	V_{CC} = 24 V, V_{IN} = 0 V, V_{OUT} = 0 V			3	µA
		V_{CC} = 60 V, V_{IN} = 0 V, V_{OUT} = 0 V			10	
$I_{OUT(OFF-min)}$	Off-state output current	V_{IN} = 0 V, V_{OUT} = 4 V	-35		0	

Table 6. Switching (V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 48 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time	I_{OUT} = 0.5 A, (see Figure 4. Timing in normal operation)		10	20	µs
t_f	Fall time			10	20	
$t_{PD(H-L)}$	Propagation delay time off			20	35	
$t_{PD(L-H)}$	Propagation delay time on			20	35	
$t_{D(VCC-ON)}$	Power-on delay time from V_{CC} rising edge	I_{OUT} = 0.5 A, (see Figure 5. Propagation delay at start-up)		32	60	

Figure 4. Timing in normal operation

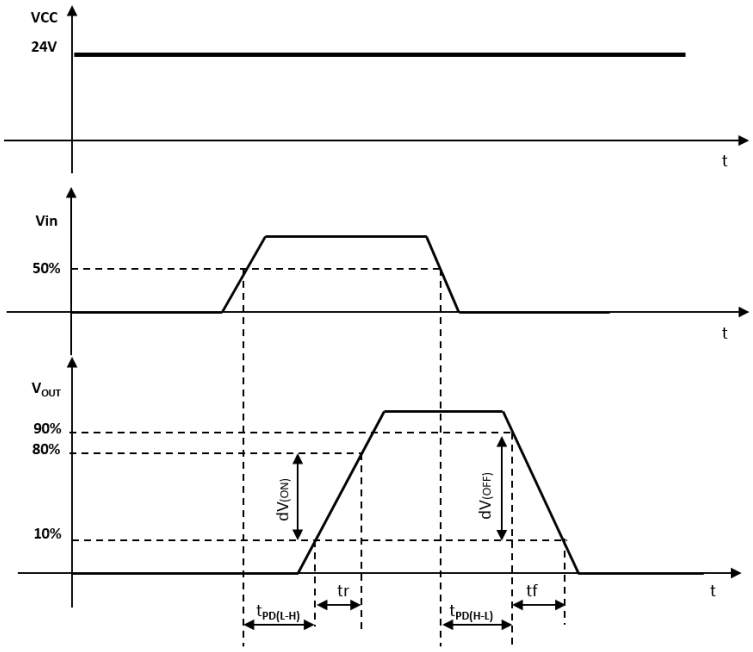


Figure 5. Propagation delay at start-up

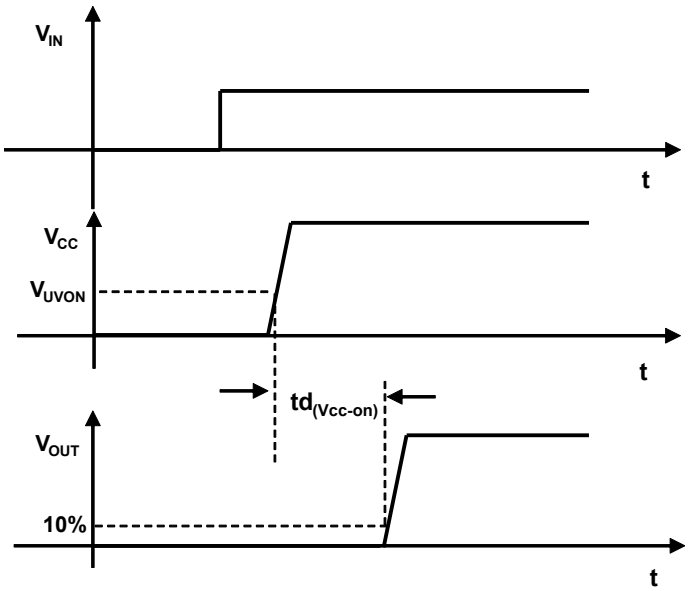


Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.2			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
I_{IN}	Input current	V_{CC} = V_{IN} = 36 V			200	µA
		V_{CC} = V_{IN} = 60 V			550	

Table 8. Protection and diagnostic

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} active clamp		I_{CC} = 10 mA	65.5	68.5	71.5	V
V_{demag}	Demagnetization voltage		I_{OUT} = 0.5 A; load =1 mH	V_{CC}-71.5	V_{CC}-68.5	V_{CC}-65.5	
V_{OLoff}	Open load (off-state) or short to V_{CC} detection threshold			2		4	
t_{BKT}	Open load blanking time					200	µs
V_{DIAG}	Voltage drop on DIAG		I_{DIAG} = 4 mA			1	V
I_{DIAG}	DIAG pin leakage current		VCC ≤ 36 V			110	µA
			36 V < VCC ≤ 60 V			180	
I_{PK}	Output current limitation activation threshold	IPS161HF	VCC ≤ 24 V, RLOAD ≤ 10 mΩ	1.3		2.1	A
		IPS160HF		3.0		4.6	
I_{LIM}	Output current limitation	IPS161HF		0.7		1.7	
		IPS160HF		2.5		4.2	
t_{coff}	Cut-off current delay time		Programmable by the external capacitor on CoD pin. Cut-off is disabled when CoD pin is connected to GND through 1 kΩ resistor. T_J< T_{JSD}	$50xC_{COD}$[nf] ± 35%(1)			µs
t_{res}	Output stage restart delay time		T_J< T_{JSD}	$32xt_{COFF}$[µs] ±40%			
T_{JSD}	Junction temperature shutdown			150	170	190	°C
T_{JHYST}	Junction temperature thermal hysteresis				15		

1. *The formula is guaranteed in the range 10 nF ≤ C_{COD} ≤ 100 nF.*

5 Output logic

Table 9. Output stage truth table

Operation	IN	OUT	DIAG
Normal	L	L	H
	H	H	H
Cut-off	L	L	L
	H	L	L
Overtemperature	L	L	L
	H	L	L
Open load	L	H(1)	L (1)
	H	H	H
UVLO	X	L	X
	X	L	X

1. *External pull-up resistor is used*

6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ($V_{UV(off)}$). Normal operation restarts after V_{CC} exceeds the turn-on threshold ($V_{UV(on)}$). Turn-on and turn-off thresholds are defined in Table 4. Supply.

6.2 Overtemperature

The output stage turns off when its internal junction temperature (T_J) exceeds the shutdown threshold T_{JSD}. Normal operation restarts when T_J comes back below the reset threshold (T_{JSD} - T_{JHYST}), see Table 8. Protection and diagnostic. The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is signaled on the DIAG pin.

6.3 Cut-off

The IC can limit the output current at the power stage by its embedded output current limitation circuit.

This circuit continuously monitor the output current and, when load is increasing, at the triggering of its activation threshold (Ipk) it starts limiting to ILIM limitation level: while current limitation is active the IC enters an high dissipation status.

The IC implements the cut-off feature which limits the duration of the current limitation condition.

The duration of the current limitation condition (T_{coff}) can be set by a capacitor (C_{CoD}) placed between CoD and GND pins. The design rule for C_{CoD} is:

$t_{coff[us]}$ ±35% = 50 x $C_{cod[nF]}$

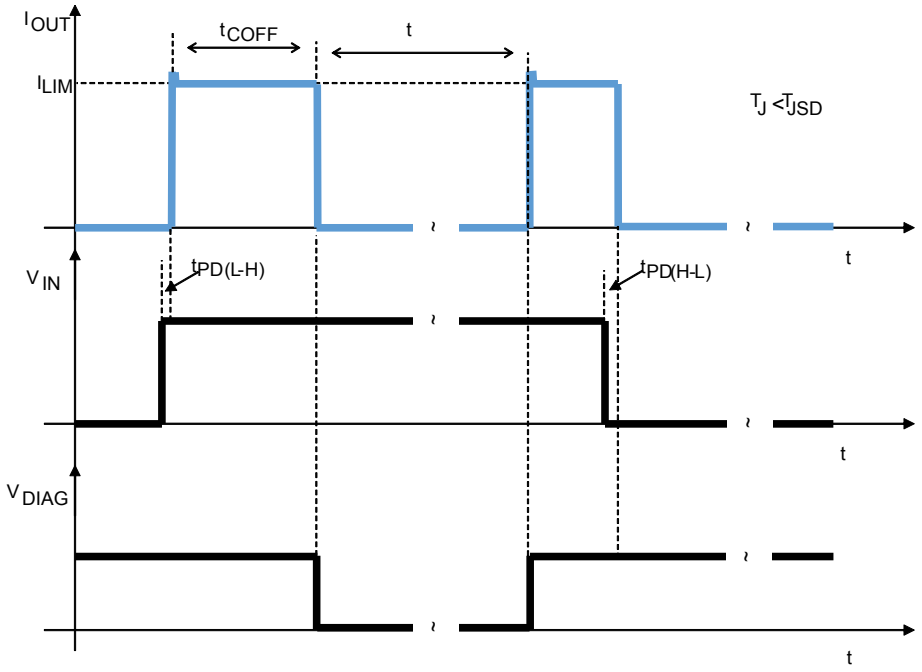
The ±35% drift is guaranteed in the range of 10 nF < C_{cod} < 100 nF; lower capacitance than 10 nF can be used.

If I_{LIM} threshold is triggered, the output stage remains in the current limitation condition (I_{OUT} = I_{LIM}) no longer than t_{COFF}. If t_{COFF} elapses, the output stage turns off and restarts after the t_{RES} restart time.

Thermal shutdown protection has higher priority than cut-off:

- IC is forced off if T_{JSD} is triggered before t_{COFF} elapses
- if T_{JSD} is triggered, IC is maintained off even after the t_{RES} has elapsed and until the T_J falls below T_{JSD}-T_{JHYST}

Figure 6. **Current limitation and cut-off**



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time t_{RES}, the same behavior is signaled on DIAG pin.

The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 1 kΩ resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

In case of low ambient temperature conditions (T_{AMB} < -20 °C) and high supply voltage (V_{CC} > 36 V), the cut-off function requires activation in order to avoid damaging the IC.

The following table shows the suggested cut-off delay for different operating voltages.

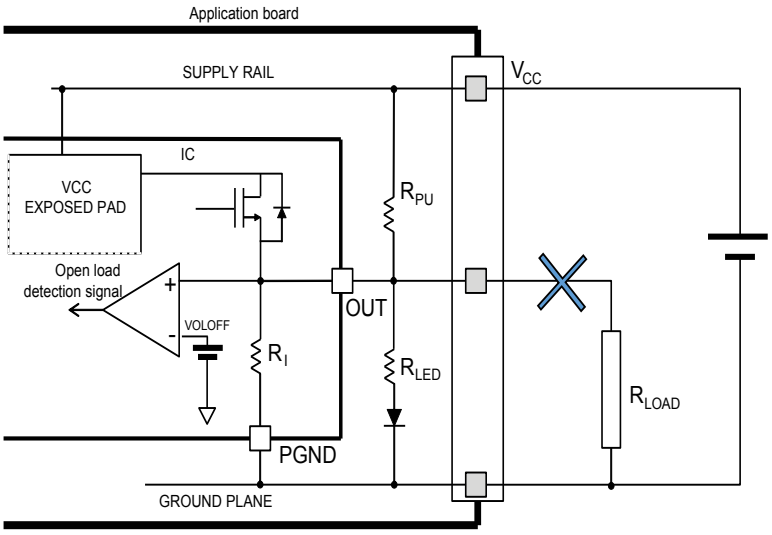
Table 10. **Minimum cut-off delay for T_{AMB} less than -20 °C**

V_{CC} [V]	Cut-off delay [µs]	Cut-off capacitance [nF]
36-48	100	2.2
48-60	50	1

6.4 Open load in off-state

The IC provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor (R_{PU}) between OUT and VCC pins.

Figure 7. Open load off-state



In case of wire break and during the OFF state (IN = low), the output voltage V_{OUT} rises according to the partitioning between the external pull-up resistor and the internal impedance of the IC (130 kΩ < R_I < 360 kΩ).

The effect of the LED (if any) on the output pin has to be considered as well. In case of wire break and during the ON state (IN = high), the output voltage V_{OUT} is pulled up to V_{CC} by the low resistive integrated switch. If the load is not connected, in order to guarantee the correct open load signalization it must result:

$V_{OUT} > V_{OLoff(max.)}$

Referring to the circuit in Figure 7. Open load off-state:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times (I_{RI} + I_{LED} + I_{RL}) \quad (1)$$

therefore:

$$R_{PU} < \frac{V_{CC(min)} - V_{OLoff(max)}}{\left(\frac{V_{OLoff(max)}}{RI(\min)} + \frac{V_{OLoff(max)} - V_{LED}}{R_{LED}}\right)} \quad (2)$$

If the load is connected, in order to avoid any false signalization of the open load, the following condition must hold:

$V_{OUT} < V_{OLoff(min)}$

By taking into account the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times \left(\frac{V_{OUT}}{R_I} + \frac{V_{OUT} - V_{LED}}{R_{LED}} + \frac{V_{OUT}}{R_L}\right) \quad (3)$$

so:

$$R_{PU} > \frac{V_{CC(max)} - V_{OLoff(min)}}{\left(\frac{V_{OLoff(min)}}{RI(\max)} + \frac{V_{OLoff(min)} - V_{LED}}{R_{LED}} + \frac{V_{OLoff(min)}}{R_L}\right)} \quad (4)$$

The fault condition is signaled on the DIAG pin and the fault reset occurs when load is reconnected.

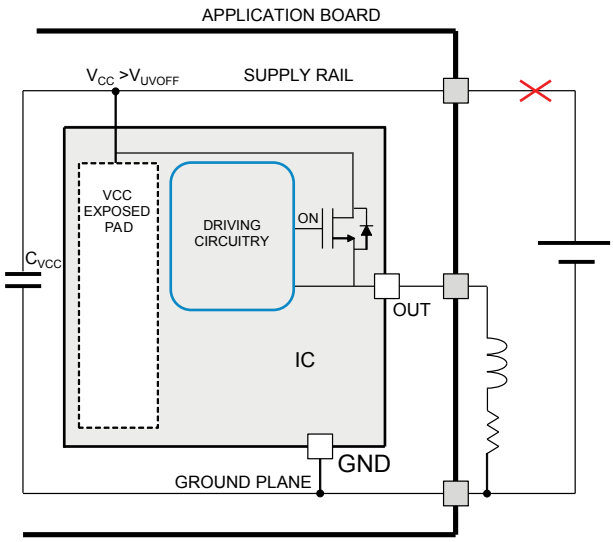
If the channel is switched on by the IN pin, the fault condition is no longer detected.

When an inductive load is driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when I_{LOAD} = 0 A and the OUT pin remains floating until next turn-on. In order to avoid false detection of the open load event when driving inductive loads, the open load signal is masked for t_{BKT}. So, the open load is reported on the DIAG pin with a delay of t_{BKT} and if the open load event is triggered for more than t_{BKT}.

6.5 VCC disconnection protection

The IC is protected despite the V_{CC} disconnection event. This event is intended as the disconnection of the V_{CC} wire from the application board, see figure below. When this condition happens, the IC continues working normally until the voltage on the V_{CC} pin is ≥ V_{UVOFF}. Once the V_{UVOFF} is triggered, the output channel is turned off independently on the input status. In case of inductive load, if the V_{CC} is disconnected while the output channel is still active, the IC allows the discharge of the energy still stored in the inductor through the integrated power switch.

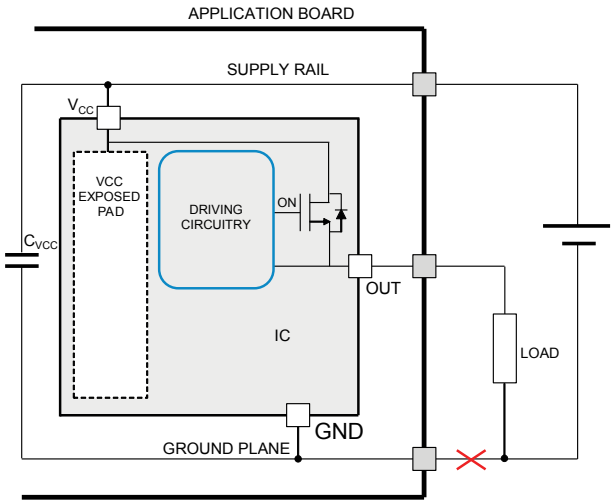
Figure 8. VCC disconnection



6.6 GND disconnection protection

GND disconnection is intended as the disconnection event of the application ground, see figure below. When this event happens, the IC continues working normally until the voltage between V_{CC} and GND pins of the IC is $\geq V_{UVOFF}$. The voltage on GND pin of the IC rises up to the supply rail voltage level. In case of GND disconnection event, a current (I_{LGND}) flows through OUT pin. Table 4. Supply shows $I_{OUT} = I_{LGND}$ for the worst case GND disconnection event where the output is shorted to ground.

Figure 9. GND disconnection



7 Active VDS clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to V_{demag}. The conduction state is modulated by internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in the IC internal switch and in the load resistance.

Figure 10. Active clamp equivalent principle schematic

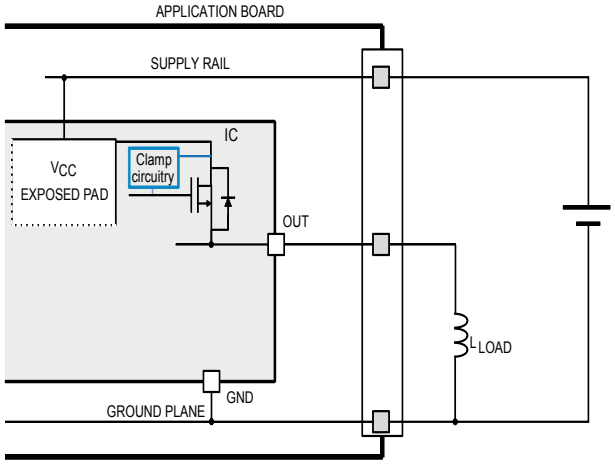
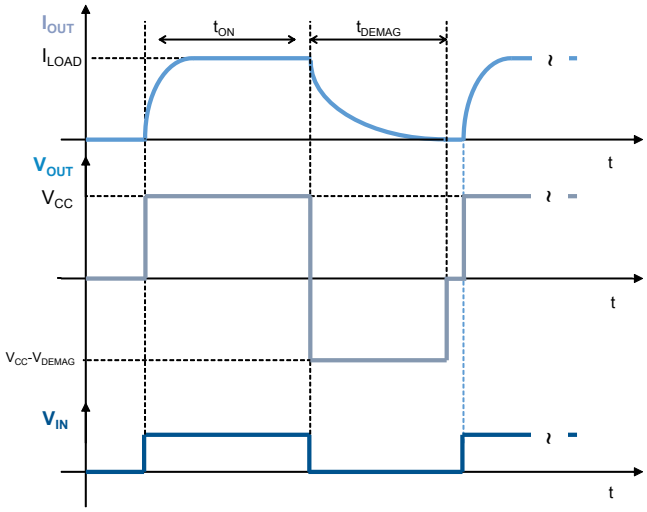
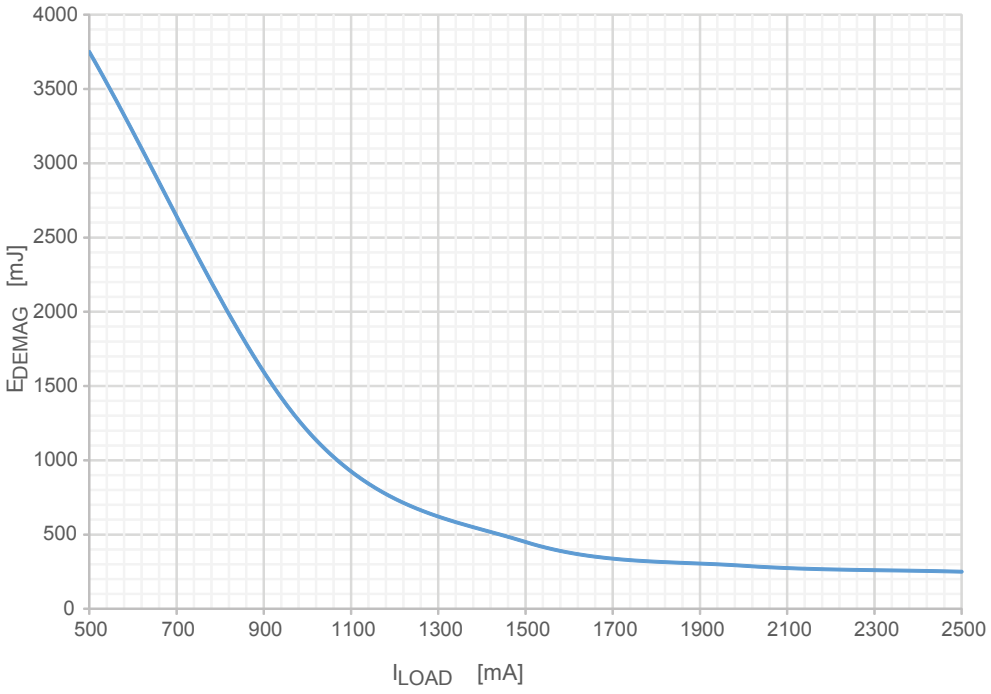


Figure 11. Fast demag waveforms



The demagnetization of inductive load causes large electrical and thermal stress on the IC. The plot below shows the maximum demagnetization energy that the IC can tolerate in a single demagnetization pulse with V_{CC} = 24 V and T_{AMB} = 125 °C. If higher demagnetization energy is required, then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 12. Typical demagnetization energy (single pulse) at V_{CC} = 24 V and T_{AMB} = 125 °C



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 PowerSSO12 package information

Figure 13. PowerSSO12 package outline

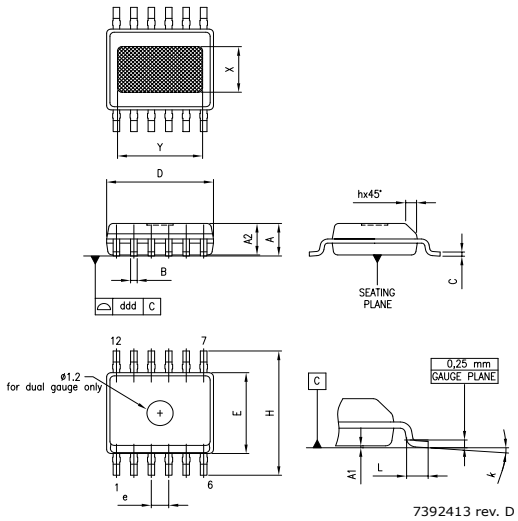


Table 11. PowerSSO12 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.55
L	0.400		1.270
k	0d		8d
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Note: Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

Figure 14. PowerSSO12 recommended footprint

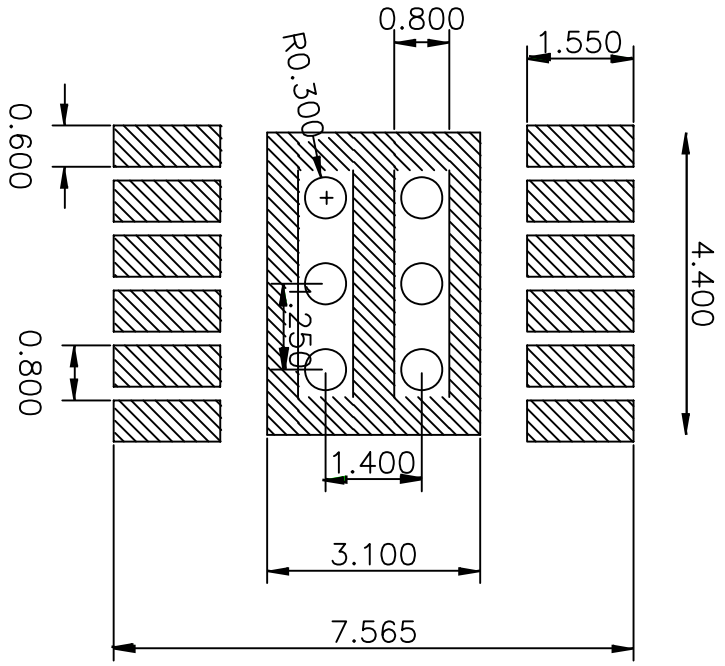
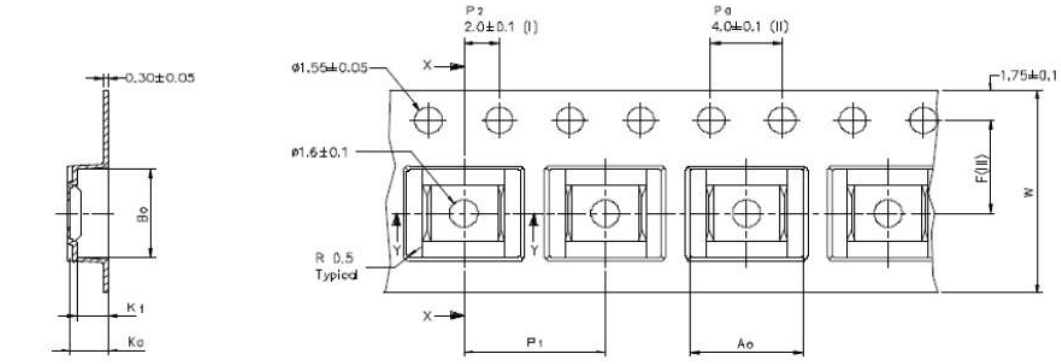
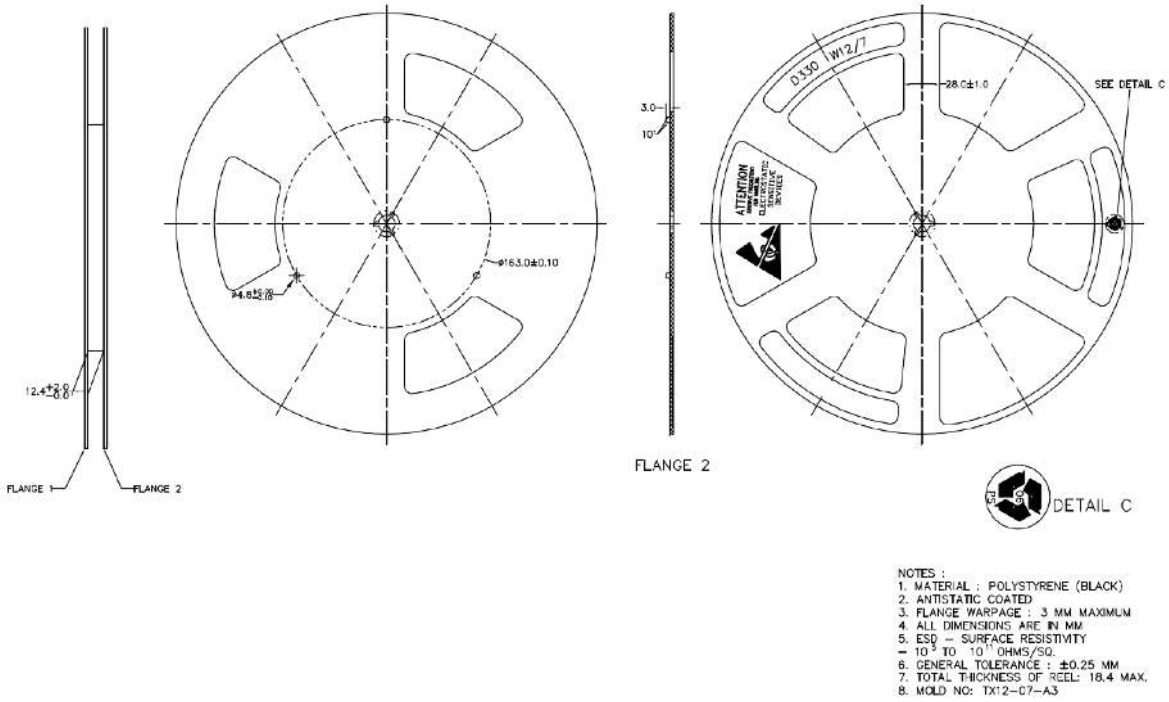


Figure 15. PowerSSO12 tape packing information [mm]



Ao	6.50 +/– 0.1
Bo	5.25 +/– 0.1
Ko	2.10 +/– 0.1
K1	1.80 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 16. PowerSS012 reel packing information [mm]



Revision history

Table 12. **Document revision history**

Date	Revision	Changes
23-Apr-2020	1	Initial release.
26-Jun-2020	2	IPS161HF RPN added to document
03-Mar-2021	3	Minor changes in Section Applications
29-Mar-2021	4	Updated I_{LGND} maximum value in Table 4
30-Jul-2021	5	Updated thermal data in Table 3 according to Jedec conditions.
06-Dec-2022	6	Filled column Max. in table Table 6. Switching (V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 48 Ω).

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