

NCP1442, NCP1443, NCP1444, NCP1445



4.0 A 280 kHz/560 kHz Boost Regulators

The NCP1442/3/4/5 products are 280 kHz/560 kHz switching regulators with a high efficiency, 4.0 A integrated switch. These parts operate over a wide input voltage range, from 2.7 V to 30 V. The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high-frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation.

Part Number	Frequency	Feedback Voltage Polarity
NCP1442	280 kHz	Positive
NCP1443	280 kHz	Negative
NCP1444	560 kHz	Positive
NCP1445	560 kHz	Negative

Features

- Pb-Free Packages are Available*
- Integrated Power Switch: 4.0 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built-in Overcurrent Protection
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Regulates Either Positive or Negative Output Voltages
- Shut Down Current: 50 μ A Maximum

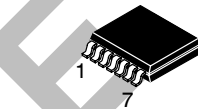
Applications

- Boost Converter
- Inverting Converter
- Distributed Power
- Portable Computers
- Battery Powered Systems

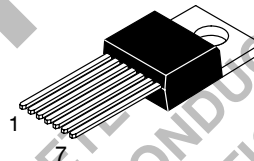
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<http://onsemi.com>

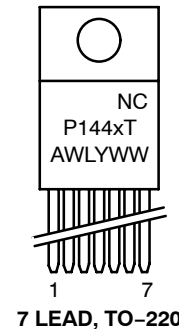
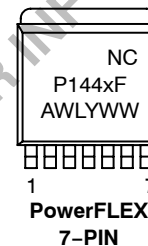


PowerFLEX™
7-PIN
F SUFFIX
CASE 936J



7 LEAD, TO-220
T SUFFIX
CASE 821P

PIN CONNECTIONS AND MARKING DIAGRAMS



Pin	NCP1442/4	NCP1443/5
1.	V _C	V _C
2.	FB	TEST
3.	TEST	NFB
4.	GND	GND
5.	V _{SW}	V _{SW}
6.	SS	SS
7.	V _{CC}	V _{CC}

x = Device Number 2, 3, 4, or 5
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

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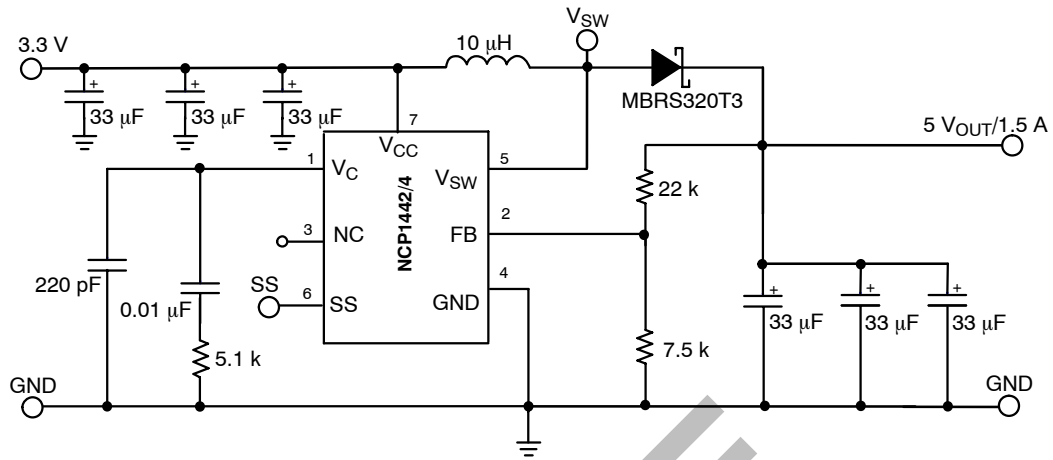


Figure 1. Application Diagram – NCP1442/4,
3.3 V to 5.0 V/1.5 A Boost Converter

MAXIMUM RATINGS

Rating	Value	Unit
Thermal Resistance Junction-to-Air, TO220-7 Version In Air (Socketed) On Cold Plate (25°C)	66.7 1.45	°C/W
Thermal Resistance Junction-to-Air, PowerFLEX on 2.1 sq. in. 1 oz.	53.8	°C/W
Junction Temperature Range, T_J	0 to +150	°C
Storage Temperature Range, $T_{STORAGE}$	-65 to +150	°C
Lead Temperature Soldering: Reflow (Note 1)	230 Peak	°C
ESD, Human Body Model	2.0	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	30 V	-0.3 V	N/A	200 mA
Shutdown/Sync	SS	30 V	-0.3 V	1.0 mA	1.0 mA
Loop Compensation	V_C	6.0 V	-0.3 V	10 mA	10 mA
Voltage Feedback Input	FB (NCP1442/4 only)	10 V	-0.3 V	1.0 mA	1.0 mA
Negative Feedback Input (Transient, 10 ms)	NFB (NCP1443/5 only)	10 V	-10 V	1.0 mA	1.0 mA
Test Pin	Test	6.0 V	-0.3 V	1.0 mA	1.0 mA
Ground	GND	0.3 V	-0.3 V	9.0 A	10 mA
Switch Input	V_{SW}	40 V	-0.3 V	10 mA	9.0 A

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ELECTRICAL CHARACTERISTICS (2.7 V < V_{CC} < 30 V; 0°C < T_A < 85°C; 0°C < T_J < 125°C; For all NCP1442/3/4/5 specifications unless otherwise stated.) (See Note 2)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Positive and Negative Error Amplifiers					
FB Reference Voltage (NCP1442/4 only)	V _C tied to FB; measure at FB	1.246	1.276	1.300	V
NFB Reference Voltage (NCP1443/5 only)	V _C = 1.25 V	-2.60	-2.475	-2.40	V
FB Input Current (NCP1442/4 only)	FB = V _{REF}	-1.0	0.1	1.0	μA
NFB Input Current (NCP1443/5 only)	NFB = NV _{REF}	-16	-10	-5.0	μA
FB Reference Voltage Line Regulation (NCP1442/4 only)	V _C = FB	-0.03	0.01	0.03	%/V
NFB Reference Voltage Line Regulation (NCP1443/5 only)	V _C = 1.25 V	-0.05	0.01	0.05	%/V
Positive Error Amp Transconductance	I _{V_C} = ±25 μA	300	550	800	μMho
Negative Error Amp Transconductance	I _{V_C} = ±5.0 μA	115	160	225	μMho
Positive Error Amp Gain	(Note 3)	200	500	-	V/V
Negative Error Amp Gain	(Note 3)	100	180	320	V/V
V _C Source Current	FB = 1.0 V or NFB = -1.9 V, V _C = 1.25 V	-90	-50	-25	μA
V _C Sink Current	FB = 1.5 V or NFB = -3.1 V, V _C = 1.25 V	200	460	1500	μA
V _C High Clamp Voltage	FB = 1.0 V or NFB = -1.9 V; V _C sources 25 μA	1.5	1.64	1.9	V
V _C Low Clamp Voltage	FB = 1.5 V or NFB = -3.1 V, V _C sinks 25 μA	0.30	0.47	0.70	V
V _C Threshold	Reduce V _C from 1.5 V until switching stops	0.70	1.05	1.30	V
Oscillator					
Base Operating Frequency	NCP1442/3, FB = 1.0 V or NFB = -1.9 V	240	280	320	kHz
Reduced Operating Frequency	NCP1442/3, FB = 0 V or NFB = 0 V	30	68	120	kHz
Maximum Duty Cycle	NCP1442/3	90	96	-	%
Base Operating Frequency	NCP1444/5, FB = 1.0 V or NFB = -1.9 V	480	560	640	kHz
Reduced Operating Frequency	NCP1444/5, FB = 0 V or NFB = 0 V	60	120	160	kHz
Maximum Duty Cycle	NCP1444/5	82	92	-	%
FB Frequency Shift Threshold	Frequency drops to reduced operating frequency	0.36	0.40	0.44	V
NFB Frequency Shift Threshold	Frequency drops to reduced operating frequency	-0.80	-0.68	-0.50	V
Sync/Shutdown					
Sync Range	NCP1442/3	-	500	-	kHz
Sync Range	NCP1444/5	-	1000	-	kHz
Sync Pulse Transition Threshold	Rise time = 20 ns	-	2.5	-	V
SS Bias Current	SS = 0 V	-10	-1.0	-	μA
	SS = 3.0 V	-	0.2	4.0	μA
Shutdown Threshold	-	0.50	0.85	1.20	V
Shutdown Delay	2.7 V ≤ V _{CC} ≤ 12 V	12	100	500	μs
	12 V < V _{CC} ≤ 30 V	12	40	400	μs

2. For the FR4 suffix parts, production testing is performed at 25°C and 85°C; limits at 0°C are guaranteed by design.

3. Guaranteed by design, not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (continued) ($2.7\text{ V} < V_{CC} < 30\text{ V}$; $0^\circ\text{C} < T_A < 85^\circ\text{C}$; $0^\circ\text{C} < T_J < 125^\circ\text{C}$; For all NCP1442/3/4/5 specifications unless otherwise stated.) (See Note 2)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Power Switch					
Switch Saturation Voltage	$I_{SWITCH} = 4.0\text{ A}$	–	0.6	1.0	V
	$I_{SWITCH} = 10\text{ mA}$, $2.7\text{ V} < V_{CC} < 12\text{ V}$	–	0.14	0.5	V
	$12\text{ V} < V_{CC} < 30\text{ V}$	–	0.9	0.4	V
Switch Current Limit	50% duty cycle (Note 4)	5.0	6.0	8.0	A
	80% duty cycle (Note 4)	4.0	–	–	A
Minimum Pulse Width	$FB = 0\text{ V}$ or $NFB = 0\text{ V}$, $I_{SW} = 4.0\text{ A}$ (Note 4)	200	250	300	ns
Switch Transconductance, $\Delta I_{CC} / \Delta I_{SW}$	$2.7\text{ V} \leq V_{CC} \leq 12\text{ V}$, $10\text{ mA} \leq I_{SW} \leq 4.0\text{ A}$	–	8.0	30	mA/A
	$12\text{ V} < V_{CC} \leq 30\text{ V}$, $10\text{ mA} \leq I_{SW} \leq 4.0\text{ A}$	–	10	50	
Switch Leakage	$V_{SW} = 40\text{ V}$, $V_{CC} = 0\text{ V}$	–	2.0	20	μA

General

Operating Current	$I_{SW} = 0$	–	15	27	mA
Shutdown Mode Current	$V_C < 0.8\text{ V}$, $SS = 0\text{ V}$, $2.7\text{ V} \leq V_{CC} \leq 12\text{ V}$	–	16	60	μA
	$V_C < 0.8\text{ V}$, $SS = 0\text{ V}$, $12\text{ V} \leq V_{CC} \leq 30\text{ V}$	–	25	60	
Minimum Operation Input Voltage	V_{SW} switching, maximum $I_{SW} = 10\text{ mA}$	–	2.2	2.6	V
Thermal Shutdown	(Note 4)	150	180	210	$^\circ\text{C}$
Thermal Hysteresis	(Note 4)	–	25	–	$^\circ\text{C}$

4. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Package Pin Number	Pin Symbol	Function
1	V_C	Loop compensation pin. The V_C pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 2.
2 (NCP1442/4 only)	FB	Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V. When the voltage at this pin falls below 0.4 V, chip switching frequency reduces to 20% of the nominal frequency.
2 (NCP1443/5 only) 3 (NCP1442/4 only)	Test	These pins are connected to internal test logic and should either be left floating or tied to ground. Connection to a voltage between 2.0 V and 6.0 V shuts down the internal oscillator and leaves the power switch running.
3 (NCP1443/5 only)	NFB	Negative feedback pin. This pin senses a negative output voltage and is referenced to -2.475 V . When the voltage at this pin goes above -0.65 V , chip switching frequency reduces to 20% of the nominal frequency.
4	GND	Ground pin. This pin provides a ground for the controller circuitry and the internal power switch. This pin is internally connected to the metal pad of the package to provide an additional ground connection as well as an effective means of dissipating heat.
5	V_{SW}	High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V. To minimize radiation, use a trace as short as practical.
6	SS	Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation.
7	V_{CC}	Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to GND.

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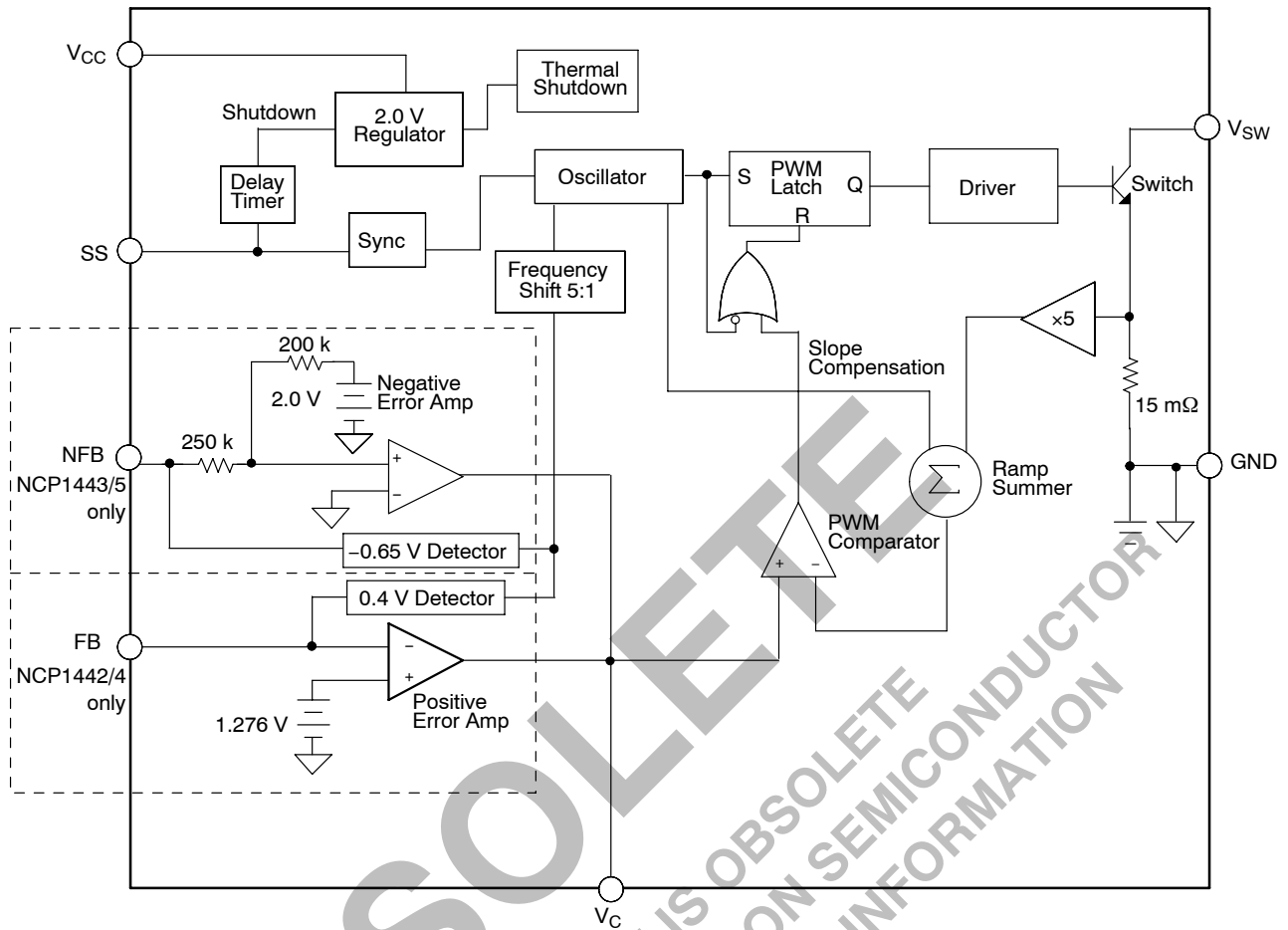


Figure 2. Block Diagram

OBSOLETE

THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

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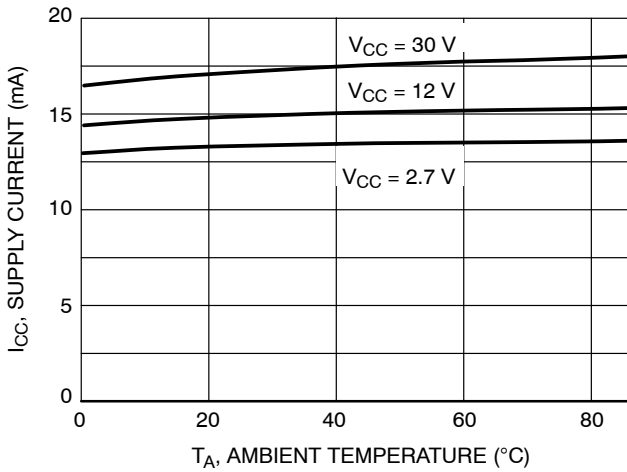


Figure 3. Supply Current versus Temperature

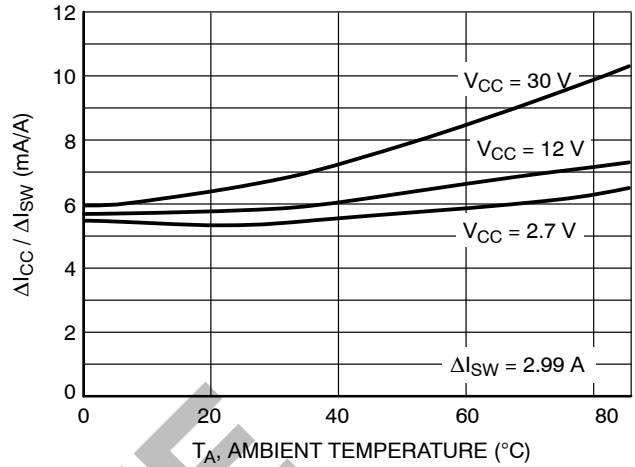


Figure 4. $\Delta I_{CC} / \Delta I_{SW}$ versus Temperature

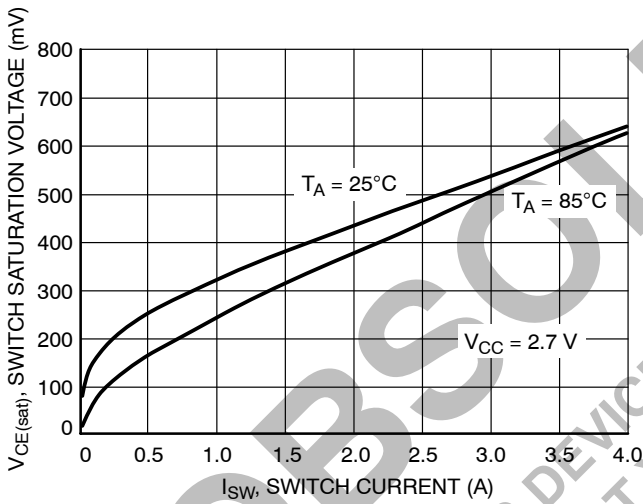


Figure 5. Switch Saturation Voltage versus Switch Current

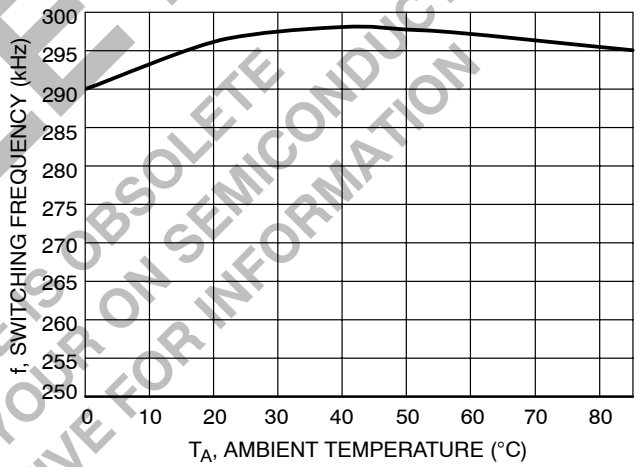


Figure 6. Switching Frequency versus Temperature (NCP1442/3 Only)

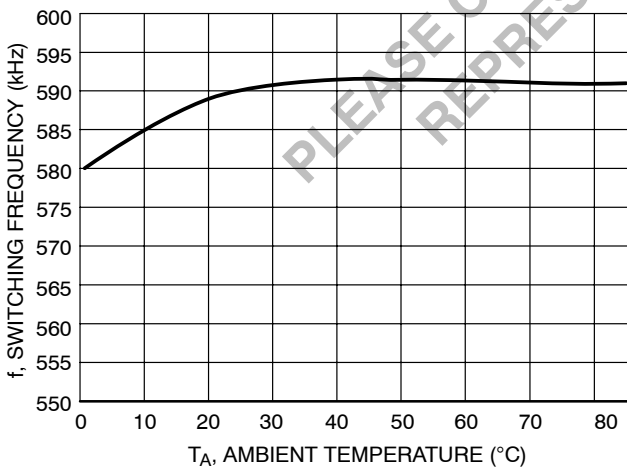


Figure 7. Switching Frequency versus Temperature (NCP1444/5 Only)

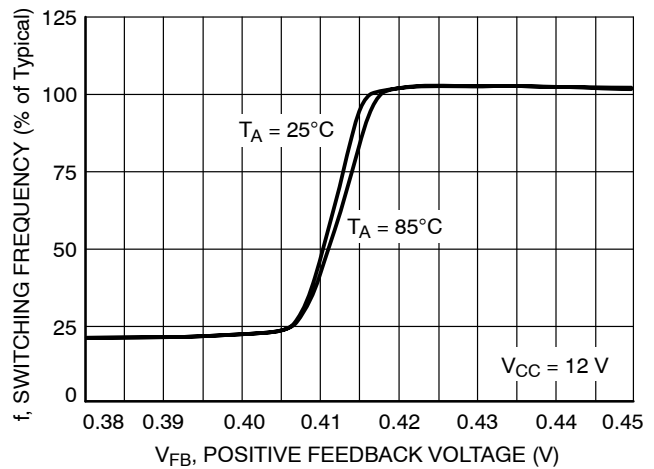


Figure 8. Switching Frequency versus Positive Feedback Voltage

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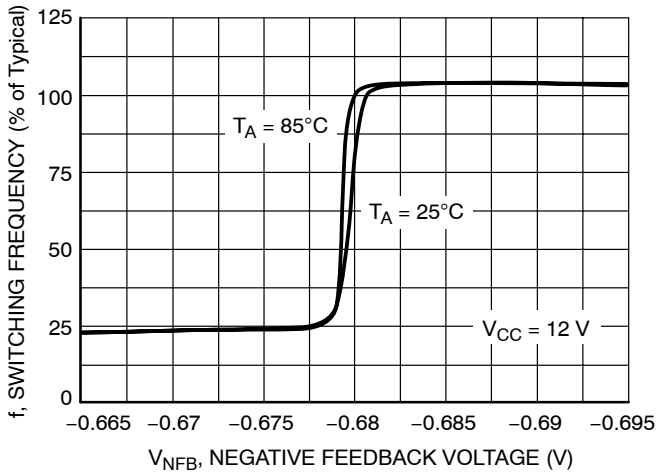


Figure 9. Switching Frequency versus Negative Feedback Voltage

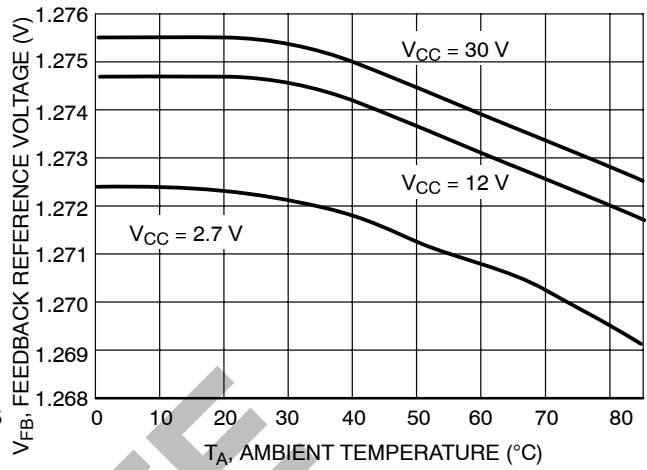


Figure 10. Feedback Reference Voltage versus Temperature (NCP1442/4 Only)

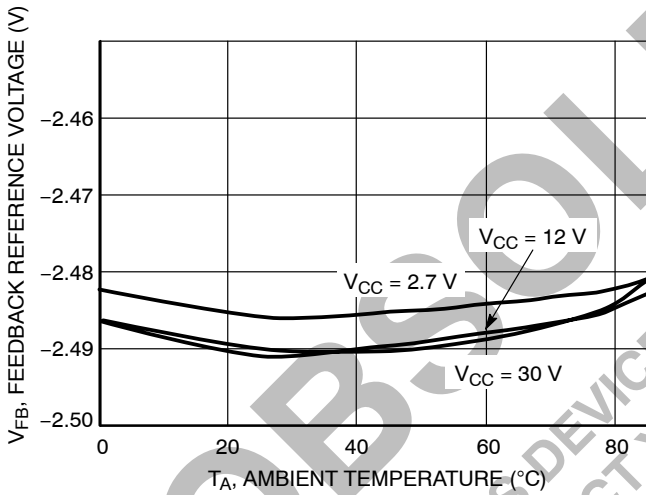


Figure 11. Feedback Reference Voltage versus Temperature (NCP1443/5 Only)

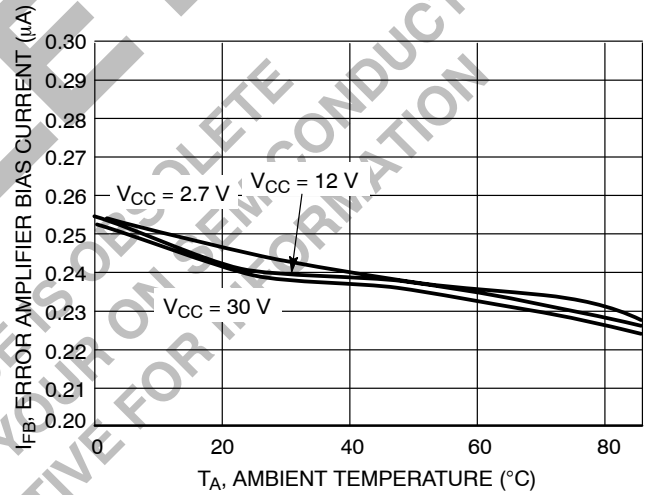


Figure 12. Error Amplifier Bias Current versus Temperature (NCP1442/3 Only)

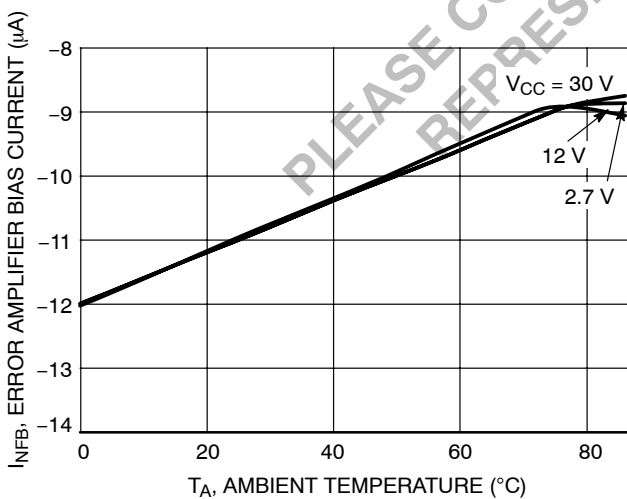


Figure 13. Error Amplifier Bias Current versus Temperature (NCP1443/5 Only)

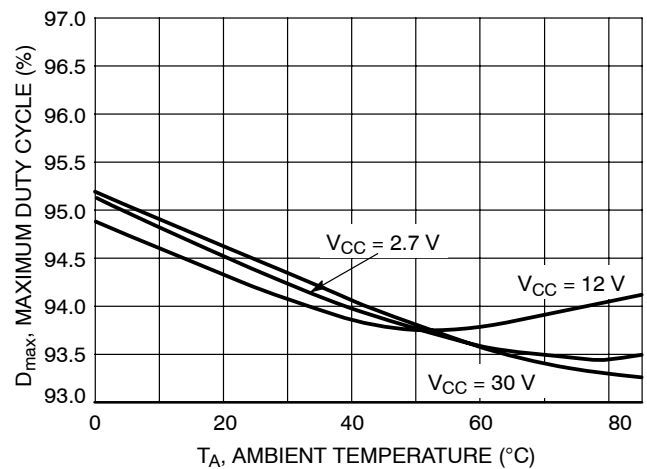


Figure 14. Maximum Duty Cycle versus Temperature

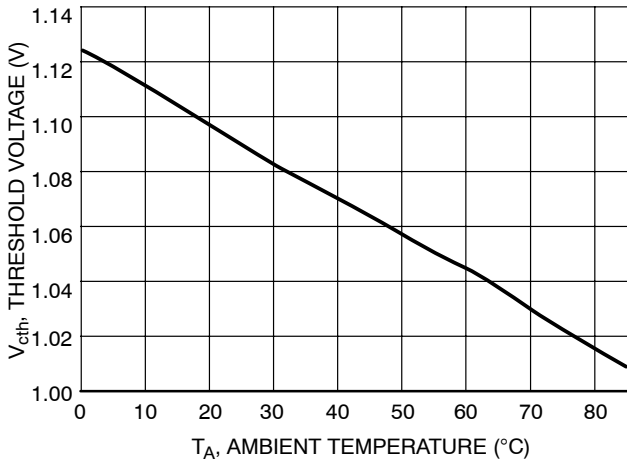


Figure 15. V_C Threshold Voltage versus Temperature

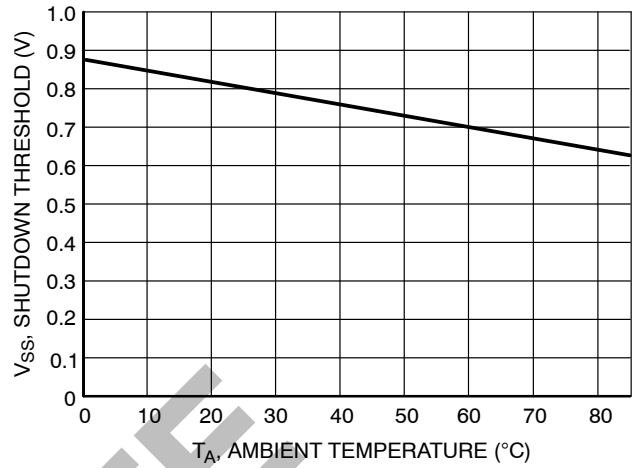


Figure 16. Shutdown Threshold versus Temperature

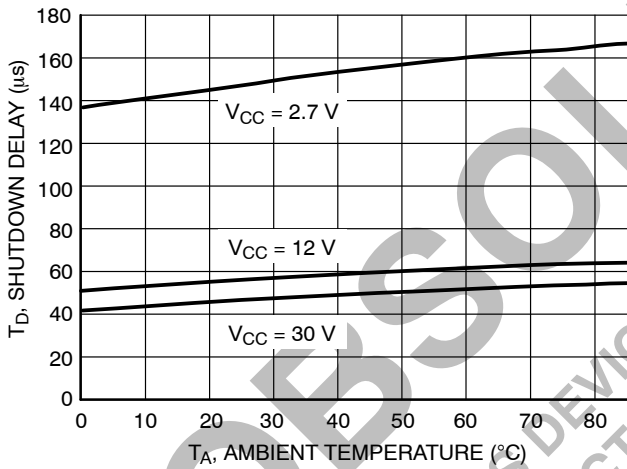


Figure 17. Shutdown Delay versus Temperature (NCP1442)

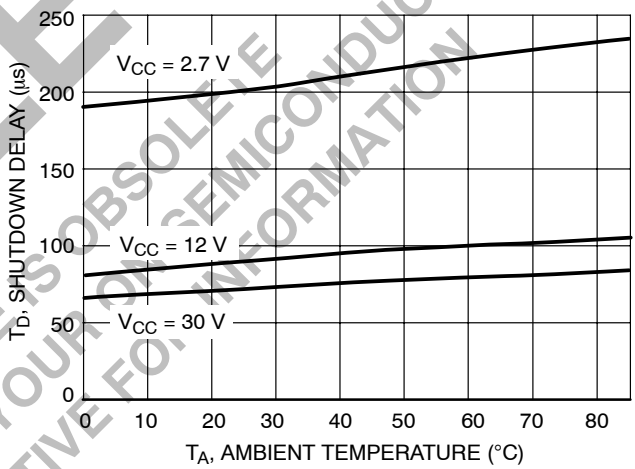


Figure 18. Shutdown Delay versus Temperature (NCP1444)

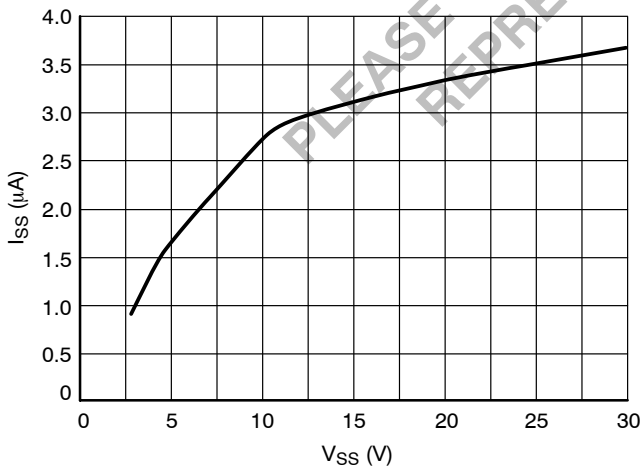


Figure 19. I_{SS} versus V_{SS}

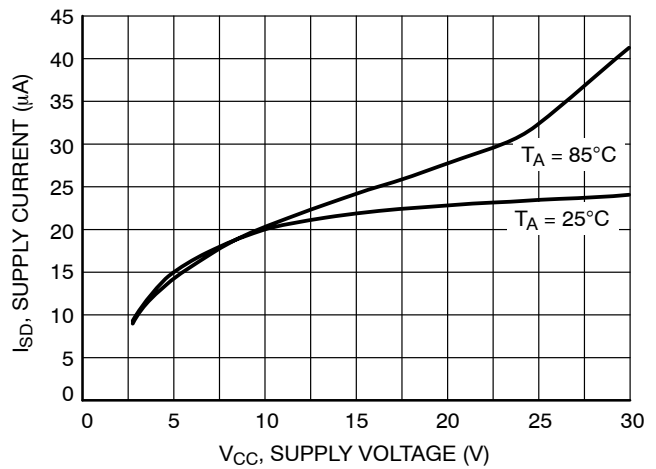


Figure 20. Supply Current versus Supply Voltage During Shutdown

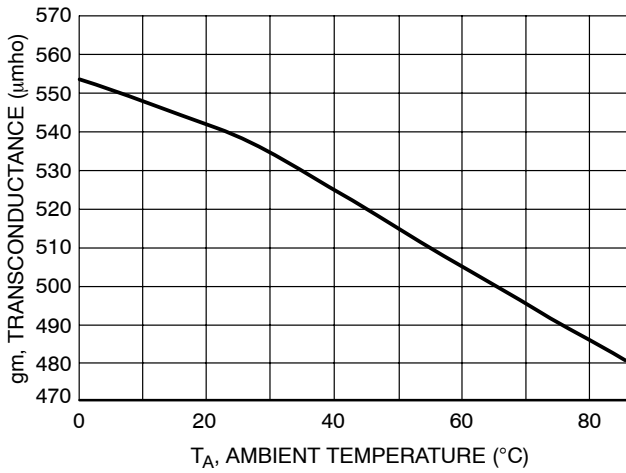


Figure 21. Error Amplifier Transconductance versus Temperature

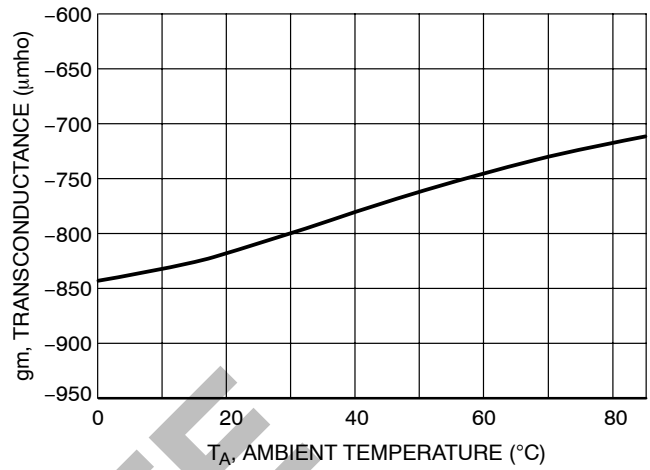


Figure 22. Negative Error Amplifier Transconductance versus Temperature

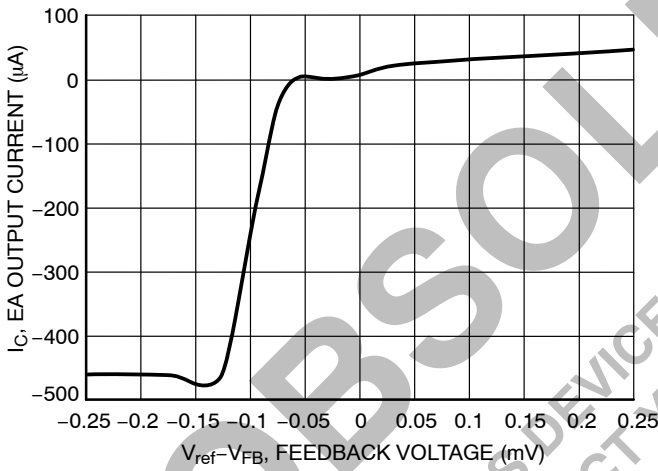


Figure 23. Error Amplifier Output Current versus Positive Feedback Voltage

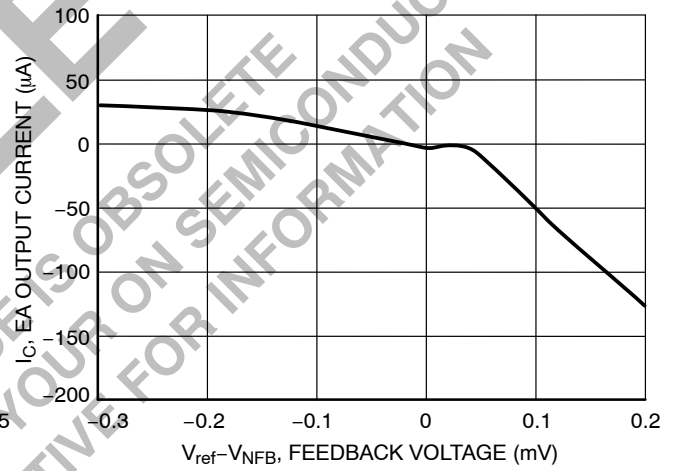


Figure 24. Error Amplifier Output Current versus Negative Feedback Voltage

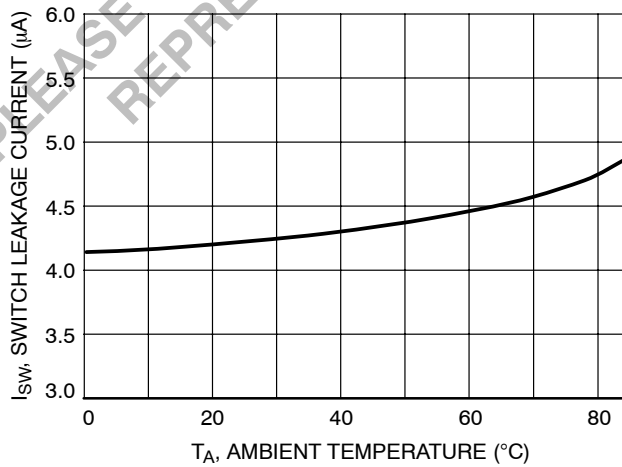


Figure 25. Switch Leakage Current versus Temperature

APPLICATIONS INFORMATION

THEORY OF OPERATION

Current Mode Control

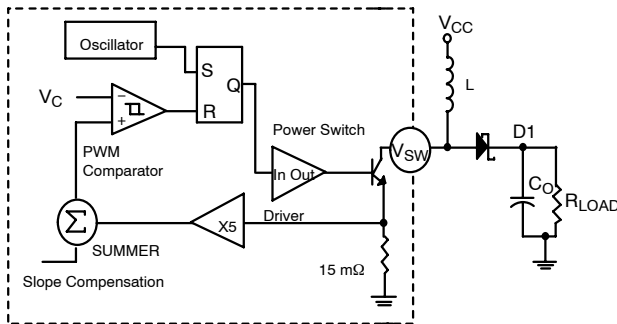


Figure 26. Current Mode Control Scheme

The NCP144X family incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on-time of the power switch. The oscillator is used as a fixed-frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain-bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over 50%. The NCP144X family solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown

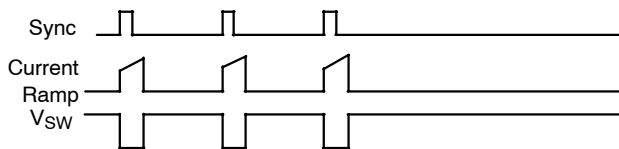


Figure 27. Timing Diagram of Sync and Shutdown

The oscillator is trimmed to guarantee frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz (NCP1442/3) or 560 kHz (NCP1444/5), as shown in Figure 26. The power switch is turned off by the output of the PWM Comparator.

A TTL-compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 27, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when either the NFB or FB pins trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on-time is limited by the PWM comparator minimum pulse width. Extra switch off-time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier

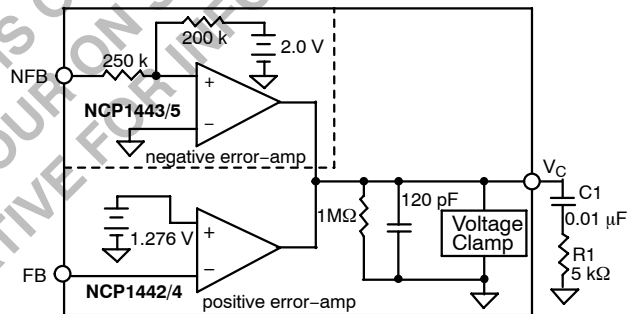


Figure 28. Error Amplifier Equivalent Circuit

For NCP1443/5, the NFB pin is internally referenced to -2.475 V with approximately a 250 kΩ input impedance. For NCP1442/4, the FB pin is directly connected to the inverting input of the positive error amplifier, whose non-inverting input is fed by the 1.276 V reference. Both amplifiers are transconductance amplifiers with a high output impedance of approximately 1.0 MΩ, as shown in Figure 28. The Vc pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the Vc pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the Vc pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (15 mΩ total) to the GND pin. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 4.0 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector (V_{SW} pin). The saturation voltage of the switch is typically less than 1.0 V to minimize power dissipation.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

output through the inductor and diode. Once V_{CC} reaches approximately 1.5 V, the internal power switch briefly turns on. This is a part of the NCP144X's normal operation. The turn-on of the power switch accounts for the initial current swing.

When the V_C pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the V_{SW} pin. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on-time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull-on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

COMPONENT SELECTION

Frequency Compensation

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 30, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 31.

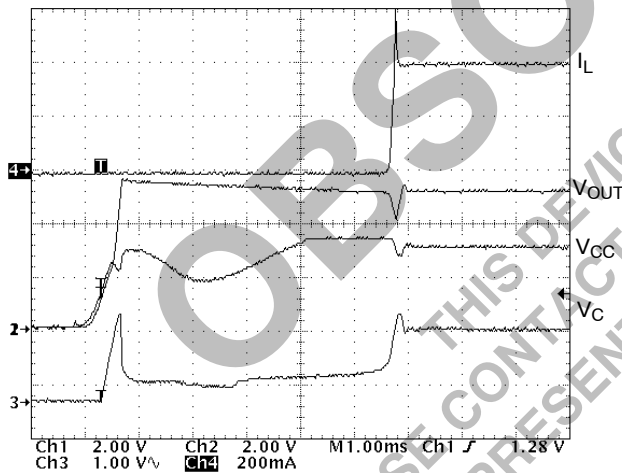


Figure 29. Startup Waveforms of Circuit Shown in the Application Diagram. Load = 400 mA.

The NCP144X can be activated by either connecting the V_{CC} pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 29 are measured in the boost converter demonstrated in the Block Diagram (Figure 2). Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the V_{CC} voltage is below the minimum supply voltage, the V_{SW} pin is in high impedance. Therefore, current conducts directly from the input power source to the

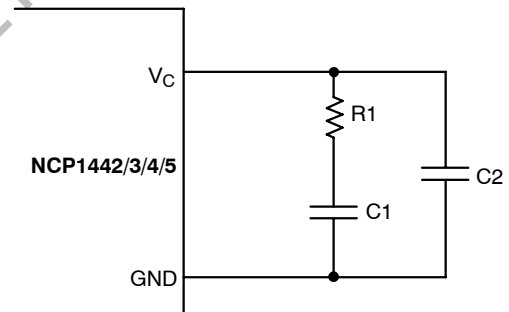


Figure 30. A Typical Compensation Network

The high DC gain in Figure 31 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

$$\text{Gain}_{DC} = G_M \times R_O$$

where:

- G_M = error amplifier transconductance;
- R_O = error amplifier output resistance ≈ 1.0 MΩ.

The low frequency pole, f_{P1} , is determined by the error amplifier output resistance and C1 as:

$$f_{P1} = \frac{1}{2\pi C1 R_{O}}$$

The first zero generated by C1 and R1 is:

$$f_{Z1} = \frac{1}{2\pi C1 R1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

$$f_P = \frac{1}{2\pi C_O R_{LOAD}}$$

where:

C_O = equivalent output capacitance of the error amplifier $\approx 120\text{pF}$;

R_{LOAD} = load resistance.

The high frequency pole, f_{P2} , can be placed at the output filter's ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

$$f_{P2} = \frac{1}{2\pi C2 R1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a -20 dB per decade slope, until unity-gain crossover. The crossover frequency should be selected at the midpoint between f_{Z1} and f_{P2} where the phase margin is maximized.

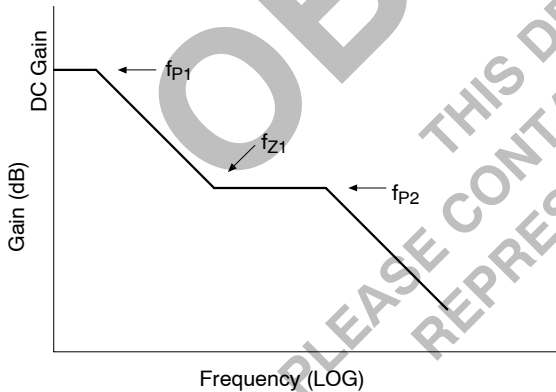


Figure 31. Bode Plot of the Compensation Network Shown in Figure 30

Negative Voltage Feedback

Since the negative error amplifier has finite input impedance as shown in Figure 32, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

$$-V_{OUT} = \left(\frac{-2.475 (R1 + R2)}{R2} \right) - 10 \mu\text{A} \times R1$$

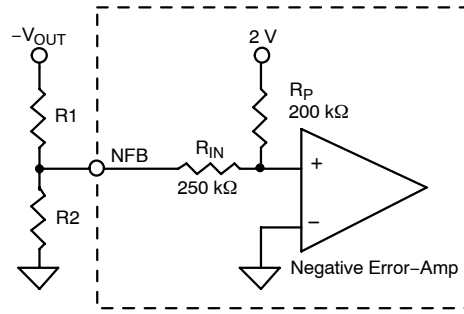


Figure 32. Negative Error Amplifier and NFB Pin

It is shown that if R1 is less than 10 k, the deviation from the design target will be less than 0.1 V. If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output V_{OFFSET} varies in the range of:

$$\begin{aligned} & \left(\frac{-0.05 (R1 + R2)}{R2} \right) - (15 \mu\text{A} \times R1) \leq V_{OFFSET} \\ & \leq \left(\frac{0.05 (R1 + R2)}{R2} \right) - (5 \mu\text{A} \times R1) \end{aligned}$$

V_{SW} Voltage Limit

In the boost topology, V_{SW} pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes:

$$V_{SW(MAX)} = V_{OUT(MAX)} + V_F$$

where:

V_F = output diode forward voltage.

In the flyback topology, peak V_{SW} voltage is governed by:

$$V_{SW(MAX)} = V_{CC(MAX)} + (V_{OUT} + V_F) \times N$$

where:

N = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the V_{SW} and GND pins. To prevent the voltage at the V_{SW} pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the V_{SW} pin and ground.

Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain (V_{OUT}/V_{CC}), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is:

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

where:

$f = 280 \text{ kHz}$ for NCP1442/3 and 560 kHz for NCP1444/5.

The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

Input Capacitor Selection

In boost circuits, the inductor becomes part of the input filter, as shown in Figure 34. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 33. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 33, the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the V_{CC} ripple. In most applications, input capacitors in the range of $10 \mu\text{F}$ to $100 \mu\text{F}$ with an ESR less than 0.3Ω work well up to a full 4.0 A switch current.

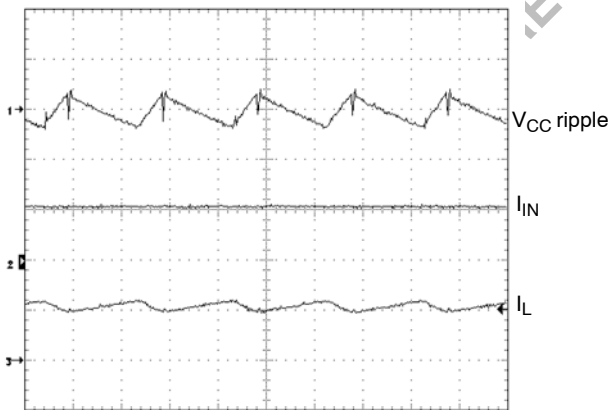


Figure 33. Boost Input Voltage and Current Ripple Waveforms

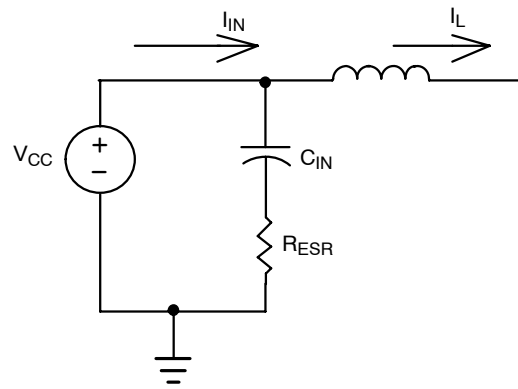


Figure 34. Boost Circuit Effective Input Filter

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than $20 \mu\text{F}$ with low ESR is required. To reduce the noise generated by the inductor, insert a $1.0 \mu\text{F}$ ceramic capacitor between V_{CC} and ground as close as possible to the chip.

Output Capacitor Selection

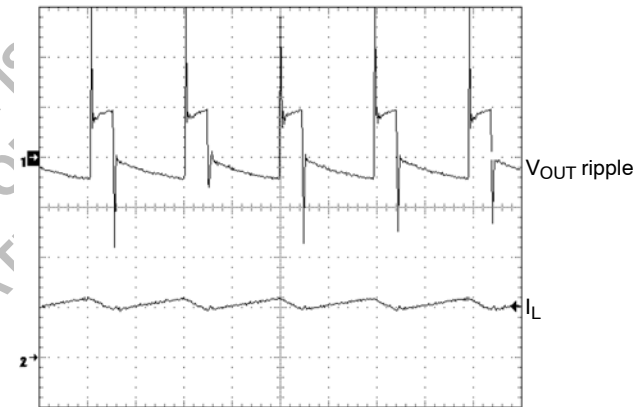


Figure 35. Typical Output Voltage Ripple

By examining the waveforms shown in Figure 35, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, I_L flows into the output capacitor causing an instant $\Delta V = I_{IN} \times \text{ESR}$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and increases the output voltage gradually. When the power switch is turned on, I_L is shunted to ground and I_{OUT} discharges the output capacitor. When the I_L ripple is small enough, I_L can be treated as a constant and is equal to input

current I_{IN} . Summing up, the output voltage peak-peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1 - D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of V_{CC} , V_{OUT} and I_{OUT} for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2(1 - D) + (I_{OUT})^2(D)} = I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

Reducing the Current Limit

In some applications, the designer may prefer a lower limit on the switch current than 4.0 A. An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the V_C pin can be evaluated with the equation:

$$V_C = I_{SW}R_E A_V$$

where:

$R_E = .015 \Omega$, the value of the internal emitter resistor;

$A_V = 5.0 \text{ V/V}$, the gain of the current sense amplifier.

Since R_E and A_V cannot be changed by the end user, the only available method for limiting switch current below 4.0A is to clamp the V_C pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in Figure 36, clamps the V_C voltage to a diode drop above the voltage on resistor R3. Unfortunately, such a simple circuit is not generally acceptable if V_{IN} is loosely regulated.

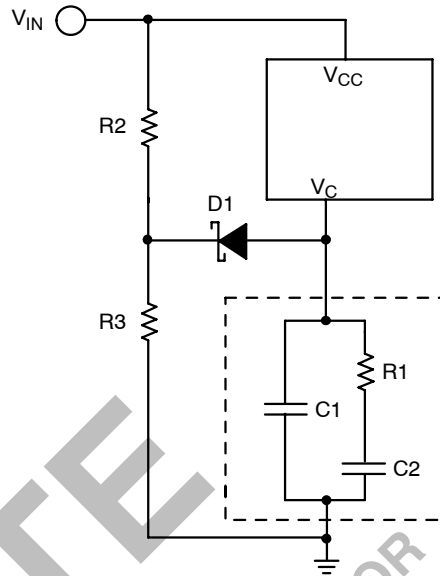


Figure 36. Current Limiting using a Diode Clamp

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 37.

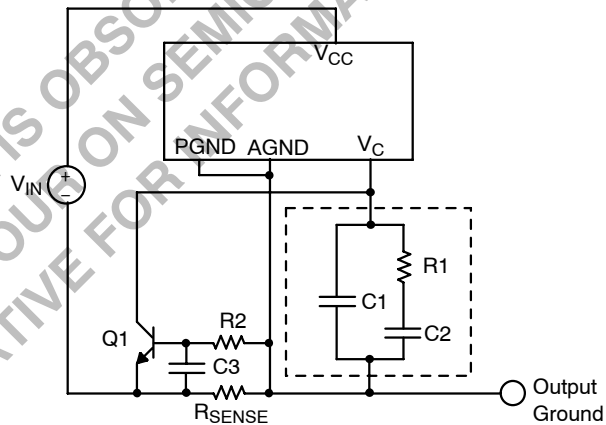


Figure 37. Current Limiting using a Current Sense Resistor

The switch current is limited to:

$$I_{SWITCH(PEAK)} = \frac{V_{BE(Q1)}}{R_{SENSE}}$$

where:

$V_{BE(Q1)}$ = the base-emitter voltage drop of Q1, typically 0.65 V.

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, R_{SENSE} , results in a considerable power loss which increases with the duty cycle. Resistor R2 and capacitor C3 form a low-pass filter to remove noise.

Subharmonic Oscillation

Subharmonic oscillation (SHM) is a problem found in current-mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high-frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal “slope compensation” to prevent any duty cycle instability from carrying through to the next switching cycle. In the NCP144X family, slope compensation is added during the entire switch on-time, typically in the amount of 180 mA/μs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is *more* slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 38, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is “tacked on” to the compensation network.

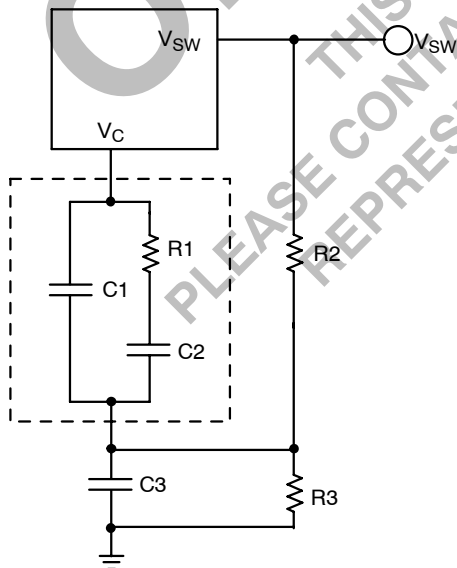


Figure 38. Technique for Increasing Slope Compensation

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the V_{SW} pin. In normal operation, V_{SW} looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating V_{SW} in the boost and flyback topologies are given in the section “ V_{SW} Voltage Limit.” The voltage on V_{SW} charges capacitor C3 when the switch is off, causing the voltage at the V_C pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the V_C pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = V_{SW} \left(\frac{R_3}{R_2 + R_3} \right) \left(1 - e^{-\frac{(1-D)}{R_3 C_3 f_{SW}}} \right) \left(\frac{f_{SW}}{(1-D) R_E A_V} \right)$$

where:

- $\Delta I/\Delta T$ = the amount of slope compensation added (A/s);
- V_{SW} = the voltage at the switch node when the transistor is turned off (V);
- f_{SW} = the switching frequency, typically 280 kHz (NCP1442/3) or 560 kHz (NCP1444/5) (Hz);
- D = the duty cycle;
- $R_E = 0.015 \Omega$, the value of the internal emitter resistor;
- $A_V = 5.0 \text{ V/V}$, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/μs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from V_{SW} . Additionally, to ensure that the control loop stability is *improved*, the time constant formed by the additional components should be chosen such that:

$$R_3 C_3 < \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a trade-off between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

Soft-Start

Through the addition of an external circuit, a soft-start function can be added to the NCP1442/3/4/5 family of components. Soft-start circuitry prevents the V_C pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 39, requires a minimum number of components and allows the soft-start circuitry to activate any time the SS pin is used to restart the converter.

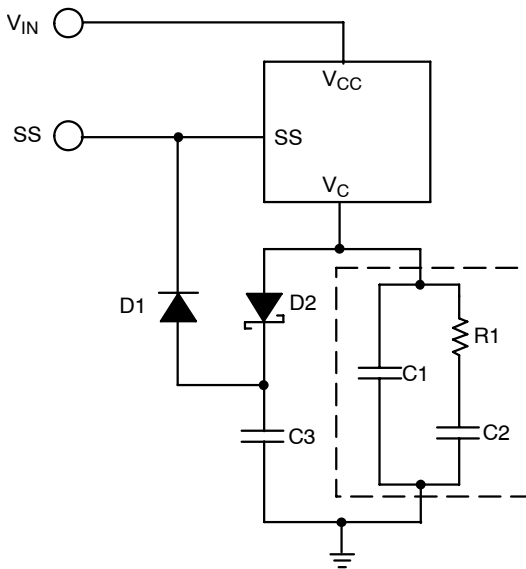


Figure 39. Soft-Start

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the V_C pin starts to come up, charging capacitor C3 through Schottky diode D2, clamping the voltage at the V_C pin such that switching begins when V_C reaches the V_C threshold, typically 1.05 V (refer to graphs for detail over temperature).

$$V_C = V_F(D2) + V_{C3}$$

Therefore, C3 slows the startup of the circuit by limiting the voltage on the V_C pin. The soft-start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to V_{IN}.

Calculating Junction Temperature

To ensure safe operation of the NCP1442/3/4/5, the designer must calculate the on-chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C ±30°. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the NCP144X:

- biasing of internal control circuitry, P_{BIAS}
- switch driver, P_{DRIVER}
- switch saturation, P_{SAT}

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, I_Q, due to this circuitry is 5.5 mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that I_Q is strongly dependent on input voltage, V_{IN}, and the ambient temperature, T_A. Then:

$$P_{BIAS} = V_{IN} I_Q$$

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the V_{IN} pin, in addition to the control circuitry current. The base drive current is listed in the specifications as ΔI_{CC}/ΔI_{SW}, or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate:

$$P_{DRIVER} = V_{IN} I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D$$

where:

I_{SW} = the current through the switch;

D = the duty cycle or percentage of switch on-time.

I_{SW} and D are dependent on the type of converter. In a boost converter,

$$I_{SW(AVG)} \cong I_{LOAD} \times D \times \frac{1}{\text{efficiency}}$$

$$D \cong \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In a flyback converter,

$$I_{SW(AVG)} \cong \frac{V_{OUT} I_{LOAD}}{V_{IN}} \times \frac{1}{\text{efficiency}}$$

$$D \cong \frac{V_{OUT}}{V_{OUT} + \frac{n_s}{n_p} V_{IN}}$$

where:

n_s = number of turns in the transformer secondary winding.

n_p = number of turns in the transformer primary winding.

The switch saturation voltage, V_{(CE)SAT}, is the last major source of on-chip power loss. V_{(CE)SAT} is the collector-emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for V_{(CE)SAT} can be obtained from the specifications or from the graphs, as “Switch Saturation Voltage.” Thus,

$$P_{SAT} \cong V_{(CE)SAT} I_{SW} \times D$$

Finally, the total on-chip power losses are:

$$P_D = P_{BIAS} + P_{DRIVER} + P_{SAT}$$

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers' data sheets as θ_{JA} , or junction-to-ambient thermal resistance. The on-chip junction temperature can be calculated if θ_{JA} , the air temperature near the surface of the IC, and the on-chip power dissipation are known.

$$T_J = T_A + (P_D \theta_{JA})$$

where:

T_J = IC or FET junction temperature ($^{\circ}\text{C}$);

T_A = ambient temperature ($^{\circ}\text{C}$);

P_D = power dissipated by part in question (W);

θ_{JA} = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$).

For ON Semiconductor components, the value for θ_{JA} can be found on page 19 of the datasheet, under "Package Thermal Data." Note that this value is different for every package style and every manufacturer. For the NCP144X, θ_{JA} varies between 10–50 $^{\circ}\text{C}/\text{W}$, depending upon the size of the copper pad to which the IC is mounted.

Once the designer has calculated T_J , the question of whether the NCP144X can be used in an application is settled. If T_J exceeds 150 $^{\circ}\text{C}$, the absolute maximum allowable junction temperature, the NCP144X is not suitable for that application.

If T_J approaches 150 $^{\circ}\text{C}$, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected to reduce the switch current. Increasing the airflow across the

surface of the chip might be considered to reduce T_A . A copper "landing pad" can be connected to ground – designers are referred to ON Semiconductor applications note SR006 for more information on properly sizing a copper area.

Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on-chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on-chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

NCP1442, NCP1443, NCP1444, NCP1445

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
NCP1442FR4	0°C < T _A < 85°C	7 Lead PowerFLEX Short-Leaded	2000 Tape & Reel
NCP1442FR4G		7 Lead PowerFLEX Short-Leaded (Pb-Free)	2000 Tape & Reel
NCP1442T		7 Lead TO-220 (Straight Lead)	50 Units/Rail
NCP1443FR4		7 Lead PowerFLEX Short-Leaded	2000 Tape & Reel
NCP1443FR4G		7 Lead PowerFLEX Short-Leaded (Pb-Free)	2000 Tape & Reel
NCP1443T		7 Lead TO-220 (Straight Lead)	50 Units/Rail
NCP1444FR4		7 Lead PowerFLEX Short-Leaded	2000 Tape & Reel
NCP1444T		7 Lead TO-220 (Straight Lead)	50 Units/Rail
NCP1445FR4		7 Lead PowerFLEX Short-Leaded	2000 Tape & Reel
NCP1445T		7 Lead TO-220 (Straight Lead)	50 Units/Rail

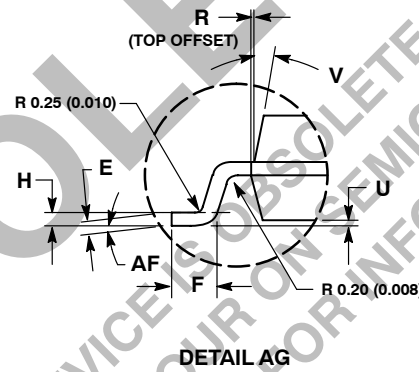
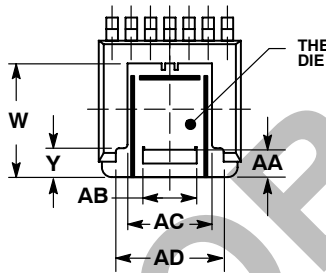
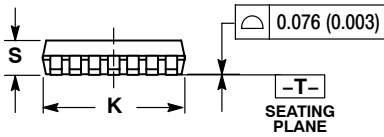
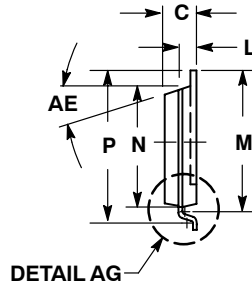
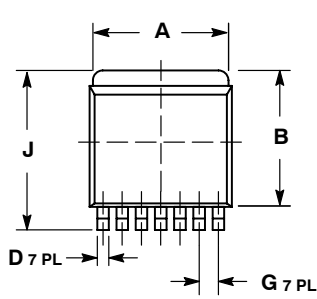
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

OBSOLETE
 THIS DEVICE IS OBSOLETE
 PLEASE CONTACT YOUR ON SEMICONDUCTOR
 REPRESENTATIVE FOR INFORMATION

NCP1442, NCP1443, NCP1444, NCP1445

PACKAGE DIMENSIONS

PowerFLEX
7-PIN
F SUFFIX
CASE 936J-01
ISSUE O



NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.350	0.360	8.89	9.14
B	0.350	0.360	8.89	9.14
C	0.070	0.080	1.78	2.03
D	0.026	0.030	0.66	0.76
E	0.005	0.015	0.13	0.38
F	0.031	0.041	0.79	1.04
G	0.050 BSC		1.270 BSC	
H	0.008	0.012	0.199	0.301
J	0.410	0.420	10.41	10.67
K	0.365	0.375	9.27	9.53
L	0.040 REF		1.02 REF	
M	0.361	0.367	9.16	9.31
N	0.310	0.320	7.87	8.13
P	0.394	0.400	10.00	10.16
R	0.002		0.05	
S	0.070	0.080	1.78	2.03
U	0.001	0.005	0.03	0.13
V	12°		12°	
W	0.296 REF		7.52 REF	
Y	0.075 REF		1.91 REF	
AA	0.071 REF		1.81 REF	
AB	0.140 REF		3.56 REF	
AC	0.220 REF		5.58 REF	
AD	0.281 REF		7.14 REF	
AE	12°		12°	
AF	3°	6°	3°	6°

PACKAGE THERMAL DATA

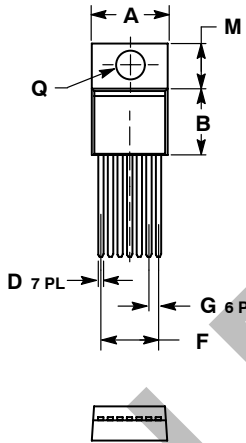
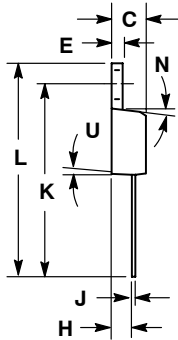
Parameter		PowerFLEX 7-PIN	Unit
$R_{\theta JC}$	Typical	1.0-4.0	°C/W
$R_{\theta JA}$	Typical	10-50*	°C/W

*Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

NCP1442, NCP1443, NCP1444, NCP1445

PACKAGE DIMENSIONS

7 LEAD TO-220
T SUFFIX
CASE 821P-03
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 821P-01 AND -02 OBSOLETE. NEW STANDARD IS 821P-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.54	0.390	0.415
B	8.23	9.40	0.324	0.370
C	4.19	4.83	0.165	0.190
D	0.66	0.81	0.026	0.032
E	0.89	1.40	0.035	0.055
F	7.62 TYP		0.3 TYP	
G	1.22	1.32	0.048	0.052
H	2.16	2.92	0.085	0.115
J	0.30	0.64	0.012	0.025
K	24.00	26.54	0.945	1.045
L	26.67	29.03	1.050	1.143
M	6.10	6.48	0.240	0.255
N	7°		7°	
Q	3.53	3.96	0.139	0.156
U	4°		6°	

OBSOLETE

THIS DEVICE IS OBSOLETE. PLEASE CONTACT YOUR ON SEMICONDUCTOR REPRESENTATIVE FOR INFORMATION.

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