2.4A, 36V, 100kHz Asynchronous Step-Down Converter with Load Line Compensation

General Description

The RT6266 is a high-efficiency, monolithic asynchronous step-down DC/DC converter that can deliver up to 2.4A output current from a 7.5V to 36V input supply. The RT6266's current mode architecture with internal compensation is optimized for 5V car charger application over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT6266 also provides output over voltage protection output under voltage protection and thermal shutdown protection. The low current (<3μA) shutdown mode provides output disconnect, enabling easy power management in battery-powered systems. The RT6266 is available in a SOP-8 (Exposed Pad) package.

Ordering Information

RT6266□□
- Package Type
  SP: SOP-8(Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **±2% High Accuracy Feedback Voltage**
- **7.5V to 36V Input Voltage Range**
- **2.4A Continuous Output Current (2.7A Peak)**
- **CC/CV Mode Control**
- **Adjustable Load Line Compensation**
- **Short Circuit Protection**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation : 100kHz**
- **Programmable Output Current Limit**
- **110mΩ Internal Power MOSFET Switch**
- **Lowe EMI signature**
- **Up to 95% Efficiency**
- **Cycle-by-Cycle Over Current Protection**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Thermal Shutdown Protection**

Applications

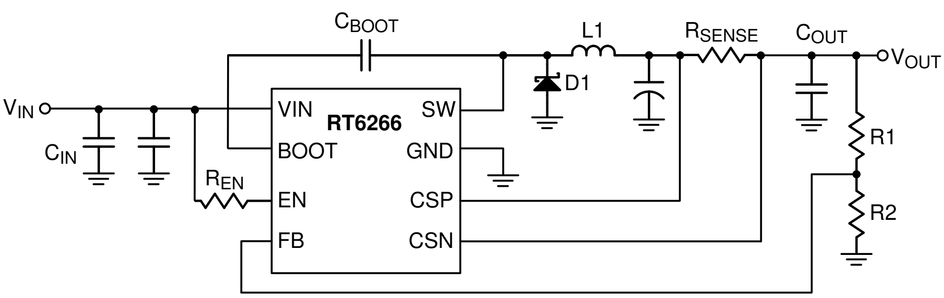
- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers
- DC/DC Converters with Current Limited

Marking Information

RT6266 GSPYMDNN •

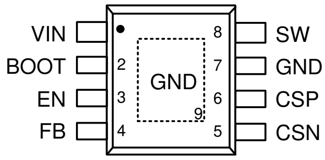
RT6266GSP : Product Number
YMDNN : Date Code

Simplified Application Circuit



Pin Configurations

(TOP VIEW)

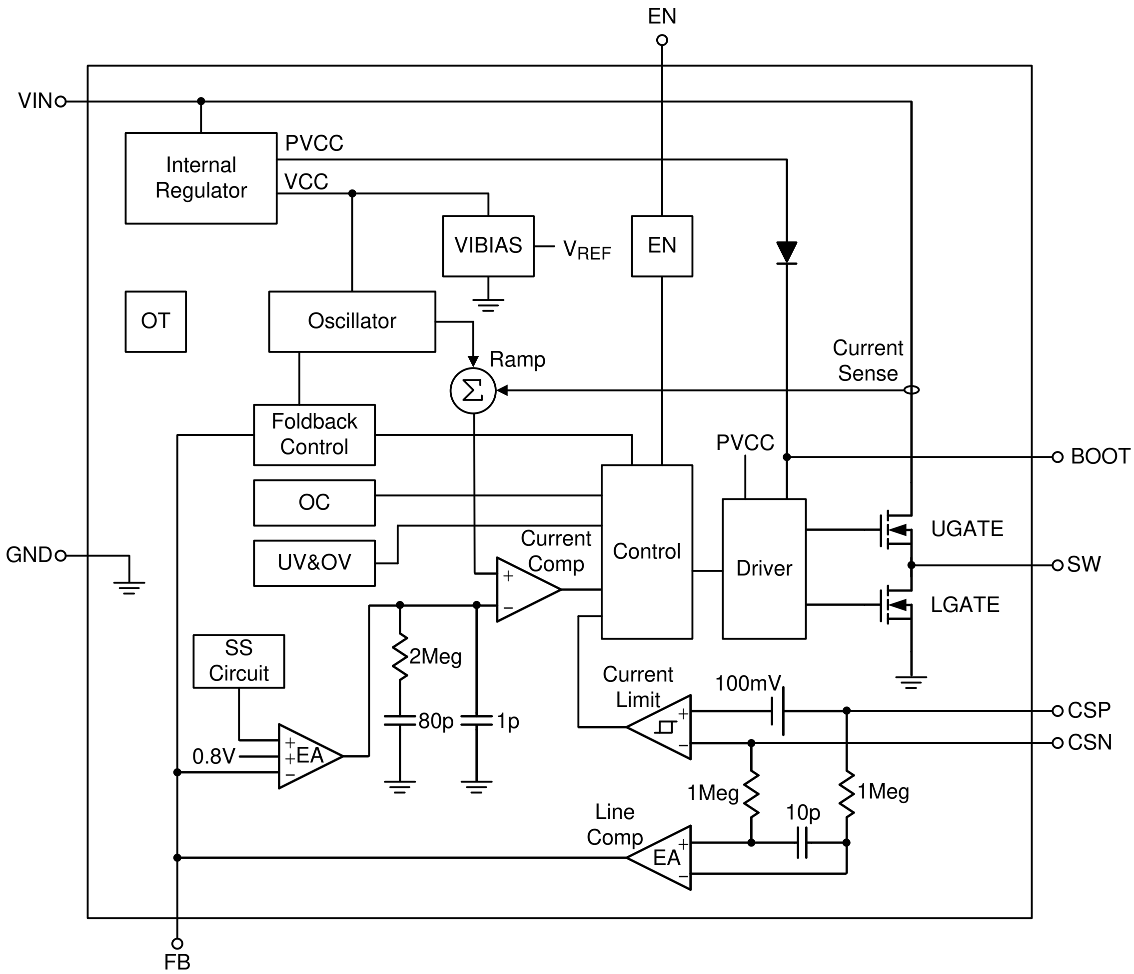


SOP-8 (Exposed Pad)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Input Supply Voltage, 7.5V to 36V. Must bypass with a suitably large ceramic capacitor.
2	BOOT	Bootstrap for High-Side Gate Driver. Connect 0.1μF or greater ceramic capacitor from BOOT to SW pins.
3	EN	Enable Input Pin. A logic high enables the converter; a logic low forces the RT6266 into shutdown mode reducing the supply current to less than 3μA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
4	FB	Feedback Input Pin. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an external resistive voltage divider. For an adjustable output, an external resistive divider is connected to this pin.
5	CSN	Current Sense Negative Input. It is used for load current limiting and load line drop compensation.
6	CSP	Current Sense Positive Input. It is used for load current limiting and load line drop compensation.
7, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. (Connect the exposed pad to Pin 7)
8	SW	Switch Output -- Connect to external L-C filter and Schottky diode.

Function Block Diagram



Operation

The RT6266 is a constant frequency, current mode asynchronous step-down converter with CC and CV control. In normal operation, the high side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the N-MOSFET is turned off, the inductor current conducts through the external diode.

Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal (V_{FB}) with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the error amplifier's output voltage then rises to allow higher inductor current to match the load current.

Oscillator

The internal oscillator runs at fixed frequency 100kHz. In short circuit condition, the frequency is reduced to 20kHz for low power consumption.

Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high side gate driver.

Enable

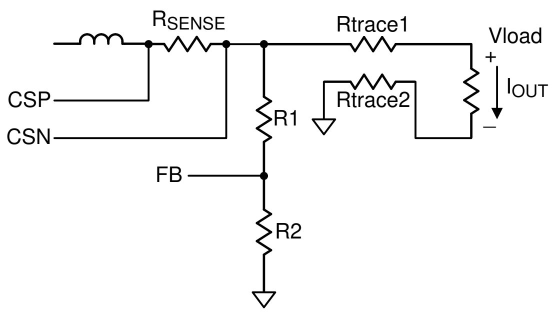
The converter is turned on when the EN pin is higher than 1.4V and turned off when the EN pin is lower than 0.4V. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.

Soft-Start (SS)

An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 3.5ms.

Output Line Drop Compensation

If the trace from RT6266 output terminator to the load is too long, there will be a voltage drop on the long trace which is variable with load current. RT6266 is capable of compensating the output voltage drop to keep a constant voltage at load, whatever the load current is. The output voltage is compensated by feeding a current to the top feedback resistance R1. The load line compensation gain can be programmed according to R_{SENSE} and Rtrace values.



$$I_{OUT} \times R_{SENSE} \times 20\mu \times R1 = I_{OUT} \times Rtrace$$

$$R1 = \frac{Rtrace}{20\mu \times R_{SENSE}}$$

Output Over Voltage Protection (OVP)

The V_{OUT} Over Voltage is sensed by CSN pin. When CSN > 5.8V, the high side switch will be turned off immediately. When CSN < 5.5V, the driver will recovers to normal state automatically.

External Current Limit Protection

The external current limit is set by outside resistance (R_{SENSE}). The average current is limited according to the following equation :

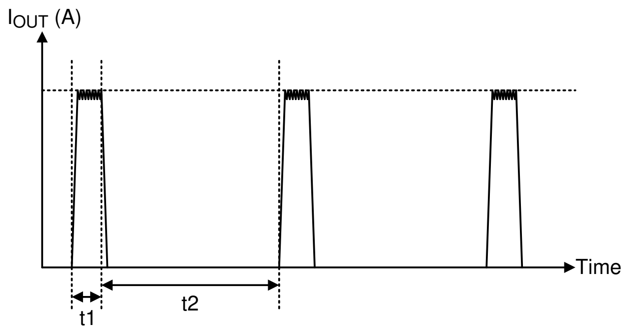
$$\text{Average Current\_Limit (A)} = \frac{100mV}{R_{SENSE}}$$

Internal Current Limit Protection

When the external R_{SENSE} is too small and the external peak current is higher than 4.4A, the high-side switch will turn off immediately and then turn at the next clock cycle. The inductor's peak current will be limited at 4.4A by internal current limit.

Output Short-Circuit Protection

When V_{OUT} is short (V_{FB} < 0.3V), the short-circuit protection function can be started that restart the regulator cycle by cycle. The cycle time is set by the driver internally. The internal current limit time is t1 and the regulator off time is t2. The typically t1 = 5ms, t2 = 200ms.



Under Voltage Lockout (UVLO)

To avoid mis-operation at low input voltage, when input voltage falls below 6.2V, and under voltage lockout is induced and the device is disabled.

Thermal Shutdown

The over temperature protection function will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the converter will automatically resume switching.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 40V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- V_{BOOT} - V_{SW} ---------- –0.3V to 6V
- EN, FB, CSP, CSN ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
- SOP-8 (Exposed Pad) ---------- 2.041W
- Package Thermal Resistance (Note 2)

  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W

  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 7.5V to 36V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, T_A = 25°C, Load Current = 0A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{OUT} OVP Detect Voltage	V_{OVP}	Normal Operation.	--	5.8	--	V
V_{OUT} OVP Hysteresis	Δ_{VOVP}	Normal Operation.	--	0.3	--	V
Shutdown Supply Current	I_{SD}	V_{EN} = 0V	--	1.5	3	μA
Supply Current	I_Q	V_{EN} = 3 V, V_{FB} = 0.9V	--	0.8	1.2	mA
Feedback Voltage (*)	V_{FB}	7.5V ≤ V_{IN} ≤ 36V	0.784	0.8	0.816	V
High-Side Switch On-Resistance	$R_{DS(ON),U}$		--	100	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON),L}$		--	15	--	Ω
High-Side Switch Leakage Current	I_{SWLEAK}	V_{EN} = 0V, V_{SW} = 0V	--	0	10	μA
Upper Switch Current Limit	I_{LIM}		--	4.4	--	A
Load Line Compensation Gain	G_{LC}	V_{CSP} – V_{CSN} = 100mV, check I_{FB}	15	20	25	μA/V
Current Sense Voltage (*)	V_{SENSE}	V_{CSP} – V_{CSN}	98	100	102	mV
Oscillation Frequency	f_{OSC1}		85	100	115	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	--	20	--	kHz
Minimum Off-Time	t_{OFF}		--	200	--	ns
Minimum On-Time	t_{ON}		--	150	--	ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Threshold Voltage	Logic-High	V_{IH}		2.7	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Input Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	6.3	6.7	7.2	V
Input Under Voltage Lockout Hysteresis		ΔV_{UVLO}		--	0.5	1	V
Soft-Start Period		t_{SS}		--	3.5	--	ms
Thermal Shutdown		T_{SD}		--	150	--	°C

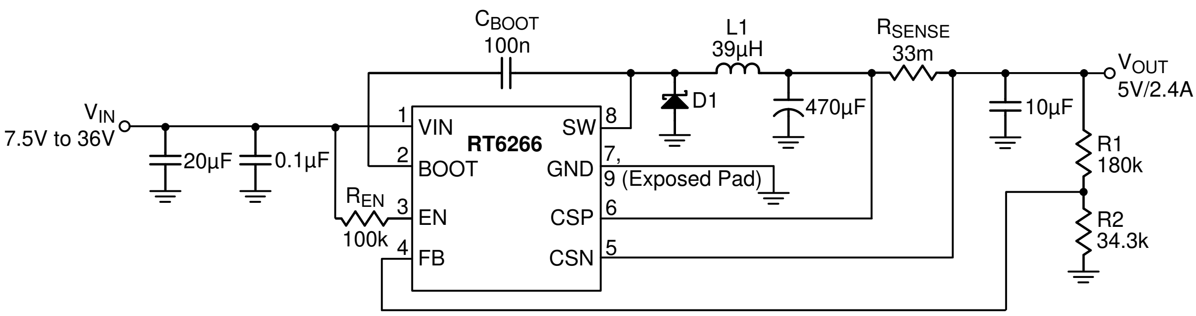
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

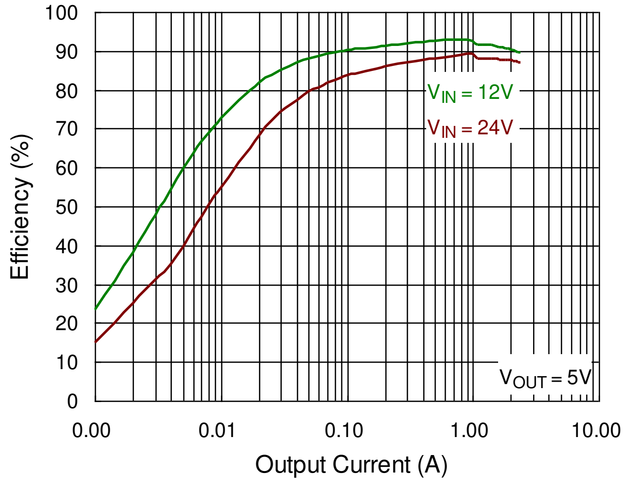
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

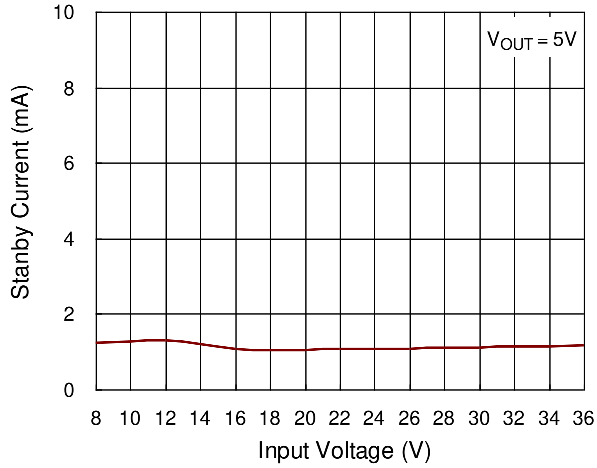


Typical Operating Characteristics

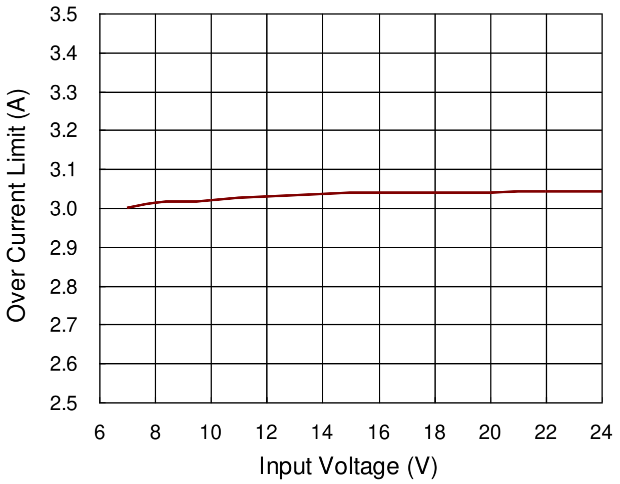
Efficiency vs. Output Current



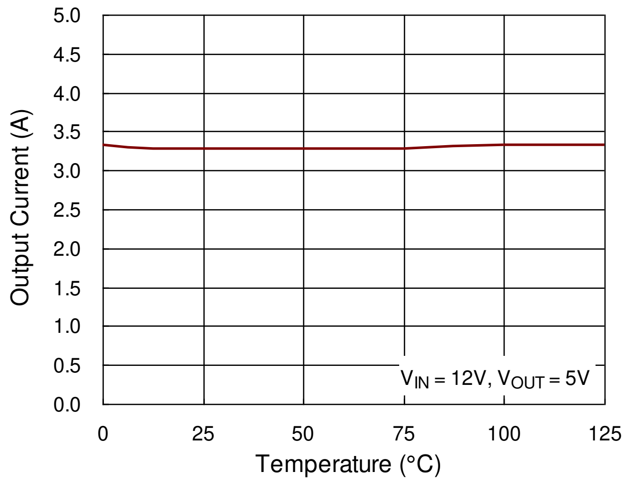
Stanby Supply Current vs. Input Voltage



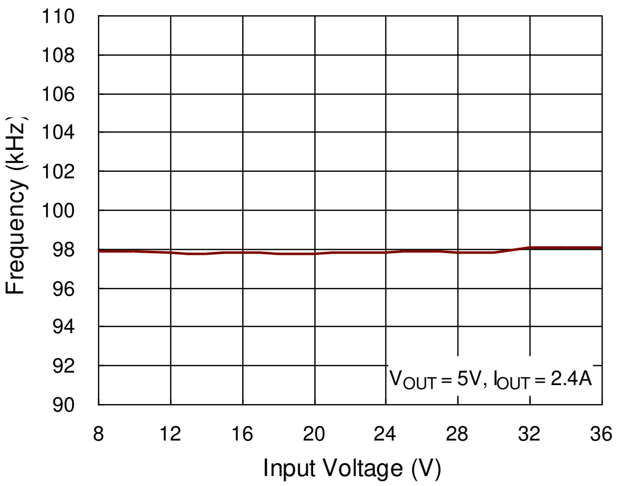
Over Current Limit vs. Input Voltage



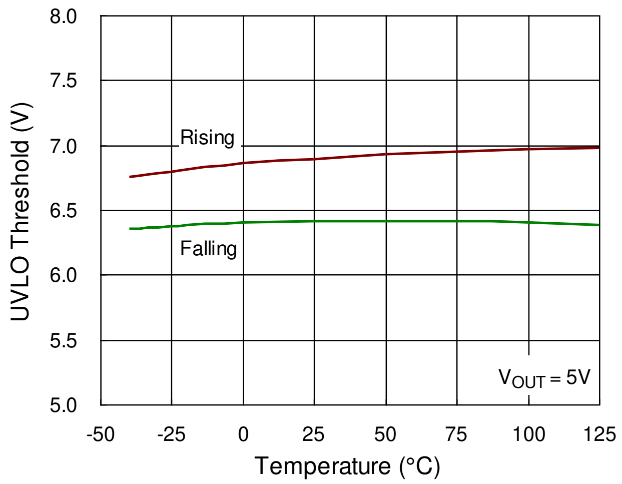
Output Current vs. Temperature



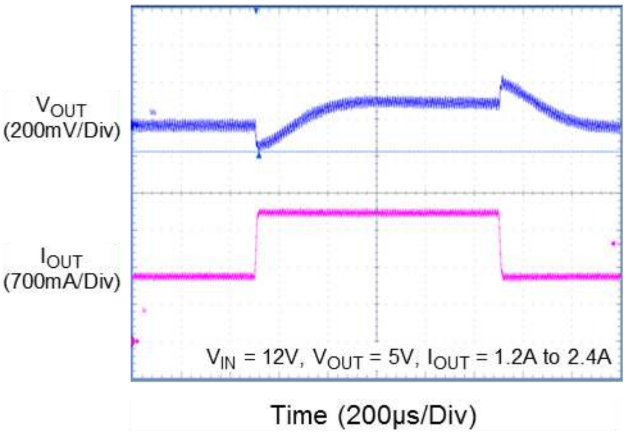
Frequency vs. Input Voltage



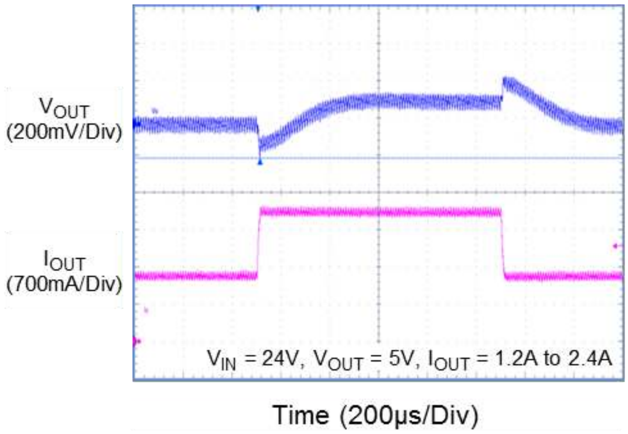
UVLO Threshold vs. Temperature



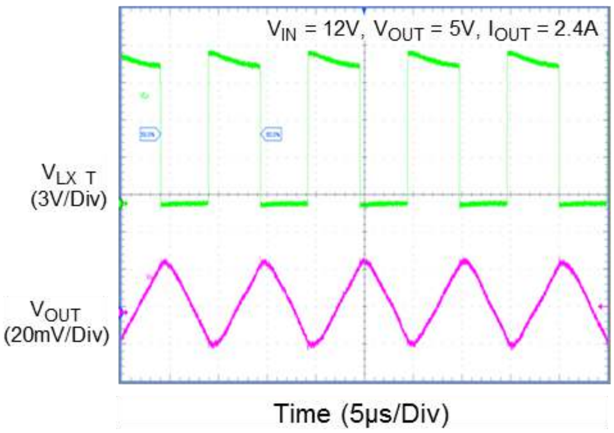
Load Transient Response



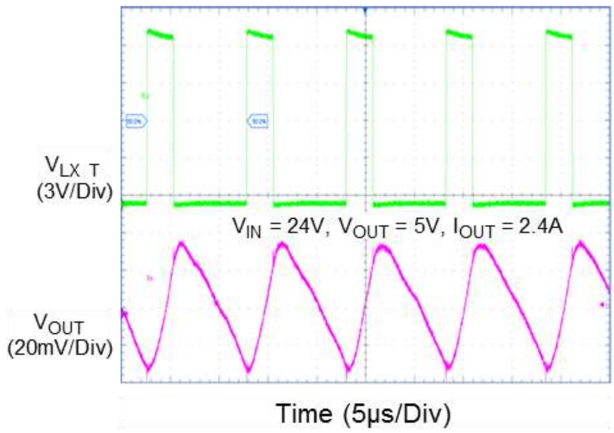
Load Transient Response



Output Ripple Voltage



Output Ripple Voltage



Application Information

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

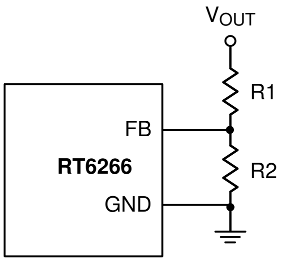


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
MAG.LAYERS	MCD110C-390K-LV	10 x 6.5 x 10.5

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current is given :

$$I_{RMS} = I_{OUT(MAX)}\frac{V_{OUT}}{V_{IN}}\sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF low ESR ceramic capacitors are Suggested. For the Suggested capacitor, please refer to Table 3 for more details. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \le \Delta I_L\left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (49°C/W) = 2.041W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

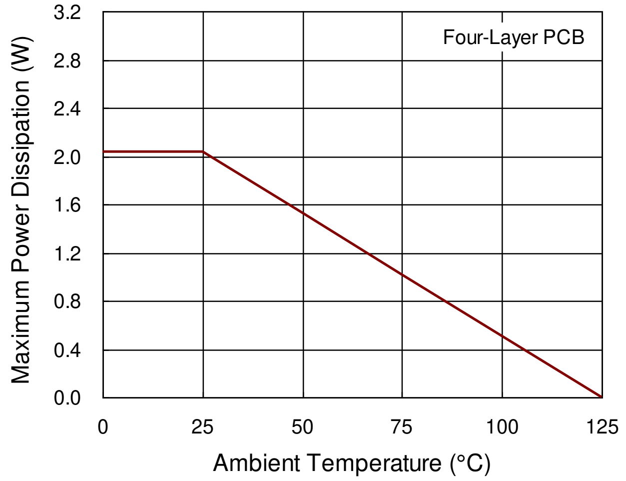


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT6266.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT6266.
- An example of PCB layout guide is shown in Figure 3 for reference.

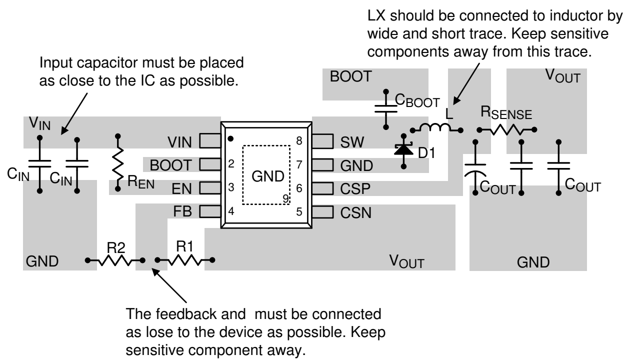
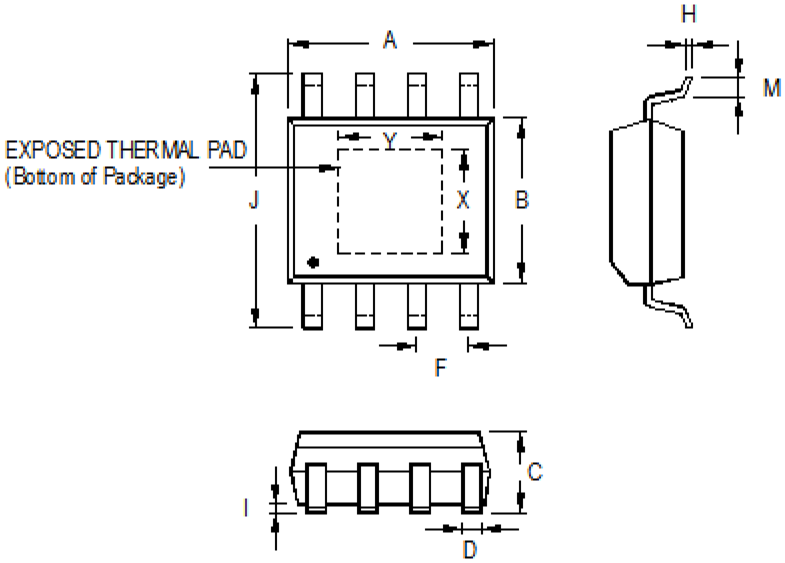


Figure 3. PCB Layout Guide

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789