

A large, light blue decorative graphic consisting of a thick, curved line that forms a partial circle. A small, solid blue circle is positioned at the top of the curve, acting as a pivot point for the line.

8-Bit

XC858CA

8-Bit Single-Chip Microcontroller

Data Sheet

V1.0 2010-03

Microcontrollers

Edition 2010-03

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Revision History:

Page	Subjects (major changes since last revision)

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1 Summary of Features

The XC858 has the following features:

- High-performance XC800 Core
 - compatible with standard 8051 processor
 - two clocks per machine cycle architecture (for memory access without wait state)
 - two data pointers
- On-chip memory
 - 8 Kbytes of Boot ROM
 - 256 bytes of RAM
 - 3 Kbytes of XRAM
 - 64/52/36 Kbytes of Flash; (includes memory protection strategy)
- I/O port supply at 5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(more features on next page)

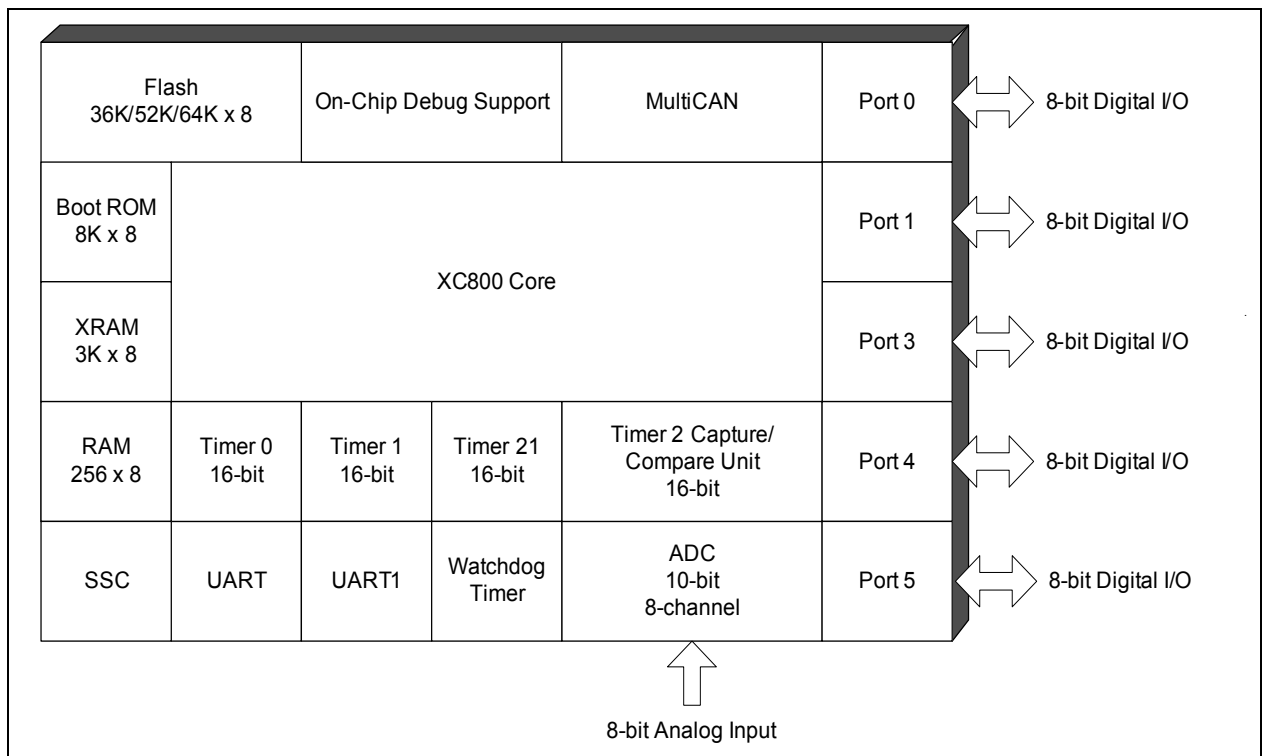


Figure 1 XC858 Functional Units

Summary of Features

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
 - Loss-of-Clock detection
- Power saving modes
 - slow-down mode
 - idle mode
 - power-down mode with wake-up capability via RXD or EXINT0
 - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Five ports
 - Up to 40 pins as digital I/O
 - 8 dedicated analog inputs used as A/D converter input
- 8-channel, 10-bit ADC
- Four 16-bit timers
 - Timer 0 and Timer 1 (T0 and T1)
 - Timer 2 and Timer 21 (T2 and T21)
- MultiCAN with 2 nodes, 32 message objects
- Timer 2 Capture/compare unit for PWM signal generation (T2CCU)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
 - 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
 - 64 bytes of monitor RAM
- PG-LQFP-64 pin package
- Temperature range T_A :
 - SAF (-40 to 85 °C)

Summary of Features
XC858 Variant Devices

The XC858 product family features devices with different program memory sizes.

The list of XC858 devices and their difference are summarized in [Table 1](#). The type of package available is the LQFP-64.

Table 1 Device Summary

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temperature (°C)	Quality Profile
SAF-XC858CA-9FFI 5V	Flash	36	5.0	-40 to 85	Industrial
SAF-XC858CA-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC858CA-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC858 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC858, please refer to your responsible sales representative or your local distributor.

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC858.

2.1 Block Diagram

The block diagram of the XC858 is shown in **Figure 2**.

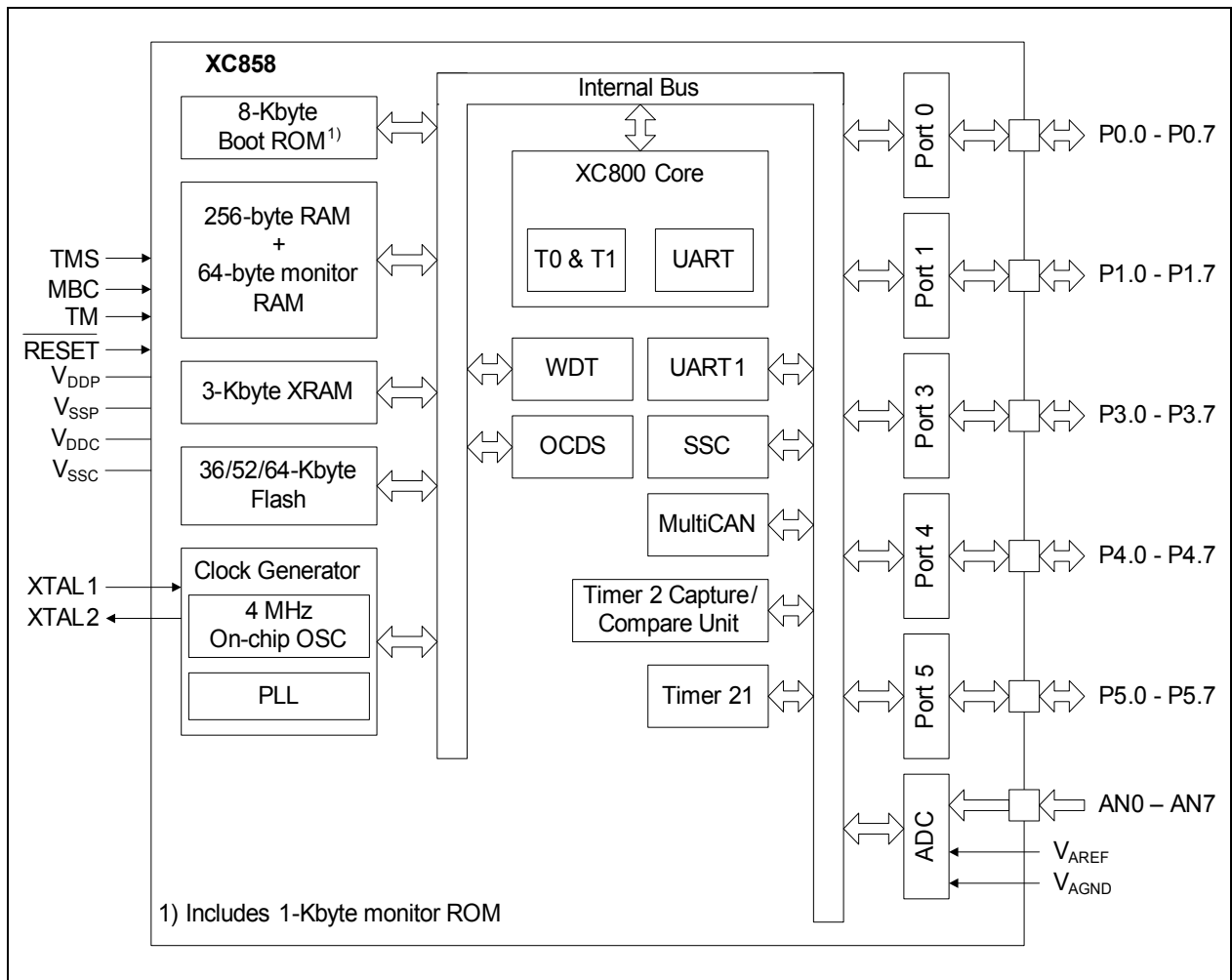


Figure 2 XC858 Block Diagram

2.2 Logic Symbol

The logic symbol of the XC858 is shown in [Figure 3](#).

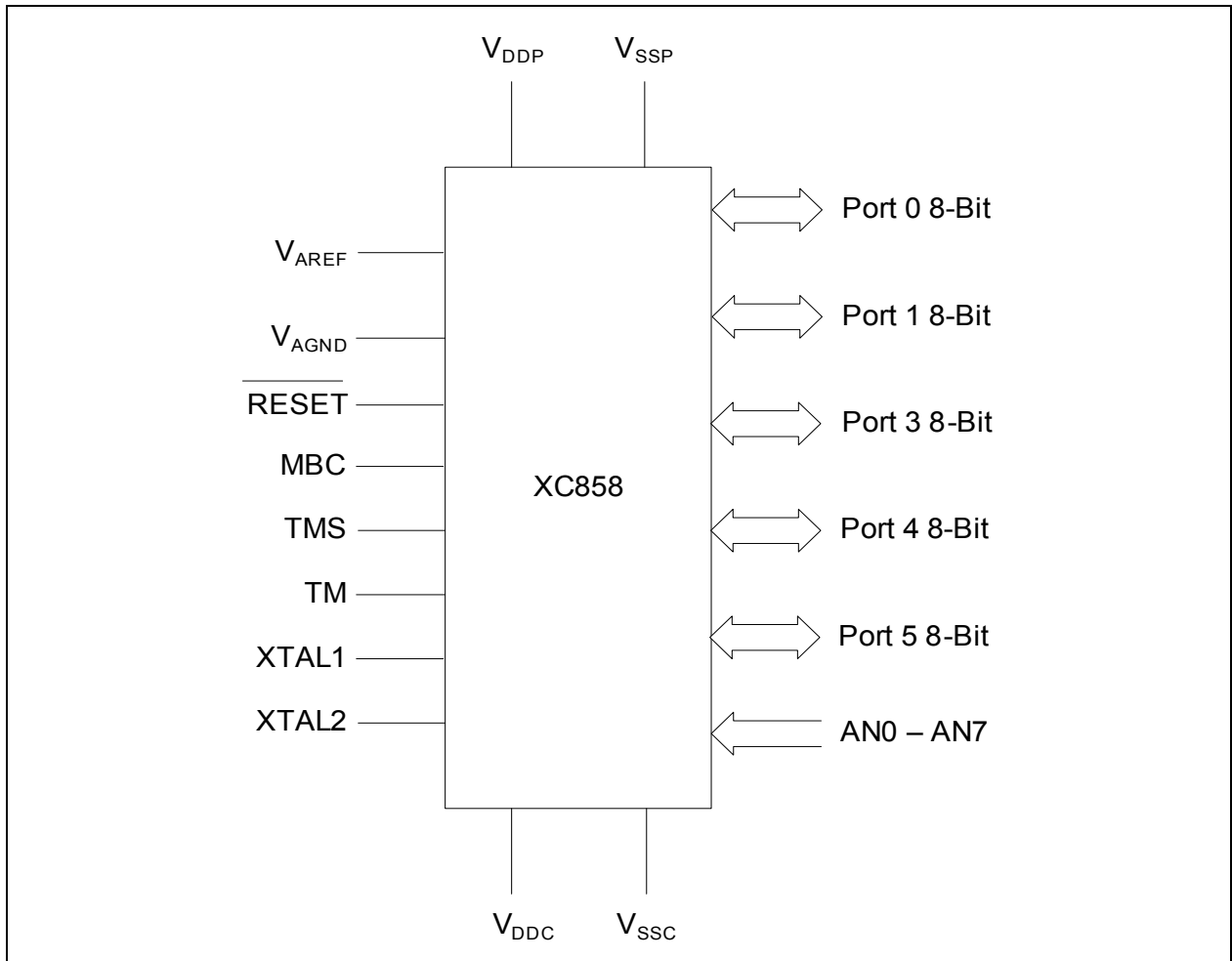


Figure 3 XC858 Logic Symbol

2.3 Pin Configuration

The pin configuration of the XC858 in [Figure 4](#).

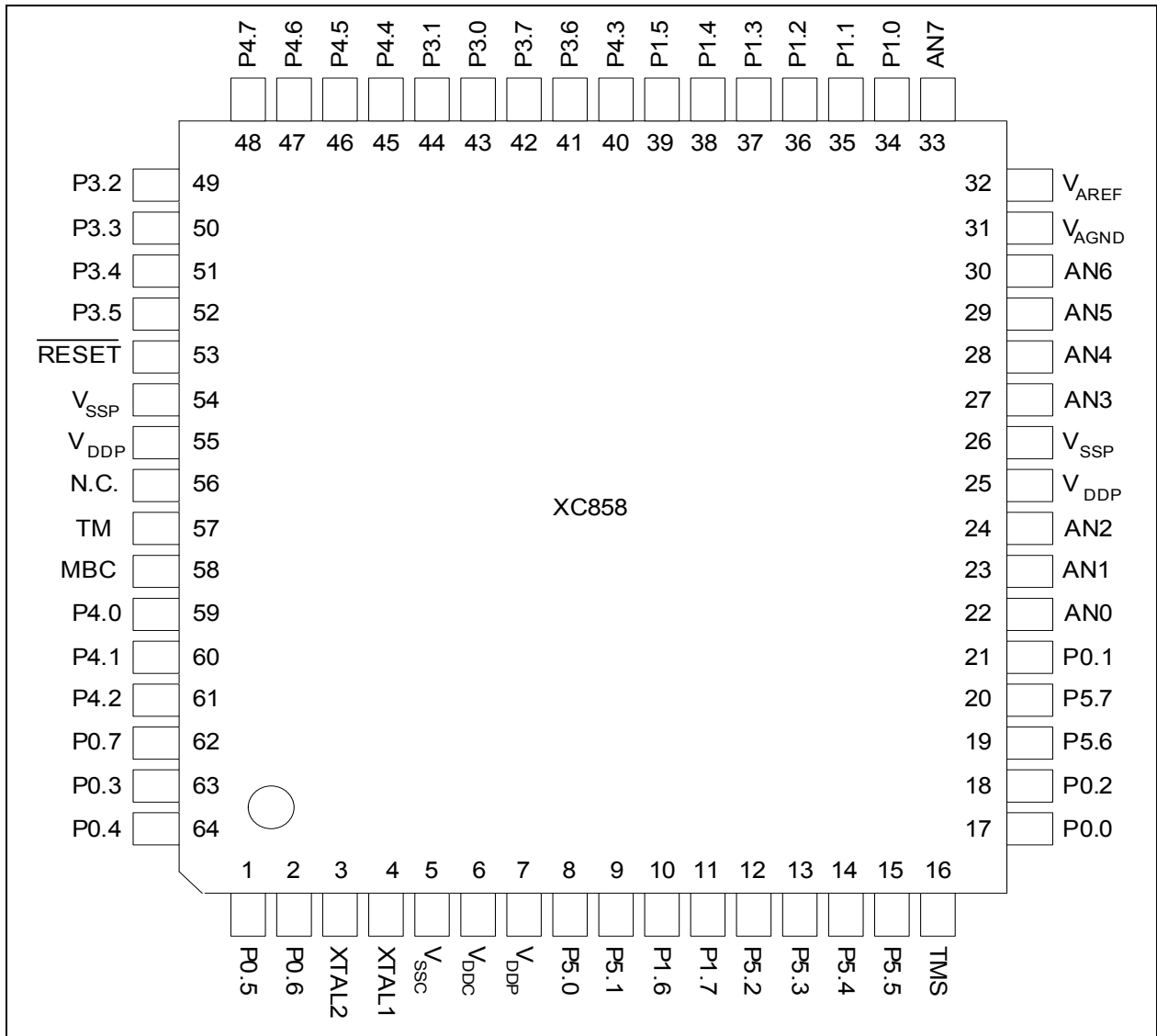


Figure 4 XC858 Pin Configuration, PG-LQFP-64 Package (top view)

2.4 Pin Definitions and Functions

The functions and default states of the XC858 external pins are provided in [Table 2](#).

Table 2 Pin Definitions and Functions

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P0		I/O		Port 0 Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, UART, UART1, T2CCU, Timer 21, MultiCAN, SSC and External Interface.
P0.0	17		Hi-Z	TCK_0 JTAG Clock Input CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	21		Hi-Z	TDI_0 JTAG Serial Data Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input EXF2_1 Timer 2 External Flag Output
P0.2	18		PU	TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output
P0.3	63		Hi-Z	SCK_1 SSC Clock Input/Output RXDO1_0 UART1 Transmit Data Output A17 Address Line 17 Output
P0.4	64		Hi-Z	M TSR_1 SSC Master Transmit Output/Slave Receive Input TXD1_0 UART1 Transmit Data Output/Clock Output A18 Address Line 18 Output
P0.5	1		Hi-Z	MRST_1 SSC Master Receive Input/Slave Transmit Output EXINT0_0 External Interrupt Input 0 T2EX1_1 Timer 21 External Trigger Input RXD1_0 UART1 Receive Data Input A19 Address Line 19 Output

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P0.6	2		PU	T2CC4_1 \overline{WR} Compare Output Channel 4 External Data Write Control Output
P0.7	62		PU	CLKOUT_1 T2CC5_1 \overline{RD} Clock Output Compare Output Channel 5 External Data Read Control Output

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Interface.
P1.0	34		PU	RXD_0 UART Receive Data Input T2EX_0 Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input A8 Address Line 8 Output
P1.1	35		PU	EXINT3_0 External Interrupt Input 3 T0_1 Timer 0 Input TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output A9 Address Line 9 Output
P1.2	36		PU	SCK_0 SSC Clock Input/Output A10 Address Line 10 Output
P1.3	37		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input SCK_2 SSC Clock Input/Output TXDC1_3 MultiCAN Node 1 Transmitter Output A11 Address Line 11 Output
P1.4	38		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input MTSR_2 SSC Master Transmit Output/Slave Receive Input A12 Address Line 12 Output

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P1.5	39		PU	EXINT5_0 External Interrupt Input 5 T1_1 Timer 1 Input MRST_2 SSC Master Receive Input/ Slave Transmit Output EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output
P1.6	10		PU	EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	11		PU	T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P3		I/O		Port 3 Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART1, T2CCU, Timer 21, MultiCAN and External Interface.
P3.0	43		Hi-Z	RXD01_1 UART1 Transmit Data Output T2CC0_1/ External Interrupt Input 3/T2CCU EXINT3_2 Capture/Compare Channel 0
P3.1	44		Hi-Z	TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	49		Hi-Z	RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input T2CC1_1/ External Interrupt Input 4/T2CCU EXINT4_2 Capture/Compare Channel 1
P3.3	50		Hi-Z	TXDC1_1 MultiCAN Node 1 Transmitter Output T2CC2_1/ External Interrupt Input 5/T2CCU EXINT5_2 Capture/Compare Channel 2 A13 Address Line 13 Output
P3.4	51		Hi-Z	RXDC0_1 MultiCAN Node 0 Receiver Input T2EX1_0 Timer 21 External Trigger Input T2CC3_1/ External Interrupt Input 6/T2CCU EXINT6_3 Capture/Compare Channel 3 A14 Address Line 14 Output
P3.5	52		Hi-Z	EXF21_0 Timer 21 External Flag Output TXDC0_1 MultiCAN Node 0 Transmitter Output A15 Address Line 15 Output
P3.6	41		PU	-
P3.7	42		Hi-Z	EXINT4_0 External Interrupt Input 4 A16 Address Line 16 Output

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P4		I/O		Port 4 Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Interface.
P4.0	59		Hi-Z	RXDC0_3 MultiCAN Node 0 Receiver Input T2CC0_0/ External Interrupt Input 3/T2CCU EXINT3_1 Capture/Compare Channel 0 D0 Data Line 0 Input/Output
P4.1	60		Hi-Z	TXDC0_3 MultiCAN Node 0 Transmitter Output T2CC1_0/ External Interrupt Input 4/T2CCU EXINT4_1 Capture/Compare Channel 1 D1 Data Line 1 Input/Output
P4.2	61		PU	EXINT6_1 External Interrupt Input 6 T21_0 Timer 21 Input D2 Data Line 2 Input/Output
P4.3	40		Hi-Z	T2EX_1 Timer 2 External Trigger Input EXF21_1 Timer 21 External Flag Output D3 Data Line 3 Input/Output
P4.4	45		Hi-Z	T0_0 Timer 0 Input T2CC2_0/ External Interrupt Input 5/T2CCU EXINT5_1 Capture/Compare Channel 2 D4 Data Line 4 Input/Output
P4.5	46		Hi-Z	T1_0 Timer 1 Input T2CC3_0/ External Interrupt Input 6/T2CCU EXINT6_2 Capture/Compare Channel 3 D5 Data Line 5 Input/Output
P4.6	47		Hi-Z	T2_0 Timer 2 Input T2CC4_0 Compare Output Channel 4 D6 Data Line 6 Input/Output
P4.7	48		Hi-Z	T2CC5_0 Compare Output Channel 5 D7 Data Line 7 Input/Output

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P5		I/O		Port 5 Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External Interface.
P5.0	8		PU	EXINT1_1 External Interrupt Input 1 A0 Address Line 0 Output
P5.1	9		PU	EXINT2_1 External Interrupt Input 2 A1 Address Line 1 Output
P5.2	12		PU	RXD_2 UART Receive Data Input T2CC2_2/ External Interrupt Input 5/T2CCU EXINT5_3 Capture/Compare Channel 2 A2 Address Line 2 Output
P5.3	13		PU	EXINT1_0 External Interrupt Input 1 TXD_2 UART Transmit Data Output/Clock Output T2CC5_2 Compare Output Channel 5 A3 Address Line 3 Output
P5.4	14		PU	EXINT2_0 External Interrupt Input 2 RXDO_2 UART Transmit Data Output T2CC4_2 Compare Output Channel 4 A4 Address Line 4 Output
P5.5	15		PU	TDO_1 JTAG Serial Data Output TXD1_2 UART1 Transmit Data Output/ Clock Output T2CC0_2/ External Interrupt Input 3/T2CCU EXINT3_3 Capture/Compare Channel 0 A5 Address Line 5 Output
P5.6	19		PU	TCK_1 JTAG Clock Input RXDO1_2 UART1 Transmit Data Output T2CC1_2/ External Interrupt Input 4/T2CCU EXINT4_3 Capture/Compare Channel 1 A6 Address Line 6 Output

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
P5.7	20		PU	TDI_1 JTAG Serial Data Input RXD1_2 UART1 Receive Data Input T2CC3_2/ External Interrupt Input 6/T2CCU EXINT6_4 Capture/Compare Channel 3 A7 Address Line 7 Output

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function
V_{DDP}	7, 25, 55	–	–	I/O Port Supply (5.0 V) Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	26, 54	–	–	I/O Ground All pins must be connected.
V_{DDC}	6	–	–	Core Supply Monitor (2.5 V)
V_{SSC}	5	–	–	Core Supply Ground
V_{AREF}	32	–	–	ADC Reference Voltage
V_{AGND}	31	–	–	ADC Reference Ground
AN0	22	I	Hi-Z	Analog Input 0
AN1	23	I	Hi-Z	Analog Input 1
AN2	24	I	Hi-Z	Analog Input 2
AN3	27	I	Hi-Z	Analog Input 3
AN4	28	I	Hi-Z	Analog Input 4
AN5	29	I	Hi-Z	Analog Input 5
AN6	30	I	Hi-Z	Analog Input 6
AN7	33	I	Hi-Z	Analog Input 7
XTAL1	4	I	Hi-Z	External Oscillator Input (Feedback resistor required, normally NC)
XTAL2	3	O	Hi-Z	External Oscillator Output (Feedback resistor required, normally NC)
TMS	16	I	PD	JTAG Test Mode Select
RESET	53	I	PU	Reset Input
MBC	58	I	PU	Monitor & BootStrap Loader Control
TM	57	–	–	Test Mode (External pull down device required)
NC	56	–	–	No Connection

3 Functional Description

Chapter 3 provides an overview of the XC858 functional description.

3.1 Processor Architecture

The XC858 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC858 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions. The XC858 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 5 shows the CPU functional blocks.

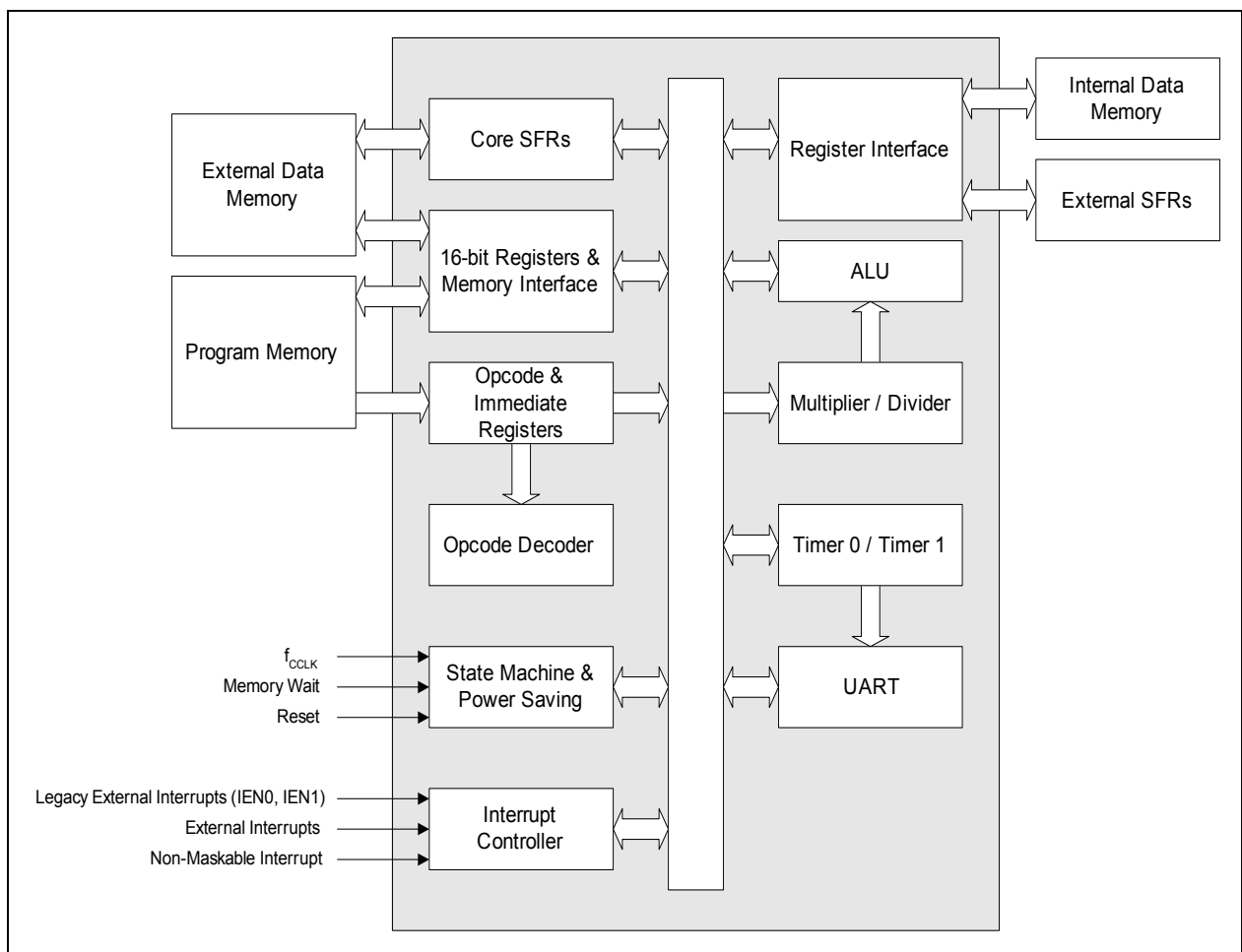


Figure 5 CPU Block Diagram

3.2 Memory Organization

The XC858 CPU operates in the following address spaces:

- 8 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 3 Kbytes of XRAM memory
(XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 64/52/36 Kbytes of Flash program memory (Flash devices)

Figure 6, Figure 7 and Figure 8 illustrates the memory address spaces of the XC858 with 64Kbytes, 52Kbytes and 36Kbytes embedded Flash respectively.

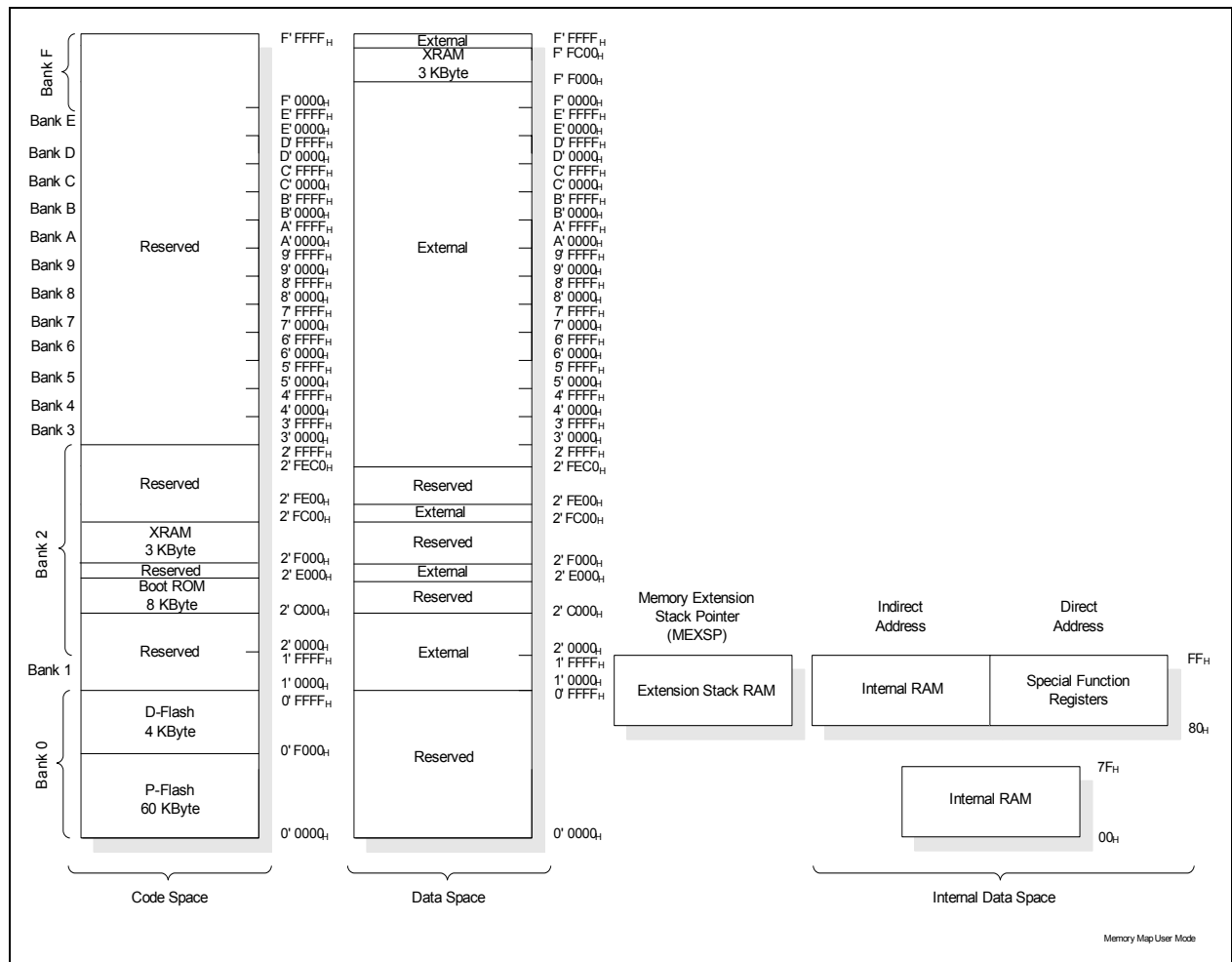


Figure 6 Memory Map of XC858 with 64K Flash Memory in user mode

Functional Description

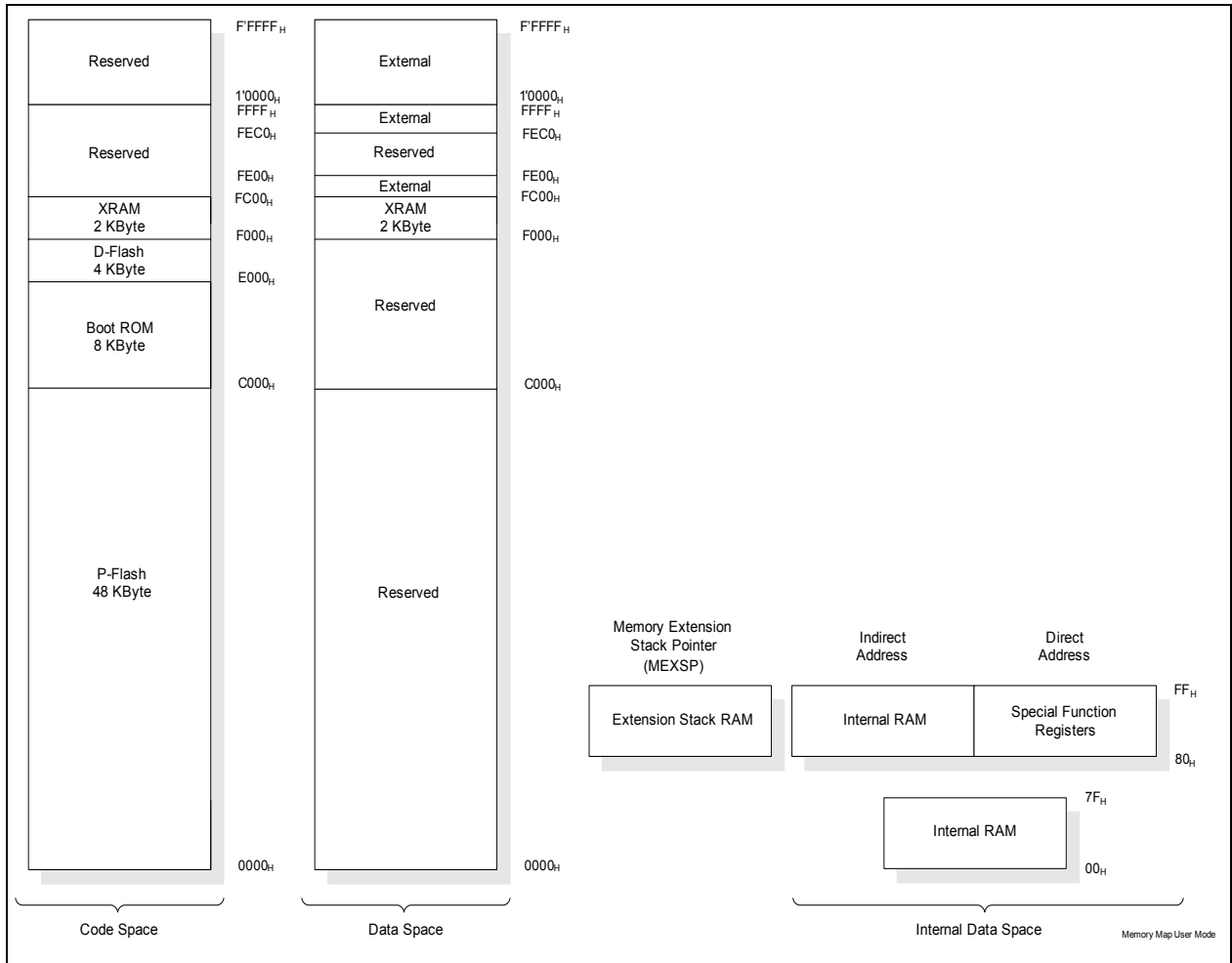


Figure 7 Memory Map of XC858 with 52K Flash Memory in user mode

Functional Description

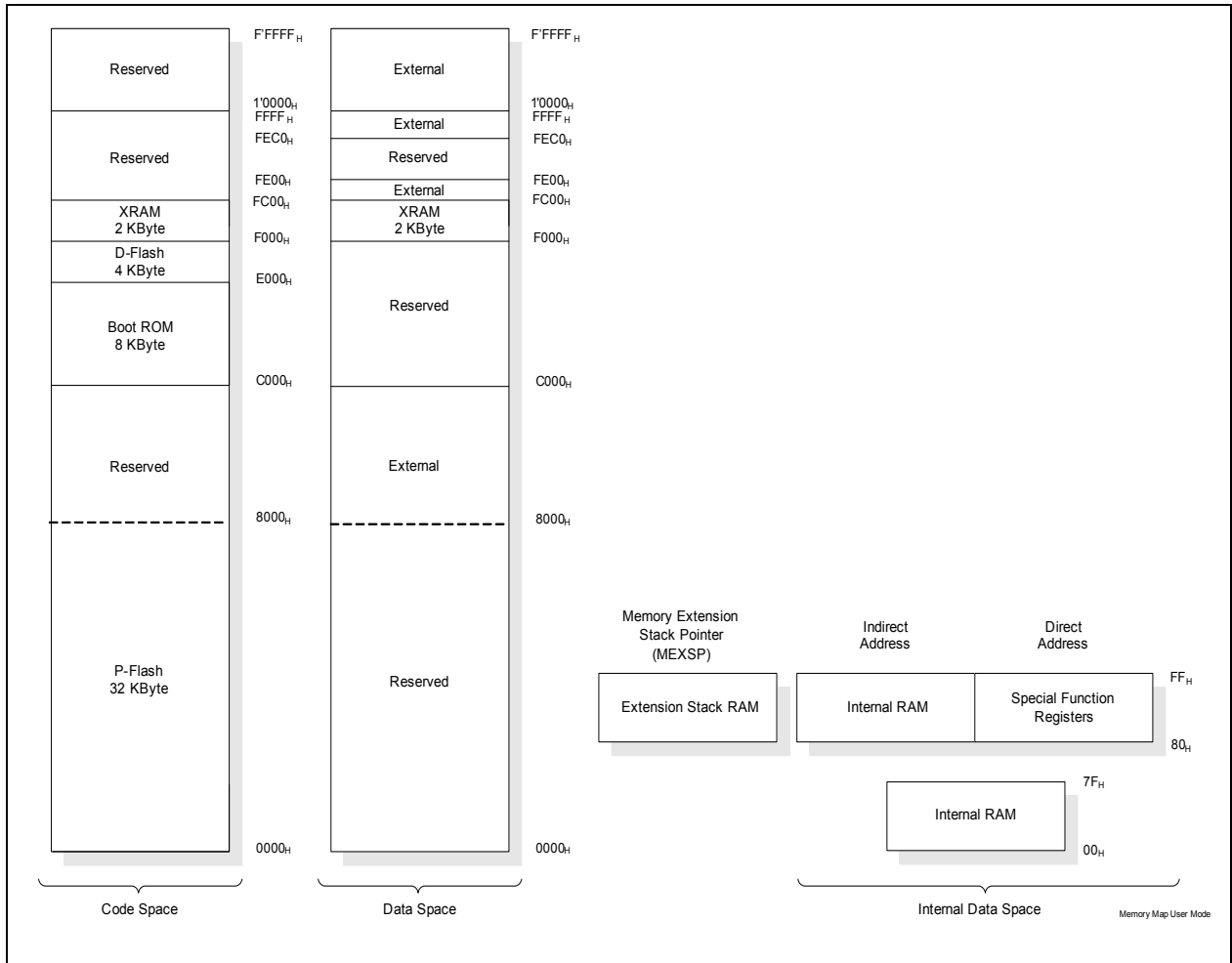


Figure 8 Memory Map of XC858 with 36K Flash Memory in user mode

3.2.1 Memory Protection Strategy

The XC858 memory protection strategy includes:

- Basic protection: The user is able to block any external access via the boot option to any memory
- Read-out protection: The user is able to protect the contents in the Flash
- Flash program and erase protection

These protection strategies are enabled by programming a valid password (16-bit non-one value) via Bootstrap Loader (BSL) mode 6.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in [Table 3](#).

Table 3 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 13 of password = 0	Bit 13 of password = 1 MSB of password = 0	Bit 13 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible

Functional Description
Table 3 Flash Protection Modes (cont'd)

Flash Protection	Without hardware protection		With hardware protection	
P-Flash program and erase	Possible		Possible only on the condition that MSB - 1 of password is set to 1	Possible only on the condition that MSB - 1 of password is set to 1
D-Flash contents can be read by	Read instructions in any program memory		Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
External access to D-Flash	Not possible		Not possible	Not possible
D-Flash program	Possible		Possible	Possible, on the condition that MSB - 1 of password is set to 1
D-Flash erase	Possible		Possible, on these conditions: <ul style="list-style-type: none"> • MISC_CON.DFLASH EN bit is set to 1 prior to each erase operation; or • the MSB - 1 of password is set to 1 	Possible, on the condition that MSB - 1 of password is set to 1

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. To disable the flash protection, a password match is required. A password match triggers an automatic erase of the protected P-Flash and D-Flash contents, including the programmed password. With a valid password, the Flash hardware protection is then enabled or disabled upon next reset. For the other protection strategies, no reset is necessary.

Although no protection scheme can be considered infallible, the XC858 memory protection strategy provides a very high level of protection for a general purpose microcontroller.

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H . All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H , bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in [Figure 9](#).

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

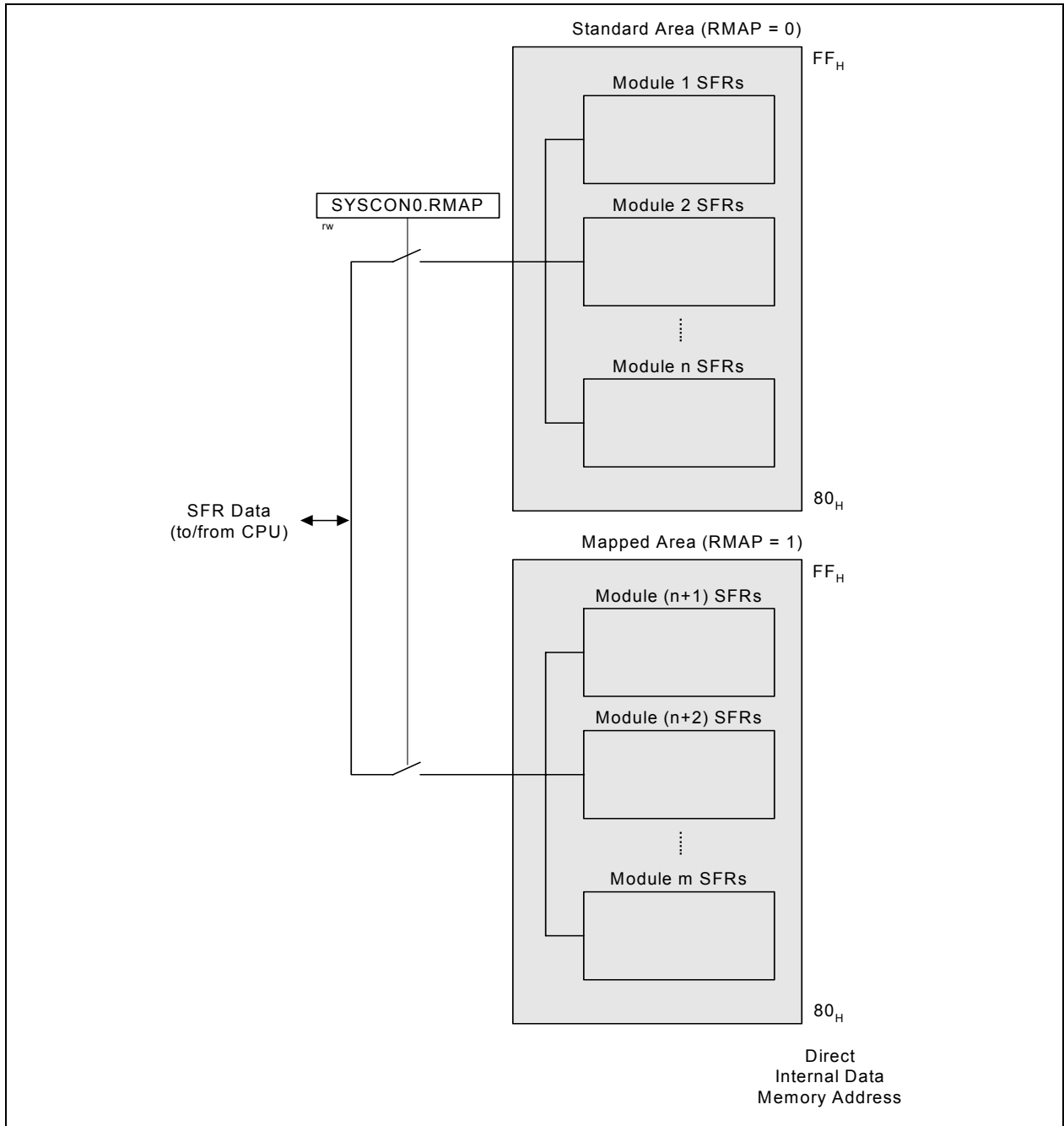


Figure 9 Address Extension by Mapping

Functional Description

SYSCON0

System Control Register 0

Reset Value: 04_H

7	6	5	4	3	2	1	0
0		IMODE		0	1	0	RMAP
r		rw		r	r	r	rw

Field	Bits	Type	Description
RMAP	0	rw	Interrupt Node XINTR0 Enable 0 The access to the standard SFR area is enabled 1 The access to the mapped SFR area is enabled
1	2	r	Reserved Returns 1 if read; should be written with 1.
0	[7:5], 3,1	r	Reserved Returns 0 if read; should be written with 0.

Note: The RMAP bit should be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC858 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in [Figure 10](#).

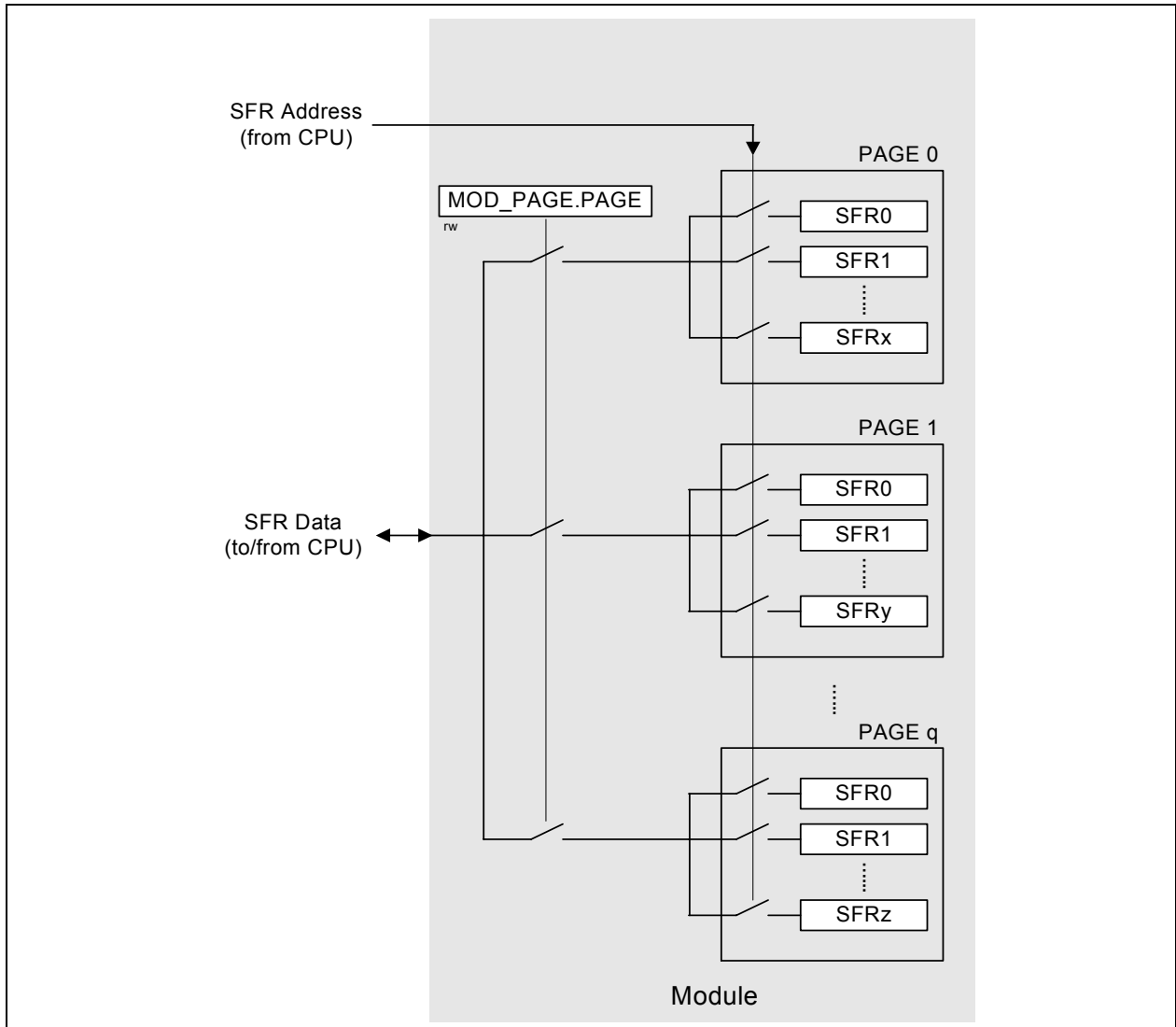


Figure 10 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or

Functional Description

- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
(this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

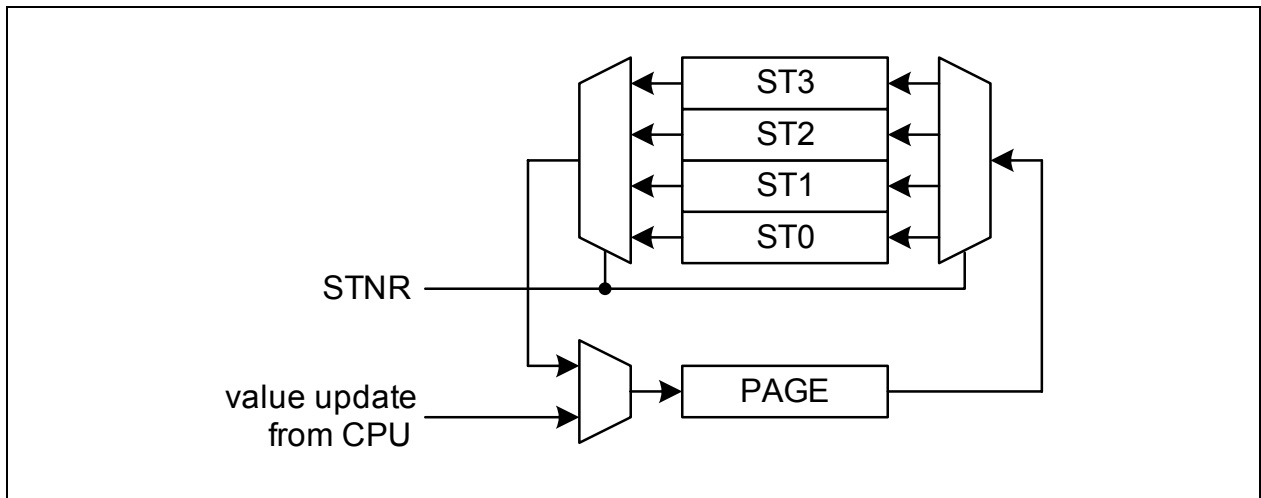


Figure 11 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC858 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- System Control Registers

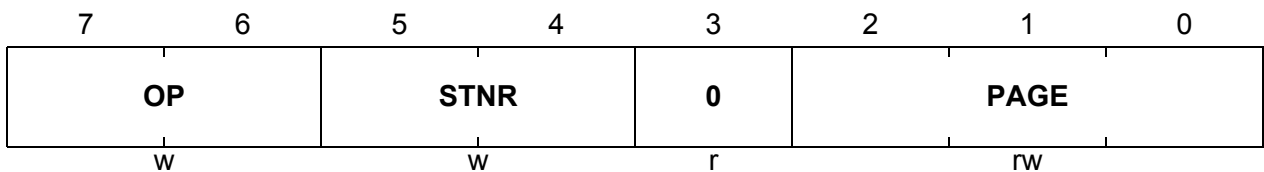
Functional Description

The page register has the following definition:

MOD_PAGE

Page Register for module MOD

Reset Value: 00_H



Field	Bits	Type	Description
PAGE	[2:0]	rw	<p>Page Bits</p> <p>When written, the value indicates the new page. When read, the value indicates the currently active page.</p>
STNR	[5:4]	w	<p>Storage Number</p> <p>This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10_B, the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11_B, the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored.</p> <p>00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.</p>

Functional Description

Field	Bits	Type	Description
OP	[7:6]	w	Operation 0X Manual page mode. The value of STNR is ignored and PAGE is directly written. 10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR. 11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.
0	3	r	Reserved Returns 0 if read; should be written with 0.

3.2.3 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected bits (i.e., protected bits) using the PASSWD register. When the bit field MODE is 11_B, writing 10011_B to the bit field PASS opens access to writing of all protected bits, and writing 10101_B to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with 98_H or A8_H. It can only be changed when bit field PASS is written with 11000_B, for example, writing D0_H to PASSWD register disables the bit protection scheme.

Note that access is opened for maximum 32 CCLKs if the “close access” password is not written. If “open access” password is written again before the end of 32 CCLK cycles, there will be a recount of 32 CCLK cycles. The protected bits include the N- and K-Divider bits, NDIV and KDIV; the Watchdog Timer enable bit, WDTEN; and the power-down and slow-down enable bits, PD and SD.

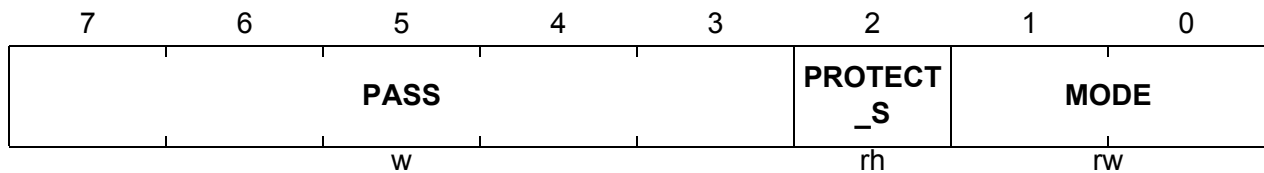
Functional Description

3.2.3.1 Password Register

PASSWD

Password Register

Reset Value: 07_H



Field	Bits	Type	Description
MODE	[1:0]	rw	<p>Bit Protection Scheme Control Bits</p> <p>00 Scheme disabled - direct access to the protected bits is allowed.</p> <p>11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default)</p> <p>Others: Scheme Enabled.</p> <p>These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B; only then, will the MODE[1:0] be registered.</p>
PROTECT_S	2	rh	<p>Bit Protection Signal Status Bit</p> <p>This bit shows the status of the protection.</p> <p>0 Software is able to write to all protected bits.</p> <p>1 Software is unable to write to any protected bits.</p>
PASS	[7:3]	w	<p>Password Bits</p> <p>The Bit Protection Scheme only recognizes three patterns.</p> <p>11000_B Enables writing of the bit field MODE.</p> <p>10011_B Opens access to writing of all protected bits.</p> <p>10101_B Closes access to writing of all protected bits</p>

Functional Description
3.2.4 XC858 Register Overview

The SFRs of the XC858 are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in [Chapter 3.2.4.1](#) to [Chapter 3.2.4.12](#).

Note: The addresses of the bitaddressable SFRs appear in bold typeface.

3.2.4.1 CPU Registers

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Table 4 CPU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP = 0 or 1											
81 _H	SP Stack Pointer Register Reset: 07 _H	Bit Field	SP								
		Type	rw								
82 _H	DPL Data Pointer Register Low Reset: 00 _H	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0	
		Type	rw	rw	rw	rw	rw	rw	rw	rw	rw
83 _H	DPH Data Pointer Register High Reset: 00 _H	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0	
		Type	rw	rw	rw	rw	rw	rw	rw	rw	rw
87 _H	PCON Power Control Register Reset: 00 _H	Bit Field	SMOD	0			GF1	GF0	0	IDLE	
		Type	rw	r			rw	rw	r	rw	
88 _H	TCON Timer Control Register Reset: 00 _H	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
		Type	rwh	rw	rwh	rw	rwh	rw	rwh	rw	
89 _H	TMOD Timer Mode Register Reset: 00 _H	Bit Field	GATE 1	T1S	T1M		GATE 0	T0S	T0M		
		Type	rw	rw	rw		rw	rw	rw		
8A _H	TL0 Timer 0 Register Low Reset: 00 _H	Bit Field	VAL								
		Type	rwh								
8B _H	TL1 Timer 1 Register Low Reset: 00 _H	Bit Field	VAL								
		Type	rwh								
8C _H	TH0 Timer 0 Register High Reset: 00 _H	Bit Field	VAL								
		Type	rwh								
8D _H	TH1 Timer 1 Register High Reset: 00 _H	Bit Field	VAL								
		Type	rwh								
94 _H	MEX1 Memory Extension Register 1 Reset: 00 _H	Bit Field	CB				NB				
		Type	r				rw				
95 _H	MEX2 Memory Extension Register 2 Reset: 00 _H	Bit Field	MCM	MCB			IB				
		Type	rw	rw			rw				
96 _H	MEX3 Memory Extension Register 3 Reset: 00 _H	Bit Field	MCB1 9	0		MXB1 9	MXM	MXB			
		Type	rw	r		rw	rw	rw			

Functional Description
Table 4 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
97 _H	MEXSP Reset: 7F _H Memory Extension Stack Pointer Register	Bit Field	0	MXSP						
		Type	r	rwh						
98 _H	SCON Reset: 00 _H Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
99 _H	SBUF Reset: 00 _H Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
A2 _H	EO Reset: 00 _H Extended Operation Register	Bit Field	0		TRAP_	0			DPSE	L0
		Type	r		rw	r			rw	
A8 _H	IEN0 Reset: 00 _H Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
B8 _H	IP Reset: 00 _H Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
B9 _H	IPH Reset: 00 _H Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
D0 _H	PSW Reset: 00 _H Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
E0 _H	ACC Reset: 00 _H Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
E8 _H	IEN1 Reset: 00 _H Interrupt Enable Register 1	Bit Field	ECCIP 3	ECCIP 2	ECCIP 1	ECCIP 0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F0 _H	B Reset: 00 _H B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F8 _H	IP1 Reset: 00 _H Interrupt Priority 1 Register	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F9 _H	IPH1 Reset: 00 _H Interrupt Priority 1 High Register	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSC H	PADC H
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 5 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP = 0 or 1											
8F _H	SYSCON0 Reset: 04 _H System Control Register 0	Bit Field	0			IMOD	0	1	0	RMAP	
		Type	r			rw	r	r	r	rw	

Functional Description
Table 5 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
BF _H	SCU_PAGE Page Register Reset: 00 _H	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
B3 _H	MODPISEL Peripheral Input Select Register Reset: 00 _H	Bit Field	0	URRIS H	JTAGT DIS	JTAGT CKS	EXINT 2IS	EXINT 1IS	EXINT 0IS	URRIS
		Type	r	rw	rw	rw	rw	rw	rw	rw
B4 _H	IRCON0 Interrupt Request Register 0 Reset: 00 _H	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B5 _H	IRCON1 Interrupt Request Register 1 Reset: 00 _H	Bit Field	0	CANS RC2	CANS RC1	ADCS R1	ADCS R0	RIR	TIR	EIR
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B6 _H	IRCON2 Interrupt Request Register 2 Reset: 00 _H	Bit Field	0			CANS RC3	0			CANS RC0
		Type	r			rwh	r			rwh
B7 _H	EXICON0 External Interrupt Control Register 0 Reset: F0 _H	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0	
		Type	rw		rw		rw		rw	
BA _H	EXICON1 External Interrupt Control Register 1 Reset: 3F _H	Bit Field	0		EXINT6		EXINT5		EXINT4	
		Type	r		rw		rw		rw	
BB _H	NMICON NMI Control Register Reset: 00 _H	Bit Field	0	NMI ECC	NMI VDDP	0	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Type	r	rw	rw	r	rw	rw	rw	rw
BC _H	NMISR NMI Status Register Reset: 00 _H	Bit Field	0	FNMI ECC	FNMI VDDP	0	FNMI OCDS	FNMI FLASH	FNMI PLL	FNMI WDT
		Type	r	rwh	rwh	r	rwh	rwh	rwh	rwh
BD _H	BCON Baud Rate Control Register Reset: 20 _H	Bit Field	BGSEL		NDOV EN	BRDIS	BRPRE			R
		Type	rw		rw	rw	rw			rw
BE _H	BG Baud Rate Timer/Reload Register Reset: 00 _H	Bit Field	BR_VALUE							
		Type	rwh							
E9 _H	FDCON Fractional Divider Control Register Reset: 00 _H	Bit Field	BGS	SYNE N	ERRS YN	EOFS YN	BRK	NDOV	FDM	FDEN
		Type	rw	rw	rwh	rwh	rw	rw	rw	rw
EA _H	FDSTEP Fractional Divider Reload Register Reset: 00 _H	Bit Field	STEP							
		Type	rw							
EB _H	FDRES Fractional Divider Result Register Reset: 00 _H	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 1										

Functional Description
Table 5 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
B3 _H	ID Reset: 49_H Identity Register	Bit Field	PRODID					VERID			
		Type	r					r			
B4 _H	PMCON0 Reset: 80_H Power Mode Control Register 0	Bit Field	VDDP WARN	WDT RST	WKRS	WK SEL	SD	PD	WS		
		Type	rh	rwh	rwh	rw	rw	rwh	rw		
B5 _H	PMCON1 Reset: 00_H Power Mode Control Register 1	Bit Field	0		CAN_ DIS	0	T2CC U_DIS	0	SSC_ DIS	ADC_ DIS	
		Type	r		rw	r	rw	r	rw	rw	
B6 _H	OSC_CON Reset: XX_H OSC Control Register	Bit Field	PLLRD RES	PLLBY P	PLLPD	0	XPD	OSC SS	EORD RES	EXTO SCR	
		Type	rwh	rwh	rw	r	rw	rwh	rwh	rh	
B7 _H	PLL_CON Reset: 18_H PLL Control Register	Bit Field	NDIV						PLL _R	PLL_ L OCK	
		Type	rw						rh	rh	
BA _H	CMCON Reset: 10_H Clock Control Register	Bit Field	KDIV		0	FCCF G	CLKREL				
		Type	rw		r	rw	rw				
BB _H	PASSWD Reset: 07_H Password Register	Bit Field	PASS					PROT ECT_ S	MODE		
		Type	w					rh	rw		
BE _H	COCON Reset: 00_H Clock Output Control Register	Bit Field	COUTS		TLEN	0	COREL				
		Type	rw		rw	r	rw				
E9 _H	MISC_CON Reset: 00_H Miscellaneous Control Register	Bit Field	ADCE TR0_ MUX	ADCE TR1_ MUX	0					DFLAS HEN	
		Type	rw	rw	r					rwh	
EA _H	PLL_CON1 Reset: 20_H PLL Control Register 1	Bit Field	NDIV			PDIV					
		Type	rw			rw					
EB _H	CR_MISC Reset: 00_H or 01_H Reset Status Register	Bit Field	0			T2CCF G	0			HDRS T	
		Type	r			rw	r			rwh	
RMAP = 0, PAGE 3											
B3 _H	XADDRH Reset: F0_H On-chip XRAM Address Higher Order	Bit Field	ADDRH								
		Type	rw								
B4 _H	IRCON3 Reset: 00_H Interrupt Request Register 3	Bit Field	0	CANS RC5	0			CANS RC4	0		
		Type	r	rwh	r			rwh	r		
B5 _H	IRCON4 Reset: 00_H Interrupt Request Register 4	Bit Field	0	CANS RC7	0			CANS RC6	0		
		Type	r	rwh	r			rwh	r		
B6 _H	MODIEN Reset: 07_H Peripheral Interrupt Enable Register	Bit Field	0			CM5E N	CM4E N	RIREN	TIREN	EIREN	
		Type	r			rw	rw	rw	rw	rw	

Functional Description
Table 5 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B7 _H	MODPISEL1 Reset: 00 _H Peripheral Input Select Register 1	Bit Field	EXINT6IS			UR1RIS		T21EXIS	0	
		Type	rw			rw		rw	r	
BA _H	MODPISEL2 Reset: 00 _H Peripheral Input Select Register 2	Bit Field	0			T2EXIS	T21IS	T2IS	T1IS	T0IS
		Type	r			rw	rw	rw	rw	rw
BB _H	PMCON2 Reset: 00 _H Power Mode Control Register 2	Bit Field	0						UART1_DIS	T21_DIS
		Type	r						rw	rw
BD _H	MODSUSP Reset: 01 _H Module Suspend Control Register	Bit Field	0	CCTSUSP		T21SUSP	T2SUSP	0		WDTUSP
		Type	r	rw		rw	rw	r		rw
BE _H	MODPISEL3 Reset: 00 _H Peripheral Input Select Register 3	Bit Field	0		CIS		SIS		MIS	
		Type	r		rw		rw		rw	
EA _H	MODPISEL4 Reset: 00 _H Peripheral Input Select Register 4	Bit Field	0		EXINT5IS		EXINT4IS		EXINT3IS	
		Type	r		rw		rw		rw	

3.2.4.3 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB _H	WDTCON Reset: 00 _H Watchdog Timer Control Register	Bit Field	0	WINBEN	WDTPR	0	WDTEEN	WDTRS	WDTIN	
		Type	r	rw	rh	r	rw	rwh	rw	
BC _H	WDTREL Reset: 00 _H Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD _H	WDTWINB Reset: 00 _H Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							
BE _H	WDTL Reset: 00 _H Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF _H	WDTH Reset: 00 _H Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.4 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Functional Description
Table 7 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
B2 _H	PORT_PAGE Page Register Reset: 00 _H	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
80 _H	P0_DATA P0 Data Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
86 _H	P0_DIR P0 Direction Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_DATA P1 Data Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
91 _H	P1_DIR P1 Direction Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_DATA P5 Data Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
93 _H	P5_DIR P5 Direction Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_DATA P3 Data Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B1 _H	P3_DIR P3 Direction Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_DATA P4 Data Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
C9 _H	P4_DIR P4 Direction Register Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 1										
80 _H	P0_PUDSEL P0 Pull-Up/Pull-Down Select Register Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_PUDEN P0 Pull-Up/Pull-Down Enable Register Reset: C4 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_PUDSEL P1 Pull-Up/Pull-Down Select Register Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91 _H	P1_PUDEN P1 Pull-Up/Pull-Down Enable Register Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_PUDSEL P5 Pull-Up/Pull-Down Select Register Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93 _H	P5_PUDEN P5 Pull-Up/Pull-Down Enable Register Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Functional Description
Table 7 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B0 _H	P3_PUDSEL Reset: BF _H P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_PUDEN Reset: 40 _H P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_PUDSEL Reset: FF _H P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_PUDEN Reset: 04 _H P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80 _H	P0_ALTSEL0 Reset: 00 _H P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_ALTSEL1 Reset: 00 _H P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_ALTSEL0 Reset: 00 _H P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91 _H	P1_ALTSEL1 Reset: 00 _H P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_ALTSEL0 Reset: 00 _H P5 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93 _H	P5_ALTSEL1 Reset: 00 _H P5 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_ALTSEL0 Reset: 00 _H P3 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_ALTSEL1 Reset: 00 _H P3 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_ALTSEL0 Reset: 00 _H P4 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_ALTSEL1 Reset: 00 _H P4 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 3										
80 _H	P0_OD Reset: 00 _H P0 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_DS Reset: FF _H P0 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_OD Reset: 00 _H P1 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Functional Description
Table 7 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
91 _H	P1_DS Reset: FF_H P1 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_OD Reset: 00_H P5 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93 _H	P5_DS Reset: FF_H P5 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_OD Reset: 00_H P3 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_DS Reset: FF_H P3 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_OD Reset: 00_H P4 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_DS Reset: FF_H P4 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.5 ADC Registers

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 8 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
D1 _H	ADC_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
CA _H	ADC_GLOBCTR Reset: 30_H Global Control Register	Bit Field	ANON	DW	CTC		0			
		Type	rw	rw	rw		r			
CB _H	ADC_GLOBSTR Reset: 00_H Global Status Register	Bit Field	0		CHNR			0	SAMP LE	BUSY
		Type	r		rh			r	rh	rh
CC _H	ADC_PRAR Reset: 00_H Priority and Arbitration Register	Bit Field	ASEN 1	ASEN 0	0	ARBM	CSM1	PRI01	CSM0	PRI00
		Type	rw	rw	r	rw	rw	rw	rw	rw
CD _H	ADC_LCBR Reset: B7_H Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE _H	ADC_INPCR0 Reset: 00_H Input Class 0 Register	Bit Field	STC							
		Type	rw							

Functional Description
Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CF _H	ADC_ETRCR Reset: 00 _H External Trigger Control Register	Bit Field	SYNE N1	SYNE N0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, PAGE 1										
CA _H	ADC_CHCTR0 Reset: 00 _H Channel Control Register 0	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CB _H	ADC_CHCTR1 Reset: 00 _H Channel Control Register 1	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CC _H	ADC_CHCTR2 Reset: 00 _H Channel Control Register 2	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CD _H	ADC_CHCTR3 Reset: 00 _H Channel Control Register 3	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CE _H	ADC_CHCTR4 Reset: 00 _H Channel Control Register 4	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CF _H	ADC_CHCTR5 Reset: 00 _H Channel Control Register 5	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D2 _H	ADC_CHCTR6 Reset: 00 _H Channel Control Register 6	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D3 _H	ADC_CHCTR7 Reset: 00 _H Channel Control Register 7	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
RMAP = 0, PAGE 2										
CA _H	ADC_RESR0L Reset: 00 _H Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB _H	ADC_RESR0H Reset: 00 _H Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC _H	ADC_RESR1L Reset: 00 _H Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD _H	ADC_RESR1H Reset: 00 _H Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE _H	ADC_RESR2L Reset: 00 _H Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF _H	ADC_RESR2H Reset: 00 _H Result Register 2 High	Bit Field	RESULT							
		Type	rh							
D2 _H	ADC_RESR3L Reset: 00 _H Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
D3 _H	ADC_RESR3H Reset: 00 _H Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										

Functional Description
Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CA _H	ADC_RESRA0L Reset: 00 _H Result Register 0, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB _H	ADC_RESRA0H Reset: 00 _H Result Register 0, View A High	Bit Field	RESULT							
		Type	rh							
CC _H	ADC_RESRA1L Reset: 00 _H Result Register 1, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD _H	ADC_RESRA1H Reset: 00 _H Result Register 1, View A High	Bit Field	RESULT							
		Type	rh							
CE _H	ADC_RESRA2L Reset: 00 _H Result Register 2, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF _H	ADC_RESRA2H Reset: 00 _H Result Register 2, View A High	Bit Field	RESULT							
		Type	rh							
D2 _H	ADC_RESRA3L Reset: 00 _H Result Register 3, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
D3 _H	ADC_RESRA3H Reset: 00 _H Result Register 3, View A High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 4										
CA _H	ADC_RCR0 Reset: 00 _H Result Control Register 0	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CB _H	ADC_RCR1 Reset: 00 _H Result Control Register 1	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CC _H	ADC_RCR2 Reset: 00 _H Result Control Register 2	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CD _H	ADC_RCR3 Reset: 00 _H Result Control Register 3	Bit Field	VFCT R	WFR	0	IEN	0			DRCT R
		Type	rw	rw	r	rw	r			rw
CE _H	ADC_VFCR Reset: 00 _H Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA _H	ADC_CHINFR Reset: 00 _H Channel Interrupt Flag Register	Bit Field	CHINF 7	CHINF 6	CHINF 5	CHINF 4	CHINF 3	CHINF 2	CHINF 1	CHINF 0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB _H	ADC_CHINCR Reset: 00 _H Channel Interrupt Clear Register	Bit Field	CHINC 7	CHINC 6	CHINC 5	CHINC 4	CHINC 3	CHINC 2	CHINC 1	CHINC 0
		Type	w	w	w	w	w	w	w	w
CC _H	ADC_CHINSR Reset: 00 _H Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w

Functional Description
Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CD _H	ADC_CHINPR Reset: 00 _H Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE _H	ADC_EVINFR Reset: 00 _H Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF _H	ADC_EVINCR Reset: 00 _H Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
D2 _H	ADC_EVINSR Reset: 00 _H Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
D3 _H	ADC_EVINPR Reset: 00 _H Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA _H	ADC_CRCR1 Reset: 00 _H Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB _H	ADC_CRPR1 Reset: 00 _H Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC _H	ADC_CRMR1 Reset: 00 _H Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD _H	ADC_QMR0 Reset: 00 _H Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE _H	ADC_QSR0 Reset: 20 _H Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF _H	ADC_Q0R0 Reset: 00 _H Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QBUR0 Reset: 00 _H Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QINR0 Reset: 00 _H Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Functional Description
3.2.4.6 Timer 2 Compare/Capture Unit Registers

The Timer 2 Compare/Capture Unit SFRs can be accessed in the standard memory area (RMAP = 0).

Table 9 T2CCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
C7 _H	T2_PAGE Reset: 00 _H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, PAGE 0										
C0 _H	T2_T2CON Reset: 00 _H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN 2	TR2	C/T ₂	CP/ RL2
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1 _H	T2_T2MOD Reset: 00 _H Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw			rw
C2 _H	T2_RC2L Reset: 00 _H Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3 _H	T2_RC2H Reset: 00 _H Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4 _H	T2_T2L Reset: 00 _H Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
C5 _H	T2_T2H Reset: 00 _H Timer 2 Register High	Bit Field	THL2							
		Type	rwh							
C6 _H	T2_T2CON1 Reset: 03 _H Timer 2 Control Register 1	Bit Field	0						TF2EN	EXF2E N
		Type	r						rw	rw
RMAP = 0, PAGE 1										
C0 _H	T2CCU_CCEN Reset: 00 _H T2CCU Capture/Compare Enable Register	Bit Field	CCM3		CCM2		CCM1		CCM0	
		Type	rw		rw		rw		rw	
C1 _H	T2CCU_CCTBSEL Reset: 00 _H T2CCU Capture/Compare Time Base Select Register	Bit Field	CASC	CCTT OV	CCTB 5	CCTB 4	CCTB 3	CCTB 2	CCTB 1	CCTB 0
		Type	rw	rwh	rw	rw	rw	rw	rw	rw
C2 _H	T2CCU_CCTRELL Reset: 00 _H T2CCU Capture/Compare Timer Reload Register Low	Bit Field	CCTREL							
		Type	rw							
C3 _H	T2CCU_CCTRELH Reset: 00 _H T2CCU Capture/Compare Timer Reload Register High	Bit Field	CCTREL							
		Type	rw							
C4 _H	T2CCU_CCTL Reset: 00 _H T2CCU Capture/Compare Timer Register Low	Bit Field	CCT							
		Type	rwh							

Functional Description

Table 9 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
C5 _H	T2CCU_CCTH Reset: 00 _H T2CCU Capture/Compare Timer Register High	Bit Field	CCT								
		Type	rwh								
C6 _H	T2CCU_CCTCON Reset: 00 _H T2CCU Capture/Compare Timer Control Register	Bit Field	CCTPRE				CCTO VF	CCTO VEN	TIMSY N	CCTS T	
		Type	rw				rwh	rw	rw	rw	rw
RMAP = 0, PAGE 2											
C0 _H	T2CCU_COSHDW Reset: 00 _H T2CCU Capture/compare Enable Register	Bit Field	ENSH DW	TXOV	COOU T5	COOU T4	COOU T3	COOU T2	COOU T1	COOU T0	
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	
C1 _H	T2CCU_CC0L Reset: 00 _H T2CCU Capture/Compare Register 0 Low	Bit Field	CCVALL								
		Type	rwh								
C2 _H	T2CCU_CC0H Reset: 00 _H T2CCU Capture/compare Register 0 High	Bit Field	CCVALH								
		Type	rwh								
C3 _H	T2CCU_CC1L Reset: 00 _H T2CCU Capture/compare Register 1 Low	Bit Field	CCVALL								
		Type	rwh								
C4 _H	T2CCU_CC1H Reset: 00 _H T2CCU Capture/compare Register 1 High	Bit Field	CCVALH								
		Type	rwh								
C5 _H	T2CCU_CC2L Reset: 00 _H T2CCU Capture/compare Register 2 Low	Bit Field	CCVALL								
		Type	rwh								
C6 _H	T2CCU_CC2H Reset: 00 _H T2CCU Capture/compare Register 2 High	Bit Field	CCVALH								
		Type	rwh								
RMAP = 0, PAGE 3											
C0 _H	T2CCU_COCON Reset: 00 _H T2CCU Compare Control Register	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	COMOD		
		Type	rw	rw	rwh	rwh	rw	rw	rw		
C1 _H	T2CCU_CC3L Reset: 00 _H T2CCU Capture/compare Register 3 Low	Bit Field	CCVALL								
		Type	rwh								
C2 _H	T2CCU_CC3H Reset: 00 _H T2CCU Capture/compare Register 3 High	Bit Field	CCVALH								
		Type	rwh								
C3 _H	T2CCU_CC4L Reset: 00 _H T2CCU Capture/compare Register 4 Low	Bit Field	CCVALL								
		Type	rwh								
C4 _H	T2CCU_CC4H Reset: 00 _H T2CCU Capture/compare Register 4 High	Bit Field	CCVALH								
		Type	rwh								
C5 _H	T2CCU_CC5L Reset: 00 _H T2CCU Capture/compare Register 5 Low	Bit Field	CCVALL								
		Type	rwh								
C6 _H	T2CCU_CC5H Reset: 00 _H T2CCU Capture/compare Register 5 High	Bit Field	CCVALH								
		Type	rwh								

Functional Description
Table 9 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 4										
C2 _H	T2CCU_CCTDTCL Reset: 00 _H T2CCU Capture/Compare Timer Dead-Time Control Register Low	Bit Field	DTM							
		Type	rw							
C3 _H	T2CCU_CCTDTCH Reset: 00 _H T2CCU Capture/Compare Timer Dead-Time Control Register High	Bit Field	DTRES	DTR2	DTR1	DTR0	DTLEV	DTE2	DTE1	DTE0
		Type	rwh	rh	rh	rh	rw	rw	rw	rw

3.2.4.7 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 10 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP = 1											
C0 _H	T21_T2CON Reset: 00 _H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/T2	CP/RL2	
		Type	rwh	rwh	r		rw	rwh	rw	rw	
C1 _H	T21_T2MOD Reset: 00 _H Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN	
		Type	rw	rw	rw	rw	rw	rw	rw	rw	
C2 _H	T21_RC2L Reset: 00 _H Timer 2 Reload/Capture Register Low	Bit Field	RC2								
		Type	rwh								
C3 _H	T21_RC2H Reset: 00 _H Timer 2 Reload/Capture Register High	Bit Field	RC2								
		Type	rwh								
C4 _H	T21_T2L Reset: 00 _H Timer 2 Register Low	Bit Field	THL2								
		Type	rwh								
C5 _H	T21_T2H Reset: 00 _H Timer 2 Register High	Bit Field	THL2								
		Type	rwh								
C6 _H	T21_T2CON1 Reset: 03 _H Timer 2 Control Register 1	Bit Field	0					TF2EN	EXF2EN		
		Type	r					rw	rw		

3.2.4.8 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

Functional Description
Table 11 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
C8 _H	SCON Serial Channel Control Register Reset: 00 _H	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
C9 _H	SBUF Serial Data Buffer Register Reset: 00 _H	Bit Field	VAL							
		Type	rwh							
CA _H	BCON Baud Rate Control Register Reset: 00 _H	Bit Field	0				BRPRE			R
		Type	r				rw			rw
CB _H	BG Baud Rate Timer/Reload Register Reset: 00 _H	Bit Field	BR_VALUE							
		Type	rwh							
CC _H	FDCON Fractional Divider Control Register Reset: 00 _H	Bit Field	0				NDOV	FDM	FDEN	
		Type	r				rwh	rw	rw	
CD _H	FDSTEP Fractional Divider Reload Register Reset: 00 _H	Bit Field	STEP							
		Type	rw							
CE _H	FDRES Fractional Divider Result Register Reset: 00 _H	Bit Field	RESULT							
		Type	rh							
CF _H	SCON1 Serial Channel Control Register 1 Reset: 07 _H	Bit Field	0				NDOV EN	TIEN	RIEN	
		Type	r				rw	rw	rw	

3.2.4.9 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
A9 _H	SSC_PISEL Port Input Select Register Reset: 00 _H	Bit Field	0				CIS	SIS	MIS	
		Type	r				rw	rw	rw	
AA _H	SSC_CONL Control Register Low Programming Mode Reset: 00 _H	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
AA _H	SSC_CONL Control Register Low Operating Mode Reset: 00 _H	Bit Field	0				BC			
		Type	r				rh			
AB _H	SSC_CONH Control Register High Programming Mode Reset: 00 _H	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
		Type	rw	rw	r	rw	rw	rw	rw	rw
AB _H	SSC_CONH Control Register High Operating Mode Reset: 00 _H	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
		Type	rw	rw	r	rh	rwh	rwh	rwh	rwh

Functional Description
Table 12 SSC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
AC _H	SSC_TBL Reset: 00_H Transmitter Buffer Register Low	Bit Field	TB_VALUE							
		Type	rw							
AD _H	SSC_RBL Reset: 00_H Receiver Buffer Register Low	Bit Field	RB_VALUE							
		Type	rh							
AE _H	SSC_BRL Reset: 00_H Baud Rate Timer Reload Register Low	Bit Field	BR_VALUE							
		Type	rw							
AF _H	SSC_BRH Reset: 00_H Baud Rate Timer Reload Register High	Bit Field	BR_VALUE							
		Type	rw							

3.2.4.10 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 13 CAN Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
D8 _H	ADCON Reset: 00_H CAN Address/Data Control Register	Bit Field	V3	V2	V1	V0	AUAD		BSY	RWEN
		Type	rw	rw	rw	rw	rw		rh	rw
D9 _H	ADL Reset: 00_H CAN Address Register Low	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
DA _H	ADH Reset: 00_H CAN Address Register High	Bit Field	0				CA13	CA12	CA11	CA10
		Type	r				rwh	rwh	rwh	rwh
DB _H	DATA0 Reset: 00_H CAN Data Register 0	Bit Field	CD							
		Type	rwh							
DC _H	DATA1 Reset: 00_H CAN Data Register 1	Bit Field	CD							
		Type	rwh							
DD _H	DATA2 Reset: 00_H CAN Data Register 2	Bit Field	CD							
		Type	rwh							
DE _H	DATA3 Reset: 00_H CAN Data Register 3	Bit Field	CD							
		Type	rwh							

3.2.4.11 OCDS Registers

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

Functional Description

Table 14 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
E9 _H	MMCR2 Reset: 8U_H Monitor Mode Control 2 Register	Bit Field	STMO DE	EXBC	DSUS P	MBCO N	ALTDI	MMEP	MMOD E	JENA
		Type	rw	rw	rw	rwh	rw	rwh	rh	rh
EA _H	MEXTCR Reset: 0U_H Memory Extension Control Register	Bit Field	0				BANKBPx			
		Type	r				rw			
EB _H	MMWR1 Reset: 00_H Monitor Work Register 1	Bit Field	MMWR1							
		Type	rw							
EC _H	MMWR2 Reset: 00_H Monitor Work Register 2	Bit Field	MMWR2							
		Type	rw							
F1 _H	MMCR Reset: 00_H Monitor Mode Control Register	Bit Field	MEXIT _P	MEXIT	0	MSTE P	MRAM S_P	MRAM S	TRF	RRF
		Type	w	rwh	r	rw	w	rwh	rh	rh
F2 _H	MMSR Reset: 00_H Monitor Mode Status Register	Bit Field	MBCA M	MBCIN	EXBF	SWBF	HWB3 F	HWB2 F	HWB1 F	HWB0 F
		Type	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
F3 _H	MMBPCR Reset: 00_H Breakpoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1 C	HWB0C	
		Type	rw	rw		rw		rw	rw	
F4 _H	MMICR Reset: 00_H Monitor Mode Interrupt Control Register	Bit Field	DVEC T	DRET R	COMR ST	MSTS EL	MMUI E_P	MMUI E	RRIE_ P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
F5 _H	MMDR Reset: 00_H Monitor Mode Data Transfer Register Receive	Bit Field	MMRR							
		Type	rh							
F6 _H	HWBPSR Reset: 00_H Hardware Breakpoints Select Register	Bit Field	0			BPSEL _P	BPSEL			
		Type	r			w	rw			
F7 _H	HWBPDR Reset: 00_H Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							

3.2.4.12 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
D1 _H	FCON Reset: 10_H P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D2 _H	ECON Reset: 10_H D-Flash Control Register	Bit Field	0	EEBS Y	YE	1	NVST R	MAS1	ERAS E	PROG
		Type	r	rh	rwh	r	rw	rw	rw	rw
D3 _H	FCS Reset: 80_H Flash Control and Status Register	Bit Field	1	SBEIE	FTEN	0	EEDE RR	EESE RR	FDER R	FSER R
		Type	r	rw	rwh	r	rwh	rwh	rwh	rwh
D4 _H	FEAL Reset: 00_H Flash Error Address Register, Low Byte	Bit Field	ECCEADDR							
		Type	rh							
D5 _H	FEAH Reset: 00_H Flash Error Address Register, High Byte	Bit Field	ECCEADDR							
		Type	rh							
D6 _H	FTVAL Reset: 78_H Flash Timer Value Register	Bit Field	MODE	OFVAL						
		Type	rw	rw						
DD _H	FCS1 Reset: 00_H Flash Control and Status Register 1	Bit Field	0							EEAB ORT
		Type	r							rwh

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The pagination of the Flash memory allows each page to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width
 - of 1-byte for D-Flash and 2-bytes for P-Flash
- 1-page minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all ones)
- Operating supply voltage: $2.5\text{ V} \pm 7.5\%$
- Read access time: $1 \times t_{\text{CCLK}} = 38\text{ ns}^1$
- Program time for 1 wordline: 1.6 ms^2
- Page erase time: 20 ms
- Mass erase time: 200 ms

1) Values shown here are typical values. $f_{\text{sys}} = 144\text{ MHz} \pm 7.5\%$ ($f_{\text{CCLK}} = 24\text{ MHz} \pm 7.5\%$) is the maximum frequency range for Flash read access.

2) Values shown here are typical values. $f_{\text{sys}} = 144\text{ MHz} \pm 7.5\%$ ($f_{\text{CCLK}} = 24\text{ MHz} \pm 7.5\%$) is the typical frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

Functional Description

Table 16 shows the Flash data retention and endurance targets for Industrial profile.

Table 16 Flash Data Retention and Endurance for Industrial Profile (Operating Conditions apply)

Retention	Endurance ¹⁾²⁾	Size	Remarks
Program Flash			
15 years	1000 cycles	up to 60 Kbytes	
Data Flash			
15 years	1000 cycles	4 Kbytes	
10 years	10,000 cycles	4 Kbytes	
5 years	30,000 cycles	4 Kbytes	
1 year	100,000 cycles	4 Kbytes	

1) In Program Flash, one cycle refers to the programming of all pages in the flash bank and a mass erase.

2) In Data Flash, one cycle refers to the programming of all wordlines in a page and a page erase.

3.3.1 Flash Bank Pagination

The XC858 product family offers Flash devices with 64 Kbytes, 52 Kbytes or 36Kbyte of embedded Flash memory. Each Flash device consists of a Program Flash (P-Flash) and a single Data Flash (D-Flash) bank. P-Flash has 120 pages of 8 wordlines per page with 64 bytes per wordline. D-Flash has 64 pages of 2 wordlines per page with 32 bytes per wordline. Both types can be used for code and data storage. The label "Data" neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different page width and wordline of each Flash bank.

The internal structure of each Flash bank represents a page architecture for flexible erase capability. The minimum erase width is always a complete page. The D-Flash bank is divided into smaller size for extended erasing and reprogramming capability; even numbers for each page size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC858 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 12 to Figure 16 give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

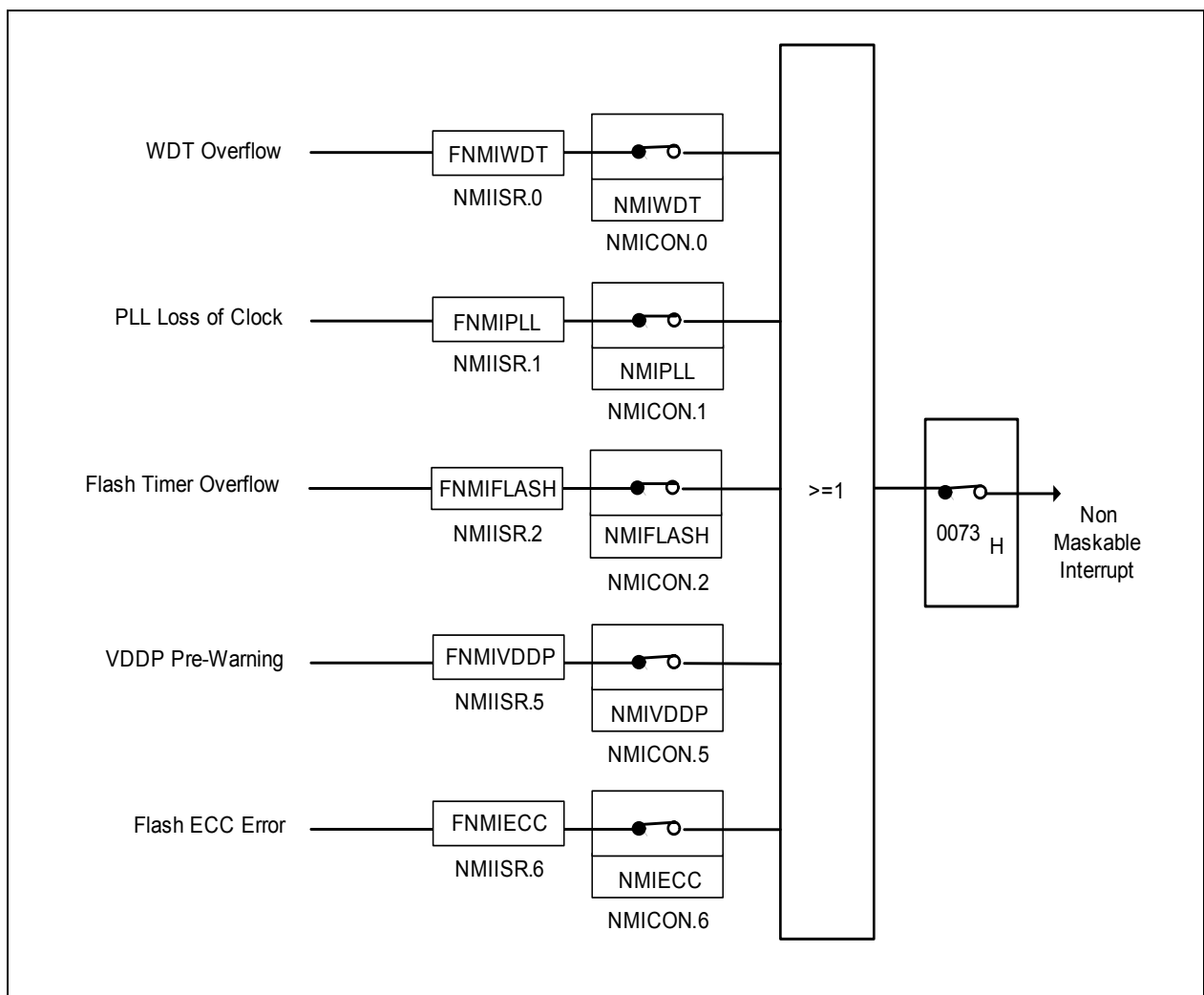


Figure 12 Non-Maskable Interrupt Request Sources

Functional Description

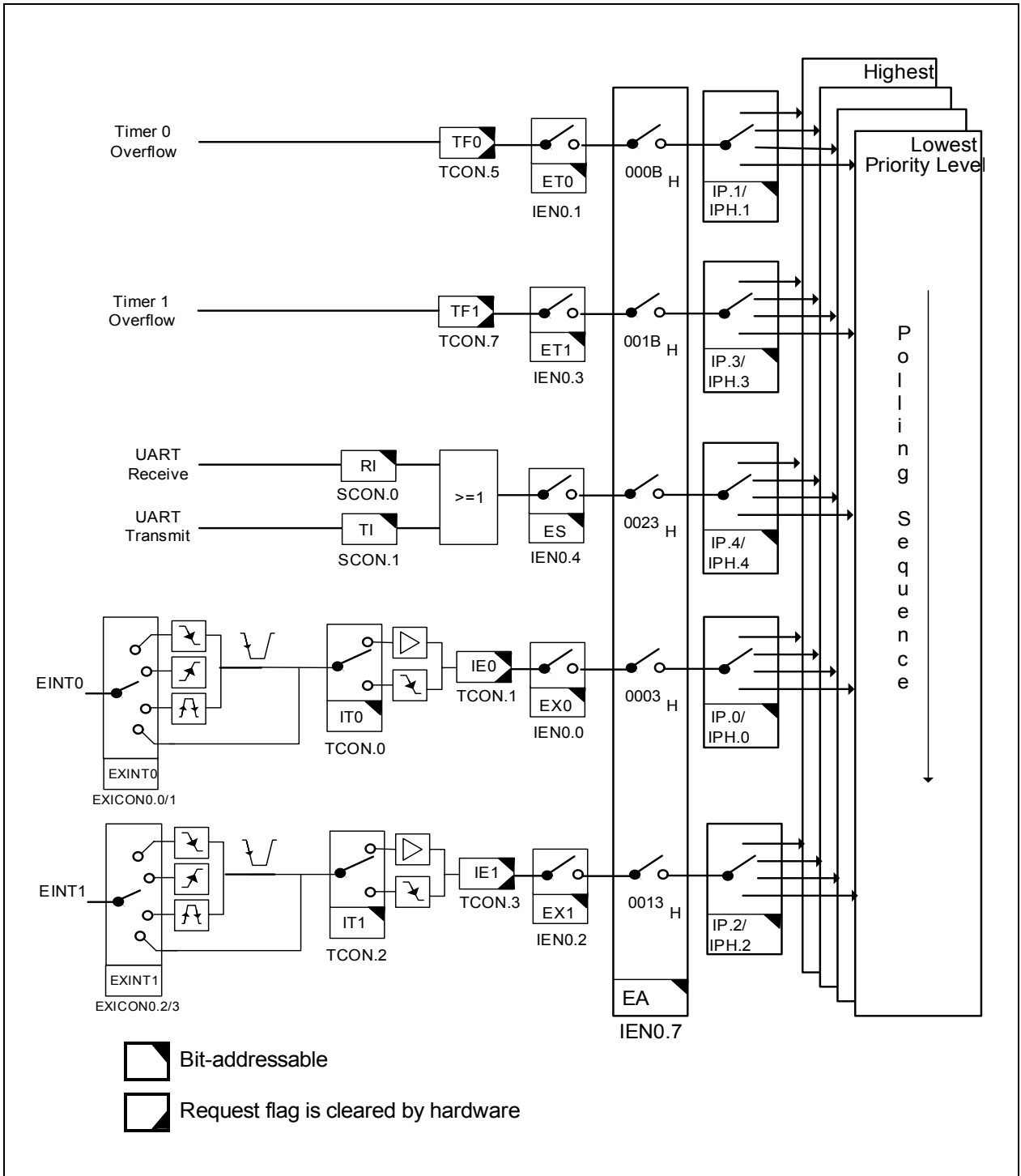


Figure 13 Interrupt Request Sources (Part 1)

Functional Description

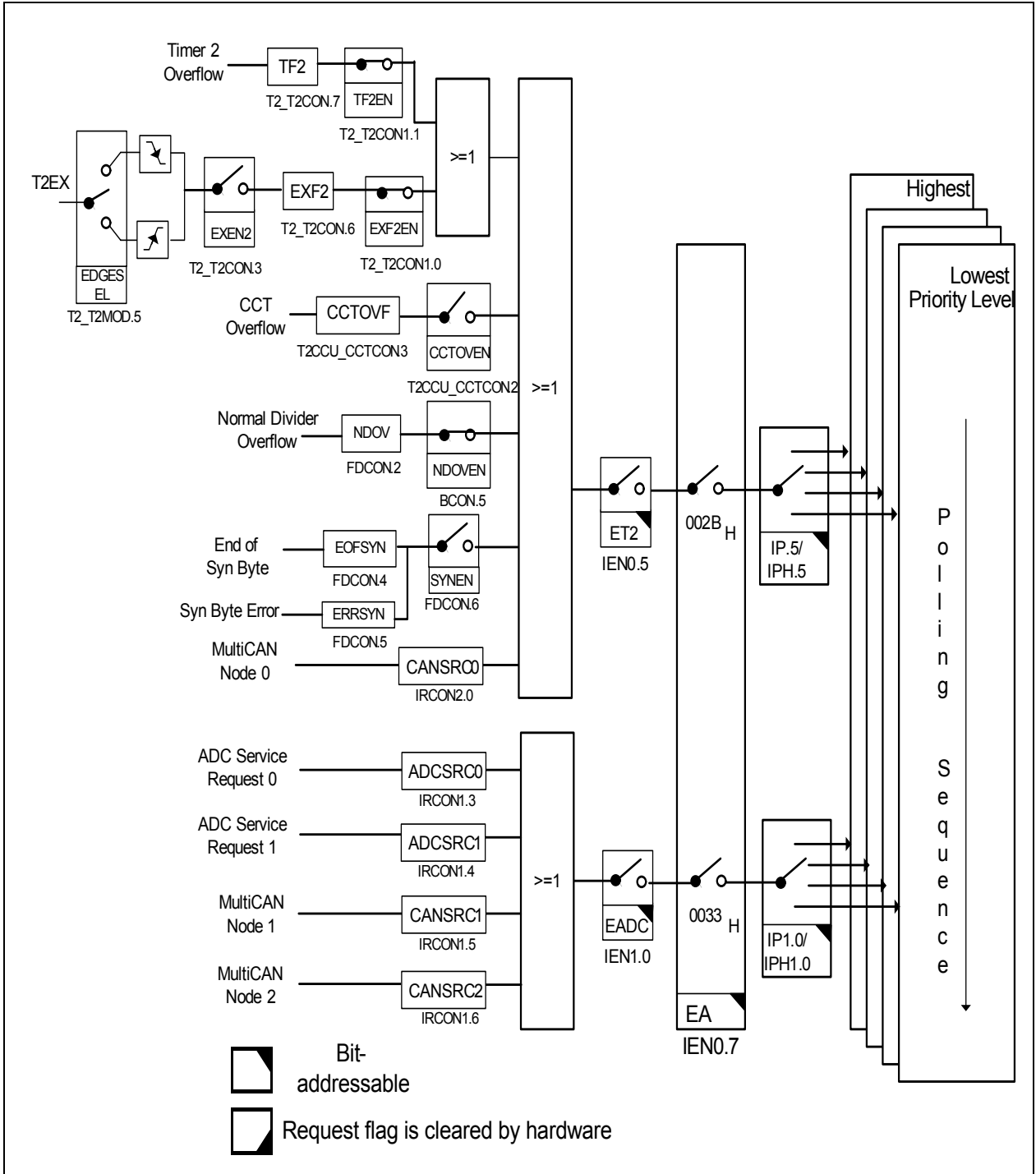


Figure 14 Interrupt Request Sources (Part 2)

Functional Description

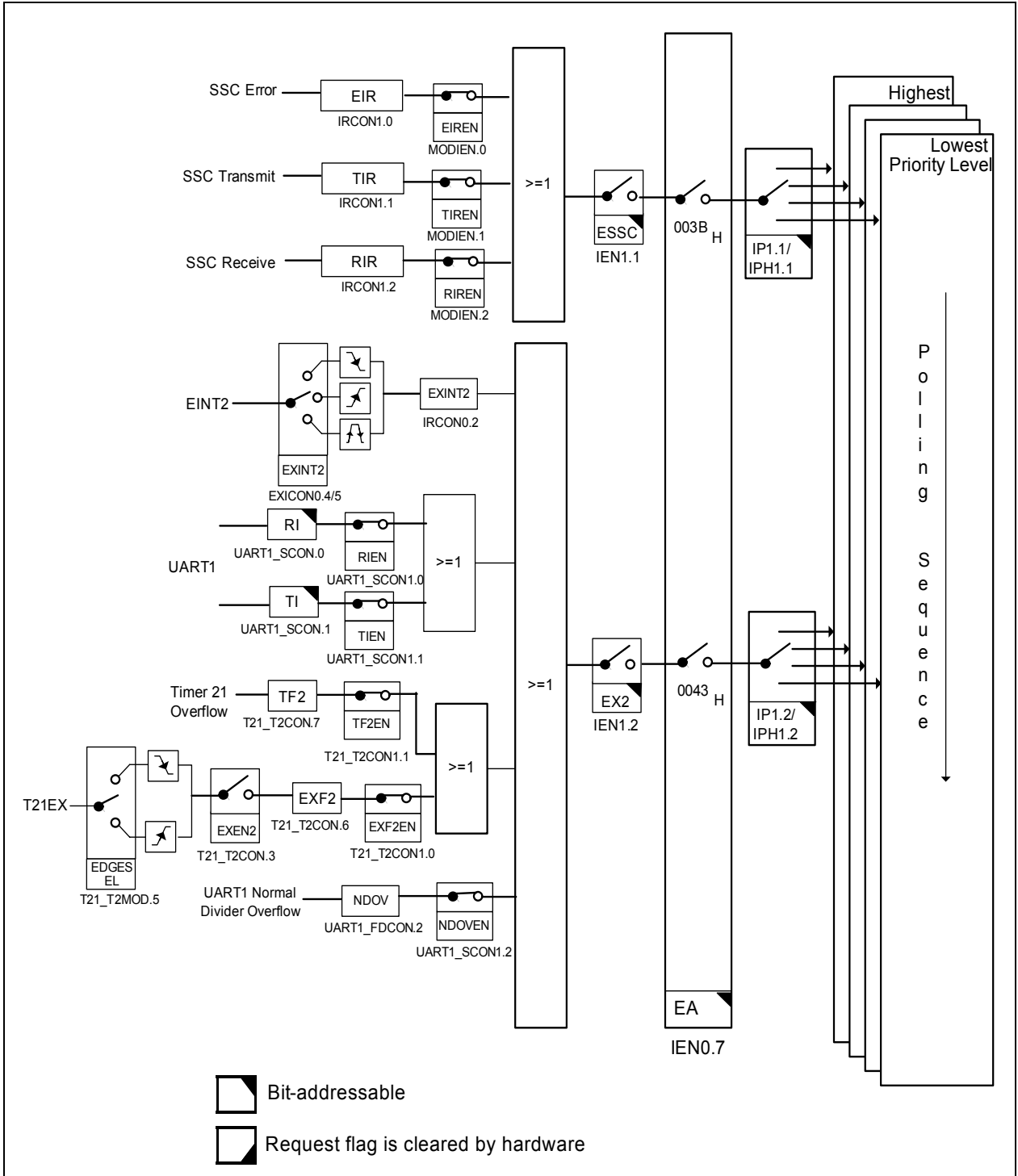


Figure 15 Interrupt Request Sources (Part 3)

Functional Description

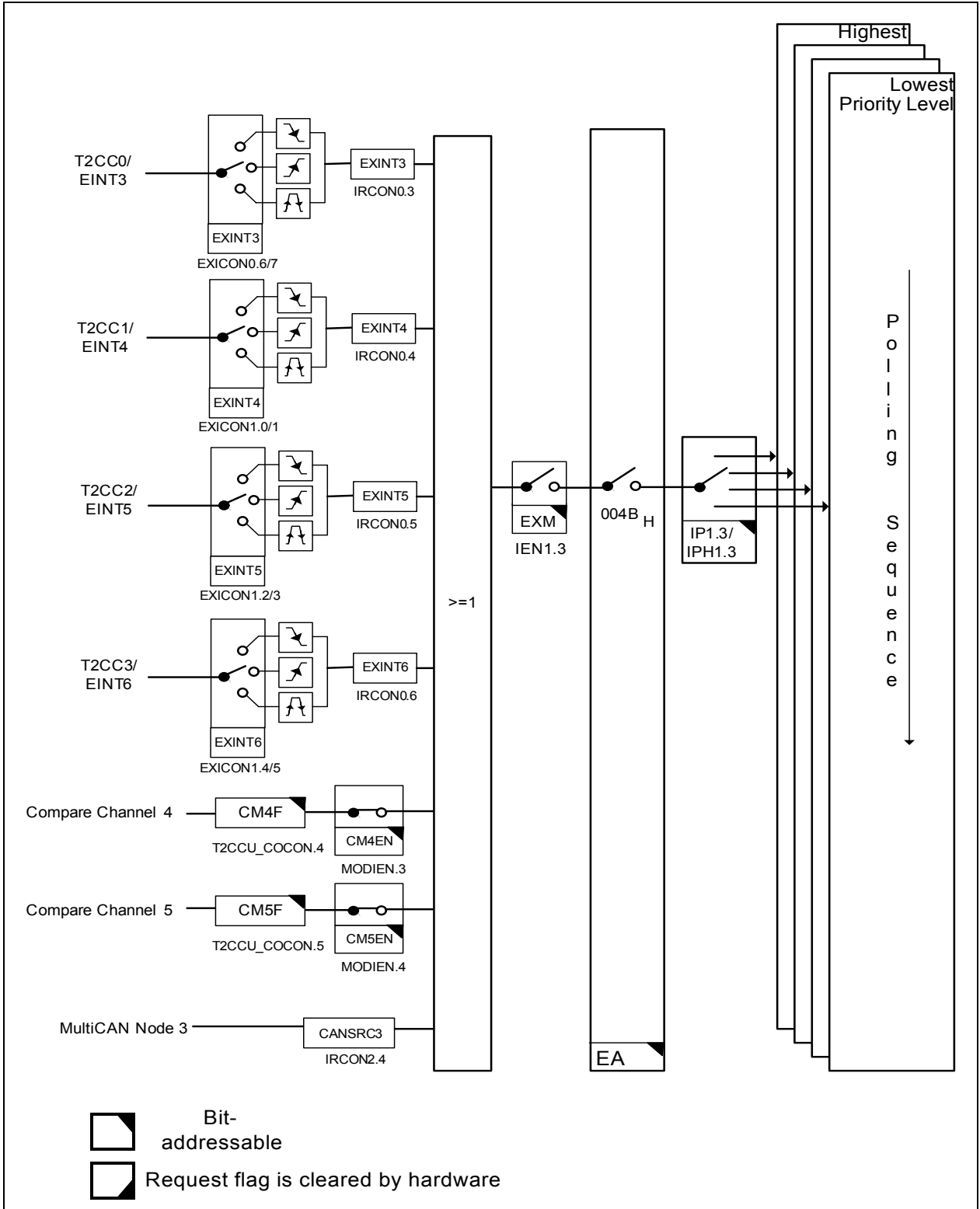


Figure 16 Interrupt Request Sources (Part 4)

Functional Description

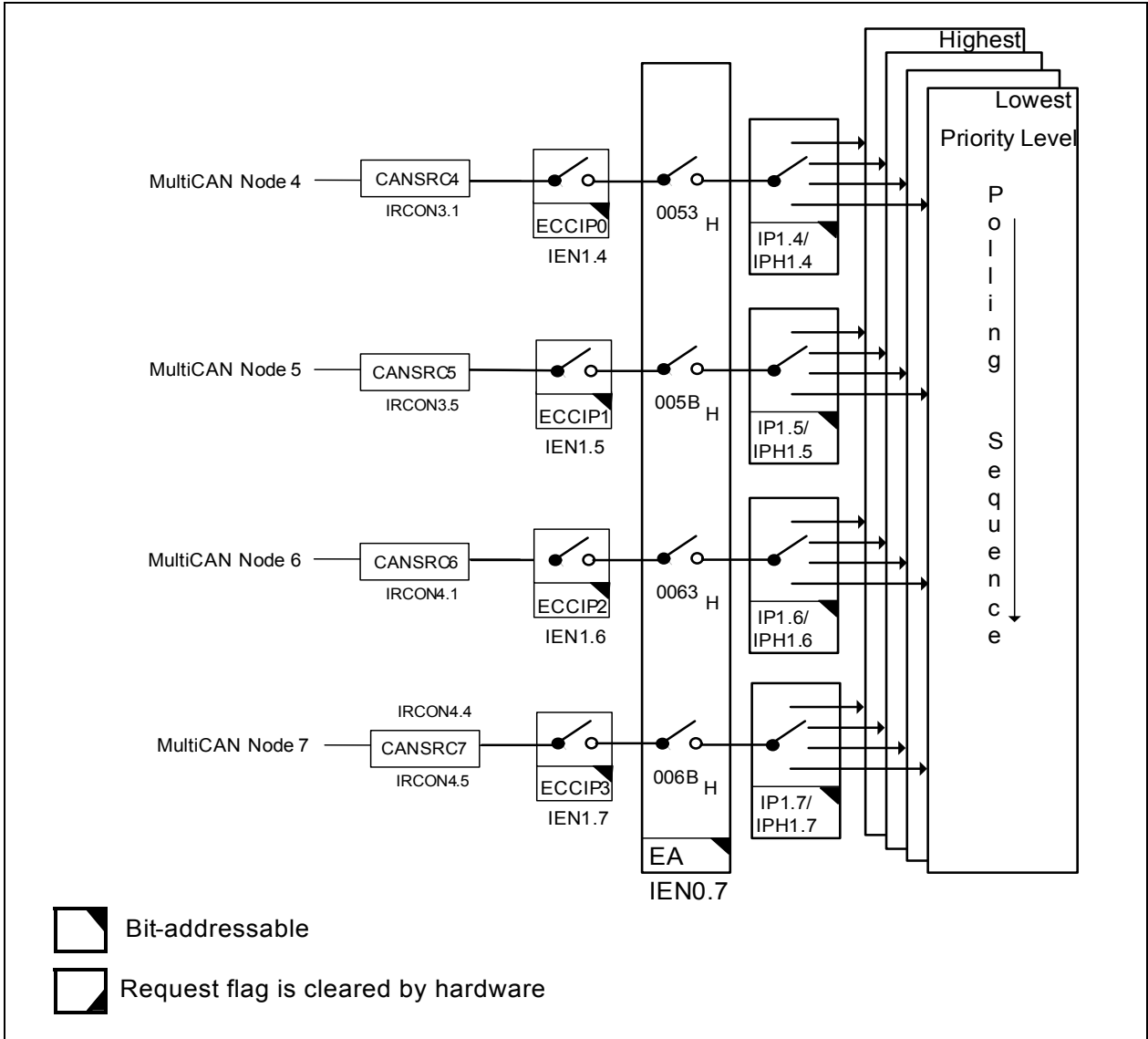


Figure 17 Interrupt Request Sources (Part 5)

3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC858 interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in [Table 17](#).

Table 17 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC858	Enable Bit	SFR
NMI	0073 _H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash Timer NMI	NMIFLASH	
		V _{DDP} Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 _H	External Interrupt 0	EX0	IEN0
XINTR1	000B _H	Timer 0	ET0	
XINTR2	0013 _H	External Interrupt 1	EX1	
XINTR3	001B _H	Timer 1	ET1	
XINTR4	0023 _H	UART	ES	
XINTR5	002B _H	T2CCU	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		

Functional Description
Table 17 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC858	Enable Bit	SFR
XINTR6	0033 _H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	003B _H	SSC	ESSC	
XINTR8	0043 _H	External Interrupt 2	EX2	
		T21		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
XINTR9	004B _H	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		T2CCU		
		MultiCAN Node 3		
XINTR10	0053 _H	MultiCAN Node 4	ECCIP0	
XINTR11	005B _H	MultiCAN Node 5	ECCIP1	
XINTR12	0063 _H	MultiCAN Node 6	ECCIP2	
XINTR13	006B _H	MultiCAN Node 7	ECCIP3	

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in [Table 18](#).

Table 18 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
T2CCU, UART Normal Divider Overflow, MultiCAN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
MultiCAN interrupt	11
MultiCAN Interrupt	12
MultiCAN Interrupt	13
MultiCAN Interrupt	14

3.5 Parallel Ports

The XC858 has 40 port pins organized into five parallel ports: Port 0 (P0), Port 1 (P1), Port 3 (P3), Port 4 (P4) and Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. These ports are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected.

Bidirectional Port Features

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Figure 18 shows the structure of a bidirectional port pin.

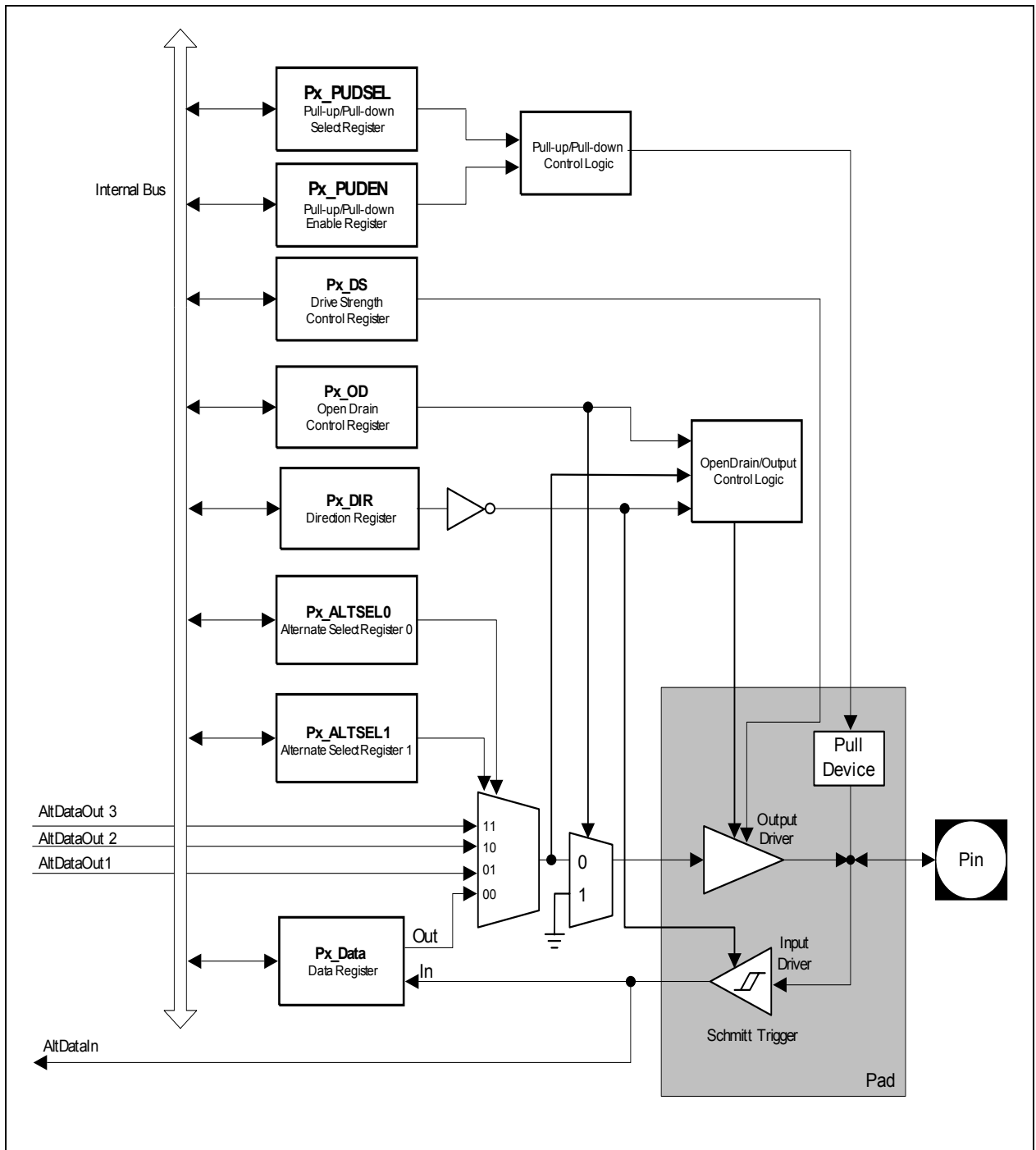


Figure 18 General Structure of Bidirectional Port

3.6 Power Supply System with Embedded Voltage Regulator

The XC858 microcontroller requires two different levels of power supply:

- 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 19 shows the XC858 power supply system. A power supply of 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

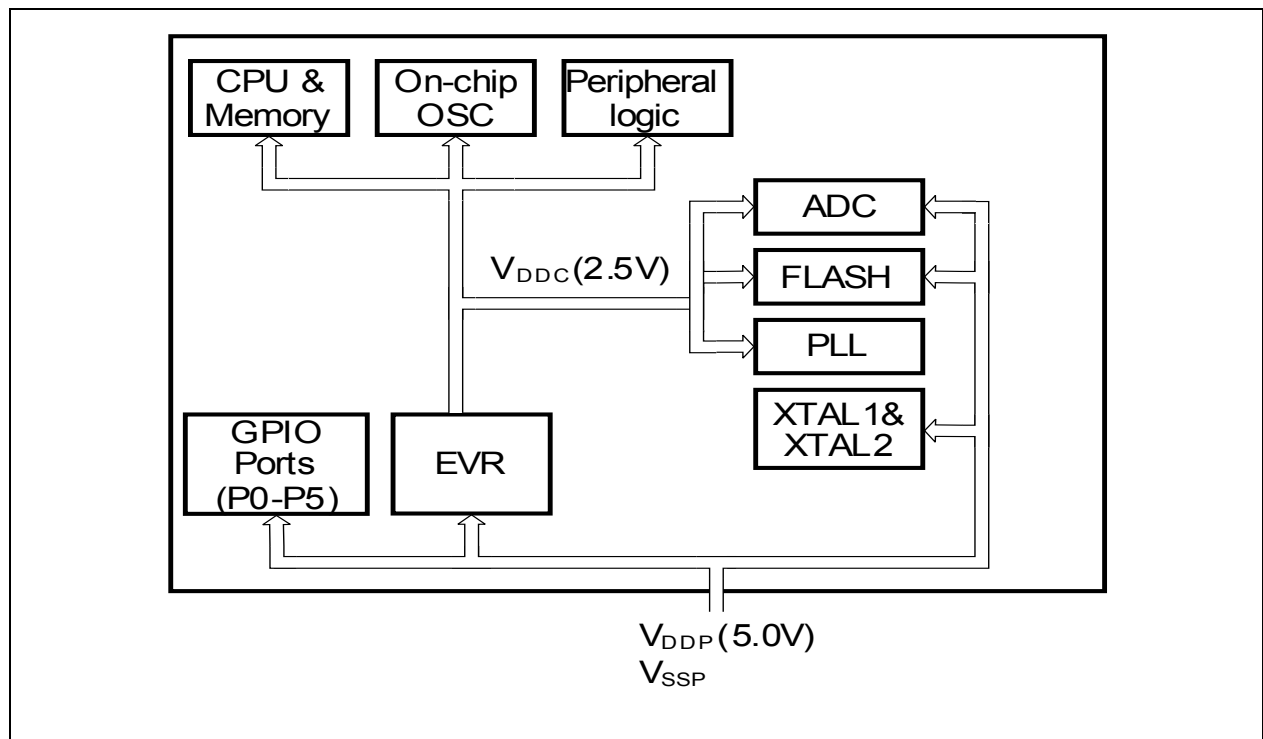


Figure 19 XC858 Power Supply System

EVR Features

- Input voltage (V_{DDP}): 5.0 V
- Output voltage (V_{DDC}): 2.5 V \pm 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDP} prewarning detection
- V_{DDC} brownout detection

3.7 Reset Control

The XC858 has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC858 is first powered up, the status of certain pins (see [Table 20](#)) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

The second type of reset in XC858 is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin **RESET** is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.

3.7.1 Module Reset Behavior

[Table 19](#) lists the functions of the XC858 and the various reset types that affect these functions. The symbol “■” signifies that the particular function is reset to its default state.

Table 19 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core	■	■	■	■	■
Peripherals	■	■	■	■	■
On-Chip Static RAM	Not affected, Reliable	Not affected, Reliable	Not affected, Reliable	Affected, un- reliable	Affected, un- reliable
Oscillator, PLL	■	Not affected	■	■	■
Port Pins	■	■	■	■	■
EVR	The voltage regulator is switched on	Not affected	Not affected	■	■
FLASH	■	■	■	■	■
NMI	Disabled	Disabled	■	■	■

3.7.2 Booting Scheme

When the XC858 is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. **Table 20** shows the available boot options in the XC858.

Table 20 XC858 Boot Selection ¹⁾

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	X	User Mode ²⁾ ; on-chip OSC/PLL non-bypassed	0000 _H
0	0	X	BSL Mode; (UART/ MultiCAN Mode ³⁾⁴⁾ and Alternate BSL Mode ⁵⁾ ; on-chip OSC/PLL non-bypassed	0000 _H
0	1	0	OCDS Mode; on-chip OSC/PLL non-bypassed	0000 _H
1	1	0	User (JTAG) Mode ⁶⁾ ; on-chip OSC/PLL non-bypassed (normal)	0000 _H

- 1) In addition to the pins MBC, TMS and P0.0, TM pin also requires an external pull down for all the boot options.
- 2) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
- 3) UART or MultiCAN BSL is decoded by firmware based on the protocol for product variant with MultiCAN. If no MultiCAN variant, UART BSL is used.
- 4) In MultiCAN BSL mode, the clock source is switched to XTAL by firmware, bypassing the on-chip oscillator. This avoids any frequency invariance with the on-chip oscillator and allows other frequency clock input, thus ensuring accurate baud rate detection (especially at high bit rates).
- 5) Alternate BSL Mode is a user defined BSL code programmed in Flash. It is entered if the AltBSLPassword is valid.
- 6) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC858. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC858, the oscillator can be from either of these two sources: the on-chip oscillator (4 MHz) or the external oscillator (2 MHz to 20 MHz). The term “oscillator” is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default. The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

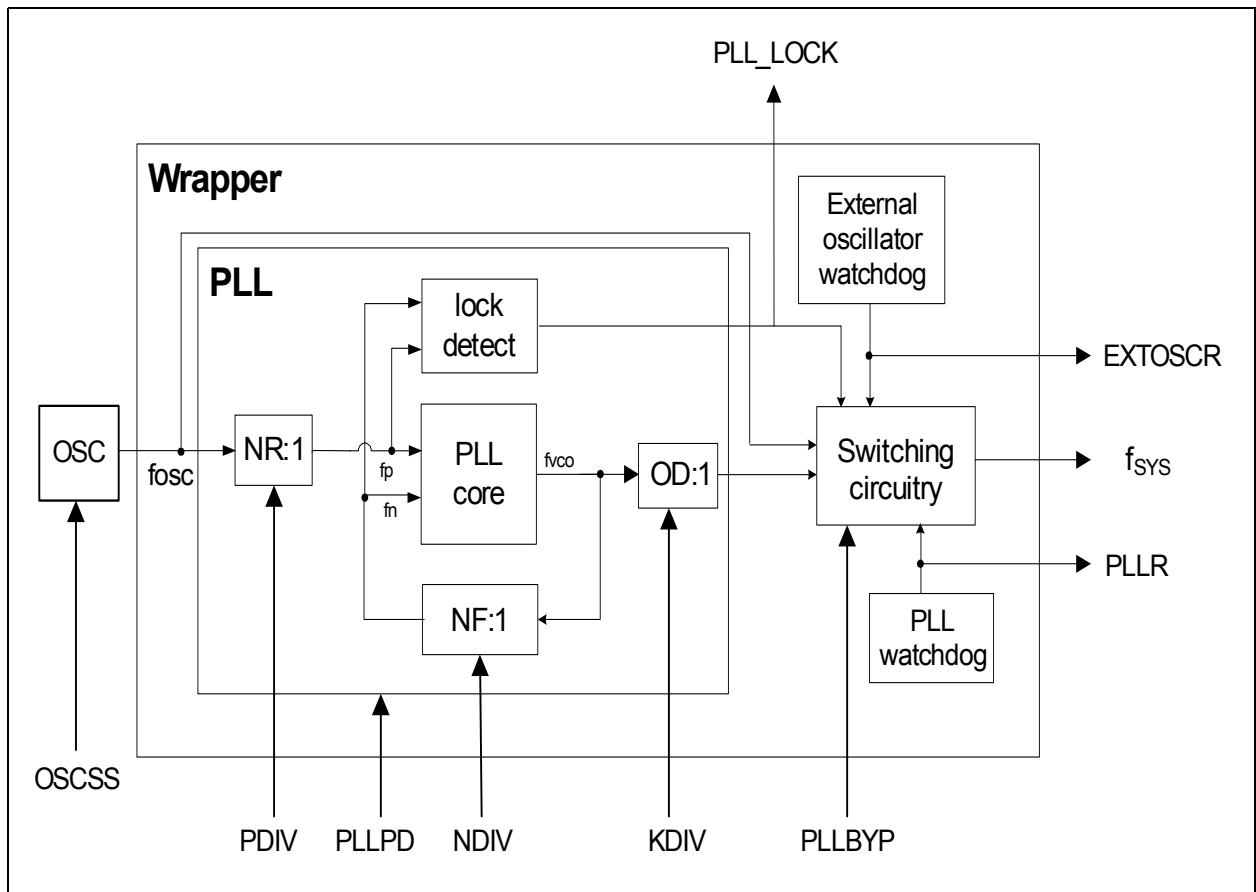


Figure 20 CGU Block Diagram

Direct Drive (PLL Bypass Operation)

During PLL bypass operation, the system clock has the same frequency as the external clock source.

$$(3.1)$$

$$f_{SYS} = f_{OSC}$$

PLL Mode

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must

Functional Description

not be bypassed for this PLL mode. The PLL mode is used during normal system operation.

(3.2)

$$f_{\text{SYS}} = f_{\text{OSC}} \times \frac{\text{NF}}{\text{NR} \times \text{OD}}$$

System Frequency Selection

For the XC858, the value of NF, NR and OD can be selected by bits NDIV, PDIV and KDIV respectively for different oscillator inputs in order to obtain the required f_{sys} . But the combination of these factors must fulfill the following condition:

- $100 \text{ MHz} < f_{\text{VCO}} < 175 \text{ MHz}$
- $800 \text{ kHz} < f_{\text{OSC}} / (2 * \text{NR}) < 8 \text{ MHz}$

Table 21 provides examples on how the typical system frequency of $f_{\text{sys}} = 144 \text{ MHz}$ and maximum frequency of 160 MHz (CPU clock = 24 MHz) can be obtained for the different oscillator sources.

Table 21 System frequency ($f_{\text{sys}} = 144 \text{ MHz}$)

Oscillator	fosc	N	P	K	f _{sys}
On-chip	4 MHz	72	2	1	144 MHz
	4 MHz	80	2	1	160 MHz
External	8 MHz	72	4	1	144 MHz
	6 MHz	72	3	1	144 MHz
	4 MHz	72	2	1	144 MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 2 MHz to 20 MHz . Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2} , and depending on the crystal type, a series resistor R_{X2} , to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. An external feedback resistor R_f is also required in the external oscillator circuitry. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative

Functional Description

resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor. **Figure 21** shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

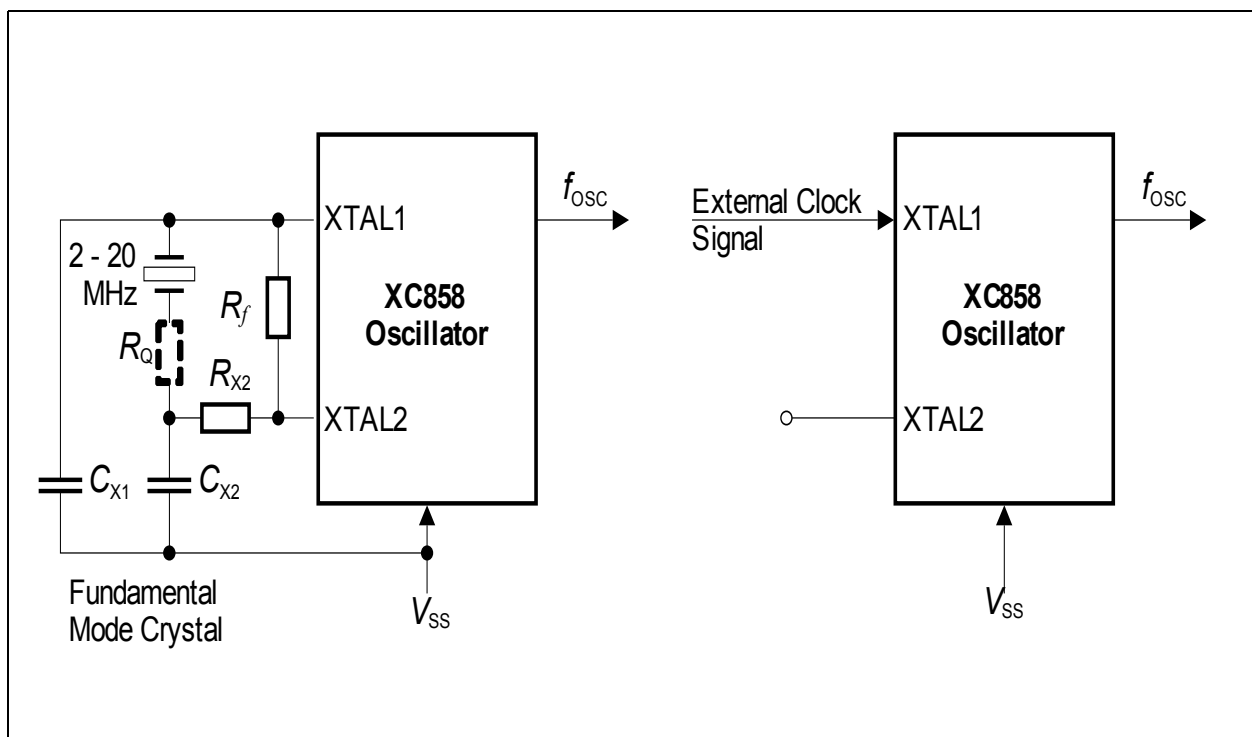


Figure 21 External Oscillator Circuitry

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

Functional Description

For power saving purposes, the clocks may be disabled or slowed down according to [Table 22](#).

Table 22 System frequency ($f_{\text{sys}} = 144 \text{ MHz}$)

Power Saving Mode	Action
Idle	Clock to the CPU is disabled.
Slow-down	Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL.
Power-down	Oscillator and PLL are switched off.

3.9 Power Saving Modes

The power saving modes of the XC858 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see [Figure 23](#)) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

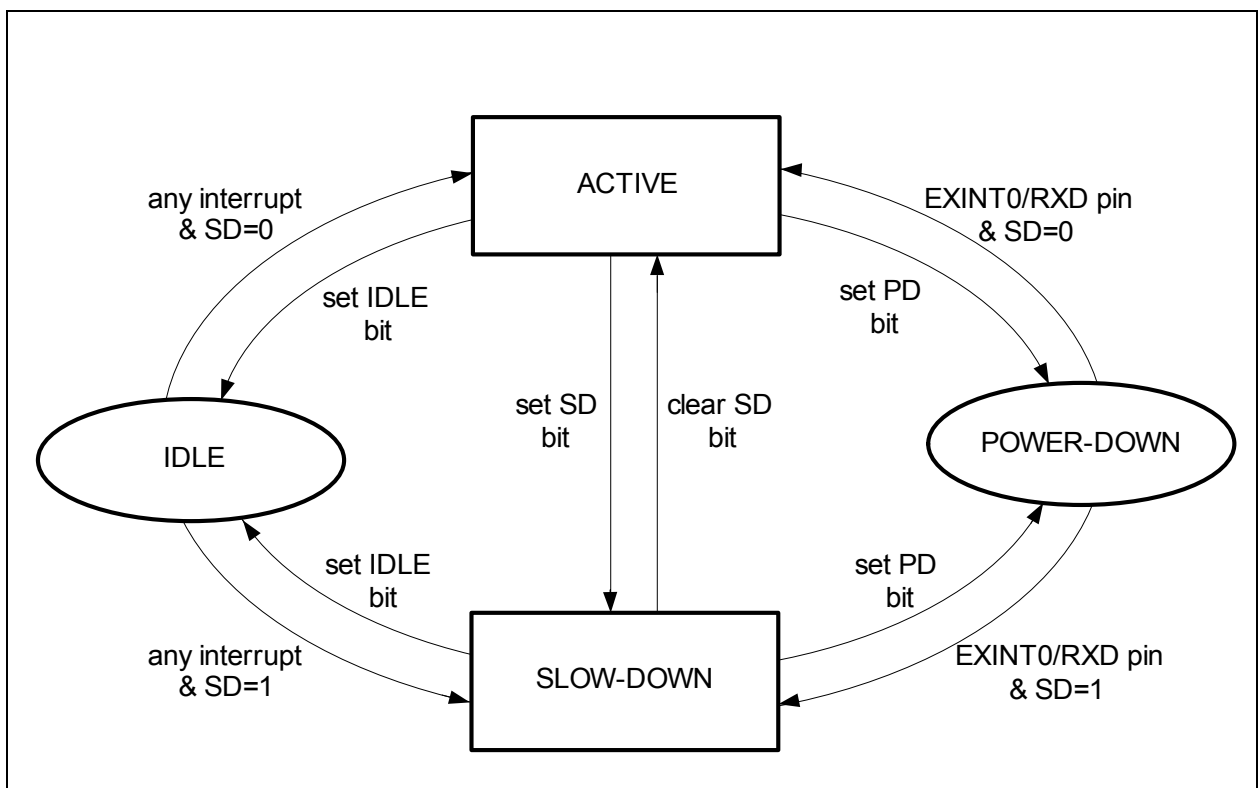


Figure 23 Transition between Power Saving Modes

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC858 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC858 will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access.

Figure 24 shows the block diagram of the WDT unit.

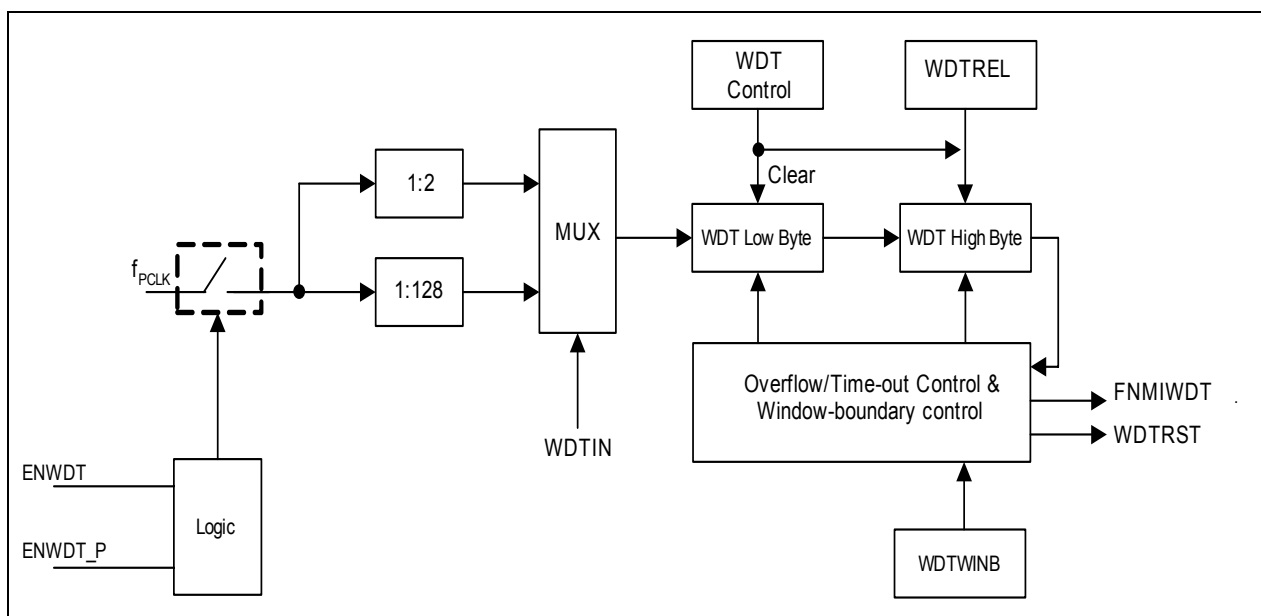


Figure 24 WDT Block Diagram

Functional Description

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2⁸). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT} , between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}} \quad (3.3)$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see [Figure 25](#). This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.

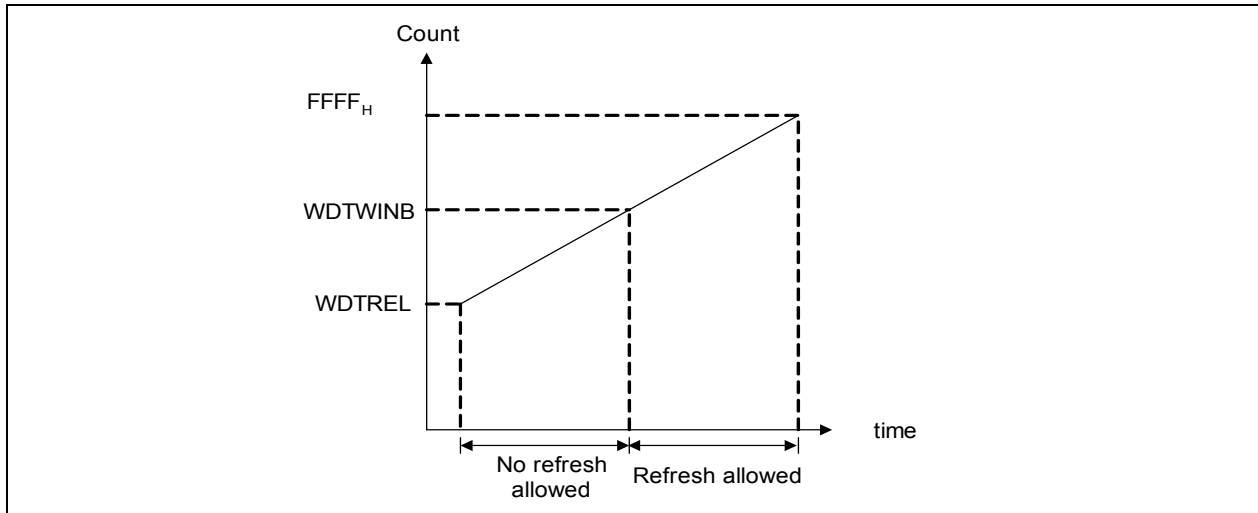


Figure 25 WDT Timing Diagram

Table 23 lists the possible watchdog time ranges that can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 23 Watchdog Time Ranges

Reload value In WDTREL	Prescaler for f_{PCLK}	
	2 (WDTIN = 0)	128 (WDTIN = 1)
	24 MHz	24 MHz
FF _H	21.3 μ s	1.37 ms
7F _H	2.75 ms	176 ms
00 _H	5.46 ms	350 ms

3.11 UART and UART1

The XC858 provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
 - 8-bit or 9-bit data frames, LSB first
 - Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication

Functional Description

- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in [Table 24](#).

Table 24 UART Modes

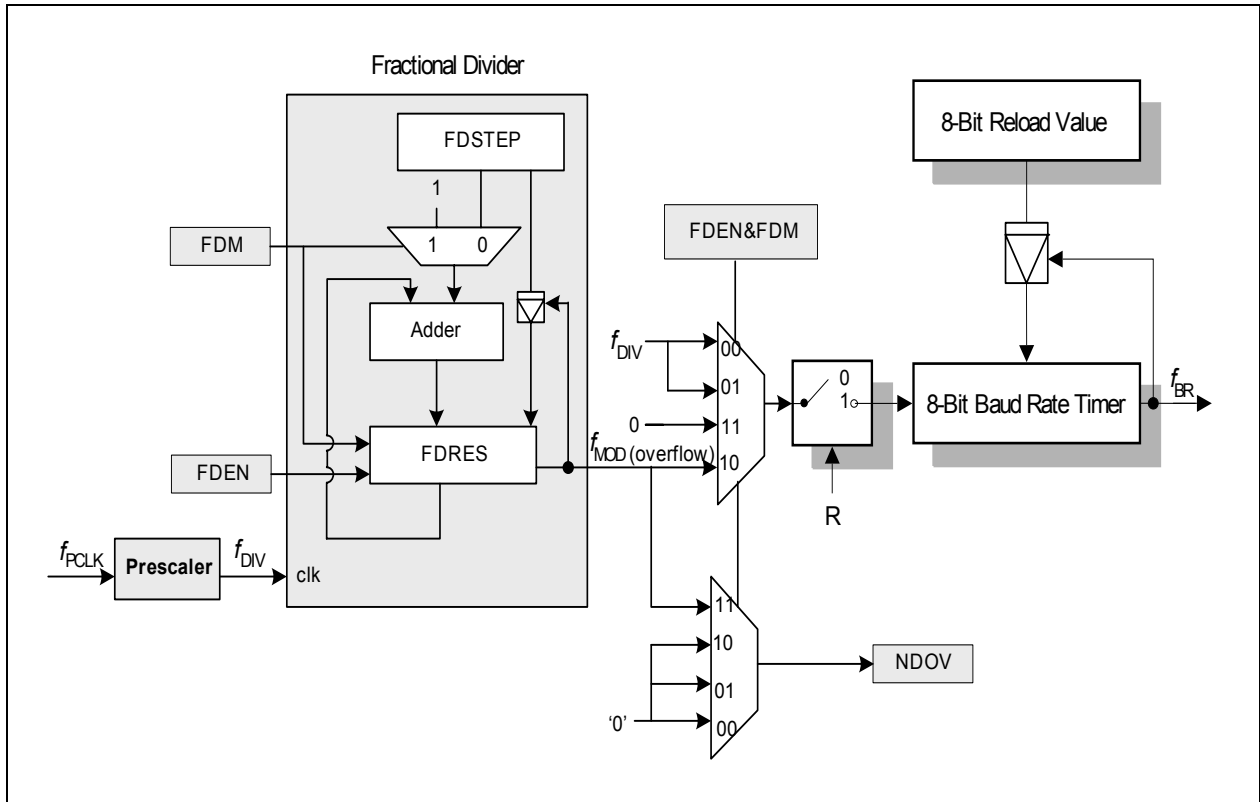
Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$ ¹⁾
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.11.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK} , see [Figure 26](#).


Figure 26 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See [Section 3.12](#).

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
(to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

Functional Description

The following formulas calculate the final baud rate without and with the fractional divider respectively:

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \quad \text{where } 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1) > 1$$

(3.4)

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \times \frac{\text{STEP}}{256}$$

(3.5)

The maximum baud rate that can be generated is limited to $f_{\text{PCLK}}/32$. Hence, for a module clock of 24 MHz, the maximum achievable baud rate is 0.75 MBaud.

Table 25 lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 24 MHz is used.

Table 25 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000 _B)	78 (4E _H)	0.17 %
9600 Baud	1 (BRPRE=000 _B)	156 (9C _H)	0.17 %
4800 Baud	2 (BRPRE=001 _B)	156 (9C _H)	0.17 %
2400 Baud	4 (BRPRE=010 _B)	156 (9C _H)	0.17 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 26** lists the resulting deviation errors from generating a baud rate of 57.6 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

Table 26 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
24 MHz	1	6 (6 _H)	59 (3B _H)	+0.03 %
12 MHz	1	3 (3 _H)	59 (3B _H)	+0.03 %
8 MHz	1	2 (2 _H)	59 (3B _H)	+0.03 %
6 MHz	1	6 (6 _H)	236 (EC _H)	+0.03 %

3.11.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{\text{SMOD}} \times f_{PCLK}}{32 \times 2 \times (256 - \text{TH1})} \quad (3.6)$$

3.12 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see [Figure 26](#)). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV} , where n is defined by 256 - STEP. The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - \text{STEP}} \quad (3.7)$$

3.13 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
 - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
 - Programmable number of data bits: 2 to 8 bits
 - Programmable shift direction: LSB or MSB shift first
 - Programmable clock polarity: idle low or high state for the shift clock
 - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 27 shows the block diagram of the SSC.

Functional Description

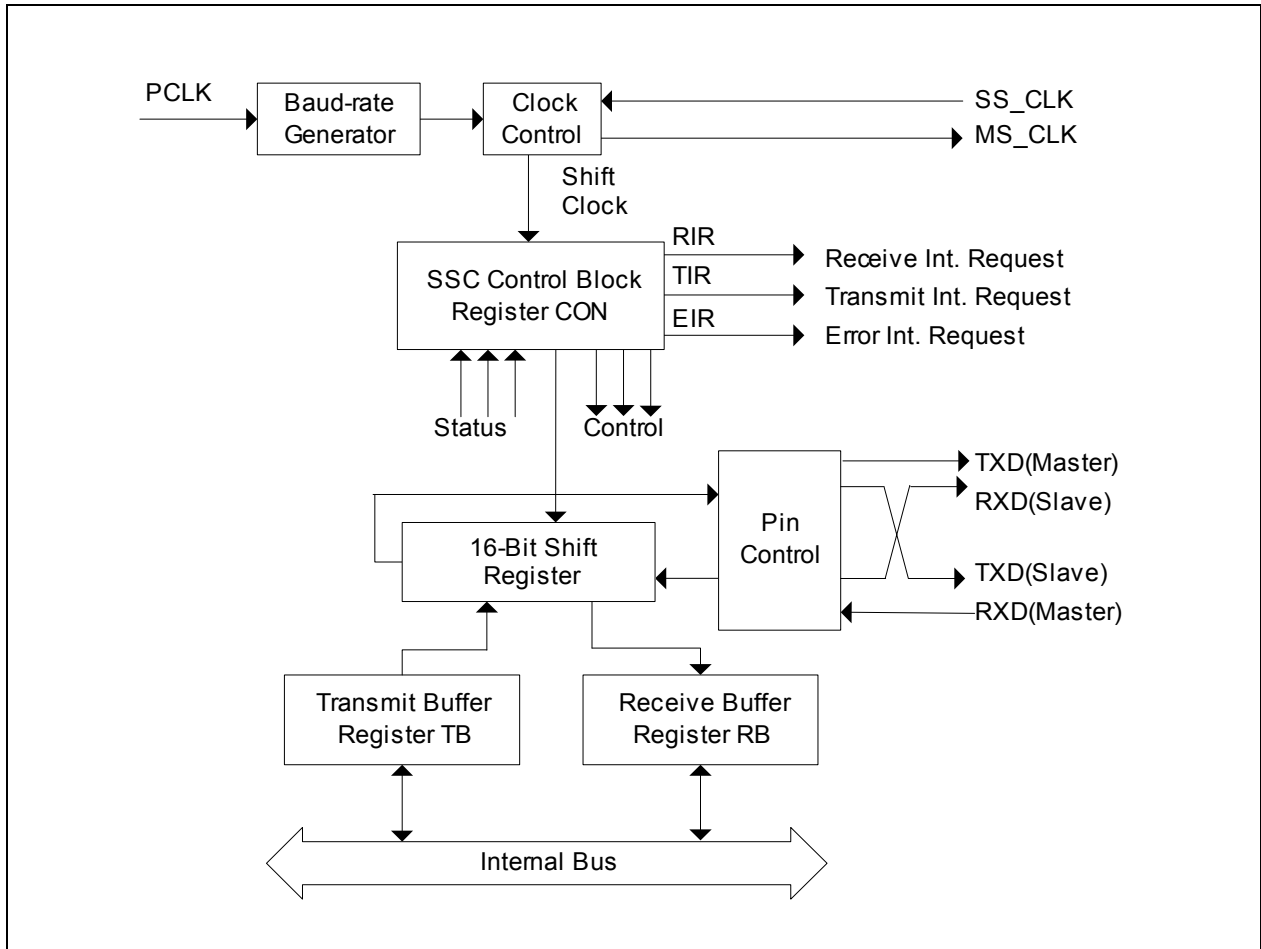


Figure 27 SSC Block Diagram

3.14 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at their respective external input pins, T0 or T1.

Timer 0 and 1 are fully compatible and can be configured in four different operating modes for use in a variety of applications, see [Table 27](#). In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 27 Timer 0 and Timer 1 Modes

Mode	Operation
0	13-bit timer The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	16-bit timer The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	8-bit timer with auto-reload The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	Timer 0 operates as two 8-bit timers The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.

3.15 Timer 2 and Timer 21

Timer 2 and Timer 21 are 16-bit general purpose timers (THL2) that are fully compatible and have two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode, see **Table 28**. As a timer, the timers count with an input clock of PCLK/12 (if prescaler is disabled). As a counter, they count 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is PCLK/24 (if prescaler is disabled).

Table 28 Timer 2 Modes

Mode	Description
Auto-reload	Up/Down Count Disabled <ul style="list-style-type: none"> • Count up only • Start counting from 16-bit reload value, overflow at FFFF_H • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload event
	Up/Down Count Enabled <ul style="list-style-type: none"> • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up <ul style="list-style-type: none"> – Start counting from 16-bit reload value, overflow at FFFF_H – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down <ul style="list-style-type: none"> – Start counting from FFFF_H, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at FFFF_H
Channel capture	<ul style="list-style-type: none"> • Count up only • Start counting from 0000_H, overflow at FFFF_H • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated with reload or capture event

3.16 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits. The clock frequency of T2CCU, f_{T2CCU} , could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

T2CCU Features

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be 'reset' immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
 - Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
 - Active level can be defined by register bit for channel groups A and B.
 - Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

3.17 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

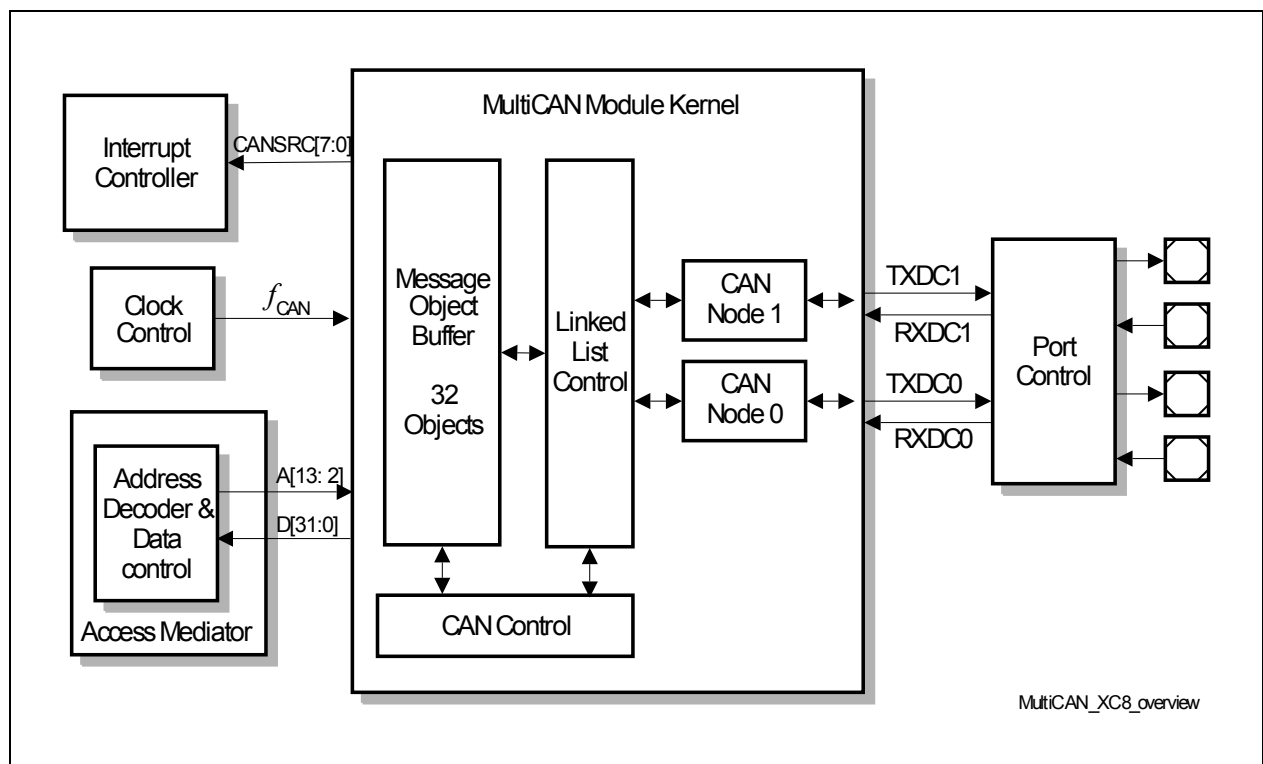


Figure 28 Overview of the MultiCAN

Features

- Compliant to ISO 11898.

Functional Description

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
 - allocated (assigned) to any CAN node
 - configured as transmit or receive object
 - setup to handle frames with 11-bit or 29-bit identifier
 - counted or assigned a timestamp via a frame counter
 - configured to remote monitoring mode
- Advanced Acceptance Filtering:
 - Each message object provides an individual acceptance mask to filter incoming frames.
 - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
 - Message objects can be grouped into 4 priority classes.
 - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
 - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
 - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
 - The Message objects are organized in double chained lists.
 - List reorganizations may be performed any time, even during full operation of the CAN nodes.
 - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
 - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
 - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
 - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
 - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

3.18 Analog-to-Digital Converter

The XC858 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at AN0 - AN7.

Features

- Successive approximation
- 8-bit or 10-bit resolution
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.18.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

Figure 29 shows the clocking scheme of the ADC module. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

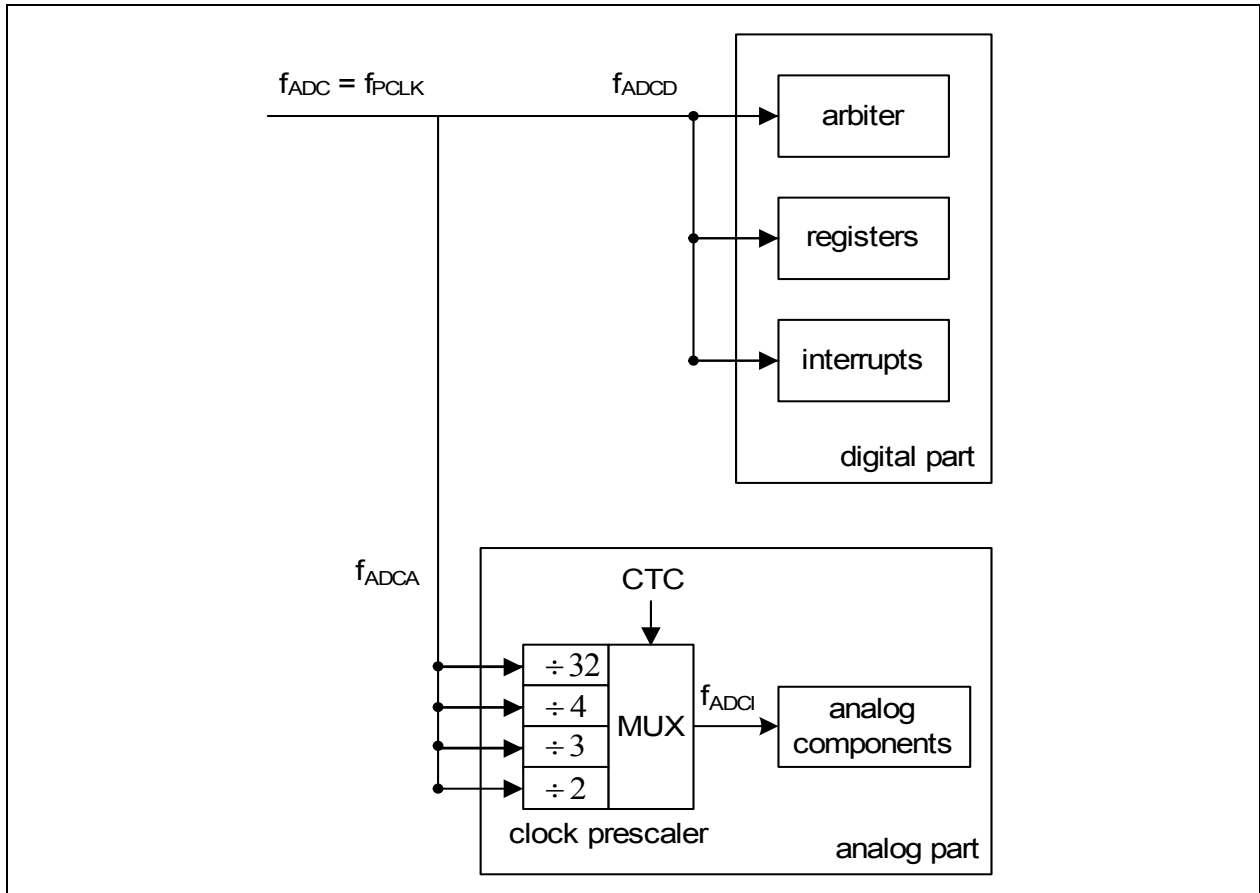


Figure 29 ADC Clocking Scheme

For module clock $f_{ADC} = 24$ MHz, the analog clock f_{ADCI} frequency can be selected as shown in [Table 29](#).

Table 29 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00 _B	$\div 2$	12 MHz
	01 _B	$\div 3$	8 MHz
	10 _B	$\div 4$	6 MHz
	11 _B (default)	$\div 32$	750 kHz

During slow-down mode, f_{ADC} may be reduced further, for example, to 12 MHz or 6 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.18.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

Functional Description

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

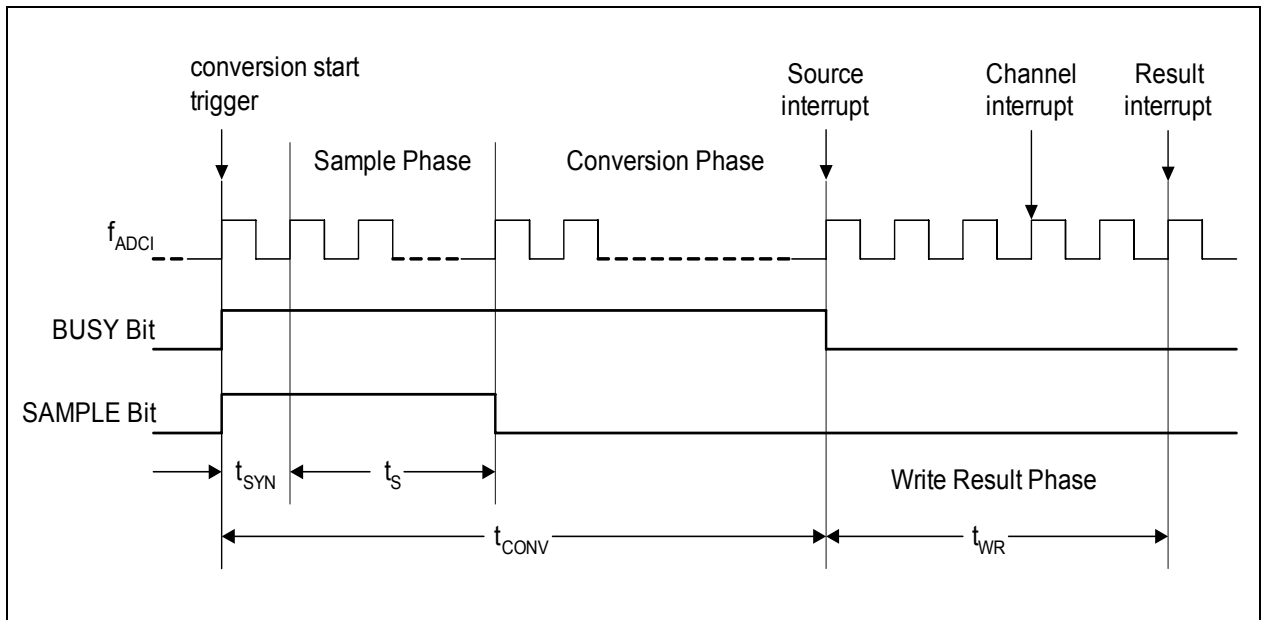


Figure 30 ADC Conversion Timing

3.19 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

Features

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in [Figure 31](#). The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG¹⁾, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC858 has been started in OCDS mode.

1) The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).

User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

Functional Description

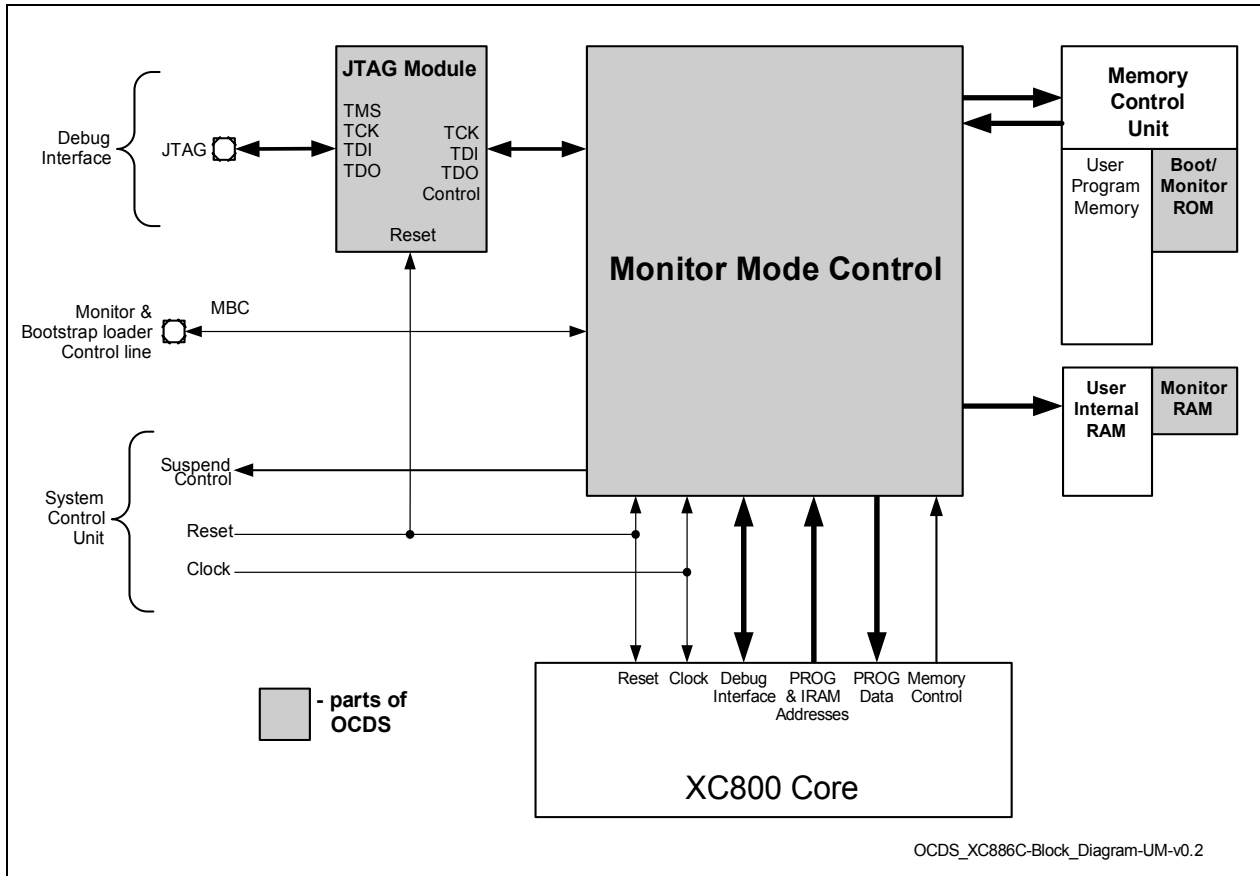


Figure 31 OCDS Block Diagram

3.19.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC858 Flash devices are given in [Table 30](#).

Table 30 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC858CA-16FF	1018 2083 _H
	XC858CA-13FF	1018 3083 _H
	XC858CA-9FF	1018 4083 _H

3.20 Chip Identification Number

The XC858 identity (ID) register is located at Page 1 of address B3_H. The value of ID register is 49_H. However, for easy identification of product variants, the Chip Identification Number, which is a unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

Table 31 lists the chip identification numbers of available XC858 Flash device variants.

Table 31 Chip Identification Number

Product Variant	Chip Identification Number
	AC-Step
Flash Devices	
XC858CA-16FF	4B5800C3 _H
XC858CA-13FF	4B5904C3 _H
XC858CA- 9FF	4B5A08C3 _H

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC858.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in [Section 4.2](#) and [Section 4.3](#).

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC858 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC858 and must be regarded for a system design.
- **SR**
These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC858 is designed in.

4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC858 can be subjected to without permanent damage.

Table 32 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	
Junction temperature	T_J	-40	120	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Voltage on any pin with respect to V_{SS}	V_{IN}	-0.5	$V_{DDP} + 0.5$ or max. 6	V	Whatever is lower
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	–	50	mA	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC858. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 33 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital ground voltage	V_{SS}	0		V	
CPU Clock Frequency ¹⁾	f_{CCLK}		24	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC858

1) f_{CCLK} is the input frequency to the XC800 core. Please refer to [Figure 22](#) for detailed description.

Electrical Parameters
4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Characteristics

Table 34 provides the characteristics of the input/output pins of the XC858.

Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
$V_{DDP} = 5\text{ V Range}$						
Output low voltage	V_{OL}	CC	–	0.6	V	$I_{OL} = 9\text{ mA (DS = 0)}^{1)}$ $I_{OL} = 12\text{ mA (DS = 1)}^{2)}$
Output high voltage	V_{OH}	CC	2.4	–	V	$I_{OH} = -20\text{ mA (DS = 0)}^{1)}$ $I_{OH} = -25\text{ mA (DS = 1)}^{2)}$
Input low voltage	V_{IL}	SR	-0.3	0.8	V	CMOS Mode
Input high voltage	V_{IH}	SR	2.2	V_{DDP}	V	CMOS Mode
Input Hysteresis	HYS	CC	0.35	–	V	CMOS Mode ³⁾⁴⁾
Input low voltage at XTAL1	V_{ILX}	SR	-0.3	0.8	V	
Input high voltage at XTAL1	V_{IHx}	SR	3.4	V_{DDP}	V	
Pull-up current	I_{PU}	SR	–	-20	μA	$V_{IH,min}$
			-88	–	μA	$V_{IL,max}$
Pull-down current	I_{PD}	SR	–	10	μA	$V_{IL,max}$
			66	–	μA	$V_{IH,min}$
Input leakage current	I_{OZ1}	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 85^\circ\text{C}^{5)}$
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\sum I_{OV} $	SR	–	25	mA	⁶⁾
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	⁷⁾

Electrical Parameters
Table 34 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR SR	–	25	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma I_M $ SR	–	150	mA	
Maximum current into V_{DDP}	I_{MVDDP} SR	–	200	mA	⁶⁾
Maximum current out of V_{SS}	I_{MVSS} SR	–	200	mA	⁶⁾

- 1) DS = 0 refers to the pin having a weak drive strength which is programmable via Px_DS register.
- 2) DS = 1 refers to the pin having a strong drive strength which is programmable via Px_DS register.
- 3) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 4) P0.1 has a minimum input hysteresis of 0.25V.
- 5) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and \overline{RESET} pin have internal pull devices and are not included in the input leakage current characteristic.
- 6) Not subjected to production test, verified by design/characterization.
- 7) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

4.2.2 Supply Threshold Characteristics

Table 35 provides the characteristics of the supply threshold in the XC858.

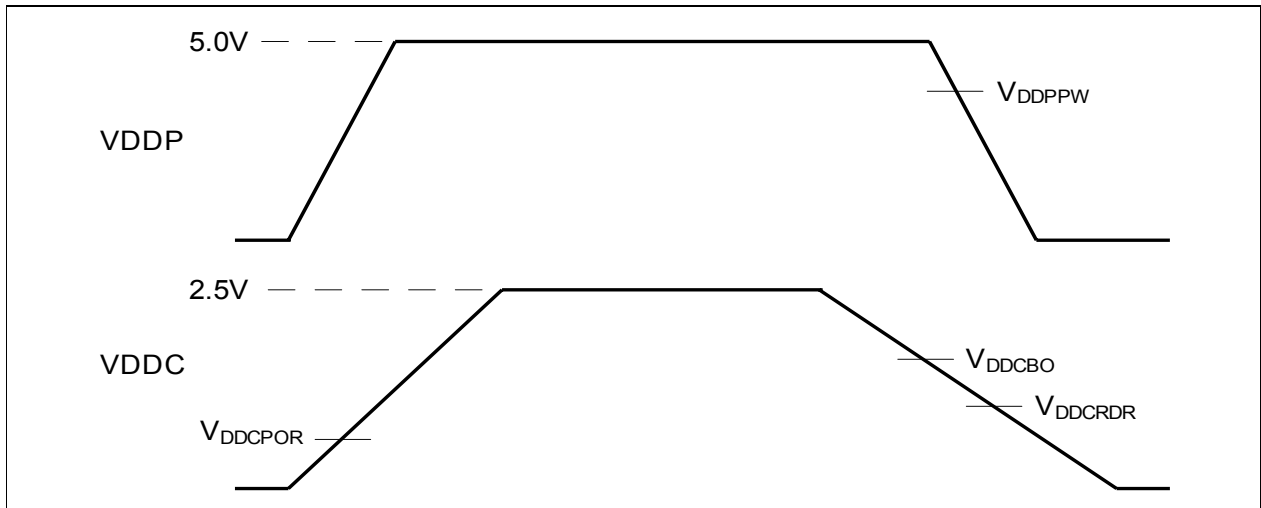


Figure 32 Supply Threshold Parameters

Table 35 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} brownout voltage ¹⁾	V_{DDCBO}	CC	1.7	1.9	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	1.2	–	–	V
V_{DDP} prewarning voltage	V_{DDPPW}	CC	3.8	4.2	4.5	V
Power-on reset voltage ¹⁾²⁾	V_{DDCPOR}	CC	1.7	1.9	2.2	V

1) Detection is enabled in both active and power-down mode.

2) The reset of EVR is extended by 300 μ s typically after the VDDC reaches the power-on reset voltage.

Electrical Parameters
4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 36 ADC Characteristics (Operating Conditions apply; $V_{DDP} = 5V$ Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	V_{AREF}	SR	$V_{AGND} + 1$	V_{DDP}	$V_{DDP} + 0.05$	V	¹⁾
Analog reference ground	V_{AGND}	SR	$V_{SS} - 0.05$	V_{SS}	$V_{AREF} - 1$	V	¹⁾
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}		–	24	–	MHz	module clock ¹⁾
	f_{ADCI}		–	–	14 ²⁾	MHz	internal analog clock ¹⁾ See Figure 29
Sample time	t_S	CC	$(2 + INPCR0.STC) \times t_{ADCI}$			μs	¹⁾
Conversion time	t_C	CC	See Section 4.2.3.1			μs	¹⁾
Differential Nonlinearity	$ EA_{DNL} $	CC	–	–	1.5	LSB	10-bit conversion
Integral Nonlinearity	$ EA_{INL} $	CC	–	–	2.5	LSB	10-bit conversion
Offset	$ EA_{OFF} $	CC	–	–	3	LSB	10-bit conversion
Gain	$ EA_{GAIN} $	CC	–	–	2.5	LSB	10-bit conversion
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	14	pF	¹⁾³⁾
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	4	5	pF	¹⁾⁴⁾

Electrical Parameters

Table 36 ADC Characteristics (Operating Conditions apply; $V_{DDP} = 5V$ Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Input resistance of the reference input	R_{AREF}	CC	–	1	2	k Ω	1)
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	3	k Ω	1)

- 1) Not subjected to production test, verified by design/characterization.
- 2) This value includes the maximum oscillator deviation.
- 3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.
- 4) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

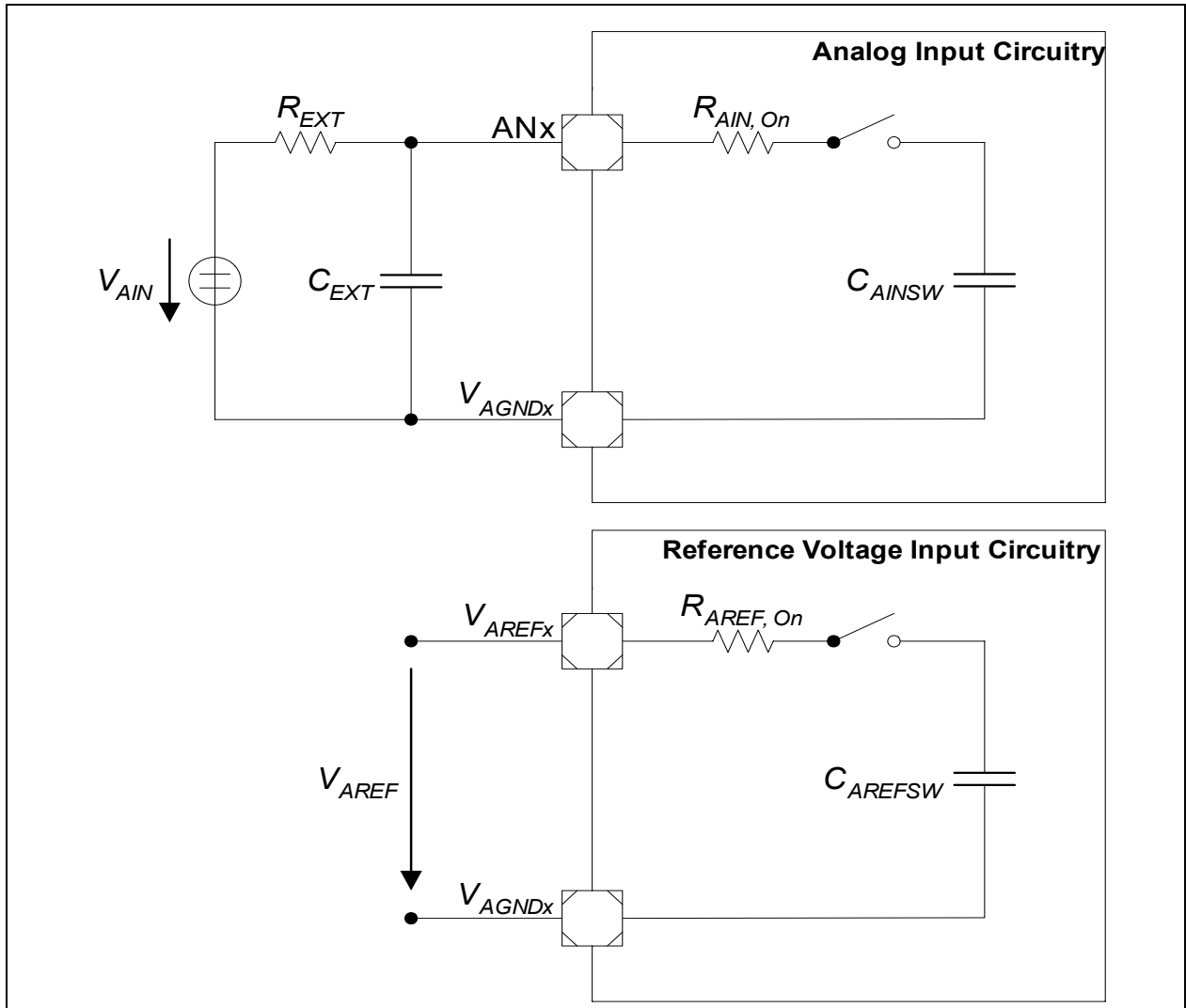


Figure 33 ADC Input Circuits

4.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + \text{STC}))$, where

$r = \text{CTC} + 2$ for $\text{CTC} = 00_{\text{B}}$, 01_{B} or 10_{B} ,

$r = 32$ for $\text{CTC} = 11_{\text{B}}$,

$\text{CTC} = \text{Conversion Time Control (GLOBCTR.CTC)}$,

$\text{STC} = \text{Sample Time Control (INPCR0.STC)}$,

$n = 8$ or 10 (for 8-bit and 10-bit conversion respectively),

$t_{ADC} = 1 / f_{ADC}$

4.2.4 Power Supply Current

Table 37 and **Table 38** provide the characteristics of the power supply current in the XC858.

**Table 37 Power Supply Current Parameters (Operating Conditions apply;
 $V_{DDP} = 5V$ range)**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. ¹⁾	max. ²⁾		
$V_{DDP} = 5V$ Range					
Active Mode	I_{DDP}	37.5	45	mA	³⁾
Idle Mode	I_{DDP}	29.2	35	mA	⁴⁾
Active Mode with slow-down enabled	I_{DDP}	10	15	mA	⁵⁾
Idle Mode with slow-down enabled	I_{DDP}	9.2	14	mA	⁶⁾

1) The typical I_{DDP} values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at $T_A = +25\text{ °C}$ and $V_{DDP} = 5.0\text{ V}$.

2) The maximum I_{DDP} values are measured under worst case conditions ($T_A = +85\text{ °C}$ and $V_{DDP} = 5.5\text{ V}$).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with on-chip oscillator of 4 MHz, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000_B, $\overline{\text{RESET}} = V_{DDP}$; all other pins are disconnected, no load on ports.

Electrical Parameters
Table 38 Power Down Current (Operating Conditions apply; $V_{DDP} = 5V$ range)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. ¹⁾	max. ²⁾		
$V_{DDP} = 5V$ Range					
Power-Down Mode	I_{PDP}	20	60	μA	$T_A = + 25\text{ }^\circ C^{3)4)}$
		-	200	μA	$T_A = + 85\text{ }^\circ C^{4)5)}$

- 1) The typical I_{PDP} values are based on preliminary measurements and are to be used as reference only. These values are measured at $V_{DDP} = 5.0\text{ V}$.
- 2) The maximum I_{PDP} values are measured at $V_{DDP} = 5.5\text{ V}$.
- 3) I_{PDP} has a maximum value of $350\text{ }\mu A$ at $T_A = + 85\text{ }^\circ C$.
- 4) I_{PDP} is measured with: $\overline{RESET} = V_{DDP}$, $V_{AGND} = V_{SS}$, $RXD/INT0 = V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.
- 5) Not subjected to production test, verified by design/characterization.

4.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in [Figure 34](#), [Figure 35](#) and [Figure 36](#).

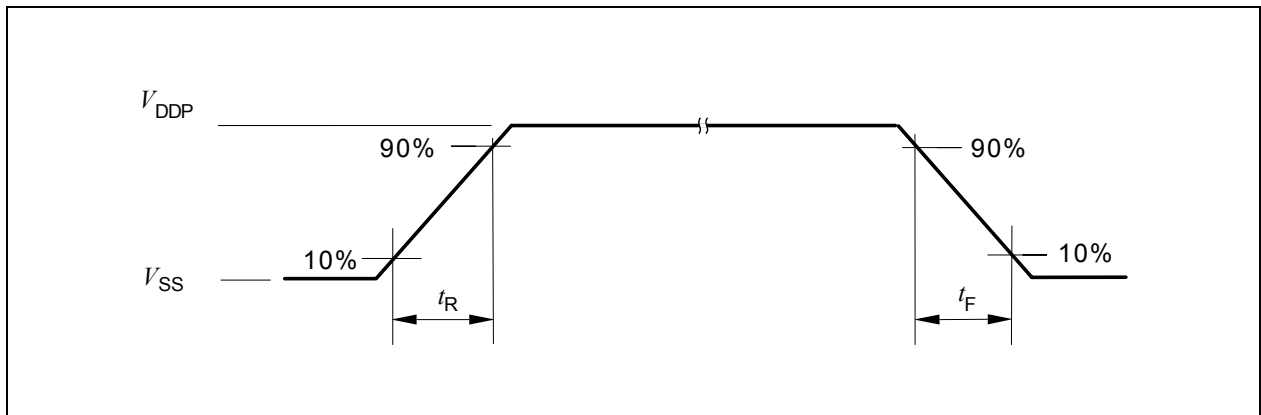


Figure 34 Rise/Fall Time Parameters

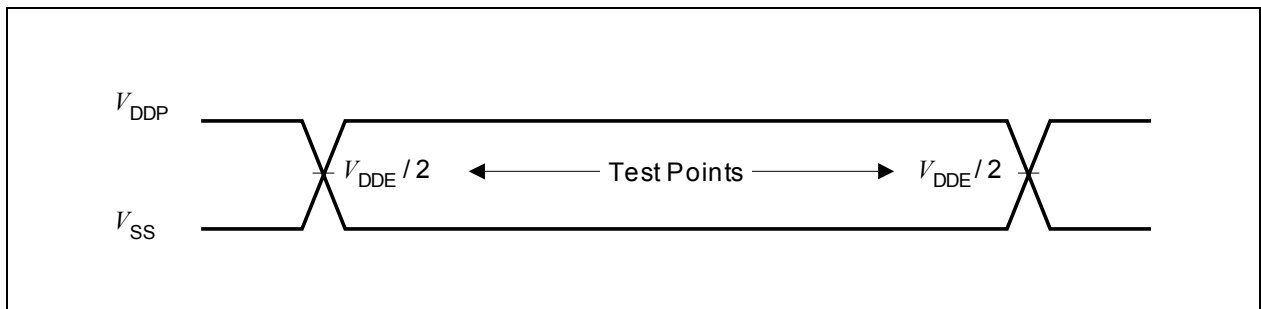


Figure 35 Testing Waveform, Output Delay

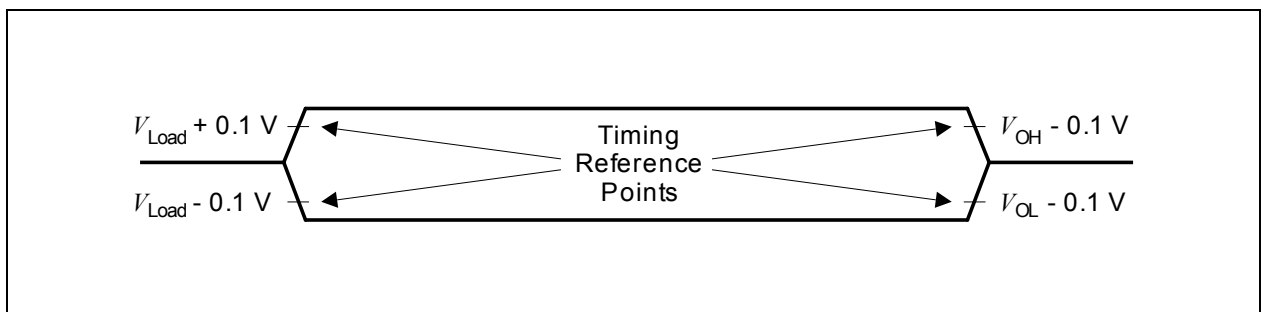


Figure 36 Testing Waveform, Output High Impedance

4.3.2 Output Rise/Fall Times

Table 39 provides the characteristics of the output rise/fall times in the XC858.

Table 39 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
$V_{DDP} = 5V$ Range					
Rise/fall times	t_R, t_F	–	10	ns	20 pF. ^{1) 2)3)}

- 1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.
- 2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 3) Additional rise/fall time valid for $C_L = 20pF - 100pF @ 0.125 ns/pF$.

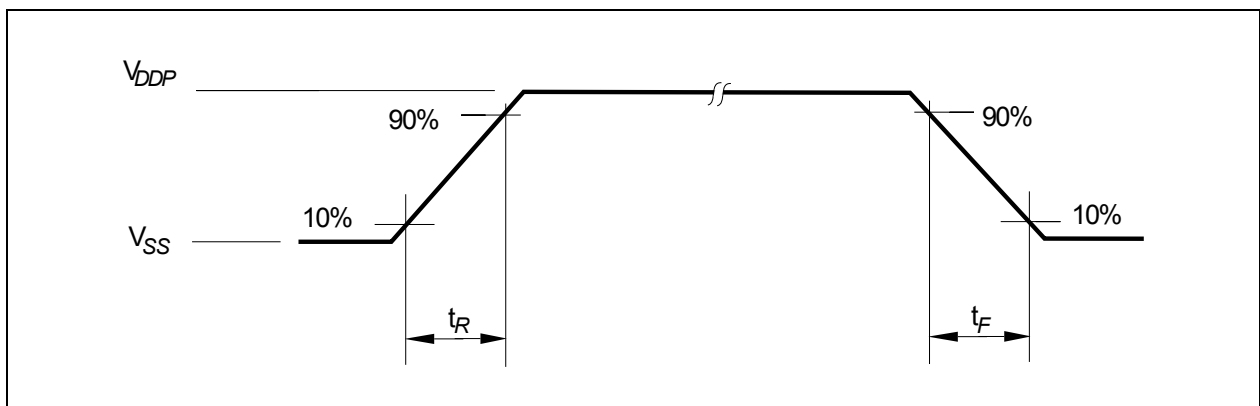


Figure 37 Rise/Fall Times Parameters

4.3.3 Power-on Reset and PLL Timing

Table 40 provides the characteristics of the power-on reset and PLL timing in the XC858.

Table 40 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol	CC	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
On-Chip Oscillator start-up time	t_{OSCST}	CC	–	–	500	ns	1)
PLL lock-in in time	t_{LOCK}	CC	–	–	200	μ s	1)
PLL accumulated jitter	D_P		–	–	1.8	ns	1)2)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) PLL lock at 144 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 72 and P = 1.

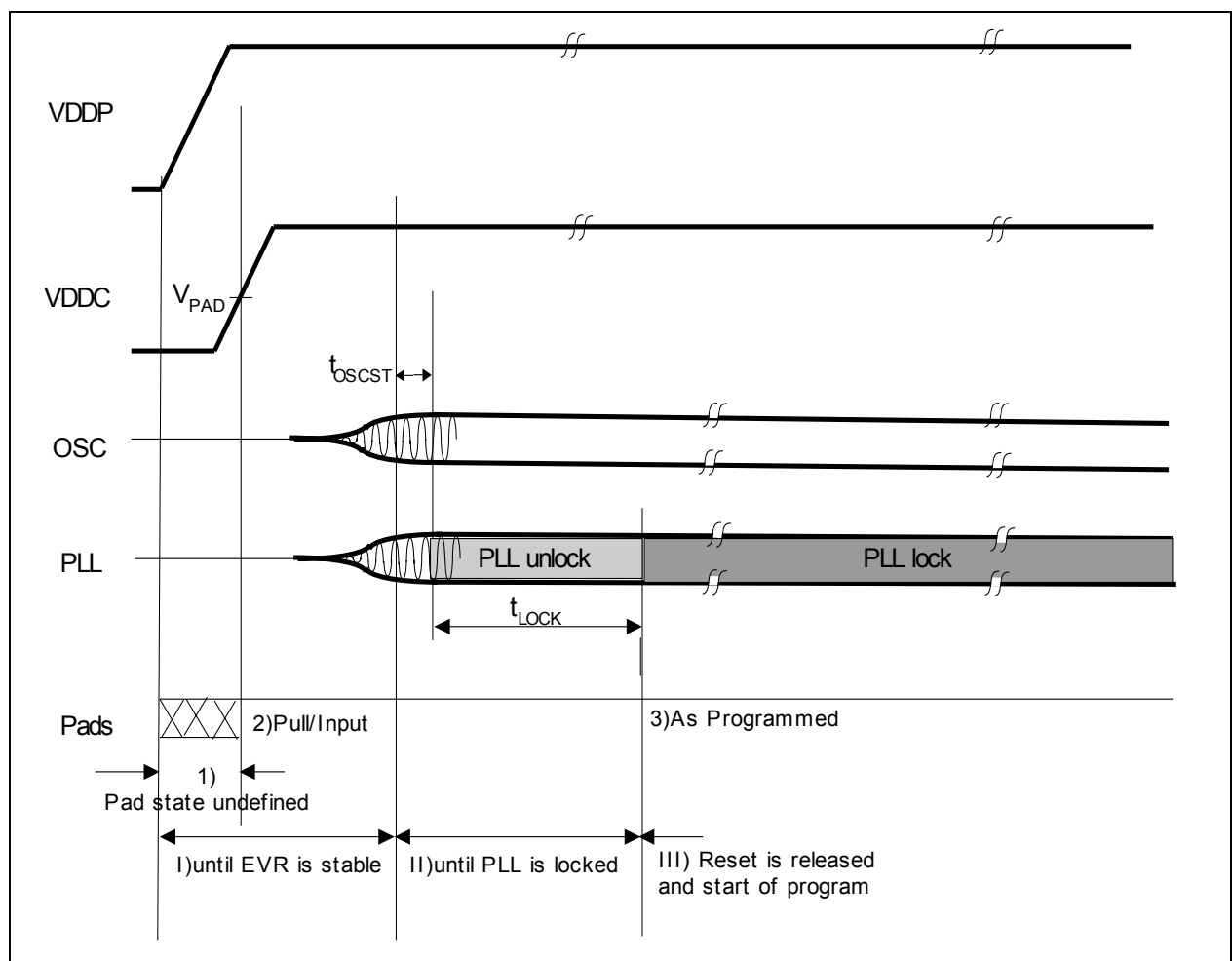


Figure 38 Power-on Reset Timing

4.3.4 On-Chip Oscillator Characteristics

Table 41 provides the characteristics of the on-chip oscillator in the XC858.

Table 41 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM} CC	3.88	4	4.12	MHz	under nominal conditions ¹⁾ after IFX-backend trimming	
Long term frequency deviation	Δf_{LT} CC	-5	–	5	%	with respect to f_{NOM} , over lifetime and temperature (-40°C to 85°C), for one given device after trimming	
Short term frequency deviation	Δf_{ST} CC	-1.0	–	1.0	%	with respect to f_{NOM} , over core supply voltage (2.5 V ± 7.5%), for one given device after trimming	

1) Nominal condition: $V_{\text{DDC}} = 2.5 \text{ V}$, $T_{\text{A}} = + 25^{\circ}\text{C}$.

4.3.5 External Data Memory Characteristics

Table 42 shows the timing of the external data memory read cycle.

Table 42 External Data Memory Read Timing (Operating Conditions apply)

Parameter	Symbol	CC	Limit Values		Unit	Test Conditions
			Min.	Max.		
$\overline{\text{RD}}$ pulse width	t_1	CC	$2 \cdot f_{\text{CCLK}} - 17$	-	ns	1)
Address valid to $\overline{\text{RD}}$	t_2	CC	$f_{\text{CCLK}} - 12$	-	ns	1)
$\overline{\text{RD}}$ to valid data in	t_3	SR	-	$1.5 \cdot f_{\text{CCLK}} - 27$	ns	1)
Address to valid data in	t_4	SR	-	$3 \cdot f_{\text{CCLK}} - 7$	ns	1)
Data hold after $\overline{\text{RD}}$	t_5	SR	$0.5 \cdot f_{\text{CCLK}} - 17$	-	ns	1)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

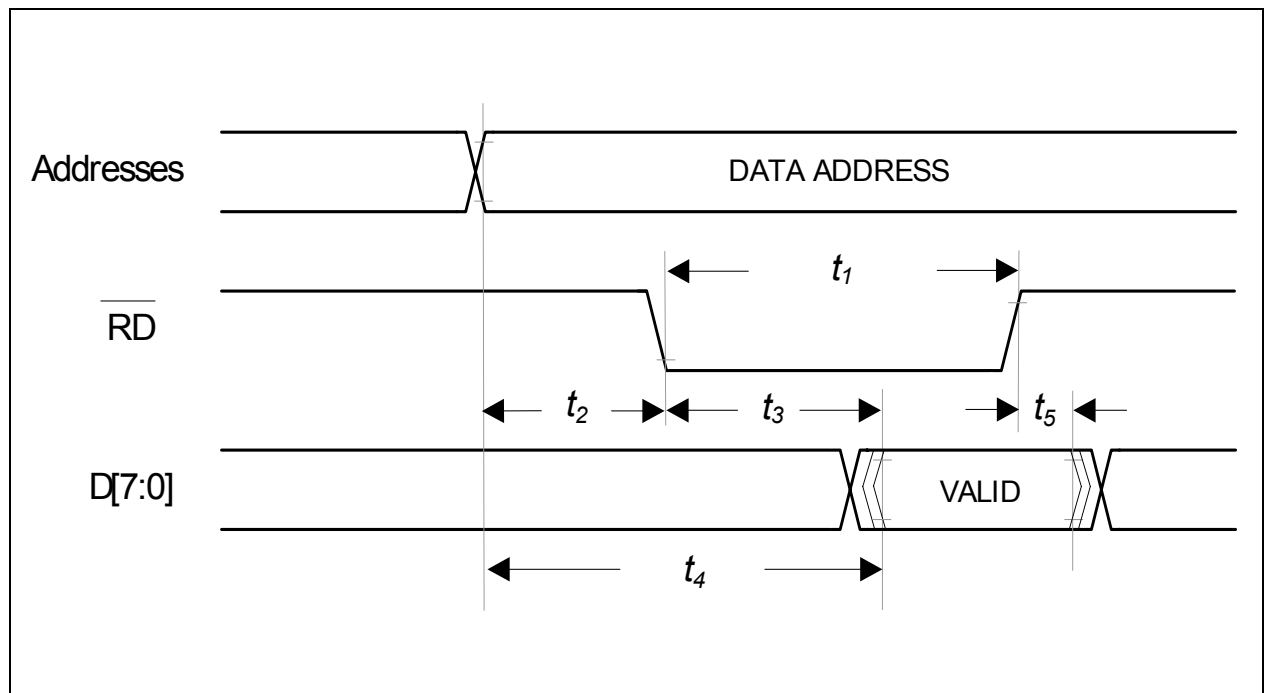


Figure 39 External Data Memory Read Cycle

Electrical Parameters

Table 43 shows the timing of the external data memory write cycle.

Table 43 External Data Memory Write Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
\overline{WR} pulse width	t_1	CC	$f_{CCLK} - 10$	-	ns	1)
Address valid to \overline{WR}	t_2	CC	$2 * f_{CCLK} - 7$	-	ns	1)
Data valid to \overline{WR} transition	t_3	SR	$f_{CCLK} - 5$	-	ns	1)
Data setup before \overline{WR}	t_4	SR	$9 * f_{CCLK} - 13$	-	ns	1)
Data hold after \overline{WR}	t_5	SR	$6 * f_{CCLK} - 3$	-	ns	1)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

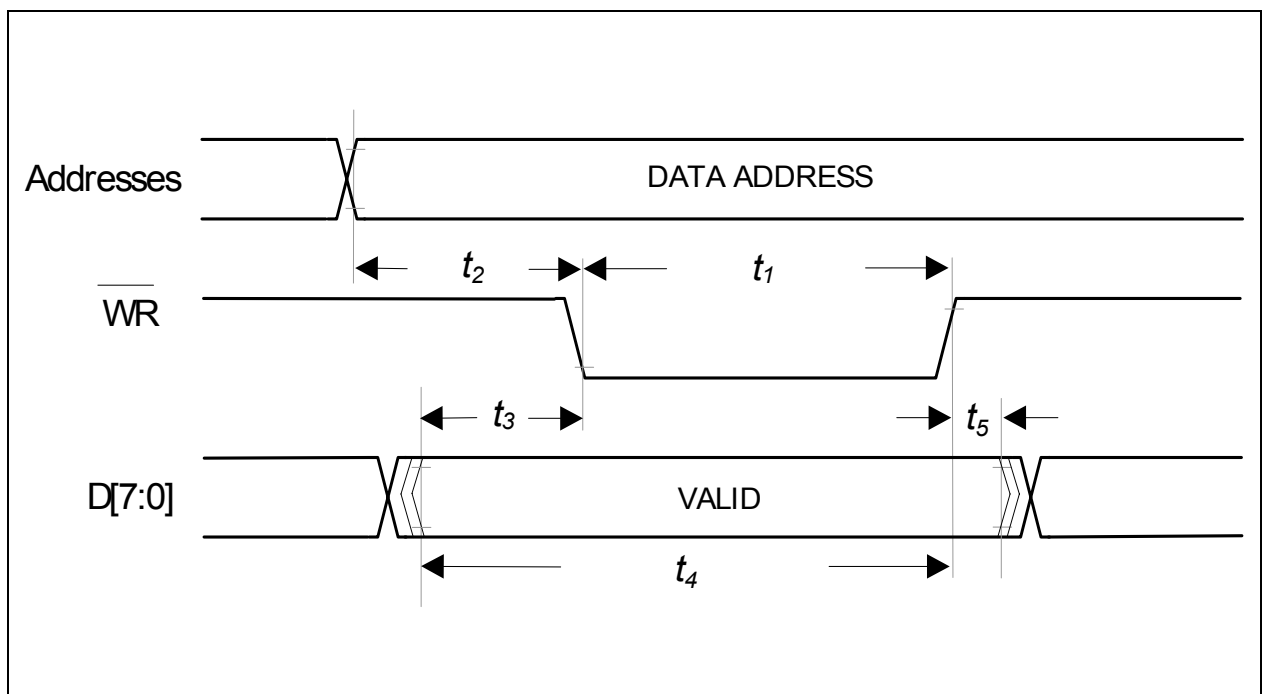


Figure 40 External Data Memory Write Cycle

4.3.6 External Clock Drive XTAL1

Table 44 shows the parameters that define the external clock supply for XC858. These timing parameters are based on the direct XTAL1 drive of clock input signals. They are not applicable if an external crystal or ceramic resonator is considered.

Table 44 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol	SR	Limit Values		Unit	Test Conditions
			Min.	Max.		
Oscillator period	t_{osc}	SR	50	500	ns	1)2)
High time	t_1	SR	15	-	ns	2)3)
Low time	t_2	SR	15	-	ns	2)3)
Rise time	t_3	SR	-	10	ns	2)3)
Fall time	t_4	SR	-	10	ns	2)3)

- 1) The clock input signals with 45-55% duty cycle are used.
- 2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 3) The clock input signal must reach the defined levels V_{ILX} and V_{IHx} .

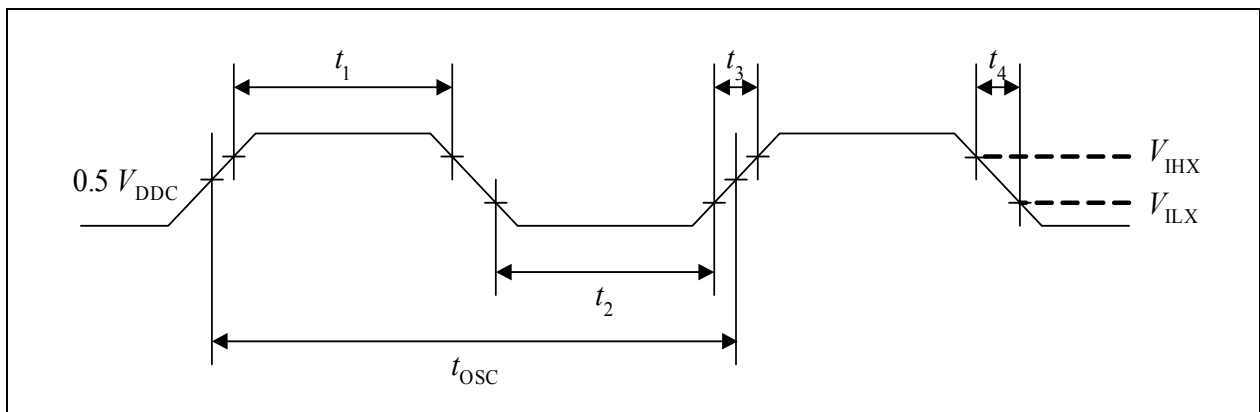


Figure 41 External Clock Drive XTAL1

4.3.7 JTAG Timing

Table 45 provides the characteristics of the JTAG timing in the XC858.

Table 45 TCK Clock Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TCK clock period	t_{TCK}	SR	50	-	ns	1)
TCK high time	t_1	SR	20	-	ns	1)
TCK low time	t_2	SR	20	-	ns	1)
TCK clock rise time	t_3	SR	-	4	ns	1)
TCK clock fall time	t_4	SR	-	4	ns	1)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

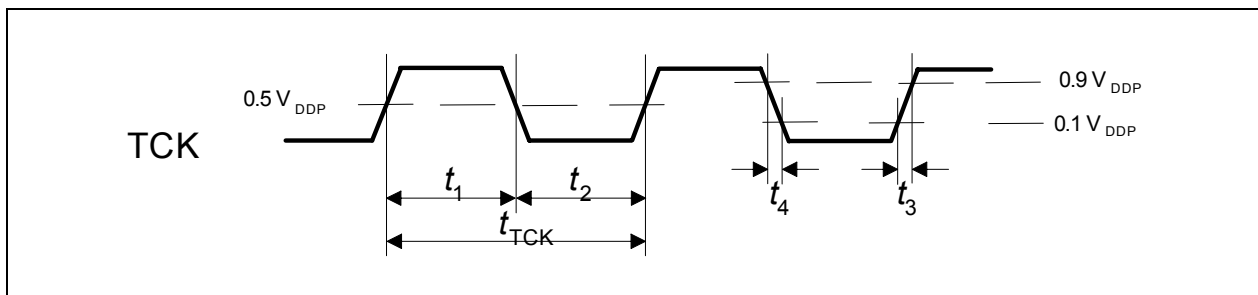


Figure 42 TCK Clock Timing

Table 46 JTAG Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TMS setup to TCK ↙	t_1	SR	8	-	ns	1)
TMS hold to TCK ↘	t_2	SR	0	-	ns	1)
TDI setup to TCK ↙	t_1	SR	8	-	ns	1)
TDI hold to TCK ↘	t_2	SR	4	-	ns	1)
TDO valid output from TCK	t_3	CC	-	24	ns	1)

Electrical Parameters

Table 46 JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter	Symbol	Limits	Unit	Test Conditions	
					min
TDO high impedance to valid output from TCK	t_4 CC	-	18	ns	1)
TDO valid output to high impedance from TCK	t_5 CC	-	21	ns	1)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

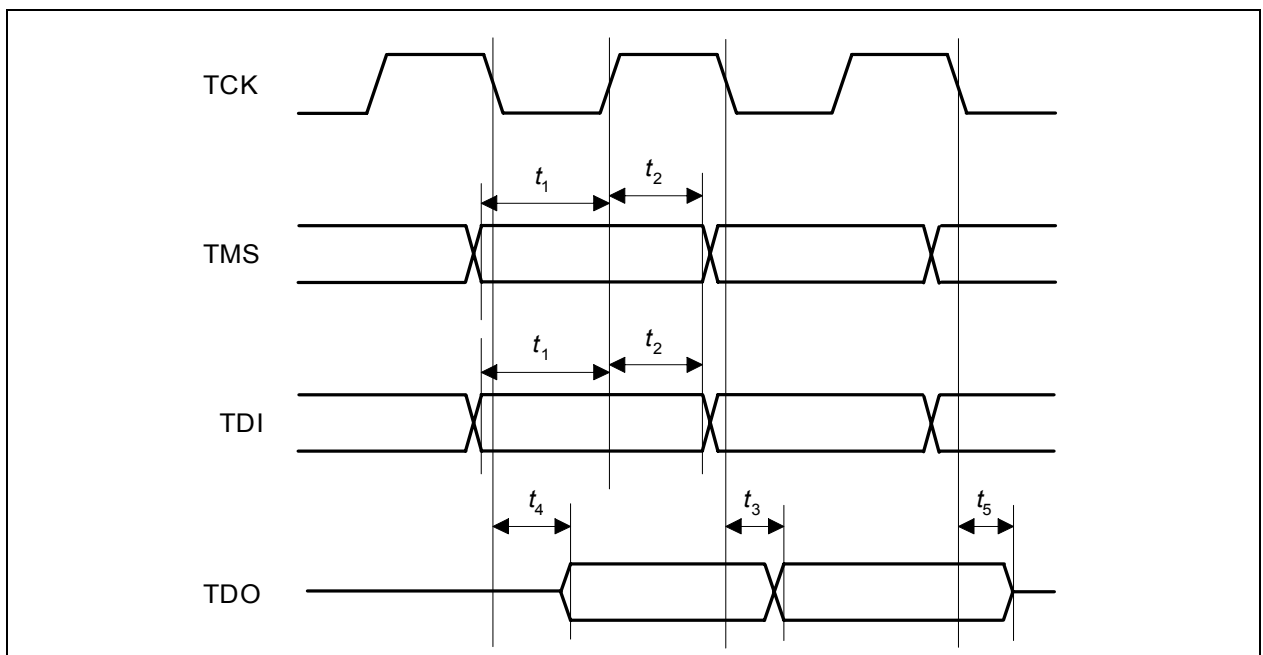


Figure 43 JTAG Timing

4.3.8 SSC Master Mode Timing

Table 47 provides the characteristics of the SSC timing in the XC858.

Table 47 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol	CC	Limit Values		Unit	Test Conditions
			min.	max.		
SCLK clock period	t_0	CC	$2 \cdot T_{SSC}$	–	ns	1)2)
MISR delay from SCLK	t_1	CC	0	5	ns	2)
MRST setup to SCLK	t_2	SR	13	–	ns	2)
MRST hold from SCLK	t_3	SR	0	–	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 83.3$ ns. T_{CPU} is the CPU clock period.

2) 1)Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

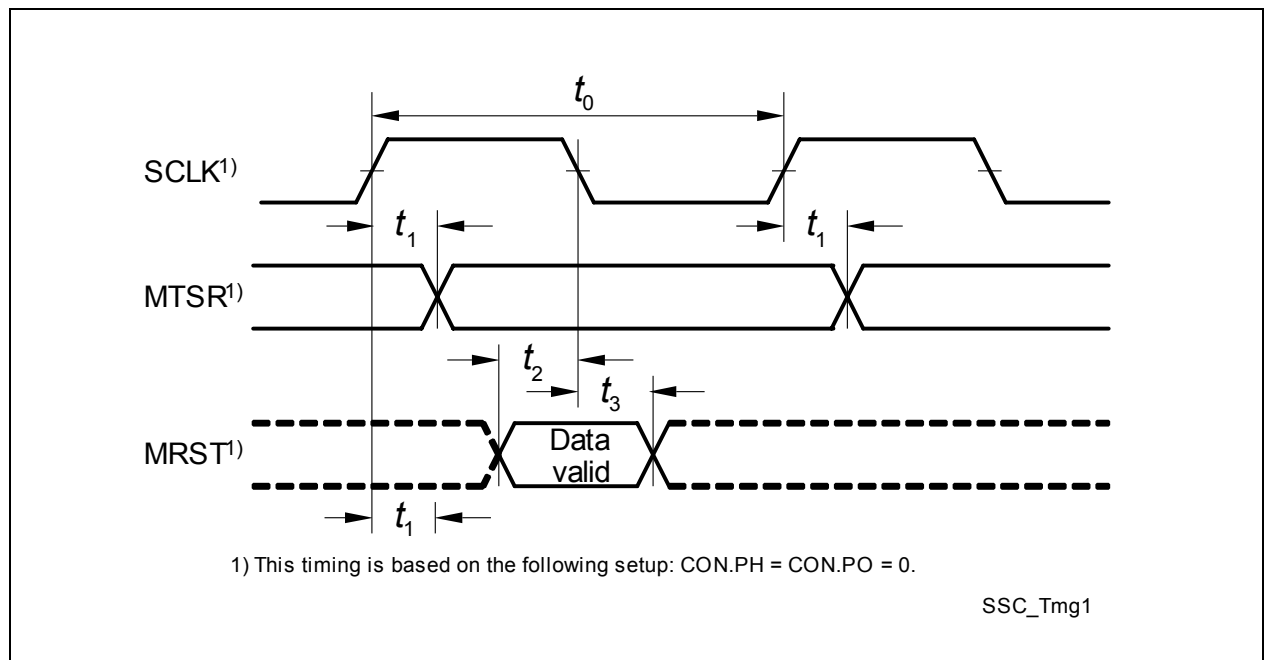


Figure 44 SSC Master Mode Timing

5 Package and Quality Declaration

Chapter 5 provides the information of the XC858 package and reliability section.

5.1 Package Parameters

Table 48 provides the thermal characteristics of the PG-LQFP-64-4 package used in XC858.

Table 48 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Thermal resistance junction case ¹⁾	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead ¹⁾	R_{TJL}	CC	-	34.6	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by

- a) simply adding only the two thermal resistances (junction lead and lead ambient), or
- b) by taking all four resistances into account, depending on the precision needed.

5.2 Package Outline

Figure 45 shows the package outlines of the XC858.

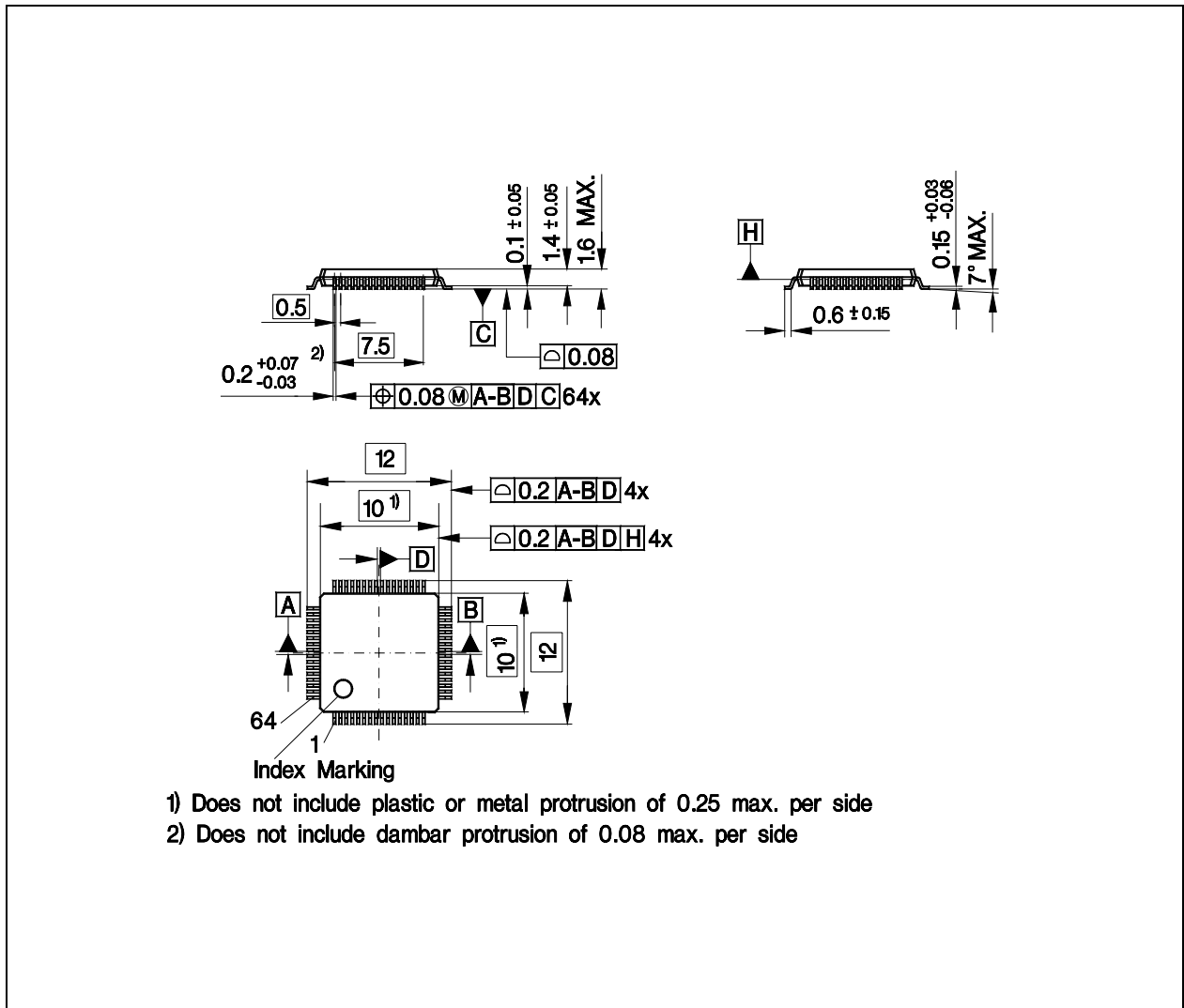


Figure 45 PG-LQFP-64-4 Package Outline

Package and Quality Declaration

5.3 Quality Declaration

Table 49 shows the characteristics of the quality parameters in the XC858.

Table 49 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C

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