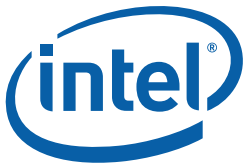

Intel® 945G/945GZ/945GC/ 945P/945PL Express Chipset Family

Datasheet

- For the Intel® 82945G/82945GZ/82945GC Graphics and Memory Controller Hub (GMCH) and Intel® 82945P/82945PL Memory Controller Hub (MCH)

June 2008

Document Number: 307502-005

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[1]Hyper-Threading Technology requires a computer system with an Intel® Pentium® 4 processor supporting HT Technology and a Hyper-Threading Technology enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. See http://www.intel.com/info/hyperthreading/ for more information including details on which processors support HT Technology.

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Contents

Figures

Tables

Revision History

Rev	Description	Date
-001	• Initial Release	May 2005
-002	• Added Intel® 82945PL specifications	October 2005
-003	• Added Intel® 82945GZ specifications	December 2005
-004	• Added Intel® 82945GC specifications	October 2006
-005	• Updated Intel® 82945GC specifications	June 2008

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Intel® 82945G/82945GZ/82945GC/82945P /82945PL (G)MCH Features

- Processor Interface
  - — Intel® Core™2 Duo, Intel® Celeron 400 Series, Intel® Pentium® 4 processor in the 90 nm process in the LGA775 Land Grid Array package or Intel® Pentium® D processor (supports 775-Land package)
  - — Intel® Atom™ 200 series and Intel Atom™ 300 Series (82945GC only)
  - — Supports Pentium 4 processor FSB interrupt delivery
  - — 533/800 MT/s (133/200 MHz) FSB
  - — 1066 MT/s (266 MHz) FSB (82945G/P only)
  - — Supports Hyper-Threading Technology[1] (HT Technology)
  - — FSB Dynamic Bus Inversion (DBI)
  - — 32-bit host bus addressing
  - — 12-deep In-Order Queue
  - — 1-deep Defer Queue
  - — GTL+ bus driver with integrated GTL termination resistors
  - — Supports a Cache Line Size of 64 bytes
- System Memory
  - — 4 GB maximum memory
  - — One or two 64-bit wide DDR2 SDRAM data channels
  - — DDR2 400, DDR2 533
  - — DDR2 667 (82945G/ GC/P only)
  - — Bandwidth up to 10.7 GB/s (DDR2 667) in dual-channel Interleaved mode.
  - — Non-ECC memory only
  - — 256-Mb, 512-Mb and 1-Gb DDR2 technologies
  - — Only x8, x16, DDR2 devices with four banks and also supports eight bank, 1-Gbit DDR2 devices.
  - — Opportunistic refresh
  - — Up to 32 simultaneously open pages in dual-channel mode
  - — SPD (Serial Presence Detect) scheme for DIMM detection support
  - — Suspend-to-RAM support using CKE
  - — Supports configurations defined in the JEDEC DDR2 DIMM specification only
- PCI Express* Graphics Interface (82945G/GC/P/PL only)
  - — One x16 PCI Express port
  - — Compatible with the *PCI Express Base Specification, Revision 1.0a*
  - — Raw bit rate on data pins of 2.5 Gb/s resulting in a real bandwidth per pair of 250 MB/s
- Integrated Graphics Device (82945G/GZ/GC only)
  - — Core frequency of 400 MHz
  - — 1.6 GP/s pixel rate
  - — High-Quality 3D Setup and Render Engine
  - — High-Quality Texture Engine
  - — VLD/iDCT for enabling dual Intel® High Definition streams for MPEG playback
  - — 3D Graphics Rendering Enhancements
  - — 2D Graphics
  - — Video Overlay
  - — Multiple Overlay Functionality
- Analog Display Support (82945G/GZ/GC only)
  - — 400 MHz Integrated 24-bit RAMDAC
  - — Up to 2048x1536 @ 75 Hz refresh
  - — Hardware Color Cursor Support
  - — DDC2B Compliant Interface
- Digital Display Support (82945G/GZ/GC only)
  - — Two SDVO ports multiplexed with PCI Express graphics interface
  - — 200 MHz dot clock on each 12-bit interface
  - — Can combine two channels to form one larger interface
  - — Flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1920x1080 @ 85Hz
  - — Dual independent display options with digital display (82945G only)
  - — Intel® Extended Desktop and Dual Display Zoom (82945G only)
  - — Intel® Dual Display Clone and Dual Display Twin
  - — Multiplexed digital display channels (Supported with ADD2 Card).
  - — Supports TMDS transmitters or TV-Out encoders
  - — ADD2/ADD2+ card uses PCI Express graphics x16 connector (ADD2+ support for 945G only)
- DMI Interface
  - — A chip-to-chip connection interface to Intel® ICH7
  - — 2 GB/s point-to-point DMI to ICH7 (1 GB/s each direction)
  - — 100 MHz reference clock (shared with PCI Express graphics attach)
  - — 32-bit downstream addressing
  - — Messaging and Error Handling
- Package
  - — 34 mm × 34 mm, 1202 balls, non-grid pattern

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1 Introduction

The Intel® 945G/945GZ/945GC/945P/945PL Express chipsets are designed for use with the Intel® Core™2 Duo, Intel® Celeron 400 series, Intel® Pentium® D processor, Intel® Pentium® 4 processor. Additionally, Intel® 945GC Express chipsets also support Intel® Atom™ Processor 200 Series and Intel® Atom™ Processor 300 Series. Each chipset contains two components: GMCH (or MCH) for the host bridge and I/O Controller Hub 7 (ICH7) for the I/O subsystem. The 82945G GMCH is part of the 945G Express chipset, 82945GZ GMCH is part of the 945GZ Express chipset, 82945GC GMCH is part of the 945GC Express chipset, 82945P MCH is part of the 945P Express chipset, and 82945PL MCH is part of the 945PL Express chipset. The ICH7 is the seventh generation I/O Controller Hub and provides a multitude of I/O related functions. Figure 1-1, Figure 1-2, and Figure 1-3 show example system block diagrams for the 945G, 945GZ, 945GC and 945P/945PL Express chipsets.

This document is the datasheet for the Intel® 82945G Graphics and Memory Controller Hub (GMCH), Intel® 82945GZ Graphics and Memory Controller Hub (GMCH), Intel® 82945GC Graphics and Memory Controller Hub (GMCH), Intel® 82945P Memory Controller Hub (MCH), and Intel® 82945PL Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the (G)MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

The primary differences between the 82945G GMCH, 82945GZ GMCH, 92945GC GMCH, 82945P MCH, and 82945PL are listed below:

	Intel® 82945G	Intel® 82945GZ	Intel® 82945GC	Intel® 82945P	Intel® 82945PL
Intel® Atom™ Processor 200 and 300 Series	No	No	Yes	No	No
Integrated Graphics Device (and associated SDVO and analog display ports)	Yes	Yes	Yes	No	No
PCI Express Interface	Yes	No	Yes	Yes	Yes
FSB Frequency	1066/800/533 MHz	800/533 MHz	800/533 MHz	1066/800/533 MHz	800/533 MHz
Memory Speed	DDR2-667/533/400	DDR2-533/400	DDR2-667/533/400	DDR2-667/533/400	DDR2-533/400
System Memory Maximum	4 GB	2 GB	2 GB	4 GB	2 GB

Note: Unless otherwise specified, the information in this document applies to Intel® 82945G Graphics and Memory Controller Hub (GMCH), Intel® 82945GZ Graphics and Memory Controller Hub (GMCH), Intel® 82945GC Graphics and Memory Controller Hub (MCH), Intel® 82945P Memory

Controller Hub (MCH), and Intel® 82945PL Memory Controller Hub (MCH),. The term (G)MCH refers to both the 82945G/82945GZ/82945GC GMCHs and 82945P/82945PL MCHs.

Note: Unless otherwise specified, ICH7 refers to the Intel® 82801GB ICH7 and 82801GR ICH7R I/O Controller Hub 7 components.

Figure 1-1. Intel® 945G Express Chipset System Block Diagram Example

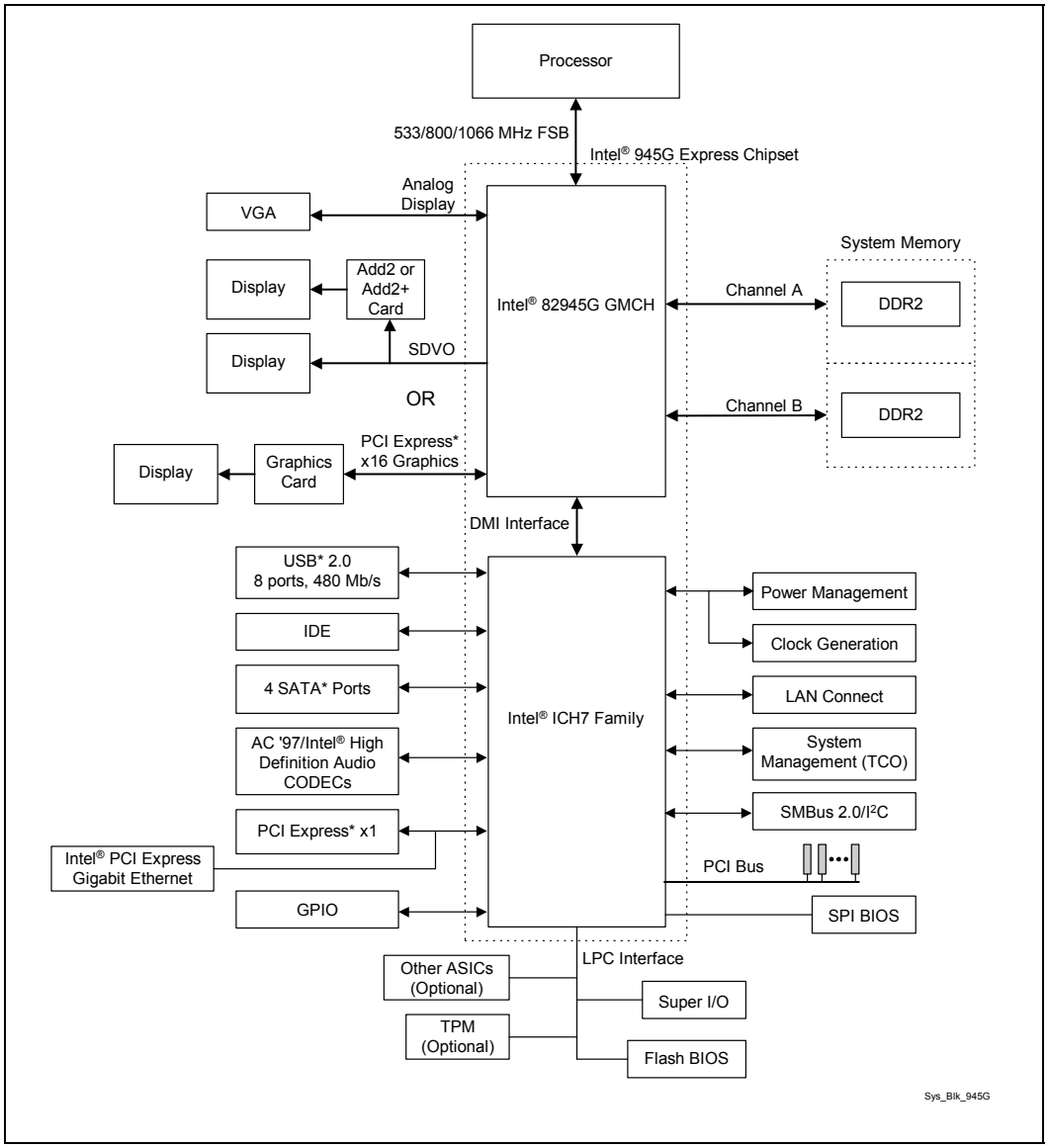


Figure 1-2. Intel® 945GZ/82945GC Express Chipset System Block Diagram Example

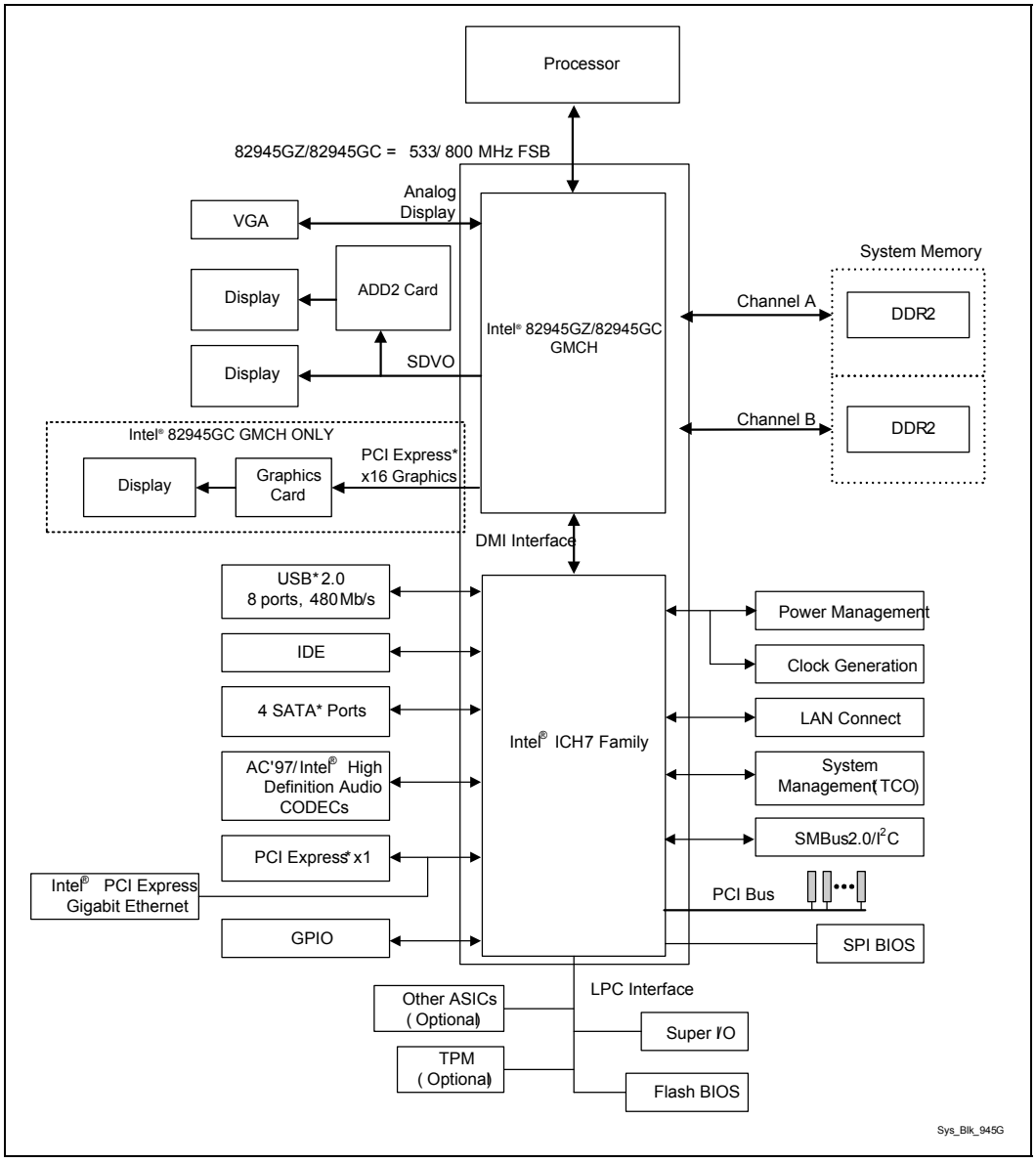
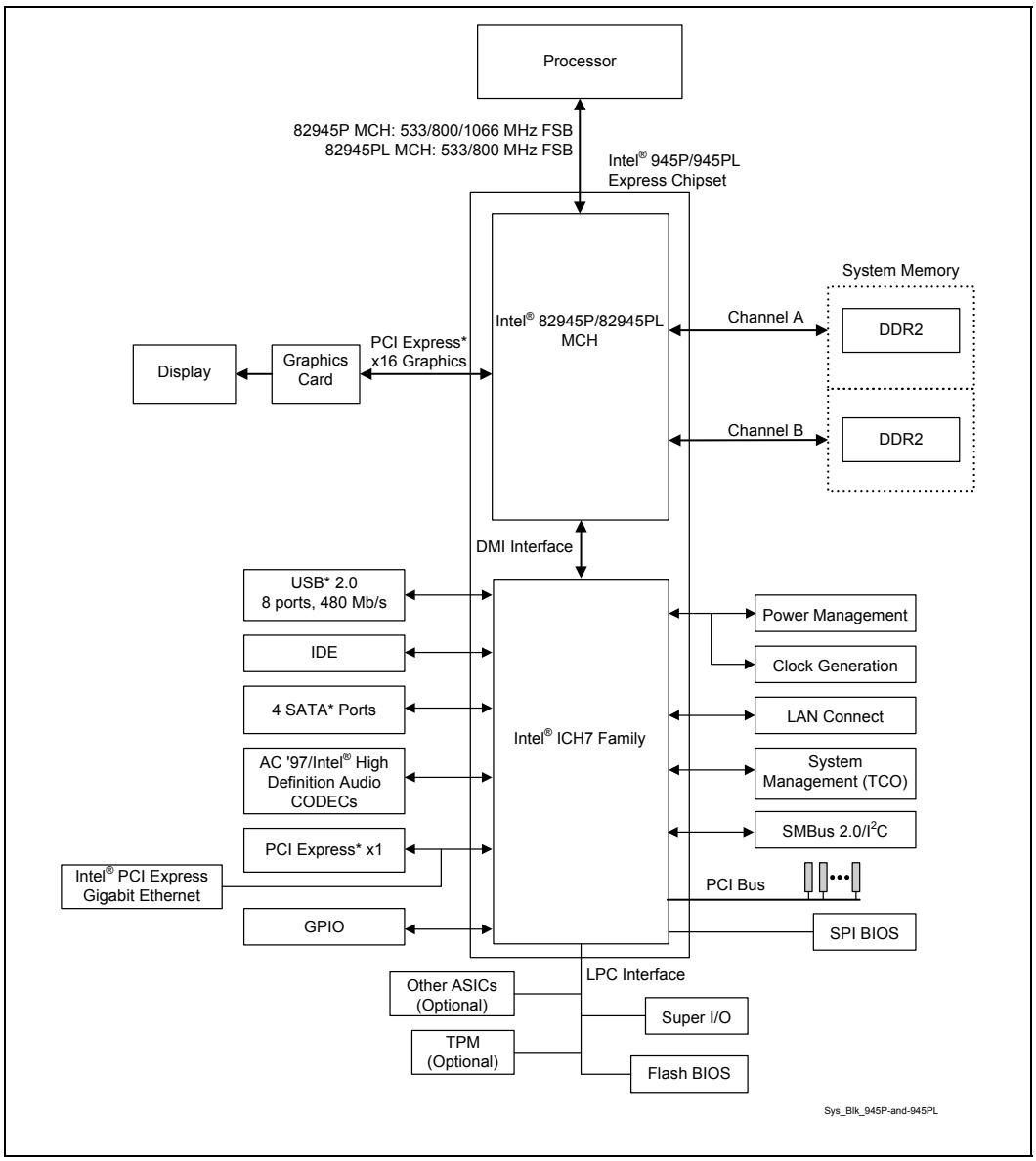


Figure 1-3. Intel® 945P/945PL Express Chipset System Block Diagram Example



1.1 Terminology

Term	Description
Accelerated Graphics Port (AGP)	Refers to the AGP/PCI interface that was previously in the (G)MCH. It has been replaced by PCI Express*.
ADD Card	AGP Digital Display Card. It provides digital display options for an Intel Graphics Controller that supports ADD cards (DVOs multiplexed with AGP interface). It is keyed like an AGP 4x card and plugs into an AGP connector. The AGP Digital Display Card will **not** work with an Intel graphics controller that implements Intel® SDVO.
ADD2 Card	Advanced Digital Display Card – **2**nd Generation. This card provides digital display options for an Intel graphics controller that supports ADD2 cards. It plugs into a x16 PCI Express* connector but uses the multiplexed SDVO interface. This Advanced Digital Display Card will **not** work with an Intel graphics controller that supports Intel® DVO and ADD cards.
ADD2+ Card	Advanced Digital Display Card – **2**nd Generation. This card provides digital display options for an Intel graphics controller that supports ADD2+ cards. It plugs into a x16 PCI Express connector but uses the multiplexed SDVO interface. The card adds Video In capabilities to the platform. This Advanced Digital Display Card will **not** work with an Intel graphics controller that supports DVO and ADD cards. It will function as an ADD2 card in an ADD2 supported system, but Video In capabilities will not work. This is only supported on the Intel® 82945G GMCH.
Core	The internal base logic in the (G)MCH
CRT	Cathode Ray Tube
DBI	Dynamic Bus Inversion
DDR	Double Data Rate SDRAM memory technology
DDR2	A second generation Double Data Rate SDRAM memory technology
DMI	(G)MCH-Intel® ICH7 Direct Media Interface
DVI	Digital Video Interface. DVI is a specification that defines the connector and interface for digital displays.
FSB	Front Side Bus. FSB is synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
GMCH	Graphics Memory Controller Hub component that contains the processor interface, DRAM controller, x16 PCI Express port (typically, the external graphics interface), and an Integrated Graphics Device (IGD). The GMCH communicates with the I/O Controller Hub 7 (ICH7*) and other I/O controller hubs over the DMI interconnect. In this document GMCH refers to the Intel 82945G GMCH and/or 82945GZ GMCH components.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all ATSC HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available through: http://www.hdmi.org/)
Host	This term is used synonymously with processor.
INTx	An interrupt request signal where “x” stands for interrupts A, B, C, and D

Term	Description
Intel® DVO	Digital Video Out port. This term is used for the first generation of Intel graphics controller's digital display channels. Digital display data is provided in a parallel format. This interface is **not** electrically compatible with the 2nd generation digital display channel discussed in this document – SDVO.
Intel® ICH7	Seventh generation I/O Controller Hub component that contains additional functionality compared to previous ICHs. The I/O Controller Hub 7 component contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. ICH7 communicates with the (G)MCH over a proprietary interconnect called DMI.
IGD	Internal Graphics Device.
LCD	Liquid Crystal Display.
LVDS	Low Voltage Differential Signaling. LVDS is a high speed, low power data transmission standard used for display connections to LCD panels.
MCH	Memory Controller Hub. The MCH contains the processor interface, DRAM controller, and x16 PCI Express port (typically, the external graphics interface). It communicates with the I/O Controller Hub 7 (ICH7) and other I/O controller hubs over the DMI interconnect. In this document MCH refers to the Intel 82945P MCH and/or 82945PL MCH components.
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	Third Generation input/output graphics attach called PCI Express Graphics. PCI Express is a high-speed serial interface. The PCI Express configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the (G)MCH to an external Graphics Controller is a x16 link and replaces AGP.
Primary PCI	The Primary PCI is the physical PCI bus that is driven directly by the ICH7 component. Communication between Primary PCI and the (G)MCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
Processor	Intel® Pentium® D processor and Intel® Pentium® 4 processor
SCI	System Control Interrupt. SCI is used in ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). SDVO is a digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel – DVO. For the 82945G/82945GZ GMCH, the SDVO interface is multiplexed on a portion of the x16 graphics PCI Express interface.
SDVO Device	Third party codec that uses SDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-Out, etc.
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. SMI is used to indicate any of several system conditions (such as, thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface from Silicon Image that is used in DVI and HDMI.

Term	Description
TOLM	Top Of Low Memory. The highest address below 4 GB where a processor-initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
VCO	Voltage Controlled Oscillator
UMA	Unified Memory Architecture. UMA describes an IGD using system memory for its frame buffers.

1.2 Reference Documents

Document Name	Doc Number/Location
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	http://developer.intel.com//design/chipsets/datashts/307013.htm
Intel® 945G/945GZ/82945GC/945P/945PL Express Chipset Family Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/chipsets/designex/307504.htm
Intel® 945G/945GZ/82945GC/945P/945PL Express Chipset Family Specification Update	http://developer.intel.com/design/chipsets/specupdt/307503.htm
Advanced Configuration and Power Interface Specification, Revision 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Revision 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Revision 2.3	http://www.pcisig.com/specifications
PCI Express* Specification, Revision 1.0a, July 22, 2002	http://www.pcisig.com/specifications

1.3 (G)MCH Overview

The (G)MCH connects to the processor as shown in the previous system block diagrams. The primary role of a (G)MCH in a system is to manage the flow of information between its interfaces: the processor interface (FSB), the system memory interface (DRAM controller), the integrated graphics interface (82945G/82945GZ/82945GC GMCH only), the external graphics interface (PCI Express), and the I/O Controller through DMI interface. This includes arbitrating between the four interfaces when each initiates transactions.

The (G)MCH supports one or two channels of DDR2 SDRAM. The (G)MCH also supports the new PCI Express based external graphics attach. To increase system performance, the (G)MCH incorporates several queues and a write cache. The (G)MCH also contains advanced desktop power management logic.

1.3.1 Host Interface

The (G)MCH is optimized for the Intel® Atom™ 200 Series, Intel® Atom™ 300 Series based on 45nm process technology in a FCBGA 437 pins socket, Intel® Core™ 2 Duo, Intel® Celeron 400 series, Intel® Pentium 4 processor in the 90 nm process in the LGA775 Land Grid Array package and Intel® Pentium D processor in a LGA775 socket; Only the 82945GC (G)MCH are designed for use with Intel® Atom™ 200 Series and Intel® Atom™ 300 Series. The (G)MCH supports FSB frequencies using a scalable FSB Vcc_CPU. FSB frequencies supported are 133 MHz (533 MT/s), 200 MHz (800 MT/s), and 266 MHz (1066 MT/s); only the 82945G/82945P (G)MCH support 266 MHz (1066 MT/s).

The (G)MCH supports the Pentium 4 processor subset of the Extended Mode Scaleable Bus Protocol. The primary enhancements over the Compatible Mode P6 bus protocol are source synchronous double-pumped (2x) address and source synchronous quad-pumped (4x) data. Other (G)MCH supported features of the host interface include: Hyper-Threading Technology (HT Technology), Pentium 4 processor FSB interrupt delivery, FSB Dynamic Bus Inversion (DBI), 12-deep in-order queue, and a 1-deep defer queue.

The (G)MCH supports 32-bit host addressing, decoding up to 4 GB (2 GB for the 82945PL/82945GC/82945GZ) of the processor's usable memory address space. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the (G)MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI or main memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system SDRAM will be snooped on the host bus.

1.3.2 System Memory Interface

The (G)MCH integrates a system memory DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR2) memory is supported; consequently, the buffers support only SSTL_1.8 V signal interfaces. The memory controller interface is fully configurable through a set of control registers. Features of the (G)MCH memory controller include:

- Maximum memory size:
  - 4 GB for 82945G GMCH and 82945P MCH
  - 2 GB for 82945GZ/82945GC GMCH and 82945PL MCH
- Directly supports one or two channels of memory (each channel consisting of 64 data lines)
  - The memory channels are asymmetric: "Stacked" channels are assigned addresses serially. Channel B addresses are assigned after all Channel A addresses.
  - The memory channels are interleaved: Addresses are ping-ponged between the channels after each cache line (64-B boundary).
- Supports DDR2 400, DDR2 533, and DDR2 667. DDR2 667 is supported on 82945G/82945GC/82945P Only.
- Available bandwidth up to 5.3 GB/s (DDR2 667) for single-channel mode or dual-channel asymmetric mode and 10.7 GB/s (DDR2 667) in dual-channel Interleaved mode.
- Supports DDR2 memory DIMM frequencies of 400 MHz, 533 MHz, and 667 MHz (82945G/82945GC/82945P Only). The speed used in all channels is the speed of the slowest DIMM in the system.
- Supports 256-Mb, 512-Mb, and 1-Gb DDR2 technologies for x8 and x16 devices.

- Supports four banks for all DDR2 devices up to 512-Mbit density. Supports eight banks for 1-Gbit DDR2 devices.
- DDR2-667 4-4-4 is Not supported.
- Supports only unbuffered DIMMs.
- Supports opportunistic refresh.
- In dual channel mode the (G)MCH supports 32 simultaneously open pages.
- SPD (Serial Presence Detect) scheme for DIMM detection support.
- Suspend-to-RAM support using CKE.
- Supports configurations defined in the JEDEC DDR2 DIMM specification only.
- Directly supports two channels of non-ECC DDR2 DIMMs.
- Supports Partial Writes to memory using Data Mask (DM) signals.
- Supports a burst length of 8 for single-channel and dual-channel interleaved and asymmetric operating modes.
- Supports Enhanced Memory Interleave.

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the (G)MCH and I/O Controller Hub 7 (ICH7). This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH7 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH7 and (G)MCH).

Configuration registers for DMI, virtual channel support, and DMI active state power management (ASPM) are in the RCRB space in the (G)MCH Register Description.

- A chip-to-chip connection interface to the ICH7
- 2 GB/s point-to-point DMI to ICH7 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express graphics attach)
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined “End Of Interrupt” broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI, and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.3.4 PCI Express* Interface (Intel® 82945G/82945GC/82945P/82945PL (G)MCH Only)

The 82945G/82945GC/82945P/82945PL (G)MCH contains one 16-lane (x16) PCI Express port intended for an external PCI Express graphics card. The PCI Express port is compliant to the *PCI Express* Base Specification,* Revision 1.0a. The x16 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical bandwidth of 4 Gb/s each direction. The 82945G GMCH multiplexes the PCI Express interface with two Intel® SDVO ports.

- One, 16-lane PCI Express port intended for Graphics Attach, compatible to the *PCI Express* Base* Specification, Revision 1.0a.
- A base PCI Express frequency of 2.5 Gb/s only.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16.
- PCI Express extended configuration space. The first 256 bytes of configuration space is aliased directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above the first 256 bytes (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism. This mechanism accesses the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports “static” lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX15->TX0, RX15->RX0). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express specification. In particular, link initialization is not affected by static lane reversal.

1.4 Graphics (Intel® 82945G/82945GC/82945GZ GMCH Only)

The 82945G/82945GC/82945GZ GMCH provides an integrated graphics device (IGD) delivering cost competitive 3D, 2D, and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, BLT and Stretch BLT operations, motion compensation, overlay, and display control. The GMCH's video engines support video conferencing and other video applications. The GMCH does not support a dedicated local graphics memory interface, it may only be used in a UMA configuration. The GMCH also has the capability to support external graphics accelerators via the PCI Express Graphics (PEG) port but cannot work concurrently with the integrated graphics device. High bandwidth access to data is provided through the system memory port. The GMCH also provides 3D hardware acceleration for block-level transfers of data (BLTs). The 2D BLTs are considered a special case of 3D transfers and use the 3D acceleration. The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces processor load, and thus improves performance.

GMCH graphics support includes:

- Core Frequency of 400 MHz
- 1.6 GP/s pixel rate
- Serial DVO port with two channels (multiplexed on PCI Express* Graphics port) for optional addition of TV-Out/TV-In and/or DVI digital display connections
  - ADD2+ card support (Concurrent PCI Express with SDVO) (82945G only)
- High Quality 3D Setup and Render Engine
  - Setup matching processor geometry delivery rates
  - Triangle lists, strips, and fans
  - Indexed vertex and flexible vertex formats
  - Vertex cache
  - Pixel accurate fast scissoring and clipping operation
  - Backface culling
  - Supports D3D* and OGL* pixelization rules
  - Anti-aliased lines
  - Sprite points
  - Zone Rendering Technology 3
  - Shadow maps
  - Double-sided stencil
- High-Quality Texture Engine
  - DX9* Compliant Hardware Pixel Shader 2.0
  - Per-pixel perspective corrected texture mapping
  - 2/10/10/10 texture format
  - 4x4 filtering
  - Single-pass quad texture compositing
  - Enhanced texture blending functions
  - 12 levels of detail mip map sizes from 1x1 to 2Kx2K
  - All texture formats including 32-bit RGBA and 8-bit palettes
  - Alpha and luminance maps
  - Texture color-keying/chromakeying
  - Bilinear, trilinear and anisotropic mip-mapped filtering
  - Cubic environment reflection mapping
  - Embossed and DOT3 bump-mapping
  - DXTn and FXT1 texture decompression
  - Non-power of 2 texture
  - Render to texture
- Video DVD/PC-VCR
  - VLD/iDCT for enabling Dual HD Streams for MPEG playback (82945G only)
  - H/W Motion Compensation for MPEG2 - 4x HWMC computes
  - Dynamic Bob and Weave Support for Video Streams
  - Source Resolution up to 1920x1080 with 2 vertical taps
  - Software DVD At 30 fps, Full Screen
  - Supports 720x480 DVD Quality Encoding at low processor Use for PC-VCR or home movie recording and editing
- 3D Graphics Rendering Enhancements
  - 1.3 Dual Texture GigaPixel/Sec Fill Rate
  - Flat and Gouraud Shading
  - Color Alpha Blending for Transparency
  - Vertex and Programmable Pixel Fog and Atmospheric Effects
  - Color Specular Lighting
  - Z Bias Support
  - Dithering
  - Anti-Aliased Lines
  - 16- and 24-bit Z Buffering
  - 8-bit Stencil Buffering
  - Double and Triple Render Buffer Support
  - 16- and 32-bit Color
  - Destination Alpha
  - Maximum 3D Resolution Supported: 1600x1200x32 @ 85 Hz
  - Fast Clear Support
- 2D Graphics
  - Optimized 256-bit BLT Engine
  - Alpha Stretch Blitter
  - Anti-aliased Lines
  - 32-bit Alpha Blended Cursor
  - Color Space Conversion
  - Programmable 3-Color Transparent Cursor
  - 8-, 16-, and 32-bit Color
  - ROP Support
- Video DVD/PC-VCR
  - VLD/iDCT for enabling Dual HD Streams for MPEG playback (82945G only)
  - H/W Motion Compensation for MPEG2 - 4x HWMC computes
  - Dynamic Bob and Weave Support for Video Streams
  - Source Resolution up to 1920x1080 with 2 vertical taps
  - Software DVD At 30 fps, Full Screen
  - Supports 720x480 DVD Quality Encoding at low processor Utilization for PC-VCR or home
  - movie recording and editing
- Video Overlay
  - Advanced Deinterlacing
  - Process Amplifier Color Control
  - Single High Quality Scalable Overlay
- Multiple Overlay Functionality provided via Stretch Blitter (PIP, Video Conferencing, etc.)
  - 5-tap Horizontal, 3-tap Vertical Filtered Scaling
  - Independent Gamma Correction
  - Independent Brightness/Contrast/Saturation
  - Independent Tint/Hue Support
  - Destination Color-keying
  - Source Chroma-keying
  - Maximum Source Resolution: 720x480x32
  - Maximum Overlay Display Resolution: 2048x1536x32
  - Video Mixer Render (VMR)

1.5 Analog and SDVO Displays (Intel® 82945G/82945GC/82945GZ GMCH Only)

The GMCH provides interfaces to a progressive scan analog monitor and two SDVO ports (multiplexed with PCI Express x16 graphics port signals on the 82945G/82945GC) capable of driving an ADD2/ADD2+ card. The digital display channels are capable of driving a variety of SDVO devices (e.g., TMDS, TV-Out). Note that SDVO only works with the Integrated Graphics Device (IGD). The ADD2+ card adds Video-in capabilities and is only supported on the 82945G GMCH. The GMCH provides two multiplexed SDVO ports that are capable of driving up to a 200 MHz pixel clock each. The GMCH can make use of these digital display channels via an Advanced Digital Display card (ADD2/2+) card.

The GMCH SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data. Alternatively, the SDVO ports can be combined to support dual channel devices, supporting higher resolutions and refresh rates. The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

The 82945G/82945GC GMCH supports Hot-Plug and Display for the PCI Express x16 graphics. This is not supported for ADD2 cards.

1.5.1 System Interrupts

- Supports both 8259 and Pentium 4 processor FSB interrupt delivery mechanisms.
- Supports interrupts signaled as upstream Memory Writes from PCI Express and DMI
- MSIs routed directly to FSB
- From I/OxAPICs
- Provides redirection for IPI(Inter-Processor Interrupts) and upstream interrupts to the FSB

1.5.2 (G)MCH Clocking

The differential Host clock of 133/200/266 MHz (HCLKP/HCLKN) supports transfer rates of 533/800/1066 MT/s, respectively. The 266 MHz HCLKP/HCLKN is only available on the 82945G GMCH and 82945P MCH. The Host PLL generates 2X, 4X, and 8X versions of the host clock for internal optimizations. The (G)MCH core clock is synchronized to the host clock.

The internal and external memory clocks of 200, 266, and 333 MHz are generated from one of two (G)MCH PLLs that use the Host clock as a reference. This includes 2x and 4x for internal optimizations.

The PCI Express core clock of 250 MHz is generated from a separate PCI Express PLL that uses the fixed 100 MHz Serial Reference Clock (GCLKP/GCLKN) for reference.

Display timings are generated from display PLLs that use a 96 MHz differential non-spread spectrum clock as a reference. Display PLLs can also use the SDVO_TVCLKIN[+/-] from an SDVO device as a reference.

All of the above clocks are capable of tolerating Spread Spectrum clocking as defined in the Clock Generator specification. Host, memory, and PCI Express PLLs, and all associated internal clocks are disabled until PWROK is asserted.

1.5.3 Power Management

(G)MCH Power Management support includes:

- PC99 suspend to DRAM support ("STR", mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1-MB TSEG from the base of graphics "stolen" memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Revision 1.0 compatible power management
- Supports processor states C0 and C1. The (G)MCH does not support the C2, C3, and C4 states.
- Supports system states S0, S1D, S3, S4, and S5
- Supports processor Thermal Management 2 (TM2)
- Microsoft Windows NT* Hardware Design Guide v1.0 compliant

§

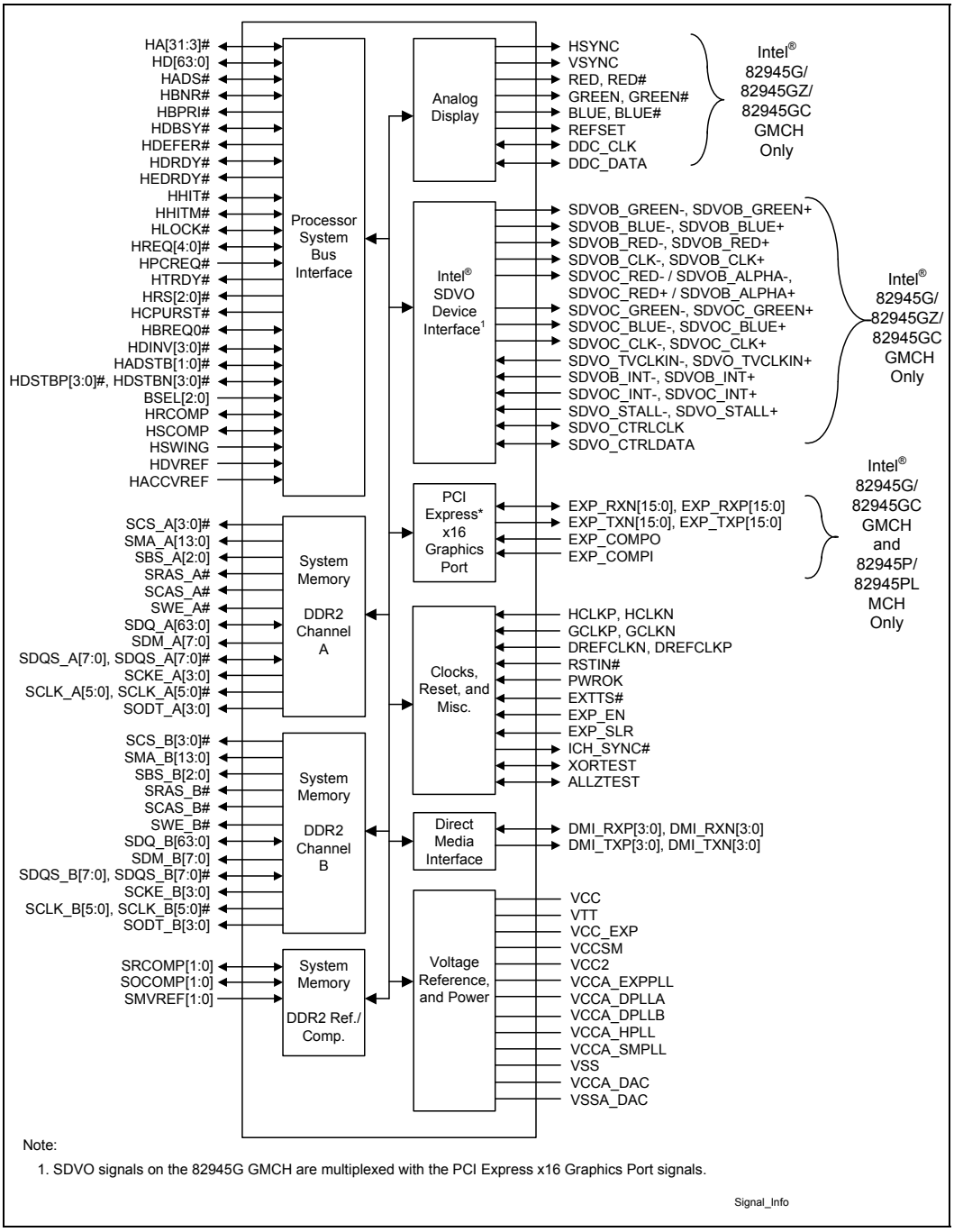
2 Signal Description

This chapter provides a detailed description of (G)MCH signals. The signals are arranged in functional groups according to their associated interface (see Figure 2-1).

The following notations are used to describe the signal type:

PCIE	PCI Express interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 2.5 V tolerant.
HCSL	Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = (|D+ - D-|) * 2 = 1.4 V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage is 0.35 V.
HVCMOS	High Voltage CMOS buffers. 2.5 V tolerant.
HVIN	High Voltage CMOS input-only buffers. 3.3 V tolerant.
SSTL-1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

Figure 2-1. Signal Information Diagram



2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** HBNR# is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH7 must provide processor frequency select strap set-up and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH7 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** HDEFER# indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0] signals. They indicate if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **HDINV[x]# — Data Bits** HDINV3# — HD[63:48] HDINV2# — HD[47:32] HDINV1# — HD[31:16] HDINV0# — HD[15:0]

Signal Name	Type	Description
HDRDY#	I/O GTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready:** This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express* initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** These signals are the source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** These signals are the differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobes** / **Data** / **Bits** HDSTBP3#, HDSTBN3# / HD[63:48] / HDINV3# HDSTBP2#, HDSTBN2# / HD[47:32] / HDINV2# HDSTBP1#, HDSTBN1# / HD[31:16] / HDINV1# HDSTBP0#, HDSTBN0# / HD[15:0] / HDINV0#
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. In addition, HHIT# is driven in conjunction with HHITM# by the target to extend the snoop window.
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. In addition, HHITM# is driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express accesses to DRAM are allowed when HLOCK# is asserted by the processor).
HPCREQ#	I GTL+ 2x	**Precharge Request:** The processor provides a “hint” to the (G)MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The (G)MCH uses this information to schedule the read request to memory using the special “AutoPrecharge” attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. HPCREQ# is asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.

Signal Name	Type	Description
HREQ[4:0]#	I/O GTL+ 2x	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half, the signals carry additional information to define the complete transaction type.
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Response Signals:** These signals indicate the type of response as shown below: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by (G)MCH) 100 = Hard Failure (not driven by (G)MCH) 101 = No data response 110 = Implicit Writeback 111 = Normal data response
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O CMOS	**Host RCOMP:** This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}).
HSCOMP	I/O CMOS	**Slew Rate Compensation:** This is the compensation signal for the Host Interface.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HDVREF	I A	**Host Reference Voltage:** Voltage input for the data, address, and common clock signals of the Host GTL interface.
HACCVREF	I A	**Host Reference Voltage**. Reference voltage input for the Address, and Common clock signals of the Host GTL interface.

2.2 DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_A[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_A#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8 2x	**Data Lines:** The SDQ_A[63:0] signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax bit for every data byte lane.
SDQS_A[7:0]	I/O SSTL-1.8 2x	**Data Strobes:** For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.
SDQS_A[7:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Ax is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

2.3 DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_B[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank
SMA_B[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_B[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_B#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SCAS_B#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8 2x	**Data Lines:** The SDQ_B[63:0] signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL-1.8 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx for every data byte lane.
SDQS_B[7:0]	I/O SSTL-1.8 2x	**Data Strobes:** For DDR2, SDQS_Bx and its complement SDQS_Bx# make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements:** These are the complementary DDR2 Strobe signals.
SCKE_B[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Bx is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

2.4 DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) Driver Compensation**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** These signals are reference voltage inputs for each SDQ_x, SDM_x, SDQS_x, and SDQS_x# input signals.

2.5 PCI Express* Interface Signals (Intel® 82945G/82945GC/82945P/82945PL Only)

Unless otherwise specified, PCI Express signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Note: PCI Express Interface signals are not on the 82945GZ.

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	**PCI Express* Receive Differential Pair**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	**PCI Express* Transmit Differential Pair**
EXP_COMPO	I A	**PCI Express* Output Current Compensation**
EXP_COMPI	I A	**PCI Express* Input Current Compensation**

2.6 Analog Display Signals (Intel® 82945G/82945GC/82945GZ GMCH Only)

Signal Name	Type	Description
RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O A	**REDB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance: however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
GREEN#	O A	**GREENB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O A	**BLUEB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 Ω 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 2.5V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5 V output
VSYNC	O 2.5V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5 V output.
DDC_CLK	I/O 2.5V CMOS	**Monitor Control Clock.** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 2.5V CMOS	**Monitor Control Data.** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

2.7 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I HCSL	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.
GCLKP GCLKN	I HCSL	**Differential PCI Express* Clock In:** These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I HCSL	**Display PLL Differential Clock In**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH7. All PCI Express graphics attach output signals will also tri-state compliant to *PCI Express* Specification, Revision 1.0a.* This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXTTS#	I CMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
EXP_EN	I CMOS	**PCI Express SDVO Concurrent Select** 0 = Only SDVO or PCI Express operational 1 = SDVO and PCI Express operating simultaneously via PCI Express port **NOTES:** For the 82945GZ GMCH and 82945P/82945PL MCH, this signal should be pulled low.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal/Form Factor Selection:** (G)MCH's PCI Express lane numbers are reversed to differentiate Balanced Technology Extended (BTX) or ATX form factors. 0 = (G)MCH's PCI Express lane numbers are reversed (BTX Platforms) 1 = Normal operation (ATX Platforms) **NOTES:** This signal does not apply to the 82945GZ.
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH7.
XORTEST	I/O GTL+	**XOR Test:** This signal is used for Bed of Nails testing by OEMs to execute XOR Chain test.
ALLZTEST	I/O GTL+	**All Z Test:** As an input this signal is used for Bed of Nails testing by OEMs to execute XOR Chain test. It is used as an output for XOR chain testing.

2.8 Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	**Direct Media Interface:** These signals are receive differential pairs (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** These signals are transmit differential pairs (Tx).

2.9 Intel® Serial DVO (SDVO) Interface (Intel® 82945G/82945GC/82945GZ GMCH Only)

For the 82945G/82945GC GMCH, all but two of the pins in this section are multiplexed with the upper 8 lanes of the PCI Express interface.

Signal Name	Type	Description
SDVOB_CLK-	O PCIE	**Serial Digital Video Channel B Clock Complement**. This signal is multiplexed with EXP_TXN12.
SDVOB_CLK+	O PCIE	**Serial Digital Video Channel B Clock**. This signal is multiplexed with EXP_TXP12.
SDVOB_RED-	O PCIE	**Serial Digital Video Channel C Red Complement**. This signal is multiplexed with EXP_TXN15.
SDVOB_RED+	O PCIE	**Serial Digital Video Channel C Red**. This signal is multiplexed with EXP_TXP15.
SDVOB_GREEN-	O PCIE	**Serial Digital Video Channel B Green Complement**. This signal is multiplexed with EXP_TXN14.
SDVOB_GREEN+	O PCIE	**Serial Digital Video Channel B Green**. This signal is multiplexed with EXP_TXP14.
SDVOB_BLUE-	O PCIE	**Serial Digital Video Channel B Blue Complement**. This signal is multiplexed with EXP_TXN13.
SDVOB_BLUE+	O PCIE	**Serial Digital Video Channel B Blue**. This signal is multiplexed with EXP_TXP13.
SDVOC_RED- / SDVOB_ALPHA-	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha Complement**. This signal is multiplexed with EXP_TXN11.
SDVOC_RED+ / SDVOB_ALPHA+	O PCIE	**Serial Digital Video Channel C Red Channel B Alpha**. This signal is multiplexed with EXP_TXP11.
SDVOC_GREEN-	O PCIE	**Serial Digital Video Channel C Green Complement**. This signal is multiplexed with EXP_TXN10.
SDVOC_GREEN+	O PCIE	**Serial Digital Video Channel C Green**. This signal is multiplexed with EXP_TXP10.
SDVOC_BLUE-	O PCIE	**Serial Digital Video Channel C Blue Complement**. This signal is multiplexed with EXP_TXN9.
SDVOC_BLUE+	O PCIE	**Serial Digital Video Channel C Blue**. This signal is multiplexed with EXP_TXP9.

Signal Name	Type	Description
SDVOC_CLK-	O PCIE	**Serial Digital Video Channel C Clock Complement**. This signal is multiplexed with EXP_TXN8.
SDVOC_CLK+	O PCIE	**Serial Digital Video Channel C Clock**. This signal is multiplexed with EXP_TXP8.
SDVO_TVCLKIN-	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock Complement**. This signal is multiplexed with EXP_RXN15.
SDVO_TVCLKIN+	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock**. This signal is multiplexed with EXP_RXP15.
SDVOB_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement.** This signal is multiplexed with EXP_RXN14.
SDVOB_INT+	I PCIE	**Serial Digital Video Input Interrupt.** This signal is multiplexed with EXP_RXP14.
SDVOC_INT+	I PCIE	**Serial Digital Video Input Interrupt.** This signal is multiplexed with EXP_RXP10
SDVOC_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement.** This signal is multiplexed with EXP_RXN10
SDVO_STALL-	I PCIE	**Serial Digital Video Field Stall Complement.** This signal is multiplexed with EXP_RXN13.
SDVO_STALL+	I PCIE	**Serial Digital Video Field Stall.** This signal is multiplexed with EXP_RXP13.
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock.**
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data.**

2.10 Power and Ground

Name	Voltage	Description
VCC	1.5 V	**Core Power**
VTT	1.2 V	**Processor System Bus Power**
VCC_EXP	1.5 V	**PCI Express* and DMI Power**
VCCSM	1.8 V	**System Memory Power**
VCC2	2.5 V	**2.5 V CMOS Power**
VCCA_EXPPLL	1.5 V	**PCI Express PLL Analog Power**
VCCA_DPLLA (GMCH ONLY)	1.5 V	**Display PLL A Analog Power**
VCCA_DPLLB (GMCH ONLY)	1.5 V	**Display PLL B Analog Power**
VCCA_HPLL	1.5 V	**Host PLL Analog Power**
VCCA_SMPLL	1.5 V	**System Memory PLL Analog Power**
VCCA_DAC	2.5 V	**Display DAC Analog Power**
VSS	0 V	**Ground**
VSSA_DAC	0 V	**Ground**

2.11 Reset States and Pull-up/Pull-downs

This section describes the expected states of the (G)MCH I/O buffers during and immediately after the assertion of RSTIN#. This table only refers to the contributions on the interface from the (G)MCH and does NOT reflect any external influence (such as, external pull-up/pull-down resistors or external drivers).

Legend:

DRIVE: Strong drive (to normal value supplied by core logic if not otherwise stated)

TERM: Normal termination devices are turned on

LV: Low voltage

HV: High voltage

IN: Input buffer enabled

TRI: Tri-state

PU: Weak internal pull-up: 7.2 KΩ – 11.1 KΩ, unless otherwise specified.

PD: Weak internal pull-down: 600 Ω – 880 Ω unless otherwise specified.

CMCT: Common Mode Center Tapped. Differential signals are weakly driven to the common mode central voltage.

STRAP: Strap input sampled during assertion edge of PWROK.

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	Pull-up/ Pull-down
Host Interface	HCPURST#	O	DRIVE LV	TERM HV after approximately 1ms	
	HADSTB[1:0]#	I/O	TERM HV	TERM HV	
	HA[35:3]#	I/O	TERM HV STRAP	POC	
	HD[63:0]	I/O	TERM HV	TERM HV	
	HDSTBP[3:0]#	I/O	TERM HV	TERM HV	
	HDSTBN[3:0]#	I/O	TERM HV	TERM HV	
	HDINV[3:0]#	I/O	TERM HV	TERM HV	
	HADS#	I/O	TERM HV	TERM HV	
	HBNR#	I/O	TERM HV	TERM HV	
	HBPRI#	O	TERM HV	TERM HV	
	HDBSY#	I/O	TERM HV	TERM HV	
	HDEFER#	O	TERM HV	TERM HV	
	HDRDY#	I/O	TERM HV	TERM HV	
	HEDRDY#	O	TERM HV	TERM HV	
	HHIT#	I/O	TERM HV	TERM HV	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	Pull-up/ Pull-down
	HHITM#	I/O	TERM HV	TERM HV	
	HLOCK#	I/O	TERM HV	TERM HV	
	HREQ[4:0]#	I/O	TERM HV	TERM HV	
	HTRDY#	O	TERM HV	TERM HV	
	HRS[2:0]#	I	TERM HV	TERM HV	
	HBREQ0#	O	TERM HV	TERM HV	
	HPCREQ#	I	TERM HV	TERM HV	
	HDREF	I	IN	IN	
	HRCOMP	I/O	TRI	TRI after RCOMP	RCOMP
	HSWING	I	IN	IN	
	HSCOMP	I/O	TRI	TRI	
	HACCVREF	I	IN	IN	
System Memory Channel A	SCLK_A[5:0]	O	TRI	TRI	
	SCLK_A[5:0]#	O	TRI	TRI	
	SCS_A[3:0]#	O	TRI	TRI	
	SMA_A[13:0]	O	TRI	TRI	
	SBS_A[2:0]	O	TRI	TRI	
	SRAS_A#	O	TRI	TRI	
	SCAS_A#	O	TRI	TRI	
	SWE_A#	O	TRI	TRI	
	SDQ_A[63:0]	I/O	TRI	TRI	
	SDM_A[7:0]	O	TRI	TRI	
	SDQS_A[7:0]	I/O	TRI	TRI	
	SDQS_A[7:0]#	I/O	TRI	TRI	
	SCKE_A[3:0]	O	LV	LV	
	SCKE_A[3:0]	O	LV	LV	
	SODT_A[3:0]	O	LV	LV	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	Pull-up/ Pull-down
System Memory Channel B	SCLK_B[5:0]	O	TRI	TRI	
	SCLK_B[5:0]#	O	TRI	TRI	
	SCS_B[3:0]#	O	TRI	TRI	
	SMA_B[13:0]	O	TRI	TRI	
	SBS_B[2:0]	O	TRI	TRI	
	SRAS_B#	O	TRI	TRI	
	SCAS_B#	O	TRI	TRI	
	SWE_B#	O	TRI	TRI	
	SDQ_B[63:0]	I/O	TRI	TRI	
	SDM_B[7:0]	O	TRI	TRI	
	SDQS_B[7:0]	I/O	TRI	TRI	
	SDQS_B[7:0]#	I/O	TRI	TRI	
	SCKE_B[3:0]	O	LV	LV	
	SODT_B[3:0]	O	LV	LV	
System Memory Reference Comp.	SRCOMP0	I/O	TRI	TRI after RCOMP	
	SRCOMP1	I/O	TRI	TRI after RCOMP	
	SMVREF[1:0]	I	IN	IN	
	SOCOMP[1:0]	I/O	TRI	TRI	External 40 Ω resistor to ground
PCI Express* (82945G/82945GC/ 82945P/ 82945PL Only)	EXP_RXN[15:0]	I/O	CMCT	CMCT	
	EXP_RXP[15:0]	I/O	CMCT	CMCT	
	EXP_TXN[15:0]	O	CMCT 1.0V	CMCT 1.0V	
	EXP_TXP[15:0]	O	CMCT 1.0V	CMCT 1.0V	
	EXP_COMPO	O	TRI	TRI	
	EXP_COMPI	I	TRI	TRI	
DMI	DMI_RXN[3:0]	I/O	CMCT	CMCT	
	DMI_RXP[3:0]	I/O	CMCT	CMCT	
	DMI_TXN[3:0]	O	CMCT 1.0V	CMCT 1.0V	
	DMI_TXP[3:0]	O	CMCT 1.0V	CMCT 1.0V	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	Pull-up/ Pull-down
Clocks	HCLKN	I	IN	IN	
	HCLKP	I	IN	IN	
	GCLKN	I	IN	IN	
	GCLKP	I	IN	IN	
	DREFCLKN	I	IN	IN	
	DREFCLKP	I	IN	IN	
Misc	RSTIN#	I	IN	IN	
	PWROK	I	HV	HV	
	ICH_SYNC#	O	PU	PU	INT 10 KΩ PU
	EXTTS#	I	IN	IN	
	BSEL[2:0]	I/O	TRI STRAP	TRI	
	EXP_SLR	I/O	TERM HV STRAP	TERM HV	
	EXP_EN	I/O	PD STRAP	TRI	INT 10 KΩ PD
	SDVO_CTRLCLK (GMCH Only)	I/O	PD	TRI	INT 10 KΩ PD
	SDVO_CTRLDATA (GMCH Only)	I/O	PDSTRAP	TRI	
	XORTEST	I/O	TERM HV STRAP	TERM HV	
	ALLZTEST	I/O	TERM HV STRAP	TERM HV	
DAC	HSYNC	O	LV		
	VSYNC	O	LV		
	RED (GMCH Only)	O	TRI	TRI	
	RED# (GMCH Only)	O	TRI	TRI	
	GREEN (GMCH Only)	O	TRI	TRI	
	GREEN# (GMCH Only)	O	TRI	TRI	
	BLUE (GMCH Only)	O	TRI	TRI	
	BLUE# (GMCH Only)	O	TRI	TRI	
	REFSET	I/O	TRI	0.5*Bandgap	255 Ω 1% Resistor to Ground
	DDC_CLK	I/O	IN	IN	
	DDC_DATA	I/O	IN	IN	

§

3 Register Description

The (G)MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space that controls access to PCI and PCI Express configuration space (see Section 3.5).
- Internal configuration registers residing within the (G)MCH are partitioned into logical device register sets (“logical” since they reside within a single physical device). One register set is dedicated to Host Bridge functionality (i.e., DRAM configuration, other chipset operating parameters, and optional features). Another register set is dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). The 82945G/82945G/82945GZ GMCH contains a third register set that is for the internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the Host processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers that reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

Some of the (G)MCH registers described in this chapter contain reserved bits. These bits are labeled "Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that the software does not need to perform read, merge, and write operation for the configuration address register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32-bits in size). Writes to “Reserved” registers have no effect on the (G)MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.

Upon a Full Reset, the (G)MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters, and optional system features that are applicable, and to program the (G)MCH registers accordingly.

3.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to 1 when read and then will continue to remain set until written. A write of 1 clears (sets to '0') the corresponding bit(s) and a write of 0 has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally, there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent read could retrieve a 1.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent read could retrieve a 1. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Registers with this attribute have bits that may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.

3.2 Platform Configuration

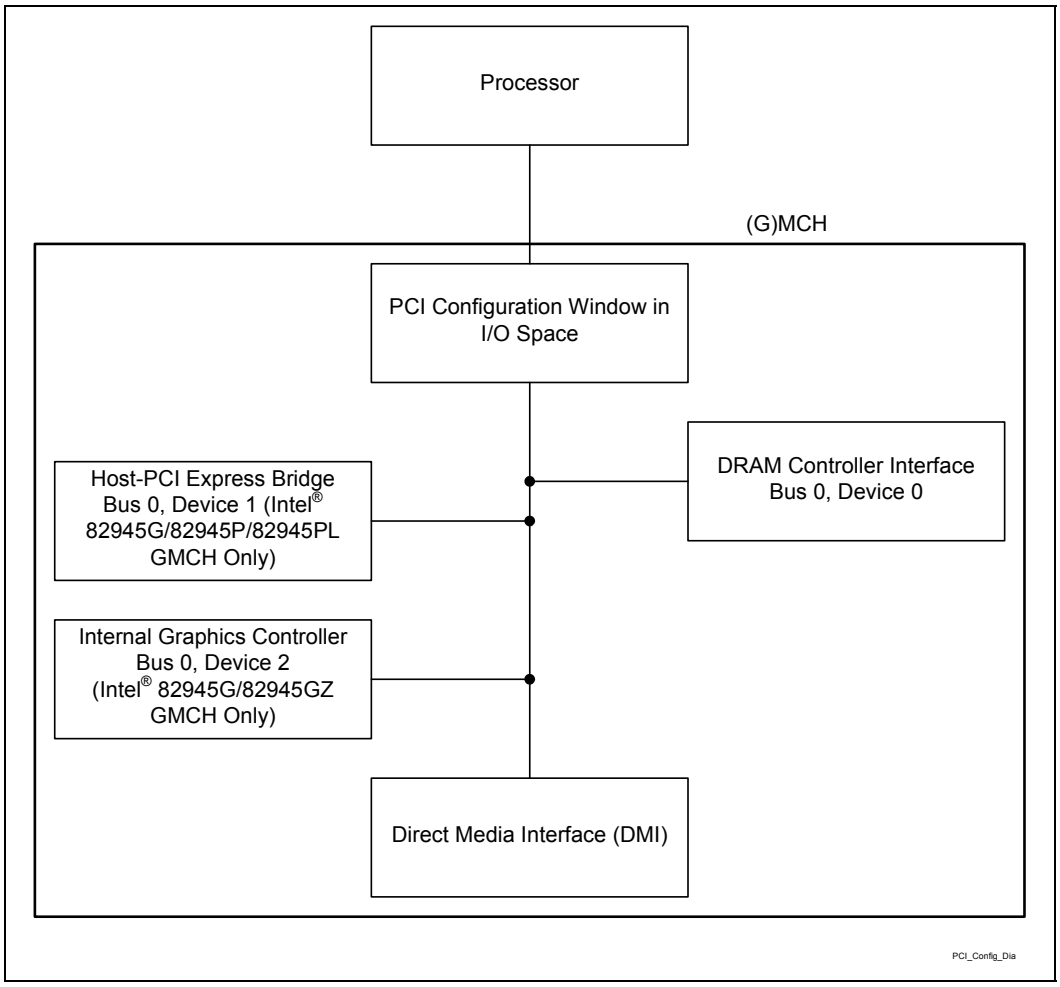
In platforms that support DMI (such as, this (G)MCH) the configuration structure is significantly different from hub architectures prior to the Intel® 915x Express chipsets. The DMI physically connects the (G)MCH and the ICH7; thus, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the (G)MCH and the ICH7 appear to be on PCI bus 0.

Note: The ICH7 internal LAN controller does not appear on bus 0; it appears on the external PCI bus (bus number is configurable).

The system's primary PCI expansion bus is physically attached to the ICH7 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and, therefore, has a programmable PCI bus number. The PCI Express graphics attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist; DMI and the internal devices in the (G)MCH and ICH7 logically constitute PCI Bus 0 to configuration software (see Figure 3-1).

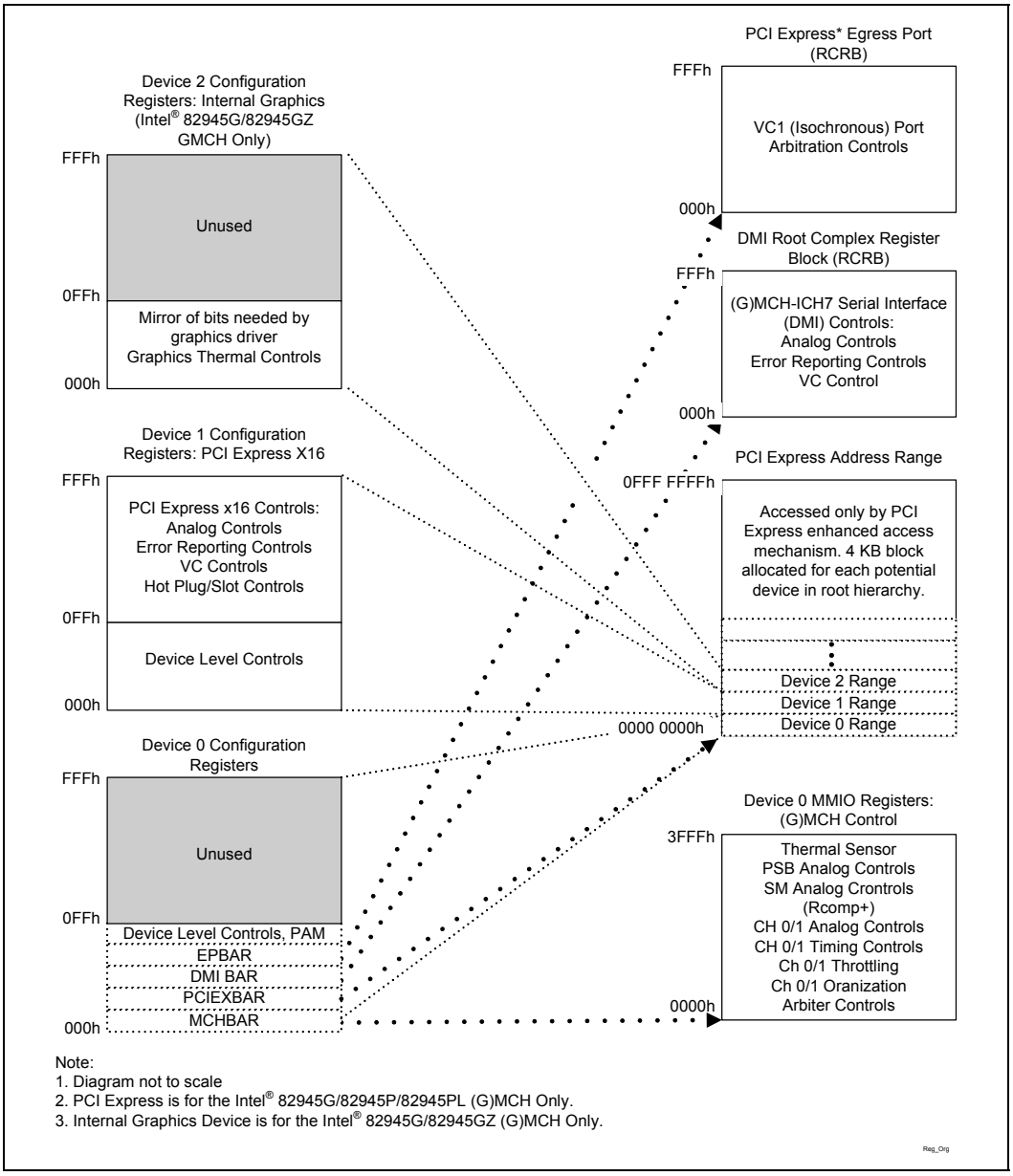
Figure 3-1. Conceptual Chipset Platform PCI Configuration Diagram



The (G)MCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus 0.

- **Device 0: Host Bridge Controller.** Logically, this device is a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other (G)MCH specific registers.
- **Device 1: Host-PCI Express Bridge (82945G/82945GC/82945P/82945PL (G)MCH Only).** Logically, this device appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express* Specification, Revision 1.0a*. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2: Internal Graphics Control (82945G/82945GC/82945GZ GMCH Only).** Logically, this device appears as a PCI device residing on PCI bus 0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.

Figure 3-2. Register Organization



NOTES:

1. Very high level representation. Many details omitted.
2. Internal graphics memory mapped registers are not shown.
3. Only Device 1 uses PCI Express extended configuration space.
4. Device 0 and Device 2 use only standard PCI configuration space.
5. Hex numbers represent address range size and not actual locations.

3.3 Configuration Mechanisms

The processor is the originator of configuration cycles; thus, the FSB is the only interface in the platform where these mechanisms are used. The MCH translates transactions received through both configuration mechanisms to the same format.

3.3.1 Standard PCI Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism uses the CONFIG_ADDRESS register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA register (at I/O address 0CFCh though 0CFFh). To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI, or PCI Express.

3.3.2 PCI Express* Enhanced Configuration Mechanism (Intel® 82945G/82945GC/82945P/82945PL (G)MCH Only)

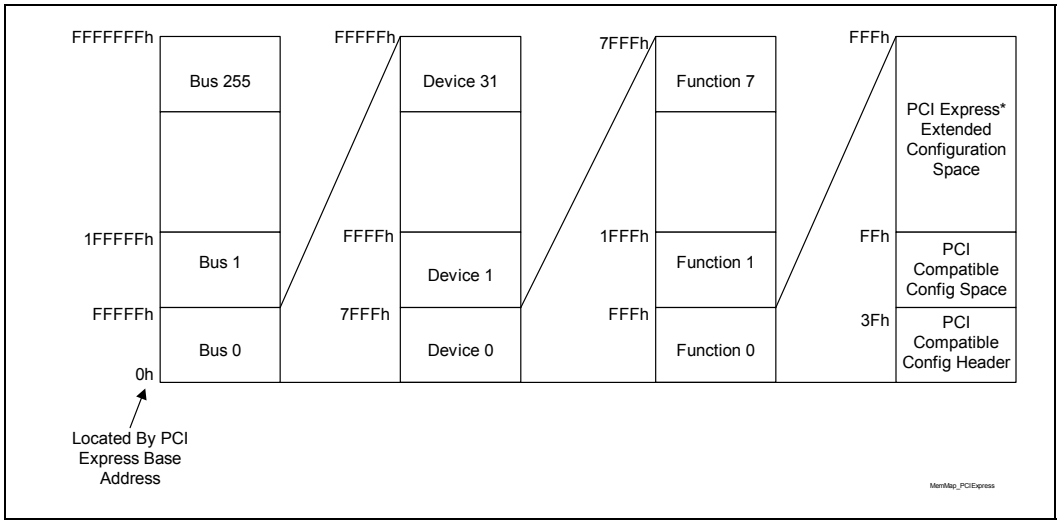
PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by the *PCI Local Bus Specification, Revision 2.3*. PCI Express configuration space is divided into a PCI 2.3 compatible region that consists of the first 256B of a logical device's configuration space and a PCI Express extended region that consists of the remaining configuration space.

The PCI compatible region can be accessed using either the Standard PCI configuration mechanism or using the PCI Express enhanced configuration mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express enhanced configuration mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory-mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express enhanced configuration mechanism uses a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. The PCIEXBAR register defines the base address for the block of addresses below 4 GB for the configuration space associated with busses, devices, and functions that are potentially a part of the PCI Express root complex hierarchy. The PCIEXBAR register contains controls to limit the size of this reserved memory-mapped space; 256 MB is the amount of address space required to reserve space for every bus, device, and function is currently available. Options for 128 MB and 64 MB are available to free up those addresses for other uses. In these cases the number of busses and all of their associated devices and functions are limited to 128 or 64 busses respectively.

The PCI Express configuration transaction header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the function number and register address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI compatible configuration requests, the Extended Register Address field must be all zeros.

Figure 3-3. Memory Map-to-PCI Express* Device Configuration Space



As with PCI devices, each PCI Express device is selected based on decoded address information that is provided as a part of the address portion of configuration request packets. A PCI Express device will decode all address information fields (bus, device, function, and extended address numbers) to provide access to the correct register.

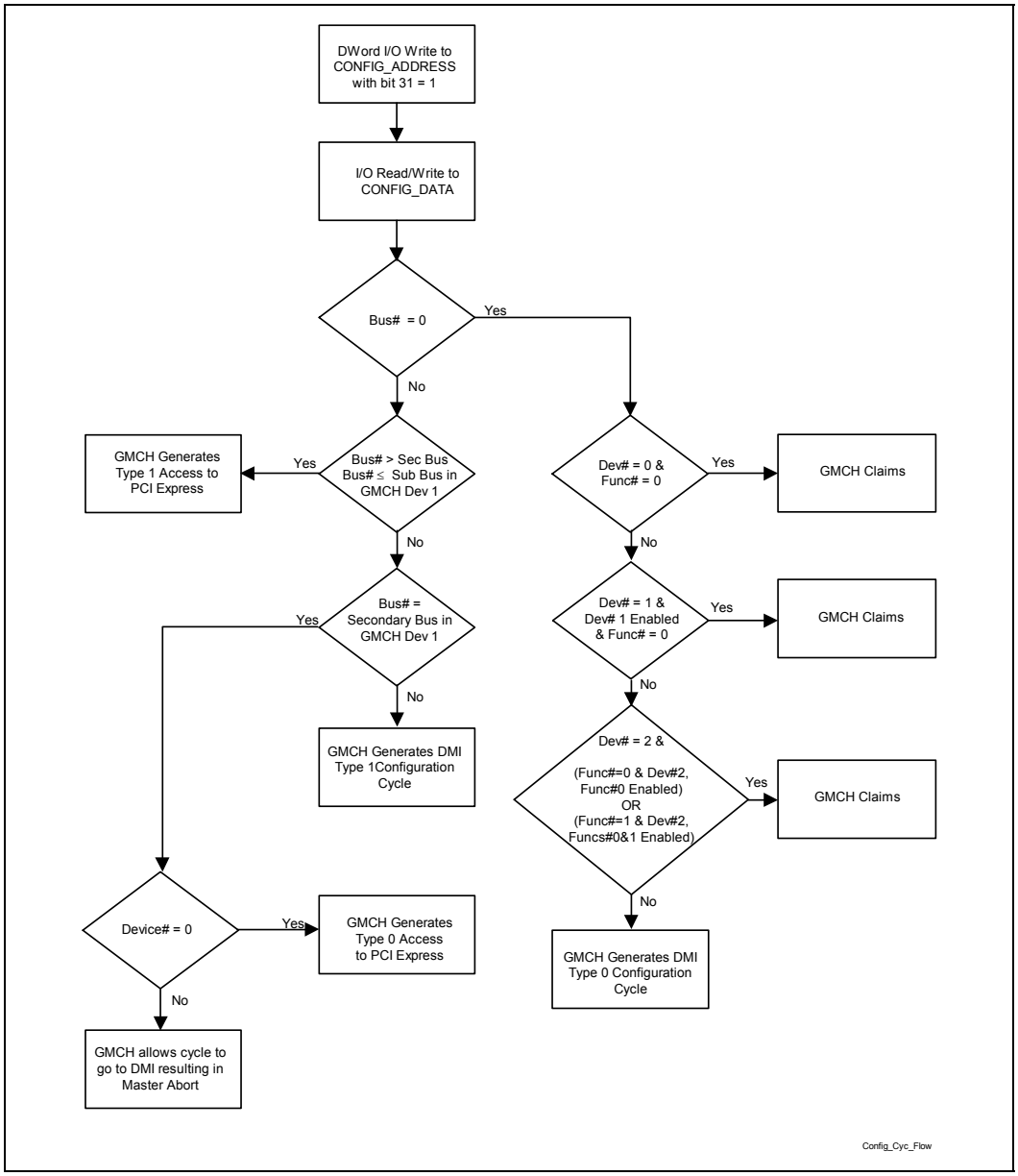
To access this space (steps 1, 2, and 3 are completed only once by BIOS):

1. use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCIEXBAR register.
2. use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register .
3. calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).
4. use a memory write or memory read cycle to the calculated host address to write or read that register.

3.4 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express. The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH7 internal devices and Primary PCI (including downstream devices) are routed to the ICH7 via DMI. Configuration cycles to both the PCI Express graphics PCI compatibility configuration space and the PCI Express graphics extended configuration space are routed to the PCI Express graphics port device or associated link.

Figure 3-4. Intel® 82945G/82945GC (G)MCH Configuration Cycle Flow Chart



3.4.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0, the configuration cycle is targeting a PCI Bus 0 device. If the targeted PCI Bus 0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

3.4.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express or DMI are PCI Express configuration TLPs (Transaction Layer Packets).

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

Special fields for this type of TLP are:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

3.4.2.1 PCI Express* Configuration Accesses (Intel® 82945G/82945GC/82945P/82945PL (G)MCH Only)

When the Bus Number of a type 1 Standard PCI configuration cycle or PCI Express enhanced configuration access matches the Device 1 Secondary Bus Number, a PCI Express type 0 configuration TLP is generated on the PCI Express link targeting the device directly on the opposite side of the link. This should be Device 0 on the bus number assigned to the PCI Express link (likely Bus 1).

The device on the other side of the link must be Device 0. The (G)MCH will Master Abort any type 0 configuration access to a non-zero device number. If there is to be more than one device on that side of the link, there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express enhanced configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but does not match the Device 1 Secondary Bus Number, a PCI Express type 1 configuration TLP is generated on the secondary side of the PCI Express link.

PCI Express Configuration Writes:

- Internally, the host interface unit translates writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express or DMI (i.e., translated to configuration writes)

3.4.2.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PCI Express bridge, or PCI Bus 0 devices not part of the (G)MCH will subtractively decode to the ICH7 and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the (G)MCH generates a type 0 configuration cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PCI Express bridge, the (G)MCH generates a type 1 configuration cycle TLP on DMI.

The ICH7 routes configuration accesses in a manner similar to the (G)MCH. The ICH7 decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus 0 may be claimed by an internal device. The ICH7 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH7, but remain unclaimed by any device or bridge, will result in a master abort.

3.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the processor I/O address space: the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.5.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h (Accessed as a DWord)
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**PCI Configuration Space Enable (CFGE):** 1 = Enabled. Accesses to PCI configuration space are Enabled. 0 = Disabled.
30:24		Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h, the target of the configuration cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is ≥ 2), then a DMI type 0 configuration cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1's Secondary Bus Number or Subordinate Bus Number register, then a DMI type 1 configuration cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a type 0 PCI configuration cycle will be generated on PCI Express*. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of Device 1, and less than or equal to the value programmed into the Subordinate Bus Number register of Device 1, a type 1 PCI configuration cycle will be generated on PCI Express. This field is mapped to byte 8 [7:0] of the request header format during PCI Express configuration cycles and A[23:16] during the DMI type 1 configuration cycles.
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00h, the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity, and Device Number 2 for the Internal Graphics Control (82945G/82945GC/82945GZ GMCH only). Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2 (82945G/82945GC/82945GZ GMCH only), the internal GMCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express configuration cycles and A [15:11] during the DMI configuration cycles.

Bit	Access & Default	Description
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

3.5.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If bit 31 of the CONFIG_ADDRESS Register is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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4 Host Bridge/DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0). Table 4-1 provides an address map of the D0:F0 registers listed by address offset in ascending order. Section 4.1 provides a detailed bit description of the registers.

Warning: Address locations that are not listed are considered Intel Reserved registers locations. Reads to reserved register locations may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 4-1. Host Bridge/DRAM Controller Register Address Map (D0:F0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2770h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	see register description	RO
09–0Bh	CC	Class Code	00h	RO
0Ch	—	*Reserved*	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0F–2Bh	—	*Reserved*	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
30–33h	—	*Reserved*	—	—
34h	CAPPTR	Capabilities Pointer	E0h	RO
35–3Fh	—	*Reserved*	—	—
40–43h	EPBAR	Egress Port Base Address	00000000h	RO
44–47h	MCHBAR	GMCH Memory Mapped Register Range Base Address	00000000h	R/W

Address Offset	Symbol	Register Name	Default Value	Access
48–4Bh	PCIEXBAR	PCI Express* Register Range Base Address (Intel® 82945G/82945GC/82945P/82945PL (G)MCH Only)	E0000000h	R/W
4C–4Fh	DMIBAR	Root Complex Register Range Base Address	00000000h	R/W
50–51h	—	*Reserved*	—	—
52–53h	GGC	GMCH Graphics Control Register (82945G/82945GC/82945GZ GMCH only)	0030h	R/W/L
54–57h	DEVEN	Device Enable	See register description	R/W
58–8Fh	—	*Reserved*	—	—
90h	PAM0	Programmable Attribute Map 0	00h	R/W
91h	PAM1	Programmable Attribute Map 1	00h	R/W
92h	PAM2	Programmable Attribute Map 2	00h	R/W
93h	PAM3	Programmable Attribute Map 3	00h	R/W
94h	PAM4	Programmable Attribute Map 4	00h	R/W
95h	PAM5	Programmable Attribute Map 5	00h	R/W
96h	PAM6	Programmable Attribute Map 6	00h	R/W
97h	LAC	Legacy Access Control	00h	R/W
98–9Bh	—	*Reserved*	—	—
9Ch	TOLUD	Top of Low Usable DRAM	08h	R/W
9Dh	SMRAM	System Management RAM Control	00h	RO, R/W, R/W/L
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RO, R/W/L
9F–C7h	—	*Reserved*	—	—
C8–C9h	ERRSTS	Error Status	0000h	RO, R/W/L
CA–CBh	ERRCMD	Error Command	0000h	R/W
CC–DBh	—	*Reserved*	—	—
DC–DFh	SKPD	Scratchpad Data	00000000h	R/W
E0–E8h	CAPID0	Capability Identifier	See register description	RO

4.1 Device 0 Configuration Register Details

4.1.1 VID—Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** This field provides the PCI standard identification for Intel.

4.1.2 DID—Device Identification (D0:F0)

PCI Device: 0
Address Offset: 02h
Default Value: 2770h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2770h	**Device Identification Number (DID):** This field provides an identifier assigned to the (G)MCH core/primary PCI device.

4.1.3 PCICMD—PCI Command (D0:F0)

PCI Device: 0
Address Offset: 04h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since (G)MCH Device 0 does not physically reside on Primary PCI bus, many of the bits are not implemented.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target, this bit is not implemented and is hardwired to 0.
8	R/W 0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have a SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over DMI to the Intel® ICH7. 1 = The (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. 0 = The SERR message is not generated by the (G)MCH for Device 0. **NOTE:** This bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Hardwired to 0. Address/data stepping is not implemented in the (G)MCH.
6	RO 0b	**Parity Error Enable (PERRE):** Hardwired to 0. PERR# is not implemented by the (G)MCH.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** Hardwired to 0. The (G)MCH does not implement this bit.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The (G)MCH will never issue memory write and invalidate commands.
3		Reserved
2	RO 1b	**Bus Master Enable (BME):** Hardwired to 1. The (G)MCH is always enabled as a master.
1	RO 1b	**Memory Access Enable (MAE):** Hardwired to 1. The (G)MCH always allows access to main memory.
0	RO 0b	**I/O Access Enable (IOAE):** Hardwired to 0. This bit is not implemented.

4.1.4 PCISTS—PCI Status (D0:F0)

PCI Device: 0
Address Offset: 06h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the (G)MCH Device 0 does not physically reside on Primary PCI, many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. Not implemented.
14	R/WC 0b	**Signaled System Error (SSE):** Software clears this bit by writing a 1 to it. 1 = (G)MCH Device 0 generated a SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS, or ERRSTS registers. 0 = (G)MCH Device 0 did Not generate a SERR message over DMI.
13	R/WC 0b	**Received Master Abort Status (RMAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives an Unsupported Request completion packet. 0 = (G)MCH did Not generate a DMI request that receives an Unsupported Request completion packet.
12	R/WC 0b	**Received Target Abort Status (RTAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives a Completer Abort completion packet. 0 = (G)MCH did Not generate a DMI request that receives a Completer Abort completion packet.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. Not implemented. The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to 00. Device 0 does not physically connect to Primary PCI. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for Primary PCI is not limited by the (G)MCH.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Hardwired to 0. Not implemented. PERR signaling and messaging are not implemented by the (G)MCH.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. Device 0 does not physically connect to the Primary PCI. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for the Primary PCI is not limited by the (G)MCH.
6		Reserved
5	RO 0b	**66 MHz Capable:** Hardwired to 0. Does not apply to PCI Express*.

Bit	Access & Default	Description
4	RO 1b	**Capability List (CLIST):** Hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via the CAPPTR register (address offset 34h). The CAPPTR register contains an offset pointing to the start address within configuration space of this device where the Capability standard register resides.
3:0		Reserved

4.1.5 RID—Revision Identification (D0:F0)

PCI Device: 0
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 0.

Bit	Access & Default	Description
7:0	RO	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the *Intel® 945G/945GC/945GZ/945P/945PL Express Chipset Specification Update* for the value of the Revision ID register.

4.1.6 CC—Class Code (D0:F0)

PCI Device: 0
Address Offset: 09h
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. 06h = Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of bridge for the (G)MCH. 00h = Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

4.1.7 MLT—Master Latency Timer (D0:F0)

PCI Device: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the (G)MCH is not a PCI master. Therefore, this register is not implemented.

Bit	Access & Default	Description
7:0		Reserved

4.1.8 HDR—Header Type (D0:F0)

PCI Device: 0
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0 to indicate that the (G)MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

4.1.9 SVID—Subsystem Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

4.1.10 SID—Subsystem Identification (D0:F0)

PCI Device: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

4.1.11 CAPPTR—Capabilities Pointer (D0:F0)

PCI Device: 0
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR register provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

4.1.12 EPBAR—Egress Port Base Address (D0:F0)

PCI Device: 0
Address Offset: 40h
Default Value: 00000000h
Access: RO
Size: 32 bits

This is the base address for the Egress Port MMIO configuration space. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space.

On reset, the Egress Port MMIO Base Address field in this register is disabled and must be enabled by writing a 1 to the EPBAREN bit.

Bit	Access & Default	Description
31:12	R/W 00000h	**Egress Port MMIO Base Address:** This field corresponds to bits 31:12 of the base address Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the (G)MCH MMIO register set.
11:1		Reserved
0	R/W 0b	**EPBAR Enable (EPBAREN):** 0 = EPBAR is disabled and does not claim any memory. 1 = EPBAR memory-mapped accesses are claimed and decoded appropriately.

4.1.13 MCHBAR—(G)MCH Memory Mapped Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 44h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the (G)MCH memory-mapped configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space.

On reset, the (G)MCH Memory Mapped Base Address field in this register is disabled and must be enabled by writing a 1 to the MCHBAREN bit.

Bit	Access & Default	Description
31:14	R/W 00000h	**(G)MCH Memory Mapped Base Address:** This field corresponds to bits 31:14 of the base address (G)MCH memory-mapped configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the (G)MCH memory-mapped register set.
13:1		Reserved
0	R/W 0b	**MCHBAR Enable (MCHBAREN):** 0 = MCHBAR is disabled and does not claim any memory. 1 = MCHBAR memory-mapped accesses are claimed and decoded appropriately

4.1.14 PCIEXBAR—PCI Express* Register Range Base Address (D0:F0) (Intel® 82945G/82945GC/82945P/82945PL (G)MCH Only)

PCI Device: 0
Address Offset: 48h
Default Value: E0000000h
Access: R/W
Size: 32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express hierarchy associated with the (G)MCH. This window of up to 256-MB does not contain actual physical memory that can be addressed. The actual length is determined by a field in this register. Each PCI Express hierarchy requires a PCI Express ase register. The (G)MCH supports one PCI Express hierarchy.

The region reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space. For example, MCHBAR reserves a 16-KB space outside of PCIEXBAR space. It cannot be overlaid on the space reserved by PCIEXBAR for device 0.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses defined by the Length field in this register), above TOLUD and still within total 32 bit addressable memory space.

All other bits not decoded are read only 0. The PCI Express Base Address cannot be less than the maximum address written to the top of physical memory register (TOLUD). Software must ensure that these ranges do not overlap with known ranges located above TOLUD.

Bit	Access & Default	Description
31:28	R/W Eh	**PCI Express* Base Address:** This field corresponds to bits 31:28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 2:1 of this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within total 32-bit addressable memory space. The address bits decoded depends on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = PCI Express Base Address + 32 KB. Remember that this address is the beginning of the 4 KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.

Bit	Access & Default	Description
27	R/W 0b	**128 MB Base Address Mask (128ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	R/W 0b	**64 MB Base Address Mask (64ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register
25:3		Reserved
2:1	R/W 00b	**Length (LENGTH):** This field describes the length of this region. 00 = 256 MB (buses 0–255). Bits 31:28 are decoded in the PCI Express Base Address Field 01 = 128 MB (Buses 0–127). Bits 31:27 are decoded in the PCI Express Base Address Field. 10 = 64 MB (Buses 0–63). Bits 31:26 are decoded in the PCI Express Base Address Field. 11 = Reserved
0	R/W 0h	**PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 31:26 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:26 match PCIEXBAR will be translated to configuration reads and writes within the (G)MCH.

4.1.15 DMIBAR—Root Complex Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 4Ch
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express hierarchy associated with the (G)MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space.

On reset, the DMI Base Address field in this register is disabled and must be enabled by writing a 1 to the DMIBAREN bit.

Bit	Access & Default	Description
31:12	R/W 00000 h	**DMI Base Address:** This field corresponds to bits 31:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB (2 GB for the 82945GC, 82945GZ and 82945PL). System Software uses this base address to program the DMI register set.
11:1		Reserved
0	R/W 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory. 1 = DMIBAR memory-mapped accesses are claimed and decoded appropriately.

4.1.16 GGC—GMCH Graphics Control Register (D0:F0) (Intel® 82945G/82945GC/82945GZ GMCH Only)

PCI Device: 0
Address Offset: 52h
Default Value: 0030h
Access: R/W/L
Size: 16 bits

Bit	Access & Default	Descriptions
15:7		Reserved
6:4	R/W/L 011 b	**Graphics Mode Select (GMS):** This field selects the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and native (linear) modes. BIOS ensures that memory is pre-allocated only when internal graphics is enabled. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within D2:F0 Class Code register is 80h. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved **NOTE:** This register is locked and becomes read only when the D_LCK bit in the SMRAM register is set.
3:2		Reserved
1	R/W 0 b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA cycles (memory and I/O); the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (memory and I/O); the Sub-Class Code field within D2:F0 Class Code register is 80h.
0		Reserved

4.1.17 DEVEN—Device Enable (D0:F0)

PCI Device: 0
Address Offset: 54h
Default Value: 82945G/82945GC/82945GZ GMCH: 0000001Bh
82945P/82945PL MCH: 00000003h
Access: R/W
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH.

Bit	Access & Default	Description
31:5		Reserved
4	R/W 1b (GMCH) 0b (MCH)	**82945G/82945GC/82945GZ GMCH** **Internal Graphics Engine Function 1 (D2F1EN):** 0 = Disable. Bus0:D2:F1 is disabled and hidden 1 = Enable. Bus0:D2:F1 is enabled and visible **NOTE:** Setting this bit to enabled when bit 3 is 0 has no meaning. **82945P/82945PL MCH** Reserved.
3	R/W 1b (GMCH) 0b (MCH)	**82945G/82945GC/82945GZ GMCH** **Internal Graphics Engine Function 0 (D2F0EN):** 0 = Disable. Bus0:D2:F0 is disabled and hidden 1 = Enable. Bus0:D2:F0 is enabled and visible **82945P/82945PL MCH** Reserved
2		Reserved
1	R/W 1b	**82945G/82945GC/82945P/82945PL (G)MCH** **PCI Express* Port (D1EN):** 0 = Disable. Bus0:D1:F0 is disabled and hidden. 1 = Enable. Bus0:D1:F0 is enabled and visible. **82945GZ GMCH** Reserved
0	RO 1b	**Host Bridge:** Hardwired to 1. Bus0:D0:F0 can not be disabled.

4.1.18 PAM0—Programmable Attribute Map 0 (D0:F0)

PCI Device:	0
Address Offset:	90h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFh

The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE (Read Enable). When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to Primary PCI.
- WE (Write Enable). When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to Primary PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0F0000h–0FFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that addresses the BIOS area from 0F0000 to 0FFFFF. 00 = DRAM Disabled: All accesses are directed to the DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0		Reserved

Warning: The (G)MCH may hang if a PCI Express graphics attach or DMI-originated access to read disabled or write disabled PAM segments occur (due to a possible IWB to non-DRAM). For these reasons, the following critical restriction is placed on the programming of the PAM regions:

> At the time that a DMI or PCI Express graphics attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

4.1.19 PAM1—Programmable Attribute Map 1 (D0:F0)

PCI Device: 0
Address Offset: 91h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h–0C7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0C4000h–0C7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C0000h–0C3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.20 PAM2—Programmable Attribute Map 2 (D0:F0)

PCI Device: 0
Address Offset: 92h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h–0CFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0CC000h–0CFFFFh Attribute (HIENABLE):** 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C8000h–0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.21 PAM3—Programmable Attribute Map 3 (D0:F0)

PCI Device: 0
Address Offset: 93h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h–0D7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00 b	**0D4000h–0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00 b	**0D0000h–0D3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.22 PAM4—Programmable Attribute Map 4 (D0:F0)

PCI Device: 0
Address Offset: 94h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h–0DFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00 b	**0DC000h–0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00 b	**0D8000h–0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.23 PAM5—Programmable Attribute Map 5 (D0:F0)

PCI Device: 0
Address Offset: 95h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h–0E7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0E4000h–0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E0000h–0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.24 PAM6—Programmable Attribute Map 6 (D0:F0)

PCI Device: 0
Address Offset: 96h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0EC000h–0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E8000h–0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.25 LAC—Legacy Access Control (D0:F0)

PCI Device: 0
Address Offset: 97h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls a fixed DRAM hole from 15–16 MB.

Bit	Access & Default	Description
7	R/W 0 b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB.
6:1		Reserved
0	R/W 0 b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, accesses to I/O address range x3BCh–x3BFh are forwarded to the DMI. If the VGA enable bit is set and MDA is not present, accesses to I/O address range x3BCh–x3BFh are forwarded to PCI Express*, if the address is within the corresponding IOBASE and IOLIMIT; otherwise, the accesses are forwarded to the DMI. MDA resources are defined as the following: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (Including ISA address aliases, A [15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN / MDAP / Description 0 / 0 / All References to MDA and VGA space are routed to the DMI 0 / 1 / Invalid combination 1 / 0 / All VGA and MDA references are routed to PCI Express graphics attach. 1 / 1 / All VGA references are routed to PCI Express graphics attach. MDA references are routed to the DMI VGA and MDA memory cycles can only be routed across the PCI Express when MAE (PCICMD1[1]) is set. VGA and MDA I/O cycles can only be routed across the PCI Express if IOAE (PCICMD1[0]) is set.

4.1.26 TOLUD—Top of Low Usable DRAM (D0:F0)

PCI Device: 0
Address Offset: 9Ch
Default Value: 08h
Access: R/W
Size: 8 bits

This register defines the Top of Low usable DRAM. TSEG and graphics stolen memory are within the DRAM space defined. From the top of the DRAM space, the (G)MCH optionally claims 1 to 8 MBs of DRAM for internal graphics if enabled, and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Bit	Access & Default	Description
7:3	R/W 01h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31:27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits 31:27 programmed to 01h implies a minimum memory size of 128 MBs. Configuration software must set this value to the smaller of the following 2 choices: • Maximum amount of memory in the system plus one byte or • Minimum address allocated for PCI memory Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address intended for DRAM if the incoming address is less than the value programmed in this register. If this register is set to 0000 0b, it implies 128 MBs of system memory. **NOTE:** The Top of Low Usable memory is the lowest address above both graphics stolen memory and TSEG. The host interface determines the base of graphics stolen memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by 1 MB to determine the base of TSEG.
2:0		Reserved

Programming Example (82945G GMCH only):

- C1DRB7 is set to 4 GB
- TSEG is enabled and TSEG size is set to 1 MB
- Internal graphics is enabled and Graphics Mode Select is set to 32 MB
- BIOS knows the OS requires 1GB of PCI space.

BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20-MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to: 4 GB = 1_0000_0000h

The system memory requirements are:

- 4 GB (max addressable space) – 1 GB (PCI space) – 20 MB (lost memory) = 3 GB – 128 MB (minimum granularity) = B800_0000h
- Since B800_0000h (PCI and other system requirements) is less than 1_0000_0000h; TOLUD should be programmed to B8h.

4.1.27 SMRAM—System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Dh
Default Value: 02h
Access: R/W, RO, R/W/L
Size: 8 bits

The SMRAMC register controls how accesses to compatible and extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when the G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7		Reserved
6	R/W/L 0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1, SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display, even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	R/W/L 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the Section 9.4 for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space; otherwise, the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

4.1.28 ESMRAMC—Extended System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Eh
Default Value: 38h
Access: R/W/L, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W/L 0 b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME=1 and H_SMRAME=1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/WC 0 b	**Invalid SMRAM Access (E_SMERR):** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and TSEG) while not in SMM space and with D_OPEN = 0. It is software's responsibility to clear this bit. Software must write a 1 to this bit to clear it.
5	RO 1 b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the (G)MCH .
4	RO 1 b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the (G)MCH.
3	RO 1 b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the (G)MCH.
2:1	R/W/L 00 b	**TSEG Size (TSEG_SZ):** This field selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to the DMI when the TSEG memory block is enabled. 00 = 1-MB TSEG (TOLUD – Graphics Stolen Memory Size – 1M) to (TOLUD – Graphics Stolen Memory Size). 01 = 2-MB TSEG (TOLUD – Graphics Stolen Memory Size – 2M) to (TOLUD – Graphics Stolen Memory Size). 10 = 8-MB TSEG (TOLUD – Graphics Stolen Memory Size – 8M) to (TOLUD – Graphics Stolen Memory Size). 11 = Reserved. Once D_LCK has been set, these bits become read only.
0	R/W/L 0 b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

4.1.29 ERRSTS—Error Status (D0:F0)

PCI Device: 0
Address Offset: C8h
Default Value: 0000h
Access: R/WC/S, RO
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. A SERR DMI message is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access & Default	Description
15:13		Reserved
12	R/WC/S 0b	**(G)MCH Software Generated Event for SMI:** 1 = Source of the SMI was a Device 2 software event.
11	R/WC/S 0b	**(G)MCH Thermal Sensor Event for SMI/SCI/SERR:** 1 = A (G)MCH Thermal Sensor trip has occurred and a SMI, SCI, or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in the Error Command, SMI Command, and SCI Command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is Invalid). Multiple trip points can generate the same interrupt. If software chooses this mode, subsequent trips may be lost. If this bit is already set, an interrupt message will not be sent on a new thermal sensor event.
10		Reserved
9	R/WC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** 1 = (G)MCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S 0b	**Received Refresh Timeout Flag(RRTOF):** 1 = 1024 memory core refreshes are enqueued.
7:0		Reserved

4.1.30 ERRCMD—Error Command (D0:F0)

PCI Device: 0
Address Offset: CAh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the (G)MCH responses to various system errors. Since the (G)MCH does not have a SERR# signal, SERR messages are passed from the (G)MCH to the ICH7 over DMI. When a bit in this register is set, a SERR message will be generated on DMI when the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access & Default	Description
15:12		Reserved
11	R/W 0b	**SERR on (G)MCH Thermal Sensor Event (TSESERR)** 1 =Enable. The (G)MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS register is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0 =Disable. Reporting of this condition via SERR messaging is disabled.
10		Reserved
9	R/W 0b	**SERR on LOCK to non-DRAM Memory (LCKERR)** 1 =Enable. The (G)MCH will generate a DMI SERR special cycle when a processor lock cycle is detected that does not hit DRAM. 0 =Disable. Reporting of this condition via SERR messaging is disabled.
8	R/W 0b	**SERR on DRAM Refresh Timeout (DRTOERR)** 1 =Enable. The (G)MCH generates a DMI SERR special cycle when a DRAM Refresh timeout occurs. 0 =Disable. Reporting of this condition via SERR messaging is disabled.
7:0		Reserved

4.1.31 SKPD—Scratchpad Data (D0:F0)

PCI Device: 0
Address Offset: DCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**Scratchpad Data:** 1 DWord of data storage.

4.1.32 CAPID0—Capability Identifier (D0:F0)

PCI Device: 0
Address Offset: E0h
Default Value: 82945G/82945GC/82945GZ GMCH: 000000000001090009h
82945P/82945PL MCH: 000000000001090009h
Access: RO
Size: 72 bits

Bit	Access & Default	Description
71:28		Reserved
27:24	RO 1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

4.2 MCHBAR Register

The MCHBAR registers are offset from the MCHBAR base address. Table 4-2 provides an address map of the registers listed by address offset in ascending order. Detailed register bit descriptions follow the table.

Table 4-2. MCHBAR Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	RO, R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	RO, R/W
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	RO, R/W
10E–10Fh	C0BNKARC	Channel A DRAM Bank Architecture	0000h	RO, R/W
114–117h	C0DRT1	Channel A DRAM Timing Register 1	02903D22h	R/W, RO
120–123h	C0DRC0	Channel A DRAM Controller Mode 0	4000280_ 00ssh	RO, R/W
124–127h	C0DRC1	Channel A DRAM Controller Mode 1	00000000h	R/W
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	RO, R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	RO, R/W
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	RO, R/W/L
18E–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	RO, R/W
194–197h	C1DRT1	Channel B DRAM Timing Register 1	02903D22h	RO
1A0–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	4000280_ 00ssh	RO, R/W
1A4–1A7h	C1DRC1	Channel B DRAM Controller Mode 1	00000000h	R/W, RO, R/W/L
F10–F13h	PMCFG	Power Management Configuration	00000000h	R/W, RO
F14–F17h	PMSTS	Power Management Status	00000000h	R/WC/S

4.2.1 C0DRB0—Channel A DRAM Rank Boundary Address 0

MMIO Range:	MCHBAR
Address Offset:	100h
Default Value:	00h
Access:	R/W
Size:	8 bits

The DRAM Rank Boundary register defines the upper boundary address of each DRAM rank with a granularity of 32 MB. Each rank has its own single-byte DRB register. These registers are used to determine which chip select will be active for a given address.

Channel and rank map:

Channel A Rank 0:	100h
Channel A Rank 1:	101h
Channel A Rank 2:	102h
Channel A Rank 3:	103h
Channel B Rank 0:	180h
Channel B Rank 1:	181h
Channel B Rank 2:	182h
Channel B Rank 3:	183h

Single Channel or Asymmetric Channels Example

If the channels are independent, addresses in Channel B should begin where addresses in Channel A left off, and the address of the first rank of Channel A can be calculated from the technology (256 Mbit, 512 Mbit, or 1 Gbit) and the x8 or x16 configuration. With independent channels, a value of 01h in **C0DRB0** indicates that 32 MB of DRAM has been populated in the first rank, and the top address in that rank is 32 MB.

Programming guide:

If Channel A is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

——

C1DRB0 = Total memory in chA rank0 + chA rank1 + chA rank2 + chA rank3 + chB rank0 (in 32-MB increments)

If Channel B is empty, all of the C1DRBs are programmed with the same value as C0DRB3.

Interleaved Channels Example

If channels are interleaved, corresponding ranks in opposing channels will contain the same value, and the value programmed takes into account the fact that twice as many addresses are spanned by this rank compared to the single-channel case. With interleaved channels, a value of 01h in **C0DRB0** and a value of 01h in **C1DRB0** indicate that 32 MB of DRAM has been populated in the first rank of each channel and the top address in that rank of either channel is 64 MB.

Programming guide:

C0DRB0 = C1DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = C1DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

——

C0DRB3 = C1DRB3 = Total memory in chA rank0 + chA rank1+ chA rank2 + chA rank3 (in 32-MB increments)

In all modes, if a DIMM is single sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each mode.

Each Rank is represented by a byte. Each byte has the following format.

Bit	Access & Default	Description
7:0	R/W 00h	**Channel A DRAM Rank Boundary Address:** This 8 bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0s. For the 82945G and 82945P, bit 7 may be programmed to a 1 in the highest DRB (DRB3) if 4 GBs of memory are present.

4.2.2 C0DRB1—Channel A DRAM Rank Boundary Address 1

MMIO Range:	MCHBAR
Address Offset:	101h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.3 C0DRB2—Channel A DRAM Rank Boundary Address 2

MMIO Range:	MCHBAR
Address Offset:	102h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.4 C0DRB3—Channel A DRAM Rank Boundary Address 3

MMIO Range:	MCHBAR
Address Offset:	103h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.5 C0DRA0—Channel A DRAM Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 108h
Default Value: 00h
Access: R/W
Size: 8 bits

The DRAM Rank Attribute registers define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks.

Channel and rank map:

Channel A Rank 0, 1: 108h
Channel A Rank 2, 3: 109h
Channel B Rank 0, 1: 188h
Channel B Rank 2, 3: 189h

Bit	Access & Default	Description
7		Reserved
6:4	R/W 000b	**Channel A DRAM odd Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved
3		Reserved
2:0	R/W 000b	**Channel A DRAM even Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved

4.2.6 C0DRA2—Channel A DRAM Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 109h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for the C0DRA0 register.

4.2.7 C0DCLKDIS—Channel A DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 10Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register can be used to disable the system memory clock signals to each DIMM slot, which can significantly reduce EMI and power concerns for clocks that go to unpopulated DIMMs. Clocks should be enabled based on whether a slot is populated, and what kind of DIMM is present.

Note: Since there are multiple clock signals assigned to each rank of a DIMM, it is important to clarify exactly which rank width field affects which clock signal.

Bit	Access & Default	Description
7:6		Reserved
5	R/W 0b	**DIMM Clock Gate Enable Pair 5:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
4	R/W 0b	**DIMM Clock Gate Enable Pair 4:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
3	R/W 0b	**DIMM Clock Gate Enable Pair 3:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
2	R/W 0b	**DIMM Clock Gate Enable Pair 2:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
1	R/W 0b	**DIMM Clock Gate Enable Pair 1:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
0	R/W 0b	**DIMM Clock Gate Enable Pair 0:** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.

Channel	Rank	Clocks Affected
0	0 or 1	SCLK_A[2:0]/ SCLK_A[2:0]#
0	2 or 3	SCLK_A[5:3]/ SCLK_A[5:3]#
1	0 or 1	SCLK_B[2:0]/ SCLK_B[2:0]#
1	2 or 3	SCLK_B[5:3]/ SCLK_B[5:3]#

4.2.8 C0BNKARC—Channel A DRAM Bank Architecture

PCI Device: MCHBAR
Function: 0
Address Offset: 10E–10Fh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register is used to program the bank architecture for each rank.

Bit	Access & Default	Description
15:8		Reserved
7:6	R/W 00b	**Rank 3 Bank Architecture** 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
5:4	R/W 00b	**Rank 2 Bank Architecture** 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
3:2	R/W 00b	**Rank 1 Bank Architecture** 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
1:0	R/W 00b	**Rank 0 Bank Architecture** 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved

4.2.9 C0DRT1—Channel A DRAM Timing Register

MMIO Range: MCHBAR
Address Offset: 114–117h
Default Value: 02903D22h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:23		Reserved
22:19	R/W 9h	**Activate to Precharge delay (t_{RAS}):** This bit controls the number of DRAM clocks for t_{RAS}. The minimum recommendations are beside their corresponding encodings. 0h – 3h = Reserved 4h – Fh = Four to fifteen clocks respectively.
18:10		Reserved
9:8	R/W 01b	**CAS# Latency (t_{CL}):** This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system. 00 = 5 01 = 4 10 = 3 11 = 6
7		Reserved
6:4	R/W 010b	**DRAM RAS to CAS Delay (t_{RCD}):** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. 000 = 2 DRAM clocks 001 = 3 DRAM clocks 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 = 6 DRAM clocks 101–111 = Reserved
3		Reserved
2:0	R/W 010b	**DRAM RAS Precharge (t_{RP}):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. 000 = 2 DRAM clocks 001 = 3 DRAM clocks 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 = 6 DRAM clocks 101–111 = Reserved

4.2.10 C0DRC0—Channel A DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 120–123h
Default Value: 400028_00ssh (s = strap dependent)
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:30	01b	Reserved
29	R/W 0b	**Initialization Complete (IC):** This bit is used for communication of the software state between the memory controller and BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28:11	00h	Reserved
10:8	R/W 000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Refresh disabled 001 = Refresh enabled. Refresh interval 15.6 usec 010 = Refresh enabled. Refresh interval 7.8 usec 011 = Refresh enabled. Refresh interval 3.9 usec 100 = Refresh enabled. Refresh interval 1.95 usec 111 = Refresh enabled. Refresh interval 64 clocks (fast refresh mode) Other = Reserved
7	RO 0b	Reserved

Bit	Access & Default	Description
6:4	R/W 000b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000 = Post Reset state – When the (G)MCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the (G)MCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During suspend, (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, the (G)MCH will be reset, which will clear this bit field to 000 and maintain CKE signals de-asserted. After internal reset is de-asserted, the CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), the (G)MCH internal signal triggers the DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, the (G)MCH signal triggers the DRAM controller to exit Self-Refresh and resume normal operation without software involvement. 001 = NOP Command Enable – All processor cycles to DRAM result in a NOP command on the DRAM interface. 010 = All Banks Pre-charge Enable – All processor cycles to DRAM result in an "all banks precharge" command on the DRAM interface. 011 = Mode Register Set Enable – All processor cycles to DRAM result in a "mode register" set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent, as shown in Volume 1, System Memory Controller section, memory Detection and Initialization. Refer to JEDEC Standard 79-2A Section 2.2.2 “Programming the Mode and Extended Mode Registers”. 100 = Extended Mode Register Set Enable – All processor cycles to DRAM result in an "extended mode register set" command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent, as shown in Volume 1, System Memory Controller section, memory Detection and Initialization. Refer to JEDEC Standard 79-2A Section 2.2.2 “Programming the Mode and Extended Mode Registers”. 110 = CBR Refresh Enable – In this mode all processor cycles to DRAM result in a CBR cycle on the DRAM interface. 111 = Normal operation
3:2		Reserved
1:0	RO ss	**DRAM Type (DT):** This field is used to select between supported SDRAM types. 00 = Reserved 01 = Reserved 10 = Second Revision Dual Data Rate (DDR2) SDRAM 11 = Reserved

4.2.11 C0DRC1—Channel A DRAM Controller Mode 1

Bus/Dev/Func/Type: 0/0/0/MCHBAR
Address Offset: 124–127h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31	R/W 0b	**Enhanced Addressing Enable (ENHADE):** 0 = Enhanced Addressing mode disabled. The DRAM address map follows the standard address map. 1 = Enhanced Address mode enabled. The DRAM address map follows the enhanced address map.
30:0		Intel Reserved

4.2.12 C1DRB0—Channel B DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 180h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.13 C1DRB1—Channel B DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 181h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.14 C1DRB2—Channel B DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 182h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.15 C1DRB3—Channel B DRAM Rank Boundary Address 3

MMIO Range:	MCHBAR
Address Offset:	183h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRB0 register.

4.2.16 C1DRA0—Channel B DRAM Rank 0,1 Attribute

MMIO Range:	MCHBAR
Address Offset:	188h
Default Value:	00h
Access:	RO, R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRA0 register.

4.2.17 C1DRA2—Channel B DRAM Rank 2,3 Attribute

MMIO Range:	MCHBAR
Address Offset:	189h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for the C0DRA0 register.

4.2.18 C1DCLKDIS—Channel B DRAM Clock Disable

MMIO Range:	MCHBAR
Address Offset:	18Ch
Default Value:	00h
Access:	RO, R/W/L
Size:	8 bits

The operation of this register is detailed in the description for the C0DCLKDIS register.

4.2.19 C1BNKARC—Channel B Bank Architecture

MMIO Range:	MCHBAR
Address Offset:	18E–18Fh
Default Value:	0000h
Access:	RO, R/W
Size:	16 bits

The operation of this register is detailed in the description for the C0BNKARC register.

4.2.20 C1DRT1—Channel B DRAM Timing Register 1

MMIO Range: MCHBAR
Address Offset: 194–197h
Default Value: 02903D22h
Access: RO
Size: 32 bits

The operation of this register is detailed in the description for the C0DRT1 register.

4.2.21 C1DRC0—Channel B DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 1A0–1A3h
Default Value: 4000280_00ssh (s = strap dependent)
Access: RO, R/W
Size: 32 bits

The operation of this register is detailed in the description for the C0DRC0 register.

4.2.22 C1DRC1—Channel B DRAM Controller Mode 1

MMIO Range: MCHBAR
Address Offset: 1A4–1A7h
Default Value: 00000000h
Access: RO, R/W, R/W/L
Size: 32 bits

The operation of this register is detailed in the description for the C0DRC1 register.

4.2.23 PMCFG—Power Management Configuration

PCI Device: MCHBAR
Address Offset: F10–F13h
Default: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:5		Reserved
4	R/W 0b	**Enhanced Power Management Features Enable:** 0 = Legacy power management mode 1 = Reserved.
3:0		Reserved

4.2.24 PMSTS—Power Management Status

PCI Device: MCHBAR
Address Offset: F14–F17h
Default: 00h
Access: R/WC/S
Size: 32 bits

This register is reset by PWROK only.

Bit	Access & Default	Description
31:2		Reserved
1	R/WC/S 0b	**Channel B in self-refresh:** This bit is set by power management hardware after Channel B is placed in self refresh as a result of a Power State or a Warm Reset sequence. This bit is cleared by power management hardware before starting Channel B self refresh exit sequence initiated by a power management exit. This bit is cleared by the BIOS in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel B not ensured to be in self refresh. 1 = Channel B in self refresh.
0	R/WC/S 0b	**Channel A in Self-refresh:** This bit is set by power management hardware after Channel A is placed in self refresh as a result of a Power State or a Reset Warn sequence. This bit is cleared by power management hardware before starting Channel A self refresh exit sequence initiated by a power management exit. This bit is cleared by the BIOS in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel A not ensured to be in self refresh. 1 = Channel A in self refresh.

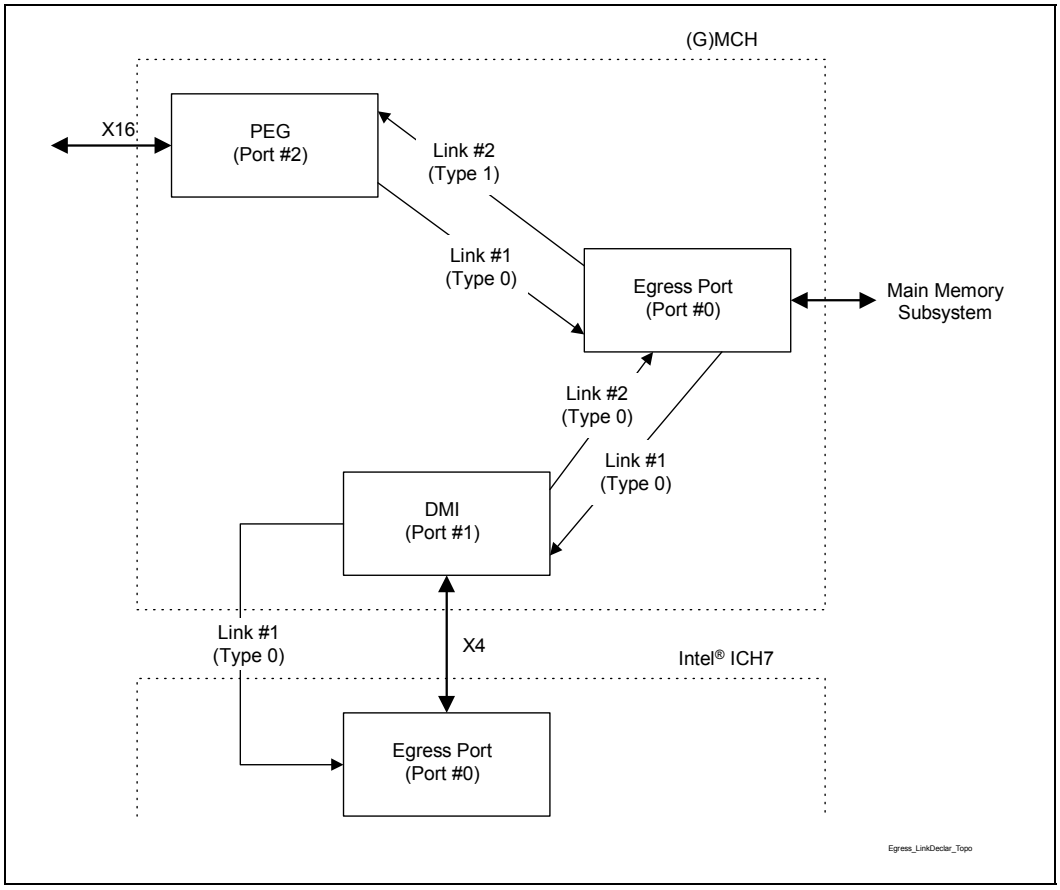
4.3 EPBAR Registers—Egress Port Register Summary

The MCHBAR registers are offset from the EPBAR base address. Table 4-3 provides an address map of the registers listed by address offset in ascending order. Detailed bit descriptions of the registers follow the table. Link Declaration Topology is shown in Figure 4-1.

Table 4-3. Egress Port Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
044h–047h	EPESD	EP Element Self Description	00000201h	R/WO, RO
050h–053h	EPLE1D	EP Link Entry 1 Description	01000000h	R/WO, RO
058h–05Fh	EPLE1A	EP Link Entry 1 Address	000000000000000h	R/WO, RO
060h–063h	EPLE2D	EP Link Entry 2 Description	02000002h	R/WO, RO
068h–06Fh	EPLE2A	EP Link Entry 2 Address	000000000008000h	RO

Figure 4-1. Link Declaration Topology



4.3.1 EPESD—EP Element Self Description

MMIO Range: EPBAR
Address Offset: 044–047h
Default Value: 00000201h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. 00h = Indicates to configuration software that this is the default egress port.
23:16	R/WO 00h	**Component ID:** This field identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 02h	**Number of Link Entries:** This field indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express* and DMI).
7:4		Reserved
3:0	RO 01h	**Element Type:** This field indicates the type of the Root Complex Element. 1h = Represents a port to system memory

4.3.2 EPLE1D—EP Link Entry 1 Description

MMIO Range: EPBAR
Address Offset: 050–053h
Default Value: 01000000h
Access: RO, R/WO
Size: 32 bits

This register provides the first part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** This bit indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

4.3.3 EPLE1A—EP Link Entry 1 Address

MMIO Range: EPBAR
Address Offset: 058–05Fh
Default Value: 00000000_00000000h
Access: R/WO
Size: 64 bits

This register is the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field provides the memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0		Reserved

4.3.4 EPLE2D—EP Link Entry 2 Description

MMIO Range: EPBAR
Address Offset: 060–63h
Default Value: 02000002h
Access: RO, R/WO
Size: 32 bits

This register provides the first part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (PCI Express). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 1b	**Link Type:** This bit indicates that the link points to configuration space of the integrated device that controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

4.3.5 EPLE2A—EP Link Entry 2 Address

MMIO Range: EPBAR
Address Offset: 068–06Fh
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register is the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28		Reserved
27:20	RO 00h	**Bus Number**
19:15	RO 0 0001b	**Device Number:** Target for this link is PCI Express* x16 port (Device 1).
14:12	RO 000b	**Function Number**
11:0		Reserved

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5 Host-PCI Express* Bridge Registers (D1:F0) (Intel® 82945G/82945GC/82945P/82945PL Only)

Device 1 contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It is typically referred to as PCI Express (PCI Express graphics) port. In addition, it also functions as the virtual PCI-to-PCI bridge. Table 5-1 provides an address map of the D1:F0 registers listed by address offset in ascending order. Section 5.1 provides a detailed bit description of the registers.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits: Reserved and Preserved.

- Reserved for future RW implementations; software must preserve value read for writes to bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

Note: Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 5-1. Host-PCI Express* Graphics Bridge Register Address Map (D1:F0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2771h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, R/W
06–07h	PCISTS1	PCI Status	0010h	RO, R/W
08h	RID1	Revision Identification	See register description	RO
09–0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W
0Dh	—	*Reserved*	—	—
0Eh	HDR1	Header Type	01h	RO

Address Offset	Symbol	Register Name	Default Value	Access
0F–17h	—	*Reserved*	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RO
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	—	*Reserved*	—	—
1Ch	IOBASE1	I/O Base Address	F0h	RO
1Dh	IOLIMIT1	I/O Limit Address	00h	R/W
1Eh–1Fh	SSTS1	Secondary Status	00h	RO, R/WC
20–21h	MBASE1	Memory Base Address	FFF0h	R/W
22–23h	MLIMIT1	Memory Limit Address	0000h	R/W
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28–33h	—	*Reserved*	—	—
34h	CAPPTR1	Capabilities Pointer	88h	RO
35–3Bh	—	*Reserved*	—	—
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
40–7Fh	—	*Reserved*	—	—
80–83h	PM_CAP1	Power Management Capabilities	C8029001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RO, R/W
94–97h	MA	Message Address	00000000h	RO, R/W
98–99h	MD	Message Data	0000h	R/W
9A–9Fh	—	*Reserved*	—	—
A0–A1h	PEG_CAPL	PCI Express* Capability List	0010h	RO
A2–A3h	PEG_CAP	PCI Express* Capabilities	0141h	RO
A4–A7h	DCAP	Device Capabilities	00000000h	RO
A8–A9h	DCTL	Device Control	0000h	R/W
AA–ABh	DSTS	Device Status	0000h	RO
AC–AFh	LCAP	Link Capabilities	02014D01h	R/WO
B0–B1h	LCTL	Link Control	0000h	RO, R/W
B2–B3h	LSTS	Link Status	1001h	RO
B4–B7h	SLOTCAP	Slot Capabilities	00000000h	R/WO
B8–B9h	SLOTCTL	Slot Control	01C0h	RO, R/W
BA–BBh	SLOTSTS	Slot Status	0000h	RO, R/WC

Address Offset	Symbol	Register Name	Default Value	Access
BC–BDh	RCTL	Root Control	0000h	R/W
BE–BFh	—	*Reserved*	—	—
C0–C3h	RSTS	Root Status	00000000h	RO, R/WC
C4–FFh	—	*Reserved*	—	—
EC–EFh	PEG_LC	PCI Express* Legacy Control	00000000h	R/W
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO, R/WO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000001h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	R/W
10E–10Fh	—	*Reserved*	—	—
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	800000FFh	RO, R/W
118–119h	—	*Reserved*	—	—
11A–11Bh	VC0RSTS	VC0 Resource Status	0002h	RO
11C–11Fh	VC1RCAP	VC1 Resource Capability	00008000h	RO
120–123h	VC1RCTL	VC1 Resource Control	01000000h	RO, R/W
124–125h	—	*Reserved*	—	—
126–127h	VC1RSTS	VC1 Resource Status	0002h	RO
128–13Fh	—	*Reserved*	—	—
140–143h	RCLDECH	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, R/WO
148–14Fh	—	*Reserved*	—	—
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
154–157h	—	*Reserved*	—	—
158–15Fh	LE1A	Link Entry 1 Address	0000000000 000000h	R/WO
160–1C5h	—	*Reserved*	—	—
1C4–1C7h	UESTS	Uncorrectable Error Status	00000000h	RO, R/WC/S
1C8–1CBh	UEMSK	Uncorrectable Error Mask	00000000h	RO, R/W/S
1D0–1D3h	CESTS	Correctable Error Status	00000000h	RO, R/W/S
1D4–1D3h	—	*Reserved*	—	—
1D4–1D7h	CEMSK	Correctable Error Mask	00000000h	R/W/S
1D8–217h	—	*Reserved*	—	—
218–21Fh	PEG_SSTS	PCI Express* Sequence Status	0000000000 000FFFh	RO
220–FFFh	—	*Reserved*	—	—

5.1 Configuration Register Details (D1:F0)

5.1.1 VID1—Vendor Identification (D1:F0)

PCI Device: 1
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086 h	**Vendor Identification (VID1):** This field provides the PCI standard identification for Intel.

5.1.2 DID1—Device Identification (D1:F0)

PCI Device: 1
Address Offset: 02h
Default Value: 2771h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2581h	**Device Identification Number (DID1):** This field is an identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express* graphics port).

5.1.3 PCICMD1—PCI Command (D1:F0)

PCI Device: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**INTA Assertion Disable:** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. This bit only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and de-assert messages.
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Hardwired to 0. Not Applicable or Implemented.
8	R/W 0b	**SERR Message Enable (SERRE1):** This bit is an enable bit for Device 1 SERR messaging. The (G)MCH communicates the SERR# condition by sending a SERR message to the Intel® ICH7. This bit, when set, enables reporting of non-fatal and fatal errors to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express* specific bits in the Device Control register. 0 = Disable. The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control register. 1 = Enable. The (G)MCH is enabled to generate SERR messages that will be sent to the ICH7 for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI-to-PCI Express bridge (not those received by the secondary side). The error status is reported in the PCISTS1 register.
7		Reserved
6	R/WO 0b	**Parity Error Enable (PERRE):** This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Disable. Master Data Parity Error bit in PCI Status register **cannot** be set. 1 = Enable. Master Data Parity Error bit in PCI Status register **can** be set.
5	RO 0b	**VGA Palette Snoop:** Hardwired to 0. Not Applicable or Implemented.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. Not Applicable or Implemented.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0. Not Applicable or Implemented.

Bit	Access & Default	Description
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the ability of the PCI Express port to forward memory and I/O read/write requests in the upstream direction. 0 = Disable. This device is prevented from making memory or I/O requests to its primary bus. Note that according to *PCI Local Bus Specification*, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, I/O writes/reads, peer writes/reads, and MSIs will all be treated as invalid cycles. Writes are forwarded to memory address 0h with byte enables de-asserted. Reads will be forwarded to memory address 0h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = Enable. This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of completions from the primary interface to the secondary interface.
1	R/W 0b	**Memory Access Enable (MAE):** 0 = Disable. All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0b	**IO Access Enable (IOAE):** 0 = Disable. All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

5.1.4 PCISTS1—PCI Status (D1:F0)

PCI Device: 1
Address Offset: 06h
Default Value: 0010h
Access: RO, R/WC
Size: 16 bits

This register reports the occurrence of error conditions associated with the primary side of the "virtual" Host-PCI Express bridge in the (G)MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. Not Applicable or Implemented. Parity (generating poisoned TLPs) is not supported on the primary side of this device; the (G)MCH does Not do error forwarding.
14	R/WC 0b	**Signaled System Error (SSE):** 1 = This Device sent a SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. Not Applicable or Implemented. The concept of a master abort does not exist on primary side of this device.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. Not Applicable or Implemented. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. Not Applicable or Implemented. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00b	**DEVSELB Timing (DEVT):** This device is not the subtractive decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality, there is no scenario where this bit will get set. Because hardware will not set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC, but for this implementation, a RO definition behaves the same way and will meet all Microsoft testing requirements.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0. Not Applicable or Implemented.
6		Reserved
5	RO 0b	**66/60MHz capability (CAP66):** Hardwired to 0. Not Applicable or Implemented.
4	RO 1b	**Capabilities List:** Hardwired to 1. This indicates that a capabilities list is present.

Bit	Access & Default	Description
3	RO 0b	**INTA Status:** 1 = An interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0		Reserved

5.1.5 RID1—Revision Identification (D1:F0)

PCI Device: 1
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH device 1. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO	**Revision Identification Number (RID1):** This field indicates the number of times that this device in this component has been "stepped" through the manufacturing process. It is always the same as the RID values in all other devices in this component. Refer to the *Intel® 945G/945GC/*945GZ/*945P/945PL Express Chipset Specification Update* for the value of the Revision ID register.

5.1.6 CC1—Class Code (D1:F0)

PCI Device: 1
Address Offset: 09h
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This field indicates the base class code for this device. 06h = Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** This field indicates the sub-class code for this device. 04h = PCI-to-PCI bridge.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 CL1—Cache Line Size (D1:F0)

PCI Device: 1
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Cache Line Size (Scratch pad):** This field is implemented by PCI Express* devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

5.1.8 HDR1—Header Type (D1:F0)

PCI Device: 1
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** This field returns 01h to indicate that this is a single function device with bridge header layout.

5.1.9 PBUSN1—Primary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0s.

5.1.10 SBUSN1—Secondary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 19h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge (i.e., to PCI Express). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access & Default	Description
7:0	R/W 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express.

5.1.11 SUBUSN1—Subordinate Bus Number (D1:F0)

PCI Device: 1
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access & Default	Description
7:0	R/W 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the PCI Express segment, this register will contain the same value as the SBUSN1 register.

5.1.12 IOBASE1—I/O Base Address (D1:F0)

PCI Device: 1
Address Offset: 1Ch
Default Value: F0h
Access: RO
Size: 8 bits

This register controls the processor-to-PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access & Default	Description
7:4	R/W Fh	**I/O Address Base (IOBASE):** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express. BIOS must not set this register to 00h; otherwise, 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0		Reserved

5.1.13 IOLIMIT1—I/O Limit Address (D1:F0)

PCI Device: 1
Address Offset: 1Dh
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the processor-to-PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purposes of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0h	**I/O Address Limit (IOLIMIT):** This field corresponds to A[15:12] of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0		Reserved

5.1.14 SSTS1—Secondary Status (D1:F0)

PCI Device: 1
Address Offset: 1Eh
Default Value: 00h
Access: RO, R/WC
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., PCI Express side) of the "virtual" PCI-PCI Bridge in the (G)MCH.

Bit	Access & Default	Description
15	R/WC 0b	**Detected Parity Error (DPE):** 0 = Parity error **Not** detected. 1 = The (G)MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC 0b	**Received System Error (RSE):** 0 = System error **Not** received. 1 = The secondary side sent an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC 0b	**Received Master Abort (RMA):** 0 = Master abort **Not** received. 1 = The Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a completion with **Unsupported Request** Completion Status.
12	R/WC 0b	**Received Target Abort (RTA):** 0 = Target abort **Not** received. 1 = The Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with **Completer Abort** completion status.
11	RO 0b	**Signaled Target Abort (STA):** Hardwired to 0. Not Applicable or Implemented. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort completion status).
10:9	RO 00b	**DEVSELB Timing (DEVT):** Hardwired to 0. Not Applicable or Implemented.
8		Reserved
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0. Not Applicable or Implemented.
6		Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Hardwired to 0. Not Applicable or Implemented.
4:0		Reserved

5.1.15 MBASE1—Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 20h
Default Value: FFF0h
Access: R/W
Size: 16 bits

This register controls the processor-to-PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Memory Address Base (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0		Reserved

5.1.16 MLIMIT1—Memory Limit Address (D1:F0)

PCI Device:	1
Address Offset:	22h
Default Value:	0000h
Access:	R/W
Size:	16 bits

This register controls the processor-to-PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-pre-fetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map pre-fetchable address ranges (typically, graphics local memory).

This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the pre-fetchable address range for improved processor -PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (pre-fetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap may be affected.

Bit	Access & Default	Description
15:4	R/W 000h	**Memory Address Limit (MLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0		Reserved

5.1.17 PMBASE1—Prefetchable Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 24h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register, in conjunction with the corresponding Upper Base Address register, controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A [31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Prefetchable Memory Base Address (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO 0h	**64-bit Address Support:** This field indicates the bridge supports only 32-bit address support.

5.1.18 PMLIMIT1—Prefetchable Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 26h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register, in conjunction with the corresponding Upper Limit Address register, controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	R/W 000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO 0h	**64-bit Address Support:** This field indicates the bridge only supports 32-bit addresses.

5.1.19 CAPPTR1—Capabilities Pointer (D1:F0)

PCI Device: 1
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

5.1.20 INTRLINE1—Interrupt Line (D1:F0)

PCI Device: 1
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather, device drivers and operating systems use it to determine priority and vector information.

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller is connected to this device's interrupt pin.

5.1.21 INTRPIN1—Interrupt Pin (D1:F0)

PCI Device: 1
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

5.1.22 BCTRL1—Bridge Control (D1:F0)

PCI Device: 1
Address Offset: 3Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-to-PCI Express bridge in the (G)MCH (e.g., VGA compatible address ranges mapping).

Bit	Access & Default	Description
15:12		Reserved
11	RO 0b	**Discard Timer SERR Enable:** Hardwired to 0. Not Applicable or Implemented.
10	RO 0b	**Discard Timer Status:** Hardwired to 0. Not Applicable or Implemented.
9	RO 0b	**Secondary Discard Timer:** Hardwired to 0. Not Applicable or Implemented.
8	RO 0b	**Primary Discard Timer:** Hardwired to 0. Not Applicable or Implemented.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Hardwired to 0. Not Applicable or Implemented.
6	R/W 0b	**Secondary Bus Reset (SRESET):** 0 = Hot reset not triggered on the corresponding PCI Express port. 1 = Setting this bit triggers a hot reset on the corresponding PCI Express port.
5	RO 0b	**Master Abort Mode (MAMODE):** Hardwired to 0. When acting as a master, unclaimed reads that experience a master abort return all 1s and any writes that experience a master abort complete normally and the data is discarded.
4	R/W 0b	**VGA 16-bit Decode:** This bit enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	R/W 0b	**VGA Enable (VGAEN):** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in the LAC Register[0] (Device 0, offset 97h).

Bit	Access & Default	Description
2	R/W 0b	**ISA Enable (ISAEN):** This bit is used to exclude legacy resource decode to route ISA resources to the legacy decode path. This bit modifies the response by the (G)MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express. 1 = (G)MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express, these cycles are forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W 0b	**SERR Enable (SERREN):** 0 = Disable. No forwarding of error messages from secondary side to primary side that could result in a SERR. 1 = Enable. ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RO 0b	**Parity Error Response Enable (PEREN):** This bit controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the (G)MCH receives across the link (upstream) a Read Data Completion Poisoned TLP. 0 = Disable. Master Data Parity Error bit in Secondary Status register **cannot** be set. 1 = Enable. Master Data Parity Error bit in Secondary Status register **can** be set.

5.1.23 PM_CAPID1—Power Management Capabilities (D1:F0)

PCI Device: 1
Address Offset: 80h
Default Value: C8029001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support:** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging: D0, D3hot, and D3cold. This device is not required to do anything to support D3hot and D3cold; it simply must report that those states are supported. Refer to the *PCI Power Management Interface Specification, Revision 1.1* for encoding explanation and other power management details.
26	RO 0b	**D2:** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current:** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock:** Hardwired to 0 to indicate this device does NOT support PME# generation.
18:16	RO 010b	**PCI PM CAP Version:** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with the *PCI Power Management Interface Specification, Revision 1.1*.
15:8	RO 90h / A0h	**Pointer to Next Capability:** This filed contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO 01h	**Capability ID:** The value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

5.1.24 PM_CS1—Power Management Control/Status (D1:F0)

PCI Device: 1
Address Offset: 84–87h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**PME Status:** This bit indicates that this device does not support PME# generation from $D3_{cold}$.
14:13	RO 00b	**Data Scale:** This field indicates that this device does not support the Power Management Data register.
12:9	RO 0h	**Data Select:** This field indicates that this device does not support the Power Management Data register.
8	R/W/S 0b	**PME Enable:** This bit indicates that this device does not generate PME# assertion from any D state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3. Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state to be fully functional. There is no hardware functionality required to support these power states.

5.1.25 SS_CAPID—Subsystem ID and Vendor ID Capabilities (D1:F0)

PCI Device: 1
Address Offset: 88h
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence as part of its compliance testing.

Bit	Access & Default	Description
31:16		Reserved
15:8	RO 80h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list that is the PCI Power Management capability.
7:0	RO 0Dh	**Capability ID:** The value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

5.1.26 SS—Subsystem ID and Subsystem Vendor ID (D1:F0)

PCI Device: 1
Address Offset: 8Ch
Default Value: 00008086h
Access: RO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field identifies the manufacturer of the subsystem and is the same as the vendor ID that is assigned by the PCI Special Interest Group.

5.1.27 MSI_CAPID—Message Signaled Interrupts Capability ID (D1:F0)

PCI Device: 1
Address Offset: 90h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case going through this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO 05h	**Capability ID:** The value of 05h identifies this linked list item (capability structure) as being for MSI registers.

5.1.28 MC—Message Control (D1:F0)

PCI Device: 1
Address Offset: 92h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing modifying the bits.

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the previous one(s).

Bit	Access & Default	Description
15:8		Reserved
7	RO 0b	**64-bit Address Capable:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field (Bits 3:1).
3:1	RO 000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. 000 = 1 001–111 = Reserved
0	R/W 0b	**MSI Enable (MSIEN):** This bit controls the ability of this device to generate MSIs. 0 = Disable. MSI will not be generated. 1 = Enable. MSI will be generated when (G)MCH receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

5.1.29 MA—Message Address (D1:F0)

PCI Device: 1
Address Offset: 94h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Message Address:** This field is used by system software to assign a MSI address to the device. The device handles a MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align:** Hardwired to 0s so that addresses assigned by system software are always aligned on a DWord address boundary.

5.1.30 MD—Message Data (D1:F0)

PCI Device: 1
Address Offset: 98–99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data:** This field is the base message data pattern assigned by system software and used to handle a MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. This register supplies the lower 16 bits.

5.1.31 PEG_CAPL—PCI Express* Capability List (D1:F0)

PCI Device: 1
Address Offset: A0–A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability:** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express extended configuration space.
7:0	RO 10h	**Capability ID:** This field identifies this linked list item (capability structure) as being for PCI Express registers.

5.1.32 PEG_CAP—PCI Express* Capabilities (D1:F0)

PCI Device: 1
Address Offset: A2–A3h
Default Value: 0141h
Access: RO, R/WO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14		Reserved
13:9	RO 00h	**Interrupt Message Number:** Hardwired to 0. Not Applicable or Implemented.
8	R/WO 1b	**Slot Implemented:** 0 = The PCI Express* Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. BIOS must initialize this field appropriately if a slot connection is not implemented.
7:4	RO 4h	**Device/Port Type:** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version:** Hardwired to 1h as it is the first version.

5.1.33 DCAP—Device Capabilities (D1:F0)

PCI Device: 1
Address Offset: A4–A7h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register indicates PCI Express link capabilities.

Bit	Access & Default	Description
31:6		Reserved
5	RO 0b	**Extended Tag Field Supported:** Hardwired to indicate support for 5-bit tags as a requestor.
4:3	RO 00b	**Phantom Functions Supported:** Hardwired to 0. Not Applicable or Implemented.
2:0	RO 000b	**Max Payload Size:** Hardwired to indicate 128 Byte maximum supported payload for Transaction Layer Packets (TLP).

5.1.34 DCTL—Device Control (D1:F0)

PCI Device: 1
Address Offset: A8–A9h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

Note: The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by the Root Port Command register.

Bit	Access & Default	Description
15:8		Reserved
7:5	R/W 000b	**Max Payload Size:** 000 =128B maximum supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value. As a transmitter, the Device must not generate TLPs exceeding the set value. 001–111 = Reserved.
4		Reserved
3	R/W 0b	**Unsupported Request Reporting Enable:** 0 = Disable. 1 = Enable. Unsupported requests will be reported. **NOTE:** Reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W 0b	**Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W 0b	**Non-Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W 0b	**Correctable Error Reporting Enable:** 0 = Disable. 1 = Enable. Correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

5.1.35 DSTS—Device Status (D1:F0)

PCI Device: 1
Address Offset: AAh
Default Value: 0000h
Access: RO
Size: 16 bits

This register reflects the status corresponding to controls in the Device Control register.

Note: The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6		Reserved
5	RO 0b	**Transactions Pending:** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used traffic classes).
4		Reserved
3	R/WC 0b	**Unsupported Request Detected:** 0 = Unsupported Request **Not** detected. 1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
2	R/WC 0b	**Fatal Error Detected:** When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the Correctable Error Mask register. 0 = Fatal Error **Not** detected. 1 = Fatal error(s) detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	R/WC 0b	**Non-Fatal Error Detected:** When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the Correctable Error Mask register. 0 = Non-fatal error **Not** detected. 1 = Non-fatal error(s) detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	R/WC 0b	**Correctable Error Detected:** When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the Correctable Error Mask register. 0 = Correctable error **Not** detected. 1 = Correctable error(s) detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.

5.1.36 LCAP—Link Capabilities (D1:F0)

PCI Device: 1
Address Offset: AC–AF
Default Value: 02014D01h
Access: R/WO, RO
Size: 16 bits

This register indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field indicates the PCI Express* port number for the given PCI Express link. It matches the value in Element Self Description [31:24].
23:15		Reserved
14:12	R/WO 100b	**L0s Exit Latency:** This field indicates the length of time this port requires to complete the transition from L0s to L0. The value 100b indicates the range of 256 ns to less than 512 ns. If this field is required to be any value other than the default, BIOS must initialize it accordingly.
11:10	RO 11b	**Active State Link PM Support:** L0s and L1 entry supported. **NOTE:** L1 state is Not supported on the 82945G/82945GC/82945GZ GMCH and 82945P/82945PL MCH.
9:4	RO 10h	**Max Link Width:** Hardwired to indicate X16. When Force X1 mode is enabled on this PCI Express device, this field reflects X1 (01h).
3:0	RO 1h	**Max Link Speed:** Hardwired to indicate 2.5 Gb/s.

5.1.37 LCTL—Link Control (D1:F0)

PCI Device: 1
Address Offset: B0–B1
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register allows control of the PCI Express link.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	Reserved. Must be 0 when writing this register.
6	R/W 0b	**Common Clock Configuration:** Components use this common clock configuration information to report the correct L0s exit latency. The state of this bit affects the L0s exit latency reported in LCAP [14:12] and the N_FTS value advertised during link training. 0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock.
5	R/W 0b	**Retrain Link:** This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0). 0 = Normal operation 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0 or L0s states to the recovery state.
4	R/W 0b	**Link Disable:** The link retraining happens automatically on a 0-to-1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. 0 = Enable. Normal operation 1 = Link is disabled. This forces the LTSSM to transition to the disabled state (via Recovery) from L0 or L0s states.
3	RO 0b	**Read Completion Boundary (RCB) :** Hardwired to 0 to indicate 64 byte.
2		Reserved
1:0	R/W 00b	**Active State PM:** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s Entry Supported

5.1.38 LSTS—Link Status (D1:F0)

PCI Device: 1
Address Offset: B2–B3h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access & Default	Description
15:13		Reserved
12	RO 1b	**Slot Clock Configuration:** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training:** Hardware clears this bit once link training is complete. 0 = Link training **Not** in progress. 1 = Link training is in progress.
10	RO 0b	**Training Error:** 0 = **No** training error 1 = Set by hardware upon detection of unsuccessful training of the link to the L0 Link state.
9:4	RO 00h	**Negotiated Width:** This field indicates negotiated link width. 00h = Reserved 01h = X1 04h = Reserved 08h = Reserved 10h = X16 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed:** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

5.1.39 SLOTCAP—Slot Capabilities (D1:F0)

PCI Device: 1
Address Offset: B4–B7h
Default Value: 00000000h
Access: R/WO
Size: 32 bits

PCI Express slot-related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
31:19	R/WO 0000h	**Physical Slot Number:** This field indicates the physical slot number attached to this port. This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18:17		Reserved
16:15	R/WO 00b	**Slot Power Limit Scale:** This field specifies the scale used for the Slot Power Limit value. If this field is written, the link sends a Set_Slot_Power_Limit message. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x
14:7	R/WO 00h	**Slot Power Limit Value:** This field, in combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot. Power limit (in watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO 0b	**Hot-plug Capable:** This bit indicates that this slot is capable of supporting hot-plug operations. 0 = **Not** capable 1 =Capable.
5	R/WO 0b	**Hot-plug Surprise:** This bit indicates that a device present in this slot might be removed from the system without any prior notification. 0 = **No** hot-plug surprise 1 = Hot plug Surprise capable.
4	R/WO 0b	**Power Indicator Present:** This bit indicates that a power indicator is implemented on the chassis for this slot. 0 = **Not** present 1 = Present
3	R/WO 0b	**Attention Indicator Present:** This bit indicates that an Attention Indicator is implemented on the chassis for this slot. 0 = **Not** present 1 = Present
2:1		Reserved
0	R/WO 0b	**Attention Button Present:** This bit indicates that an attention button is implemented on the chassis for this slot. The attention button allows the user to request hot-plug operations. 0 = **Not** present 1 = Present

5.1.40 SLOTCTL—Slot Control (D1:F0)

PCI Device: 1
Address Offset: B8h
Default Value: 01C0h
Access: R/W
Size: 16 bits

PCI Express slot related registers allow for the support of hot-plug.

Bit	Access & Default	Description
15:10		Reserved
9:8	R/W 01b	**Power Indicator Control:** Reads to this field return the current state of the power indicator. Writes to this field set the power indicator and cause the port to send the appropriate POWER_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
7:6	R/W 11 b	**Attention Indicator Control:** Reads to this field return the current state of the attention indicator. Writes to this field set the attention indicator and cause the port to send the appropriate ATTENTION_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
5	R/W 0b	**Hot plug Interrupt Enable:** 0 =Disable. 1 = Enables generation of hot plug interrupt on enabled hot plug events.
4	R/W 0b	**Command Completed Interrupt Enable:** 0 = Disable. 1 = Enables the generation of a hot-plug interrupt when the hot-plug controller completes a command.
3	R/W 0b	**Presence Detect Changed Enable:** 0 = Disable. 1 = Enables the generation of a hot-plug interrupt or wake message on a presence detect changed event.
2:1		Reserved
0	R/W 0b	**Attention Button Pressed Enable:** 0 = Disable. 1 = Enables the generation of hot-plug interrupt or wake message on an attention button pressed event.

5.1.41 SLOTSTS—Slot Status (D1:F0)

PCI Device: 1
Address Offset: BA–BBh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

PCI Express slot-related registers allow for the support of hot-plug.

Bit	Access & Default	Description
15:7		Reserved
6	RO Strap	**Presence Detect State:** This bit indicates the presence of a card in the slot. 0 = Slot Empty 1 = Card Present in slot.
5		Reserved
4	R/WC 0b	**Command Completed:** 0 = Command **Not** completed. 1 = Hot-plug controller completes an issued command.
3	R/WC 0b	**Presence Detect Changed:** 0 = **No** Presence Detect change. 1 = Presence detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2:1		Reserved
0	R/WC 0b	**Attention Button Pressed:** 0 = Attention button **Not** pressed. 1 = Attention button is pressed.

5.1.42 RCTL—Root Control (D1:F0)

PCI Device: 1
Address Offset: BCh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when the device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR, as controlled by these bits, takes precedence over the SERR Enable in the PCI Command register.

Bit	Access & Default	Description
15:4		Reserved
3	R/W 0b	**PME Interrupt Enable:** 0 = Disable. **No** interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status register. A PME interrupt is also generated if the PME Status bit of the Root Status register is set when this bit is set from a cleared state.
2	R/W 0b	**System Error on Fatal Error Enable:** This bit controls the root complex's response to fatal errors. 0 = Disable. **No** SERR generated on receipt of fatal error. 1 = SERR is generated if a fatal error is reported by any of the devices in the hierarchy associated with this root port, or by the Root Port itself.
1	R/W 0b	**System Error on Non-Fatal Uncorrectable Error Enable:** This bit controls the Root Complex's response to non-fatal errors. 0 = Disable. **No** SERR generated on receipt of non-fatal error. 1 = SERR is generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0b	**System Error on Correctable Error Enable:** This bit controls the Root Complex's response to correctable errors. 0 = Disable. **No** SERR generated on receipt of correctable error. 1 = SERR is generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

5.1.43 RSTS—Root Status (D1:F0)

PCI Device: 1
Address Offset: C0–C3h
Default Value: 00000000h
Access: RO, R/WC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18		Reserved
17	RO 0b	**PME Pending:** 0 = PME **Not** pending. 1 = Another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/WC 0b	**PME Status:** 0 = Requestor ID did **Not** assert PME. 1 = Requestor ID indicated in the PME Requestor ID field asserted PME. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID:** This field indicates the PCI requestor ID of the last PME requestor.

5.1.44 PEG_LC—PCI Express* Legacy Control (D1:F0)

PCI Device: 1
Address Offset: EC–EFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register controls functionality that is needed by legacy (non-PCI Express aware) operating systems during run time.

Bit	Access & Default	Description
31:3		Reserved
2	R/W 0b	**PME GPE Enable (PMEGPE):** 0 = Disable. Do **Not** generate GPE PME message when PME is received. 1 = Enable. Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PCI Express* port under legacy operating systems.
1	R/W 0b	**Hot-Plug GPE Enable (HPGPE):** 0 = Disable. Do **Not** generate GPE hot-plug message when a hot-plug event is received. 1 = Enable. Generate a GPE hot-plug message when a hot-plug event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PCI Express port under legacy operating systems.
0	R/W 0b	**General Message GPE Enable (GENGPE):** 0 = Disable. Do **Not** forward received GPE assert/de-assert messages. 1 = Enable. Forward received GPE assert/de-assert messages. These general GPE message can be received via the PCI Express port from an external Intel device and will be subsequently forwarded to the Intel® ICH7 (via Assert_GPE and Deassert_GPE messages on DMI).

5.1.45 VCECH—Virtual Channel Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 100–103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities.

Note: Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability:** The Link Declaration Capability is the next in the PCI Express* extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version:** Hardwired to 1 to indicate compliances with the *PCI Express specification, Revsion 1.0a*.
15:0	RO 0002h	**Extended Capability ID:** A value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

5.1.46 PVCCAP1—Port VC Capability Register 1 (D1:F0)

PCI Device: 1
Address Offset: 104h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. **BIOS Requirement:** Set this field to 000b for all configurations.

5.1.47 PVCCAP2—Port VC Capability Register 2 (D1:F0)

PCI Device: 1
Address Offset: 108–10Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset:** This field indicates the location of the VC arbitration table. This field contains the zero-based offset of the table in DQWords (16 bytes) from the base address of the Virtual Channel capability structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority, VC0 is the lowest priority.

5.1.48 PVCCTL—Port VC Control (D1:F0)

PCI Device: 1
Address Offset: 10C–10Dh
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field is programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b, when written to this field, indicates the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0		Reserved

5.1.49 VC0RCAP—VC0 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 110–113h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

5.1.50 VC0RCTL—VC0 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 114–117h
Default Value: 800000FFh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable:** For VC0, this bit is hardwired to 1 and read only as VC0 can never be disabled.
30:27		Reserved
26:24	RO 000b	**VC0 ID:** This field assigns a VC ID to the VC resource. For VC0, this is hardwired to 0 and read only.
23:8		Reserved
7:1	R/W 7Fh	**TC/VC0 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map:** Traffic Class 0 is always routed to VC0.

5.1.51 VC0RSTS—VC0 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 11A–11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC0 Negotiation Pending:** This bit indicates the status of the process of Flow Control initialization. It is set by default on reset, as well as when the corresponding Virtual Channel is disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both components on a Link.
0		Reserved

5.1.52 VC1RCAP—VC1 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 11C–11Fh
Default Value: 00008000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 1b	**Reject Snoop Transactions:** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

5.1.53 VC1RCTL—VC1 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 120–123h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**VC1 Enable:** Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express* port); a 0 read from this bit indicates that the Virtual Channel is currently disabled. 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled. See exceptions in following notes. **NOTES:** 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel. **BIOS Requirement:** This field must not be set to 1b.
30:27		Reserved
26:24	R/W 001b	**VC1 ID:** This field assigns a VC ID to the VC resource. The assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:8		Reserved
7:1	R/W 00h	**TC/VC1 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b	**TC0/VC1 Map:** Traffic Class 0 is always routed to VC0.

5.1.54 VC1RSTS—VC1 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 126–127h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1 b	**VC1 Negotiation Pending:** This bit indicates the status of the process of Flow Control initialization. It is set by default on reset, as well as when the corresponding Virtual Channel is disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

5.1.55 RCLDECH—Root Complex Link Declaration Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 140–143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PCI Express) to other elements of the root complex component to which it belongs. See the PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability:** This is the last capability in the PCI Express* extended capabilities list.
19:16	RO 1h	**Link Declaration Capability Version:** Hardwired to 1 to indicate compliances with *PCI Express Specification, Revision 1.0a.*
15:0	RO 0005h	**Extended Capability ID:** The value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

Note: See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

5.1.56 ESD—Element Self Description (D1:F0)

PCI Device: 1
Address Offset: 144–147h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. The egress port of the component to provide arbitration to this Root Complex Element uses this port number value.
23:16	R/WO 00h	**Component ID:** This field identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 01h	**Number of Link Entries:** This field identifies the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as no peer-to-peer capabilities are reported in this topology).
7:4		Reserved
3:0	RO 0h	**Element Type:** This field identifies the type of the Root Complex Element. Value of 0h represents a root port.

5.1.57 LE1D—Link Entry 1 Description (D1:F0)

PCI Device: 1
Address Offset: 150–153h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

This register contains the first part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry.
15:2		Reserved
1	RO 0b	**Link Type:** This bit identifies that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is **not** valid and will be ignored. 1 = Link Entry specifies a valid link.

5.1.58 LE1A—Link Entry 1 Address (D1:F0)

PCI Device: 1
Address Offset: 158158–15Fh
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

This register contains the second part of a Link Entry that declares an internal link to another Root Complex element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field contains the memory-mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0		Reserved

5.1.59 UESTS—Uncorrectable Error Status (D1:F0)

Bus/Dev/Func/Type: 0/1/0/MMR
Address Offset: 1C4–1C7h
Default Value: 00000000h
Access: RO, R/WC/S
Size: 32 bits

This register reports error status of individual error sources on a PCI Express device. An individual error status bit that is set indicates that a particular error occurred.

Note: Software clears an error status by writing a 1 to the respective bit.

Bit	Access & Default	Description
31:21		Reserved
20	R/WC/S 0b	**Unsupported Request Error Status:** 0 = Error did **Not** occur 1 = Error occurred
19		Reserved
18	R/WC/S 0b	**Malformed TLP Status:** 0 = Error did **Not** occur 1 = Error occurred
17	R/WC/S 0b	**Receiver Overflow Status:** 0 = Error did **Not** occur 1 = Error occurred
16	R/WC/S 0b	**Unexpected Completion Status:** 0 = Error did **Not** occur 1 = Error occurred
15		Reserved
14	R/WC/S 0b	**Completion Timeout Status:** 0 = Error did **Not** occur 1 = Error occurred
13:5		Reserved
4	R/WC/S 0b	**Data Link Protocol Error Status (DLPES):** The Data Link Layer Protocol Error that causes this bit to be set will also cause the Fatal Error Detected bit (bit 2) in the DSTS (Device Status, D1:F0) to be set if not already set. 0 = Error did **Not** occur 1 = Error occurred
3:0		Reserved

5.1.60 UEMSK—Uncorrectable Error Mask (D1:F0)

Bus/Dev/Func/Type: 0/1/0/MMR
Address Offset: 1C8–1CBh
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

This register controls reporting of individual errors by the device (or logic associated with this port) to the PCI Express Root Complex. As these errors are not originating on the other side of a PCI Express link, no PCI Express error message is sent, but the unmasked error is reported directly to the root control logic. A masked error (respective bit set to 1 in the mask register) has no action taken. There is a mask bit per error bit of the Uncorrectable Error Status register.

Bit	Access & Default	Description
31:21		Reserved
20	R/W/S 0b	**Unsupported Request Error Mask:** 0 = **Not** masked 1 = Masked
19		Reserved
18	R/W/S 0b	**Malformed TLP Mask:** 0 = **Not** masked 1 = Masked
17	R/W/S 0b	**Receiver Overflow Mask:** 0 = **Not** masked 1 = Masked
16	R/W/S 0b	**Unexpected Completion Mask:** 0 = Not masked 1 = Masked
15		Reserved
14	R/W/S 0b	**Completion Timeout Mask:** 0 = **Not** masked 1 = Masked
13:5		Reserved
4	R/W/S 0b	**Data Link Protocol Error Mask** 0 = **Not** masked 1 = Masked
3:0		Reserved

5.1.61 CESTS—Correctable Error Status (D1:F0)

Bus/Dev/Func/Type: 0/1/0/MMR
Address Offset: 1D0–1D3h
Default Value: 00000000h
Access: RO,R/WC/S
Size: 32 bits

This register reports error status of individual error sources on a PCI Express device. An individual error status bit that is set indicates that a particular error occurred.

Note: Software clears an error status by writing a 1 to the respective bit.

Bit	Access & Default	Description
31:13		Reserved
12	R/WC/S 0b	**Replay Timer Timeout Status:** 0 = Error did **Not** occur 1 = Error occurred
11:9		Reserved
8	R/WC/S 0b	**Replay Number Rollover Status:** 0 = Error did **Not** occur 1 = Error occurred
7	R/WC/S 0b	**Bad DLLP Status:** 0 = Error did **Not** occur 1 = Error occurred
6	R/WC/S 0b	**Bad TLP Status:** 0 = Error did **Not** occur 1 = Error occurred
5:1		Reserved
0	R/WC/S 0b	**Receiver Error Status (RES):** Receiver errors will be indicated due to all of the following: 8b/10b Decode Errors, Framing Errors, Lane Deskew Errors, and Elasticity Buffer Overflow/Underflow. 0 = Error did **Not** occur 1 = Error occurred

5.1.62 CEMSK—Correctable Error Mask (D1:F0)

Bus/Dev/Func/Type: 0/1/0/MMR
Address Offset: 1D4–1D7h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

This register controls reporting of individual correctable errors by the device (or logic associated with this port) to the PCI Express Root Complex. As these errors are not originating on the other side of a PCI Express link, no PCI Express error message is sent; however, the unmasked error is reported directly to the root control logic. A masked error (respective bit set to 1 in the mask register) has no action taken. There is a mask bit per error bit of the Correctable Error Status register.

Bit	Access & Default	Description
31:13		Reserved
12	R/W/S 0b	**Replay Timer Timeout Mask:** 0 = **Not** masked 1 = Masked
11:9		Reserved
8	R/W/S 0b	**Replay Number Rollover Mask:** 0 = **Not** masked 1 = Masked
7	R/W/S 0b	**Bad DLLP Mask:** 0 = **Not** masked 1 = Masked
6	R/W/S 0b	**Bad TLP Mask:** 0 = **Not** masked 1 = Masked
5:1		Reserved
0	R/W/S 0b	**Receiver Error Mask:** 0 = **Not** masked 1 = Masked

5.1.63 PEG_SSTS—PCI Express* Sequence Status (D1:F0)

PCI Device: 1
Address Offset: 218–21Fh
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60		Reserved
59:48	RO 000h	**Next Transmit Sequence Number:** This field contains the value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44		Reserved
43:32	RO 000h	**Next Packet Sequence Number:** This field contains the packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28		Reserved
27:16	RO 000h	**Next Receive Sequence Number:** This field contains the sequence number associated with the TLP that is expected to be received next.
15:12		Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number:** This field contains the sequence number associated with the last acknowledged TLP.

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6 Direct Media Interface (DMI) RCRB

This Root Complex Register Block (RCRB) controls the (G)MCH-ICH7 serial interconnect. The base address of this space is programmed in DMIBAR in D0:F0 configuration space. Table 6-1 provides an address map of the DMI registers listed by address offset in ascending order. Section 6.1 provides a detailed bit description of the registers.

Note: All RCRB register spaces need to remain organized as they are here.

Table 6-1. DMI Register Address Map

Offset Address	Register Symbol	Register Name	PCI Dev #
000–003h	DMIVCECH	DMI Virtual Channel Enhanced Capability Header	DMIBAR
004–007h	DMIPVCCAP1	DMI Port VC Capability Register 1	DMIBAR
008–00Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	DMIBAR
00C–00Dh	DMIPVCCTL	DMI Port VC Control	DMIBAR
00E–00Fh	—	*Reserved*	DMIBAR
010–013h	DMIVC0RCAP	DMI VC0 Resource Capability	DMIBAR
014–017h	DMIVC0RCTL	DMI VC0 Resource Control	DMIBAR
018–019h	—	*Reserved*	DMIBAR
01A–01Bh	DMIVC0RSTS	DMI VC0 Resource Status	DMIBAR
01C–01Fh	DMIVC1RCAP	DMI VC1 Resource Capability	DMIBAR
020–023h	DMIVC1RCTL	DMI VC1 Resource Control	DMIBAR
024–025h	—	*Reserved*	DMIBAR
026–027h	DMIVC1RSTS	DMI VC1 Resource Status	DMIBAR
028–083h	—	*Reserved*	DMIBAR
084–087h	DMILCAP	DMI Link Capabilities	DMIBAR
088–089h	DMILCTL	DMI Link Control	DMIBAR
08A–08Bh	DMILSTS	DMI Link Status	DMIBAR
1C4–1C7h	DMIUESTS	DMI Uncorrectable Error Status	DMIBAR
1C8–1CBh	DMIUEMSK	DMI Uncorrectable Error Mask	DMIBAR
1D0–1D3h	DMICESTS	DMI Correctable Error Status	DMIBAR
08C–1FFh	—	*Reserved*	DMIBAR

6.1 DMI RCRB Configuration Register Details

6.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability Header

MMIO Range: DMIBAR
Address Offset: 000–003h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability:** This field indicates the next item in the list.
19:16	RO 1h	**Capability Version:** This field indicates support as a version 1 capability structure.
15:0	RO 0002h	**Capability ID:** This field indicates this is the Virtual Channel capability item.

6.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

MMIO Range: DMIBAR
Address Offset: 004–007h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:12		Reserved
11:10	RO 00b	**Port Arbitration Table Entry Size (PATS):** This field indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports).
9:8	RO 00b	**Reference Clock (RC):** This field is hardwired for a clock of 10 ns.
7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVC):** This field indicates that there are no additional VCs of low priority with extended capabilities.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates that there is one additional VC (VC1) that exists with extended capabilities.

6.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

MMIO Range: DMIBAR
Address Offset: 008–00Bh
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (ATO):** This field indicates that no table is present for VC arbitration since it is fixed.
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the VC arbitration is fixed in the root complex. VC1 is highest priority and VC0 is lowest priority.

6.1.4 DMIPVCCTL—DMI Port VC Control

MMIO Range: DMIBAR
Address Offset: 00C–00Dh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0		Reserved

6.1.5 DMIVC0RCAP—DMI VC0 Resource Capability

MMIO Range: DMIBAR
Address Offset: 010–013h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This VC implements fixed arbitration; therefore, this field is not used.
15	RO 0b	**Reject Snoop Transactions (RTS):** This VC must be able to take snoopable transactions.
14:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates that this VC uses fixed port arbitration.

6.1.6 DMIVC0RCTL—DMI VC0 Resource Control

MMIO Range: DMIBAR
Address Offset: 014–017h
Default Value: 800000FEh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel Enable (EN):** 0 = Disable 1 = Enable.
30:27		Reserved
26:24	RO 000b	**Virtual Channel Identifier (ID):** This field indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** This field indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16:8		Reserved
7:1	R/W 7Fh	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. For example when bit 7 is set in this field, Transaction Class 7 is mapped to this Virtual channel resource. When more than one bit in this field is set, it indicates that multiple Transaction Classes from the Transcation Class/Virtual Channel map of an enabled Virtual Channel, software must ensure that no new or outstanding transactions with the Transaction Class labels are targeted at the given Link.
0		Reserved

6.1.7 DMIVC0RSTS—DMI VC0 Resource Status

MMIO Range: DMIBAR
Address Offset: 01A–01Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1 b	**VC Negotiation Pending (NP):** 0 = The Virtual Channel negotiation is complete. 1 =The Virtual Channel resource is still in the process of negotiation (initialization or disabling). **NOTE:** Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both components on a link.
0		Reserved

6.1.8 DMIVC1RCAP—DMI VC1 Resource Capability

MMIO Range: DMIBAR
Address Offset: 01C–01Fh
Default Value: 00008001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 1b	**Reject Snoop Transactions (RTS):** 0 =Transactions with or without the no snoop bit set within the TLP header are allowed on this VC. 1 =Any transaction without the no Snoop bit set within the TLP header will be rejected as an unsupported request.
14:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates the port arbitration capability is time-based WRR of 128 phases.

6.1.9 DMIVC1RCTL—DMI VC1 Resource Control

MMIO Range: DMIBAR
Address Offset: 020–023h
Default Value: 01000000h
Access: R/W
Size: 32 bits

This register controls the resources associated with Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**Virtual Channel 1 Enable (VC1E):** 0 = Disable 1 = Enable
30:27		Reserved
26:24	R/W 001b	**Virtual Channel 1 Identifier (VC1ID):** This field indicates the ID to use for this virtual channel. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** This field indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16:8		Reserved
7:1	R/W 00h	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

6.1.10 DMIVC1RSTS—DMI VC1 Resource Status

MMIO Range: DMIBAR
Address Offset: 026–027h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC Negotiation Pending (NP):** 0 = VC negotiation **Not** pending 1 = Virtual channel is still being negotiated with ingress ports.
0		Reserved

6.1.11 DMILCAP—DMI Link Capabilities

MMIO Range: DMIBAR
Address Offset: 084–087h
Default Value: 00012C41h
Access: RO, R/WO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency (EL1):** L1 is not supported on DMI.
14:12	R/WO 010b	**L0s Exit Latency (EL0):** This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	RO 11b	**Active State Link PM Support (APMS):** This field indicates that L0s is supported on DMI.
9:4	RO 4h	**Maximum Link Width (MLW):** This field indicates the maximum link width is 4 ports.
3:0	RO 1h	**Maximum Link Speed (MLS):** This field indicates the link speed is 2.5 Gb/s.

6.1.12 DMILCTL—DMI Link Control

MMIO Range: DMIBAR
Address Offset: 088–089h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of DMI.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0 h	**Extended Synch (ES):** 1 = Forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0.
6:2		Reserved
1:0	R/W 00 b	**Active State Link PM Control (APMC):** This field indicates whether DMI should enter L0s. 00 = Disabled 01 = L0s entry enabled 10 = Reserved 11 = Reserved

6.1.13 DMILSTS—DMI Link Status

MMIO Range: DMIBAR
Address Offset: 08A–08Bh
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access & Default	Description
15:10		Reserved
9:4	RO 00h	**Negotiated Link Width (NLW):** The negotiated link width is x4 (000100b).
3:0	RO 1h	**Link Speed (LS):** Link is 2.5 Gb/s.

6.1.14 DMIUESTS—DMI Uncorrectable Error Status

Bus/Dev/Func/Type: 0/0/0/DMIBAR
Address Offset: 1C4–1C7h
Default Value: 00000000h
Access: R/WC/S
Size: 32 bits

This register reports error status of individual uncorrectable error sources on DMI. An individual error status bit that is set indicates that a particular error occurred.

Note: Software clears an error status by writing a 1 to the respective bit.

Bit	Access & Default	Description
31:21		Reserved
20	R/WC/S 0b	**Unsupported Request Error Status:** 0 = Error did **Not** occur 1 = Error occurred
19		Reserved
18	R/WC/S 0b	**Malformed TLP Status:** 0 = Error did **Not** occur 1 = Error occurred
17	R/WC/S 0b	**Receiver Overflow Status:** 0 = Error did **Not** occur 1 = Error occurred
16	R/WC/S 0b	**Unexpected Completion Status:** 0 = Error did **Not** occur 1 = Error occurred
15		Reserved
14	R/WC/S 0b	**Completion Timeout Status:** 0 = Error did **Not** occur 1 = Error occurred
13:5		Reserved
4	R/WC/S 0b	**Data Link Protocol Error Status:** 0 = Error did **Not** occur 1 = Error occurred
3:0		Reserved

6.1.15 DMIUEMSK—DMI Uncorrectable Error Mask

Bus/Dev/Func/Type: 0/0/0/DMIBAR
Address Offset: 1C8–1CBh
Default Value: 00000000h
Access: R/W/S
Size: 32 bits

This register controls reporting of individual uncorrectable errors over DMI. A masked error (respective bit set to 1 in the mask register) has no action taken. There is a mask bit per error bit of the DMIUESTS register.

Bit	Access & Default	Description
31:21		Reserved
20	R/W/S 0b	**Unsupported Request Error Mask:** 0 = **Not** masked 1 = Masked
19		Reserved
18	R/W/S 0b	**Malformed TLP Mask:** 0 = **Not** masked 1 = Masked
17	R/W/S 0b	**Receiver Overflow Mask:** 0 = **Not** masked 1 = Masked
16	R/W/S 0b	**Unexpected Completion Mask:** 0 = **Not** masked 1 = Masked
15		Reserved
14	R/W/S 0b	**Completion Timeout Mask:** 0 = **Not** masked 1 = Masked
13:5		Reserved
4	R/W/S 0b	**Data Link Protocol Error Mask:** 0 = **Not** masked 1 = Masked
3:0		Reserved

6.1.16 DMICESTS—DMI Correctable Error Status

Bus/Dev/Func/Type: 0/0/0/DMIBAR
Address Offset: 1D0–1D3h
Default Value: 00000000h
Access: R/WC/S
Size: 32 bits

This register reports error status of individual correctable error sources on DMI. An individual error status bit that is set indicates that a particular error occurred.

Note: Software clears an error status by writing a 1 to the respective bit.

Bit	Access & Default	Description
31:13		Reserved
12	R/WC/S 0b	**Replay Timer Timeout Status:** 0 = Error did **Not** occur 1 = Error occurred
11:9		Reserved
8	R/WC/S 0b	**REPLAY_NUM Rollover Status:** 0 = Error did **Not** occur 1 = Error occurred
7	R/WC/S 0b	**Bad DLLP Status:** 0 = Error did **Not** occur 1 = Error occurred
6	R/WC/S 0b	**Bad TLP Status:** 0 = Error did **Not** occur 1 = Error occurred
5:1		Reserved
0	R/WC/S 0b	**Receiver Error Status (RES):** Receiver errors will be indicated due to all of the following: 8b/10b Decode Errors, Framing Errors, Lane Deskew Errors, and Elasticity Buffer Overflow/Underflow. 0 = Error did **Not** occur 1 = Error occurred

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7 Integrated Graphics Device (D2:F0) (Intel® 82945G/82945GC/ 82945GZ GMCH Only)

The Integrated Graphics Device registers are located in Device 2 (D2), Function 0 (F0) and Function 1 (F1). This chapter provides the descriptions for the D2:F0 registers. Table 7-1 provides an address map of the D2:F0 registers listed in ascending order by address offset. Section 7.1 provides a detailed bit description of the registers.

Function 0 can be VGA compatible or not; this is selected through bit 1 of the GGC register (D0:F0, offset 52h).

Note: The following sections describe Device 2 PCI configuration registers only.

Table 7-1. Integrated Graphics Device Register Address Map (D2:F0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2772h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
0Fh	—	*Reserved*	—	—
10–13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14–17h	IOBAR	I/O Base Address	00000001h	RO, R/W
18–1Bh	GMADR	Graphics Memory Range Address	00000008h	RO, R/W/L
1C–1Fh	GTTADR	Graphics Translation Table Range Address	00000000h	RO, R/W
20–2Bh	—	*Reserved*	—	—
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO

Address Offset	Symbol	Register Name	Default Value	Access
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	90h	RO
35–3Bh	—	*Reserved*	—	—
3Ch	INTRLINE	Interrupt Line	01h	R/W
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–43h	—	*Reserved*	—	—
44h	MCAPPTR	Mirror of Device 0 Capability Pointer	E0h	RO
45–47h	—	*Reserved*	—	—
48–50h	MCAPID	Mirror of Device 0 Capability Identification	0000000000 01090009h	RO
51h	—	*Reserved*	—	—
52–53h	MGGC	Mirror of Device 0 GMCH Graphics Control	0030h	RO
54–57h	MDEVEN	Mirror of Device 0 Device Enable	See register description	RO
58–5Bh	—	*Reserved*	—	—
5C–5Fh	BSM	Base of Stolen Memory	07800000h	RO
60–61h	—	*Reserved*	0000h	R/W
63–CFh	—	*Reserved*	—	—
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6–D7h	—	*Reserved*	—	—
E0–E1h	SWSMI	Software SMI	0000h	R/W
E2–E3h	—	*Reserved*	—	—
E4–E7h	ASLE	System Display Event	00000000h	R/W
E8h–FBh	—	*Reserved*	—	—
FC–FFh	ASLS	ASL Storage	00000000h	R/W

7.1 Configuration Register Details (D2:F0)

7.1.1 VID2—Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** This field provides the PCI standard identification for Intel.

7.1.2 DID2—Device Identification (D2:F0)

PCI Device: 2
Address Offset: 02h
Default Value: 2772h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2772h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device

7.1.3 PCICMD2—PCI Command (D2:F0)

PCI Device: 2
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0 = Enable the assertion of this device's INTx# signal. 1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to the DMI.
9	RO 0b	**Fast Back-to-Back (FB2B)**: Hardwired to 0. Not Implemented.
8	RO 0b	**SERR Enable (SERRE):** Hardwired to 0. Not Implemented.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Hardwired to 0. Not Implemented.
6	RO 0b	**Parity Error Enable (PERRE):** Hardwired to 0. Not Implemented. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0. The IGD ignores special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE)**: This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

7.1.4 PCISTS2—PCI Status (D2:F0)

PCI Device: 2
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS2 reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. The IGD does not detect parity.
14	RO 0b	**Signaled System Error (SSE):** Hardwired to 0. The IGD never asserts SERR#.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. The IGD never gets a Master Abort.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The IGD never gets a Target Abort.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. Hardwired to 00b.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Hardwired to 0. Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection).
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** N/A. Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI configuration space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the Command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0		Reserved

7.1.5 RID2—Revision Identification (D2:F0)

PCI Device: 2
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number for Device 2, Functions 0 and 1.

Bit	Access & Default	Description
7:0	RO	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH. Refer to the *Intel® 945G/945GC*/945GZ*/945P/945PL Express Chipset Specification Update* for the value of the Revision ID register.

7.1.6 CC—Class Code (D2:F0)

PCI Device: 2
Address Offset: 09h
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display Controller.
15:8	RO 00h	**Sub-Class Code (SUBCC):** The value in this field is determined based on Device 0 GGC register, bit 1. 00h = VGA compatible 80h = Non VGA
7:0	RO 00h	**Programming Interface (PI):** 00h = Display controller.

7.1.7 CLS—Cache Line Size (D2:F0)

PCI Device: 2
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD, as a PCI compliant master, does not use the memory write and invalidate command and, in general, does not perform operations based on cache line size.

7.1.8 MLT2—Master Latency Timer (D2:F0)

PCI Device: 2
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value:** Hardwired to 0s.

7.1.9 HDR2—Header Type (D2:F0)

PCI Device: 2
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFunc):** This bit indicates if the device is a multi-function device. The value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFunc bit is also set.
6:0	RO 00h	**Header Code (H):** This field is a 7-bit value that indicates the header code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

7.1.10 MMADR—Memory Mapped Range Address (D2:F0)

PCI Device: 2
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000h	**Memory Base Address:** Set by the operating system, these bits correspond to address signals 31:19.
18:4	RO 0000h	**Address Mask:** Hardwired to 0s to indicate 512 KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

7.1.11 IOBAR—I/O Base Address (D2:F0)

PCI Device:	2
Address Offset:	14h
Default Value:	00000001h
Access:	RO, R/W
Size:	32 bits

This register provides the base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O base to be located anywhere in 16-bit I/O address space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8 Bytes of I/O space is allowed in PM state D0 when the I/O Enable bit (PCICMD[0]) is set to 1. Access is disallowed in PM states D1–D3 or if the I/O Enable is clear or if Device 2 is turned off. Note that access to this I/O BAR is independent of VGA functionality within Device 2. Also, note that this mechanism is available only through function 0 of Device 2 and is not duplicated in Function 1.

If accesses to this I/O bar are allowed, the GMCH claims all 8, 16, or 32 bit I/O cycles from the processor that fall within the 8 Bytes claimed.

Bit	Access & Default	Description
31:16		Reserved
15:3	R/W 0000h	**IO Base Address:** Set by the operating system, these bits correspond to address signals 15:3.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 1b	**Memory / IO Space:** Hardwired to 1 to indicate I/O space.

7.1.12 GMADR—Graphics Memory Range Address (D2:F0)

PCI Device: 2
Address Offset: 18h
Default Value: 00000008h
Access: RO, R/W/L
Size: 32 bits

The IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
31:28	R/W 0h	**Memory Base Address:** Set by the OS, these bits correspond to address signals 31:28.
27:4	RO 000000h	**Address Mask:** Hardwired to 0s to indicate a 256-MB address range
3	RO 1b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching
2:1	RO 00b	**Memory Type:** Hardwired to 0 to indicate 32-bit address.
0	RO 0b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

7.1.13 GTTADR—Graphics Translation Table Range Address (D2:F0)

PCI Device: 2
Address Offset: 1Ch
Default Value: 00000000h
Access: RO, R/W/L
Size: 32 bits

This register requests allocation for the Graphics Translation Table Range. The allocation is for 256 KB and the base address is defined by bits 31:18.

Bit	Access & Default	Description
31:18	R/W 0000h	**Memory Base Address (MBA):** Set by the operating system, these bits correspond to address signals 31:18.
17:4	RO 0000h	**Address Mask (ADMSK):** Hardwired to 0s to indicate a 256 KB address range.
3	RO 0b	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type (MEMTYP):** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

7.1.14 SVID2—Subsystem Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a reset.

7.1.15 SID2—Subsystem Identification (D2:F0)

PCI Device: 2
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a reset.

7.1.16 ROMADR—Video BIOS ROM Base Address (D2:F0)

PCI Device: 2
Address Offset: 30h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore, this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address:** Hardwired to 0s.
17:11	RO 00h	**Address Mask:** Hardwired to 0s to indicate 256-KB address range.
10:1		Reserved
0	RO 0b	**ROM BIOS Enable:** Hardwired to 0 to indicate ROM is not accessible.

7.1.17 CAPPOINT—Capabilities Pointer (D2:F0)

PCI Device: 2
Address Offset: 34h
Default Value: 90h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 90h	**Capabilities Pointer Value:** This field contains an offset into the function's PCI configuration space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h, or the Power Management Capabilities ID registers at address D0h.

7.1.18 INTRLINE—Interrupt Line (D2:F0)

PCI Device: 2
Address Offset: 3Ch
Default Value: 01h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 01h	**Interrupt Connection:** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that is connected to the device's interrupt pin.

7.1.19 INTRPIN—Interrupt Pin (D2:F0)

PCI Device: 2
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a device that only has interrupts associated with a single function, the IGD specifies INTA# as its interrupt pin. 01h = INTA#.

7.1.20 MINGNT—Minimum Grant (D2:F0)

PCI Device: 2
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

7.1.21 MAXLAT—Maximum Latency (D2:F0)

PCI Device: 2
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

7.1.22 MCAPPTR—Mirror of Device 0 Capability Pointer (D2:F0) (Mirrored_D0_34)

PCI Device: 2
Address Offset: 44h
Default Value: E0h
Access: RO
Size: 8 bits

This register is a read only copy of Device 0, offset 34h register.

7.1.23 MCAPID—Mirror of Device 0 Capability Identification (D2:F0) (Mirrored_D0_E0)

PCI Device: 2
Address Offset: 48h
Default Value: 000000000001090009h
Access: RO
Size: 72 bits

This register is a read only copy of Device 0, offset E0h register.

7.1.24 MGGC—Mirror of Device 0 GMCH Graphics Control (D2:F0) (Mirrored_D0_52)

PCI Device: 2
Address Offset: 52h
Default Value: 0030h
Access: RO
Size: 16 bits

This register is a read only copy of Device 0, offset 52h register.

7.1.25 MDEVEN—Mirror of Device 0 Device Enable (D2:F0) (Mirrored_D0_54)

PCI Device: 2
Address Offset: 54h
Default Value: 82945G/82945GC/82945GZ GMCH: 0000001Bh
82945P/82945PL MCH: 00000003h
Access: RO
Size: 32 bits

This register is a read only copy of Device 0, Function 0, offset 54h register.

7.1.26 BSM—Base of "Stolen" Memory (D2:F0)

PCI Device: 2
Address Offset: 5Ch
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, the GMCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0		Reserved

7.1.27 PMCAPID—Power Management Capabilities ID (D2:F0)

PCI Device: 2
Address Offset: D0h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**NEXT_PTR:** This field contains a pointer to the next item in the capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**CAP_ID:** SIG defines this ID is 01h for power management.

7.1.28 PMCAP—Power Management Capabilities (D2:F0)

PCI Device: 2
Address Offset: D2h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. The field is hardwired to 0s to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2:** Hardwired to 0 to indicate that the D2 power management state is not supported.
9	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6		Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO 0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with the *PCI Power Management Interface Specification, Revision 1.1*.

7.1.29 PMCS—Power Management Control/Status (D2:F0)

PCI Device: 2
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME_Status:** This bit is 0 to indicate that the IGD does not support PME# generation from D3 (cold).
14:9		Reserved
8	RO 0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

7.1.30 SWSMI—Software SMI (D2:F0)

PCI Device: 2
Address Offset: E0h
Default Value: 0000h
Access: R/W
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist that expect this register at this address, D2, F0, address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	R/W 00h	**SW scratch bits**
7:1	R/W 00h	**Software Flag:** This field indicates the caller and SMI function desired, as well as return result.
0	R/W 0b	**GMCH Software SMI Event:** Software must write a 0 to clear this bit. 0 = SMI Not triggered. 1 = When set, this bit will trigger an SMI.

7.1.31 ASLE—System Display Event Register (D2:F0)

PCI Device: 2
Address Offset: E4h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Byte, Word, or Double Word PCI configuration cycles can access this register.

Bit	Access & Default	Description
31:24	R/W 00h	**ASLE Scratch Trigger 3:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W 00h	**ASLE Scratch Trigger 2:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W 00h	**ASLE Scratch Trigger 1:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W 00h	**ASLE Scratch Trigger 0:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

7.1.32 ASLS—ASL Storage (D2:F0)

PCI Device: 2
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register is read/write accessible. The exact bit register usage must be worked out in common between system BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/Non VGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000h	RW according to a software controlled usage to support device switching.

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8 Integrated Graphics Device (D2:F1) Registers (Intel® 82945G/82945GC/82945GZ GMCH Only)

The Integrated Graphics Device registers are located in Device 0 (D0), Function 0 (F0) and Function 1 (F1). This chapter provides the descriptions for the D2:F1 registers. Table 8-1 provides an address map of the D2:F1registers listed in ascending order by address offset. Detailed bit descriptions follow this table.

Table 8-1. Device 2 Function 1 Register Address Map (D2:F1)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2776h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code Register	03800h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type Register	80h	RO
0Fh	—	*Reserved*	—	—
10–13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14–2Bh	—	*Reserved*	—	—
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35–3Dh	—	*Reserved*	—	—
3Eh	MINGNT	Minimum Grant Register	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–43h	—	*Reserved*	—	—

Address Offset	Symbol	Register Name	Default Value	Access
44h	MCAPPTR	Mirror of Device 0 Capability Pointer	E0h	RO
45–47h	—	*Reserved*	—	—
48–50h	MCAPID	Mirror of Device 0 Capability Identification	0000000000 01090009h	RO
51h	—	*Reserved*	—	—
52–53h	MGGC	Mirror of Device 0 GMCH Graphics Control	0030h	RO
54–57h	MDEVEN	Mirror of Device 0 Device Enable	0000001Bh	RO
58–5Bh	—	*Reserved*	—	—
5C–5Fh	BSM	Base of Stolen Memory Register	07800000h	RO
60–CFh	—	*Reserved*	0000h	—
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6–DFh	—	*Reserved*	—	—
E0–E1h	SWSMI	Software SMI	0000h	R/W
E2–FBh	—	*Reserved*	—	—
FC–FFh	ASLS	ASL Storage	00000000h	R/W

8.1.1 VID2—Vendor Identification (D2:F1)

PCI Device: 2
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register is a copy of Device2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.2 DID2—Device Identification (D2:F1)

PCI Device: 2
Address Offset: 02h
Default Value: 2776h
Access: RO
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of Function 1 when both Function 0 and Function 1 have the same class code.

8.1.3 PCICMD2—PCI Command (D2:F1)

PCI Device: 2
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back (FB2B)**: Hardwired to 0. Not Implemented.
8	RO 0b	**SERR Enable (SERRE):** Hardwired to 0. Not Implemented.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Hardwired to 0. Not Implemented.
6	RO 0b	**Parity Error Enable (PERRE):** Hardwired to 0. Not Implemented. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** Hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0. The IGD ignores special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable. 1 = Enable. Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

8.1.4 PCISTS2—PCI Status (D2:F1)

PCI Device: 2
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS2 reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS2 also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. The IGD does not detect parity.
14	RO 0b	**Signaled System Error (SSE):** Hardwired to 0. The IGD never asserts SERR#.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. The IGD never gets a master abort.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The IGD never gets a target abort.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. Hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Hardwired to 0. Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI configuration space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status:** Hardwired to 0.
2:0		Reserved

8.1.5 RID2—Revision Identification (D2:F1)

PCI Device: 2
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

Bit	Access & Default	Description
7:0	RO	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH. Refer to the *Intel® 945G/945GC/945GZ/945P/945PL Express Chipset Specification Update* for the value of the Revision ID register.

8.1.6 CC—Class Code Register (D2:F1)

PCI Device: 2
Address Offset: 09h
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display controller.
15:8	RO 80h	**Sub-Class Code (SUBCC):** 80h = Non VGA
7:0	RO 00h	**Programming Interface (PI):** 00h = Display controller.

8.1.7 CLS—Cache Line Size (D2:F1)

PCI Device:	2
Address Offset:	0Ch
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.8 MLT2—Master Latency Timer (D2:F1)

PCI Device:	2
Address Offset:	0Dh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.9 HDR2—Header Type Register (D2:F1)

PCI Device:	2
Address Offset:	0Eh
Default Value:	80h
Access:	RO
Size:	8 bits

This register is a copy of Device2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.10 MMADR—Memory Mapped Range Address (D2:F1)

PCI Device: 2
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits 31:19.

Bit	Access & Default	Description
31:19	R/W 0000h	**Memory Base Address:** Set by the operating system, these bits correspond to address signals 31:19.
18:4	RO 0000h	**Address Mask:** Hardwired to 0s to indicate 512-KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

8.1.11 SVID2—Subsystem Vendor Identification (D2:F1)

PCI Device: 2
Address Offset: 2Ch
Default Value: 0000h
Access: RO
Size: 16 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.12 SID2—Subsystem Identification (D2:F1)

PCI Device: 2
Address Offset: 2Eh
Default Value: 0000h
Access: RO
Size: 16 bits

This register is a read only copy of Device 2, Function 0.

8.1.13 ROMADR—Video BIOS ROM Base Address (D2:F1)

PCI Device:	2
Address Offset:	30h
Default Value:	00000000h
Access:	RO
Size:	32 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.14 CAPPOINT—Capabilities Pointer (D2:F1)

PCI Device:	2
Address Offset:	34h
Default Value:	D0h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.15 MINGNT—Minimum Grant Register (D2:F1)

PCI Device:	2
Address Offset:	3Eh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.16 MAXLAT—Maximum Latency (D2:F1)

PCI Device:	2
Address Offset:	3Fh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.17 MCAPPTR—Mirror of Device 0 Capability Pointer (D2:F1) (Mirrored_D0_34)

PCI Device:	2
Address Offset:	44h
Default Value:	D0h
Access:	RO
Size:	8 bits

This register is a read only copy of Device 0, Offset 34h register.

8.1.18 MCAPID—Mirror of Device 0 Capability Identification (D2:F1) (Mirrored_D0_E0)

PCI Device:	2
Address Offset:	48h
Default Value:	000000000001090009h
Access:	RO
Size:	72 bits

This register is a read only copy of Device 0, Offset E0h register.

8.1.19 MGGC—Mirror of Device 0 GMCH Graphics Control (D2:F1) (Mirrored_D0_52)

PCI Device:	2
Address Offset:	52h
Default Value:	0030h
Access:	RO
Size:	16 bits

This register is a read only copy of Device 0, Offset 52h register.

8.1.20 MDEVEN—Mirror of Device 0 Device Enable (D2:F1) (Mirrored_D0_54)

PCI Device:	2
Address Offset:	54h
Default Value:	82945G/82945GC/82945GZ GMCH: 0000001Bh 82945P/82945PL MCH: 00000003h
Access:	RO
Size:	32 bits

This register is a read only copy of Device 0, Function 0, Offset 54h register.

8.1.21 BSM—Base of Stolen Memory Register (D2:F1)

PCI Device:	2
Address Offset:	5Ch
Default Value:	07800000h
Access:	RO
Size:	32 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.22 PMCAPID—Power Management Capabilities ID (D2:F1)

PCI Device:	2
Address Offset:	D0h
Default Value:	0001h
Access:	RO
Size:	16 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.23 PMCAP—Power Management Capabilities (D2:F1)

PCI Device:	2
Address Offset:	D2h
Default Value:	0022h
Access:	RO
Size:	16 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.24 PMCS—Power Management Control/Status (D2:F1)

PCI Device: 2
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		Reserved
8	RO 0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

8.1.25 SWSMI—Software SMI (D2:F1)

PCI Device: 2
Address Offset: E0h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register is a copy of Device 2, Function 0. It has the same read, write attributes as Function 0. It is implemented as common hardware with two access addresses.

8.1.26 ASLS—ASL Storage (D2:F1)

PCI Device: 2
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register is read/write accessible. The exact bit register usage must be worked out in common between system BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000h	R/W according to a software controlled usage to support device switching.

8.2 Device 2 – PCI I/O Registers

The following are not PCI configuration registers; they are I/O registers.

8.2.1 MMIO Index—MMIO Address Register

I/O Address: IOBAR + 0h
Default: 00000000h
Access: R/W
Size: 32 bits

A 32 bit I/O write to this port loads the **offset** of the MMIO register that needs to be accessed. An I/O read returns the current value of this register. An 8/16-bit I/O write to this register is completed by the GMCH but does not update this register. This mechanism is used to access internal graphics MMIO registers; however, it must not be used to access VGA I/O registers that are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access & Default	Description
31:2	R/W 00000000h	**Register Offset**: This field selects any one of the DWord registers within the MMIO register space of Device 2.
1:0		Reserved

8.2.2 MMIO Data—MMIO Data Register

I/O Address: IOBAR + 4h
Default: 00000000h
Access: R/W
Size: 32 bits

A 32 bit I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. A 32 bit I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register. 8 or 16 bit I/O writes are completed by the GMCH and may have un-intended side effects; hence, must not be used to access the data port. 8 or 16 bit I/O reads are completed normally.

Bit	Access & Default	Description
31:0	R/W 00000000h	**MMIO Data Window**

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9 System Address Map

The 82945G/82945P (G)MCH supports 4 GB of addressable memory space (see Figure 9-1) and 64 KB+3 bytes of addressable I/O space. The 82945GC/82945GZ/82945PL (G)MCH supports 2 GB of addressable memory space and 64 KB+3 bytes of addressable I/O space. A programmable memory address space under the 1-MB region is divided into regions that can be individually controlled with programmable attributes such as disable, read/write, write only, or read only. This section focuses on how the memory space is partitioned and memory region usage. The I/O address space has simpler mapping and is explained near the end of this section.

Note: Address mapping information for the Integrated Graphics Device applies to the 82945G/82945GC/82945GZ GMCH only. The 82945P/82945PL MCH does not have an IGD.

Note: References to PCI Express applies to the 82945G/82945GC/82945P/82945PL (G)MCH only. The 82945GZ GMCH does not support PCI Express.

Note: References to 4 GB addressable memory space applies to the 82945G/82945P only. The 82945GC/82945GZ/82945PL support 2 GB addressable memory space.

Addressing of memory ranges larger than 4 GB (2 GB for 82945GC/82945GZ/82945PL) is **not** supported. The HREQ[4:3] FSB pins are decoded to determine whether the access is above or below 4 GB (2 GB for 82945GC/82945GZ/82945PL).

The (G)MCH does not support the PCI Dual Address Cycle (DAC) mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB (2 GB for 82945GC/82945GZ/82945PL) on either the DMI or PCI Express interface. The (G)MCH does not limit system memory space in hardware. There is no hardware lock to prevent someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges that may be mapped to PCI Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device, respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

- Device 0
  - EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4-KB window)
  - MCHBAR – Memory mapped range for internal (G)MCH registers. For example, memory buffer register controls. (16-KB window)
  - PCIEXBAR (82945G/82945GC/82945P/82945PL Only) – Flat memory-mapped address space to access device configuration registers. This mechanism can be used to access PCI configuration space (0–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64 MB, 128 MB, or 256-MB window)

  - DMIBAR – This window is used to access registers associated with the (G)MCH/ICH7 (DMI) register memory range. (4-KB window)
  - IFPBAR – Any write to this window will trigger a flush of the (G)MCH's Global Write Buffer to let software include coherency between writes from an isochronous agent and writes from the processor (4-KB window).
  - GGC – GMCH graphics control register (82945G/82945GC/82945GZ GMCH only). This register is used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes (0–64-MB options).

- Device 1, Function 0
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - IOBASE1/IOLIMIT1 – PCI Express port I/O access window.

- Device 2, Function 0 (82945G/82945GC/82945GZ GMCH only)
  - MMADR – IGD registers and internal graphics instruction port (512-KB window)
  - IOBAR – I/O access window for internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note that this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
  - GMADR – Internal graphics translation window (256-MB or 512-MB window)
  - GTTADR – Internal graphics translation table location (256-KB or 512-KB window).

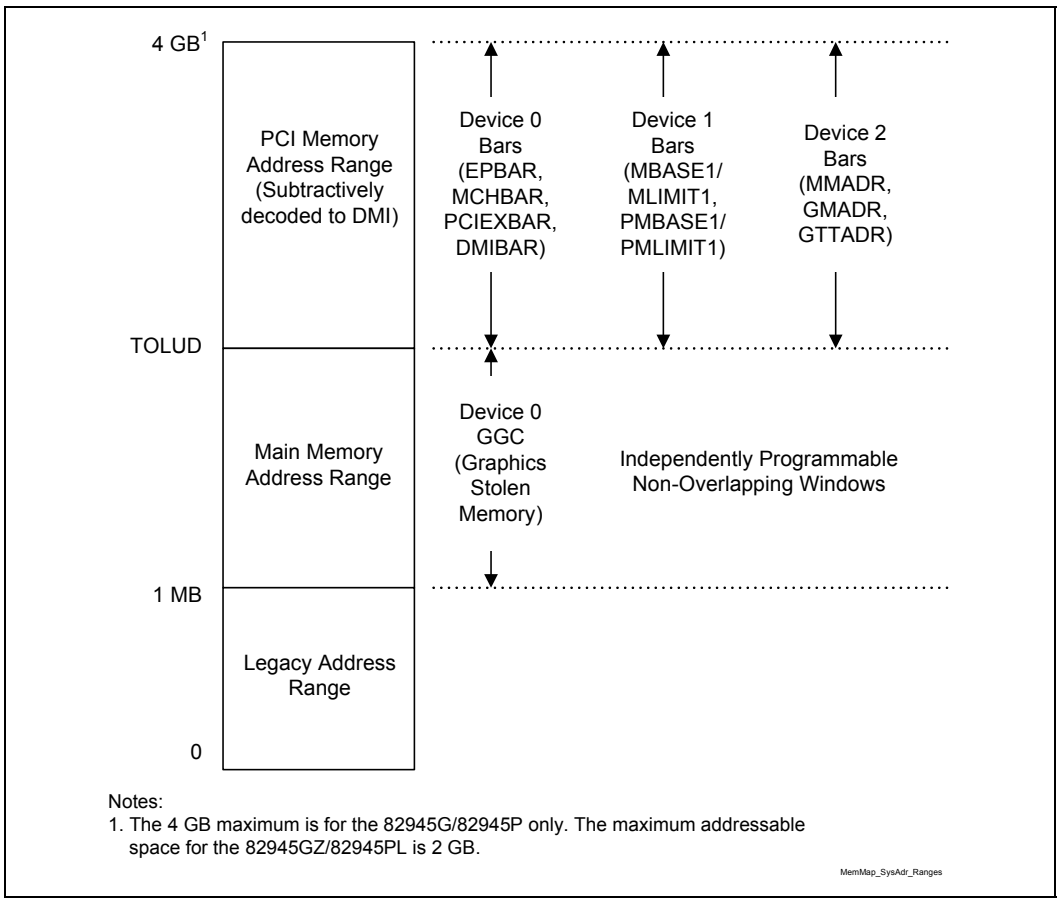
- Device 2, Function 1 (82945G/82945GC/82945GZ GMCH only)
  - MMADR – Function 1 IGD registers and internal graphics instruction port (512-KB window)

The rules for the above programmable ranges are:

- ALL of these ranges **Must** be unique and **Non-Overlapping**. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express , High BIOS, PCI Express memory-mapped space, and APIC memory space can be allocated.
- In the case of overlapping ranges with memory, the memory decode will be given priority.
- There are **No** Hardware Interlocks to prevent problems in the case of overlapping ranges.
- Accesses to overlapped ranges may produce indeterminate results.
- The only peer-to-peer cycles allowed below the top of memory (TOLUD register) are DMI to PCI Express VGA range writes. Note that peer-to-peer cycles to the internal graphics VGA range are not supported.

Figure 9-1 shows a simplified form of the the system memory address map.

Figure 9-1. System Address Ranges



9.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB – DOS Area
- 640 – 768 KB – Legacy Video Buffer Area
- 768 – 896 KB in 16-KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16-KB sections (total of 4 sections) – Extended System BIOS Area
- 960-KB – 1-MB Memory – System BIOS Area

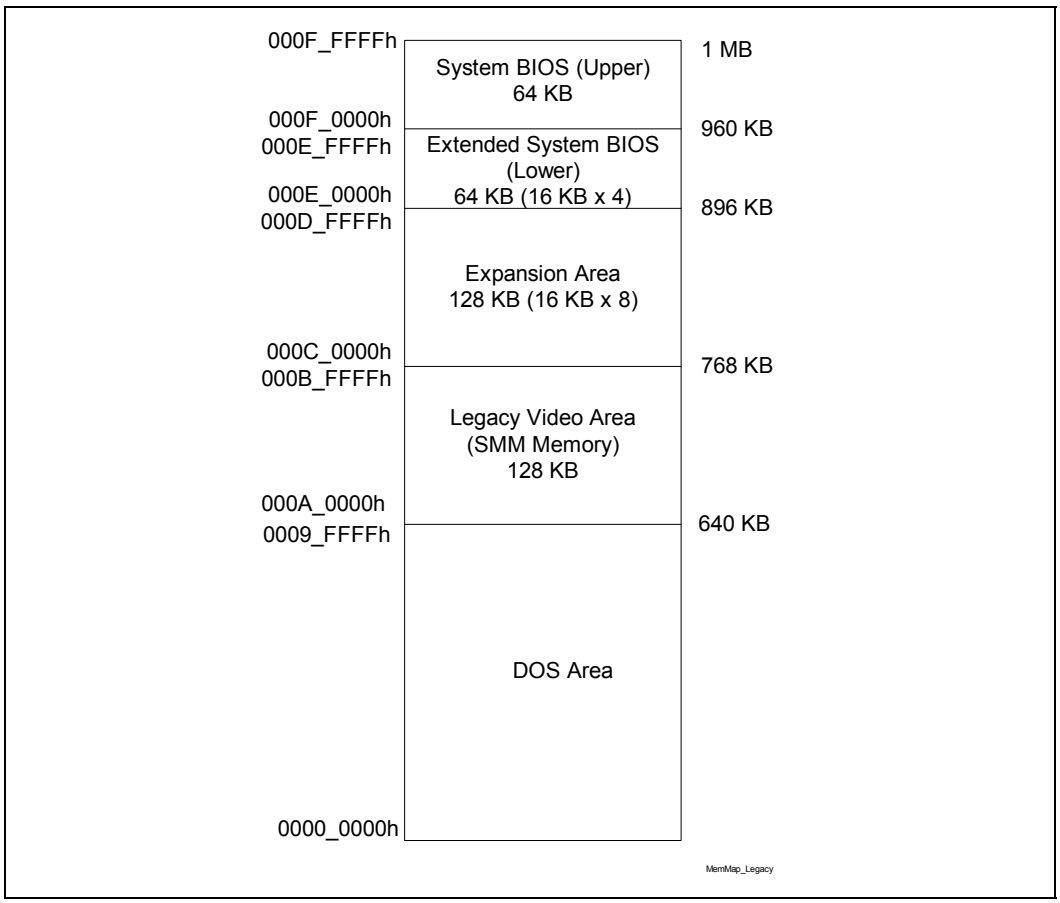


Figure 9-2. Microsoft MS-DOS* Legacy Address Range

9.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

9.1.2 Legacy Video Area (A_0000h–B_FFFFh)

The legacy 128-KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP); see the LAC register (Device 0, offset 97h). This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h–B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A 0000h –000B FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the video buffer area as previously described. PCI Express and DMI-originated cycles to enabled SMM space are not allowed and are considered to be to the video buffer area if IGD (82945G/82945GC/82945GZ GMCH on ly) is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h–B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h – 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

9.1.3 Expansion Area (C_0000h–D_FFFFh)

This 128-KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16-KB segments. Each segment can be assigned one of four read/write states: read only, write only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 9-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h–0C3FFFh	W/R	Add-on BIOS
0C4000h–0C7FFFh	W/R	Add-on BIOS
0C8000h–0CBFFFh	W/R	Add-on BIOS
0CC000h–0CFFFFh	W/R	Add-on BIOS
0D0000h–0D3FFFh	W/R	Add-on BIOS
0D4000h–0D7FFFh	W/R	Add-on BIOS
0D8000h–0DBFFFh	W/R	Add-on BIOS
0DC000h–0DFFFFh	W/R	Add-on BIOS

9.1.4 Extended System BIOS Area (E_0000h–E_FFFFh)

This 64-KB area (000E_0000h–000E_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main memory or to the DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 9-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h–0E3FFFh	W/R	BIOS Extension
0E4000h–0E7FFFh	W/R	BIOS Extension
0E8000h–0EBFFFh	W/R	BIOS Extension
0EC000h–0EFFFFh	W/R	BIOS Extension

9.1.5 System BIOS Area (F_0000h–F_FFFFh)

This area is a single, 64-K segment (000F_0000h–000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the DMI. By manipulating the read/write attributes, the (G)MCH can “shadow” BIOS into main memory. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 9-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h–0FFFFFh	WE RE	BIOS Area

9.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM memory area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI.

However, DMI becomes the default target for processor and DMI-originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB (writeback) or RC (reference clock), it is possible to get IWB cycles targeting DMI. This may occur for DMI originated cycles to disabled PAM regions.

For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is read disabled, the default target for the memory read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

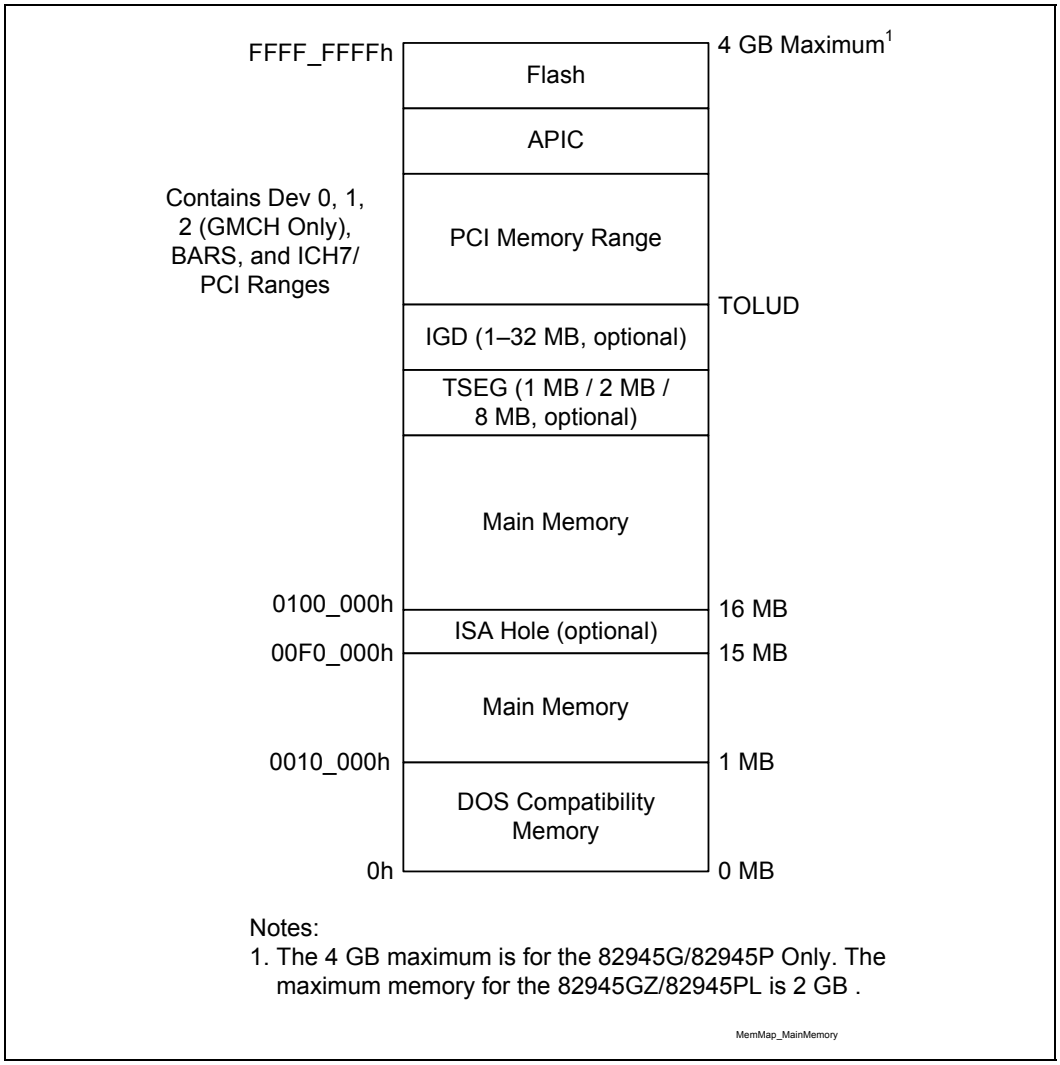
9.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range are forwarded by the (G)MCH to main memory unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

The (G)MCH provides a maximum main memory address decode space of 4 GB (2 GB for the 82945GC/82945GZ /82945PL). The (G)MCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4 GB (2 GB for the 82945GC/82945GZ/82945PL), there will be physical memory that exists yet is non-addressable and therefore unusable by the system.

The (G)MCH does not limit main memory address space in hardware.

Figure 9-3. Main Memory Address Range



9.2.1 ISA Hole (15 MB–16 MB)

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable bit in the LAC register (Device 0, offset 97h). Accesses within this hole are forwarded to the DMI. The range of physical main memory disabled by opening the hole is not remapped to the top of the memory; that physical main memory space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used by validation and customer SV teams for test cards. That is why it is being supported. There is no inherent BIOS request for the 15–16-MB window.

9.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non- processor originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register that is fixed at 1 MB, 2 MB, or 8 MB.

9.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 9-4 details the location and attributes of the regions. How to enable and disable these ranges are described in the (G)MCH Control Register Device 0 (GCC).

Table 9-4. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available system memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM mode only - processor reads	TSEG address range and pre-allocated memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated graphics VGA memory. 1 MB (or 4/8/16/32/64 MB) when IGD is enabled.

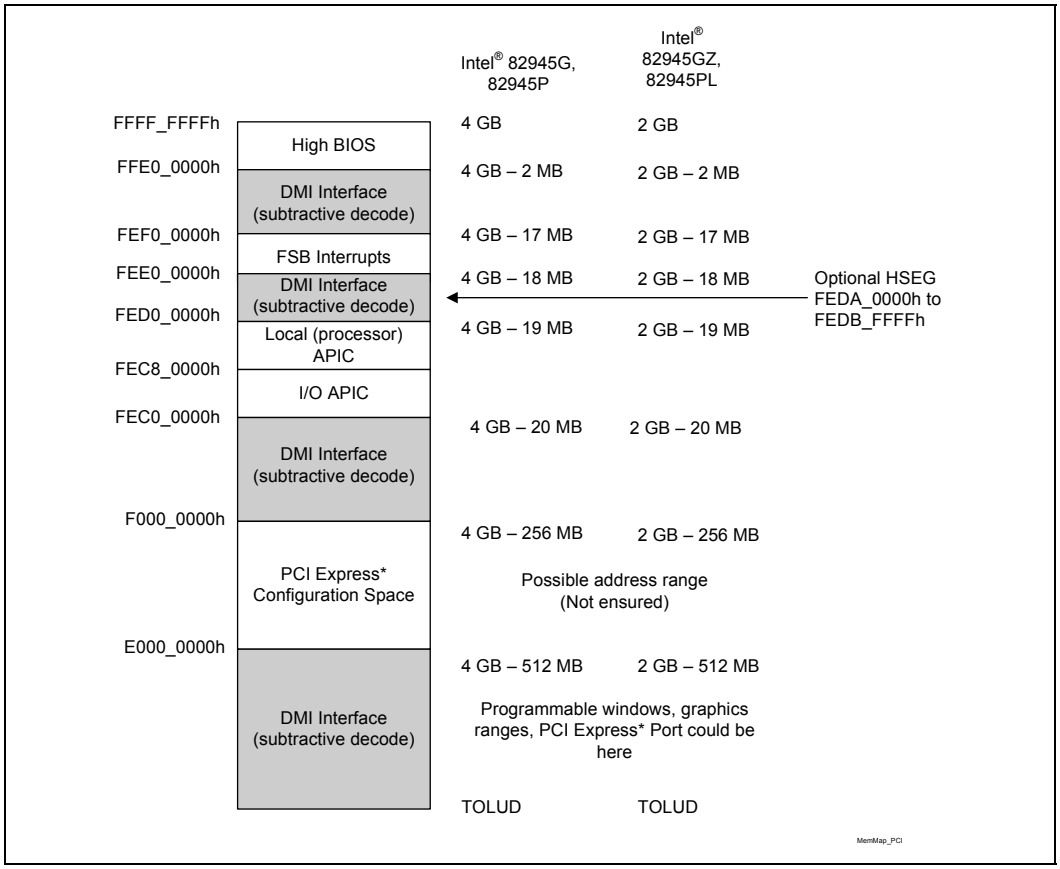
9.3 PCI Memory Address Range (TOLUD – 4 GB)

This address range (see Figure 9-4), from the top of physical memory to 4 GB (2 GB for the 82945GC/82945GZ/82945PL) is normally mapped via the DMI to PCI. Exceptions to this mapping include the BAR memory mapped regions that include:

- EPBAR, MCHBAR, DMIBAR
- The second exception to the mapping rule deals with the PCI Express port
  - Addresses decoded to the PCI Express memory window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
  - Addresses decoded to PCI Express configuration space are mapped based on bus, device, and function number. (PCIEXBAR range).
- The third exception to the mapping rule occurs in an internal graphics configuration (82945G/82945GC/82945GZ GMCH only)
  - Addresses decoded to the graphics memory range. (GMADR range)
  - Addresses decoded to the Graphics Translation Table range (GTTADR range).
  - Addresses decoded to the memory mapped range of the Internal Graphics Device (MMADR range). There is a MMADR range for Device 2, Function 0 and a MMADR range for Device 2, Function 1. Both ranges are forwarded to the Internal Graphics Device.

The exceptions listed above for internal graphics and the PCI Express ports **Must Not** overlap with APCI Configuration, FSB Interrupt space, and High BIOS address range.

Figure 9-4. PCI Memory Address Range



9.3.1 APIC Configuration Space (FEC0_0000h–FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH7 portion of the chipset, but may also exist as stand-alone components.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

9.3.2 HSEG (FEDA_0000h–FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h–000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode writeback cycles that are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All Cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to main memory like an SMM cycle.

9.3.3 FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a memory write to 0FEEx_xxxxh. The (G)MCH will forward this memory write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDY#. This memory write cycle does not go to main memory.

9.3.4 High BIOS Area

The top 2 MB (FFE0_0000h–FFFF_FFFFh) of the PCI memory address range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to the DMI so that the upper subset of this region aliases to the 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB, but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

9.3.5 PCI Express* Configuration Address Space

The device 0 PCIEXBAR register defines the base address for the 256-MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This range will be aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

9.3.6 PCI Express* Graphics Attach (Intel® 82945G/82945GC/82945P/82945PL GMCH Only)

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in the (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base (MBASE) register and Memory Limit (MLIMIT) register.
- The second range is controlled via the Prefetchable Memory Base (PMBASE) register and Prefetchable Memory Limit (PMLIMIT) register.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following inequalities:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

It is essential to support a separate prefetchable range to apply the USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note: The (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

9.3.7 AGP DRAM Graphics Aperture

Unlike AGP4x, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the (G)MCH has no APBASE and APSIZE registers.

9.3.8 Graphics Memory Address Ranges (Intel® 82945G/82945GC/82945GZ GMCH Only)

The GMCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in the GMCH's Device 2 configuration space.

- The Memory Map Base register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base register (GTTADR) is used to access the translation table.

Normally, these ranges will reside above the Top-of-Main-DRAM and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space.

GMADR is a prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

9.4 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. The (G)MCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers' code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

9.4.1 SMM Space Definition

SMM space is defined by its addressed SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped; therefore, the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped, the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. The following table describes three unique address ranges:

- Compatible Transaction Address
- High Transaction Address
- TSEG Transaction Address

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

9.4.2 SMM Space Restrictions

If any of the following conditions are not met, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any PCI devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the operating system as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR TLB **must not** target DRAM from A_0000–F_FFFFh.

9.4.3 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1), the compatible SMM space is effectively disabled. Processor originated accesses to the compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP); otherwise, they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 9-5. SMM Space

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

9.4.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of main memory.

Table 9-6. SMM Control

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	X	X	X	X	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	X	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	X	Invalid	Invalid
1	1	X	X	0	Disable	Disable
1	1	0	X	1	Enable	Enable
1	1	1	X	1	Enable	Disable

9.4.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to access SMM space.

9.4.6 Processor WB Transaction to an Enabled SMM Address Space

Processor writeback transactions (HREQ1# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

9.4.7 SMM Access through GTT TLB (Intel® 82945G/82945GC/82945GZ GMCH Only)

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to memory address 0h with byte enables de-asserted and reads will be routed to memory address 0h.

PCI Express and DMI originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, the Invalid Translation Table Entry Flag (ITTEF) in the ERRSTS register is set.

PCI Express and DMI write accesses through GMADR range will be snooped. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 0h with de-asserted byte enables.

PCI Express and DMI read accesses to the GMADR range are not supported; therefore, users/systems will have no address translation concerns. PCI Express and DMI reads to GMADR will be remapped to address 0h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure they are not in SMM (actually, anything above base of TSEG or 640 KB–1 MB). Thus, they will be invalid and go to address 0h. This is not specific to PCI Express or DMI; it applies to processor or internal graphics engines. Also, since the GMADR snoop would not be directly to the SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 0h.

9.4.8 Memory Shadowing

Any block of memory that can be designated as read only or write only can be “shadowed” into (G)MCH DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM memory. ROM is used as read only during the copy process while DRAM, at the same time, is designated write only. After copying, the DRAM is designated read only so that ROM is shadowed. Processor bus transactions are routed accordingly.

9.4.9 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the (G)MCH contains two internal registers in the processor I/O space: Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. These locations are used to implement a configuration space access mechanism.

The processor allows 64 K+3 bytes to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus and, therefore, provides addressability for 64 K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when the processor bus HA16# address signal is asserted. HA16# is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control are explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are **not** posted. Memory writes to ICH7 or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For Pentium 4 processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The (G)MCH splits this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

9.4.10 PCI Express* I/O Address Mapping

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor-initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

9.4.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

The following are (G)MCH decode rules and cross-bridge address mapping used in this chipset:

- VGAA = 000A_0000 – 000A_FFFF
- MDA = 000B_0000 – 000B_7FFF
- VGAB = 000B_8000 – 000B_FFFF
- MAINMEM = 0100_0000 to TOLUD

9.4.12 Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A_0000h–000B_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to the IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP) in the LAC register (Device 0).

§

10 Functional Description

This chapter describes the (G)MCH interfaces and major functional units.

10.1 Host Interface

The (G)MCH supports the Pentium® 4 processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 200/267 MHz bus clock, the address signals run at 400/533MT/s. The data is quad pumped and an entire 64 B cache line can be transferred in two bus clocks. At 200/267 MHz bus clock, the data signals run at 800/1066MT/s for a maximum bandwidth of 10.7 GB/s.

10.1.1 FSB IOQ Depth

The Scalable bus supports up to 12 simultaneous outstanding transactions.

10.1.2 FSB OOQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

10.1.3 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die. Also, approximately 2.8 pf (fast) – 3.3 pf (slow) per pad of on die capacitance will be implemented to provide better FSB electrical performance.

10.1.4 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV0#	HD15:0#
HDINV1#	HD31:16#
HDINV2#	HD47:32#
HDINV3#	HD63:48#

When the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINVx# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the (G)MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

10.1.4.1 APIC Cluster Mode Support

This is required for backwards compatibility with existing software, including various operating systems. As one example, beginning with Microsoft Windows 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

The (G)MCH supports three types of interrupt re-direction:

- Physical
- Flat-Logical
- Clustered-Logical

10.2 System Memory Controller

The system memory controller supports two styles of memory organization (Interleaved and Asymmetric). Rules for populating DIMM slots are included in this section. Sample memory organizations are provided in Table 10-1 and Table 10-2.

Note: The 82945G/82945P (G)MCH maximum memory size is 4 GB.

Note: The 82945GC/82945GZ/82945PL (G)MCH maximum memory size is 2 GB.

Table 10-1. Sample System Memory Organization with Interleaved Channels

Rank	Channel A Population	Cumulative Top Address in Channel A	Channel B Population	Cumulative Top Address in Channel B
Rank 3	0 MB	2560 MB	0 MB	2560 MB
Rank 2	256 MB	2560 MB	256 MB	2560 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

Table 10-2. Sample System Memory Organization with Asymmetric Channels

Rank	Channel A Population	Cumulative Top address in Channel A	Channel B Population	Cumulative Top Address in Channel B
Rank 3	0 MB	1280 MB	0 MB	2560 MB
Rank 2	256 MB	1280 MB	256 MB	2560 MB
Rank 1	512 MB	1024 MB	512 MB	2304 MB
Rank 0	512 MB	512 MB	512 MB	1792 MB

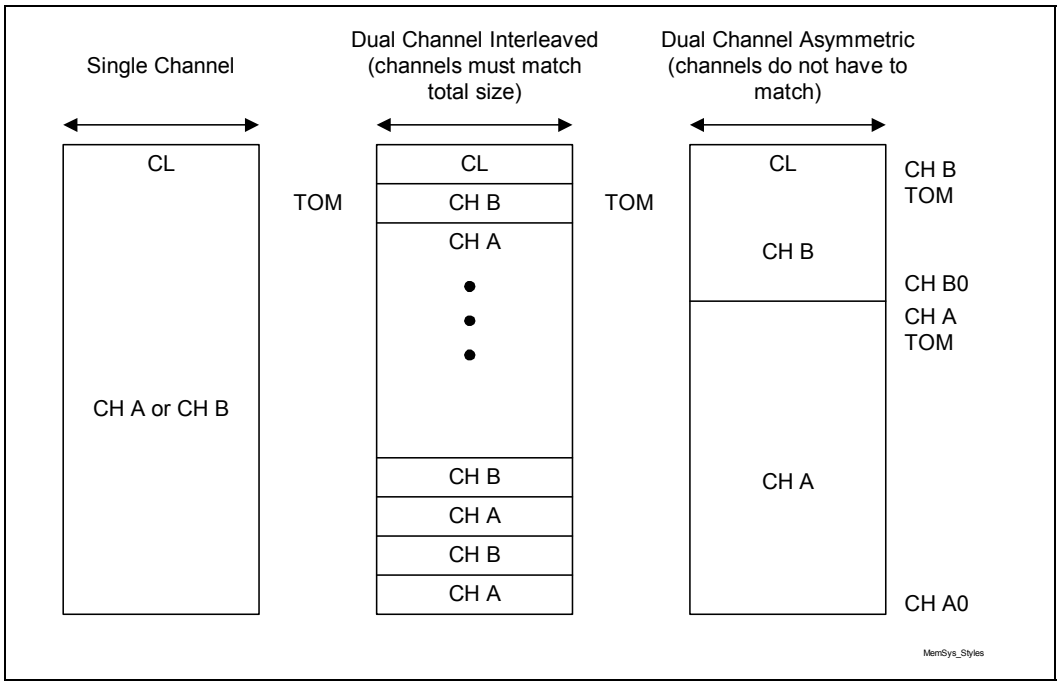
Interleaved Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64 byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. The drawbacks of Interleaved Mode are that the system designer must populate both channels of memory such that they have equal capacity, but the technology and device width may vary from one channel to the other. Refer to Figure 10-1 for further clarification.

Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A; then, addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case. Refer to Figure 10-1 for further clarification.

Figure 10-1. System Memory Styles



10.2.1 System Memory Configuration Registers Overview

The configuration registers located in the PCI configuration space of the (G)MCH control the system memory operation. Following is a brief description of configuration registers.

- **DRAM Rank Boundary (CxDRBy):** The x represents a channel, either A or B. The y represents a rank, 0 through 3. DRB registers define the upper addresses for a rank of DRAM devices in a channel. When the (G)MCH is configured in asymmetric mode, each register represents a single rank. When the (G)MCH is configured in a dual interleaved mode, each register represents a pair of corresponding ranks in opposing channels. There are 4 DRB registers for each channel.
- **DRAM Rank Architecture (CxDRAy):** The x represents a channel, either A or B. The y represents a rank, 0 through 3. DRA registers specify the architecture features of each rank of devices in a channel. The only architecture feature specified is page size. When the (G)MCH is configured in asymmetric mode, each DRA represents a single rank in a single channel. When (G)MCH is configured in a dual-channel interleaved mode, each DRA represents a pair of corresponding ranks in opposing channels. There are 4 DRA registers per channel. Each requires only 3 bits, so there are two DRAs packed into a byte.
- **Clock Configuration (CLKCFG):** CLKCFG specifies DRAM frequency. The same clock frequency will be driven to all DIMMs.
- **DRAM Timing (CxDRT1):** The x represents a channel, A or B represented by 0 and 1 respectively. The DRT Register defines the timing parameters for all devices in a channel. BIOS programs this register with “least common denominator” values after reading the SPD registers of each DIMM in the channel**.**
- **DRAM Control (CxDRC0):** The x represents a channel, A or B represented by 0 and 1 respectively. DRAM refresh mode, rate, and other controls are selected here.

10.2.2 DRAM Technologies and Organization

"Single sided" below is a logical term referring to the number of chip selects attached to the DIMM. A real DIMM may put the components on both sides of the substrate, but be logically indistinguishable from single-sided DIMM if all components on the DIMM are attached to the same chip select signal.

- x8 means that each component has 8 data lines.
- x16 means that each component has 16 data lines

All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices.

For DDR2:

400 MHz (PC2 3200)

Non-ECC

Version A = Single sided x8

Version B = Double sided x8

Version C = Single sided x16

533 MHz (PC 4300)

Non-ECC

Version A = Single sided x8

Version B = Double sided x8

Version C = Single sided x16

667 MHz (PC 5300) (82945G/82945GC/82945P (G)MCH Only)
- Non-ECC
  - Version C = Single sided x16
  - Version D = Single sided x8
  - Version E = Double sided x8

There is No support for DIMMs with different technologies or capacities on opposite sides of the same DIMM. If one side of a DIMM is populated, the other side is either identical or empty.

Supported components include:

For DDR2 at 533 MHz (PC4300) and 667 MHz (PC5300) (667 MHz on 82945G/82945GC/82945P (G)MCH Only)
- 256-Mb technology
  - 32-M cells x8 data bits/cell
    - 1-K columns
    - 4 banks
    - 8-K rows
    - Each component has a 1-KB page.
    - One DIMM has 8 components resulting in an 8-KB page.
    - The capacity of one rank is 256 MB.
  - 16-M cells x16 data bits/cell
    - 512 columns
    - 4 banks
    - 8-K rows
    - Each component has a 1-KB page.
    - One DIMM has 4 components resulting in a 4-KB page.
    - The capacity of one rank is 128 MB.
- 512-Mb technology
  - 64-M cells x8 data bits/cell
    - 1K columns
    - 4 banks
    - 16K rows
    - Each component has a 1-KB page.
    - One DIMM has 8 components resulting in an 8-KB page.
    - The capacity of one rank is 512 MB.
  - 32-M cells x16 data bits/cell
    - 1-K columns
    - 4 banks
    - 8-K rows
    - Each component has a 2-KB page.
    - One DIMM has 4 components resulting in an 8-KB page.
    - The capacity of one rank is 256 MB.

1-Gb technology
128-M cells x8 data bits/cell
1-K columns
8 banks
16-K rows
Each component has a 1-KB page.
One DIMM has 8 components resulting in an 8-KB page.
The capacity of one rank is 1 GB.
64-M cells x16 data bits/cell
1-K columns
8 banks
8-K rows
Each component has a 2-KB page.
One DIMM has 4 components resulting in an 8-KB page.
The capacity of one rank is 512MB.

The DRAM sub-system supports single or dual channels, 64b wide per channel. There can be a maximum of 4 ranks populated (2 Double Sided DIMMs) per channel. Mixed mode DDR DS-DIMMs (x8 and x16 on the same DIMM) are not supported (not validated)

By using 1Gb technology, the largest memory capacity is 8 GB (16K rows * 1K columns * 1 cell/(row * column) * 8 b/cell * 8 banks/device * 8 devices/rank * 4 ranks/channel * 2 channel *1M/(K*K) * 1G/1024M * 1B/8b = 8 GB). Using 8 GB of memory is only possible in Interleaved mode with all ranks populated at maximum capacity. The Intel 82945G GMCH and 82894P MCH are limited to 4 GB of address space. Any memory in the system beyond 4 GB cannot be addressed and should not be populated due to the additional loading it places on the memory subsystem.

By using 256Mb technology, the smallest memory capacity is 128 MB (8K rows * 512 columns * 1 cell/(row * column) * 16b/cell * 4 banks/device * 4 devices/rank * 1 rank * 1M/1024K * 1B/8b = 128 MB)

10.2.2.1 Rules for Populating DIMM Slots

- In all modes, the frequency of system memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs.
- In the single channel mode, any DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, do not populate the unused channel.
- In dual channel asymmetric mode, any DIMM slot may be populated in any order.
- In dual channel interleaved mode, any DIMM slot may be populated in any order, but the total memory in each channel must be the same.

10.2.2.2 System Memory Supported Configurations

The (G)MCH supports the 256 Mbit, 512 Mbit and 1 Gbit technology based DIMMs from Table 10-3.

Table 10-3. DDR2 DIMM Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256Mbit	16M X 16	13	9	2	4K	128 MB
256Mbit	32M X 8	13	10	2	8K	256 MB
512Mbit	32M X 16	13	10	2	8K	256 MB
512Mbit	64M X 8	14	10	2	8K	512 MB
1Gbit	64M X 16	13	10	3	8K	512 MB
1Gbit	128M X 8	14	10	3	8K	1 GB

10.2.2.3 Main Memory DRAM Address Translation and Decoding

Table 10-4 and Table 10-5 specify the host interface to memory interface address multiplex for the (G)MCH. Refer to the details of the various DIMM configurations as described in Table 10-3. The address lines specified in the column header refer to the host (processor) address lines.

Table 10-4. DRAM Address Translation (Single Channel/Dual Asymmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB						r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB				r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x16	8i	8 KB	512 MB				r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB			R13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

NOTES:

1. b – 'bank' select bit
2. c – 'column' address bit
3. r – 'row' address bit

Table 10-5. DRAM Address Translation (Dual Channel Interleaved Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB					R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB				r12	R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB				r12	R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB			r13	r12	R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x16	8i	4 KB	512 MB			r11	r12	R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB		r13	r11	r12	R10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0

NOTES:

1. b – 'bank' select bit
2. c – 'column' address bit
3. h – channel select bit
4. r – 'row' address bit

10.2.3 DRAM Clock Generation

The (G)MCH generates three differential clock pairs for every supported DIMM. There are a total of 6 clock pairs driven directly by the (G)MCH to 2 DIMMs per channel.

10.2.4 Suspend to RAM and Resume

When entering the Suspend to RAM (STR) state, the SDRAM controller will flush pending cycles and then enter all SDRAM rows into self refresh. In STR, the CKE signals remain Low so the SDRAM devices will perform self-refresh.

10.2.5 DDR2 On Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each SDQ_x, SDM_x, SDQS_x, and SDQS_x# signal for x8 and x16 configurations via the SODT_x control signals. The SODT_x feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the SDQ_x, SDM_x, SDQS_x, and SDQS_x# signals to be located inside the DRAM devices themselves instead of on the motherboard. The (G)MCH drives out the required SODT_x signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM rank to enable or disable their termination resistance.

10.3 PCI Express* (Intel® 82945G/82945GC/ 82945P/82945PL (G)MCH Only)

Refer to Section 1.3.4 for list of PCI Express features, and the PCI Express specification for further details. Refer to Section 10.4 for additional information on the features/capabilities of the multiplexed PCI Express interface and SDVO ports.

The (G)MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in device 1 configuration space and two Root Complex Register Blocks (RCRBs). The DMI RCRB contains registers for control of the ICH7 attach ports.

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 Gb/s/direction that provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

10.3.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

10.3.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

10.3.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.4 Intel® Serial Digital Video Output (SDVO) (Intel® 82945G/82945GC/82945GZ GMCH Only)

The 82945G/82945GC GMCH SDVO ports are multiplexed with the PCI Express x16 interface. The 82945GZ GMCH SDVO ports are not multiplexed. The Intel® SDVO port is the second generation of digital video output from compliant Intel GMCHs. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant on the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, a SDVO port will transmit display data in a high speed, serial format across differential AC coupled signals. A SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

10.4.1 Intel® SDVO Capabilities

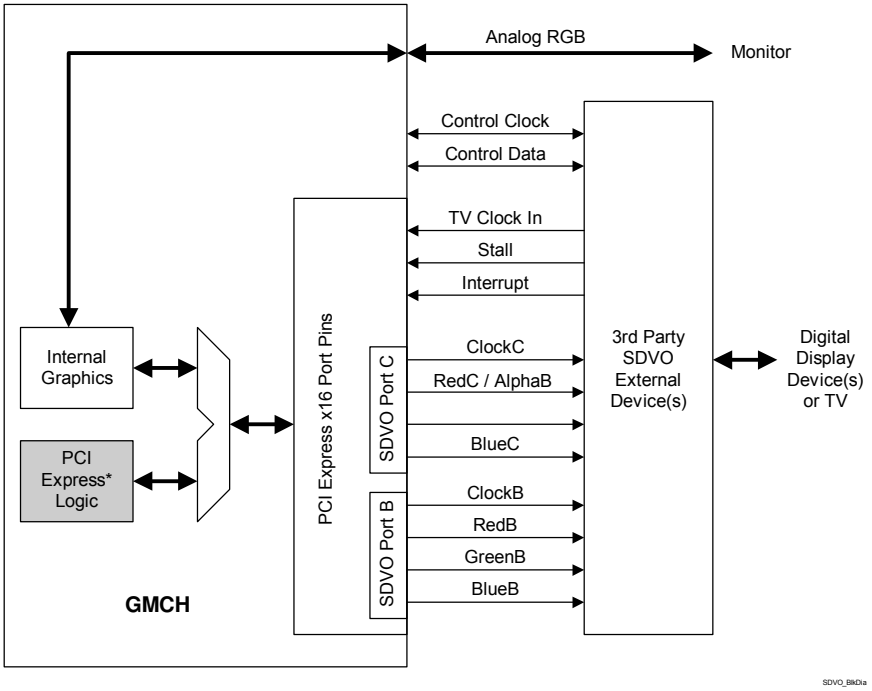
SDVO ports can support a variety of display types including LVDS, DVI, Analog CRT, TV-Out and external CE type devices. The GMCH uses an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

The internal graphics controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface. When an external x16 PCI Express graphics accelerator is not in use, an ADD2 card may be plugged into the x16 connector or if a x16 slot is not present, the SDVO(s) may be located ‘down’ on the motherboard to access the multiplexed SDVO ports and provide a variety of digital display options.

The ADD2/ADD2+ card is designed to fit in a x16 PCI Express connector. The ADD2/ADD2+ card can support one or two devices. If a single channel SDVO device is used, it should be attached to the channel B SDVO pins. The ADD2 card can support two separate SDVO devices when the interface is in Dual Independent or Dual Simultaneous Standard modes. The ADD2+ card adds Video in capabilities.

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and GMCH. The SDVO control clock and data provide similar functionality to I^2C. However, unlike I^2C, this interface is intended to be point-to-point (from the GMCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface.

Figure 10-2. SDVO Conceptual Block Diagram



Note: PCI Express ports are only on the 82945G/82945GC GMCH. On the 82945GZ, these pins are dedicated SDVO pins.

10.4.2 Intel® SDVO Modes

The port can be dynamically configured in several modes:

- **Standard**. This mode provides baseline SDVO functionality. It supports pixel rates between 25 MP/s and 200 MP/s. It uses three data pairs to transfer RGB data.
- **Extended**. This mode adds Alpha support to data stream. It supports pixel rates between 25 MP/s and 200 MP/s. This mode uses four data channels and is only supported on SDVOB. It leverages channel C (SDVOC) Red pair as the Alpha pair for channel B (SDVOB).
- **Dual Standard**. This mode uses standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports pixel rates between 25 MP/s and 200 MP/s.
  - Dual Independent Standard. In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVOB will not be the same as the data stream across SDVOC.
  - Dual Simultaneous Standard. In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVOB will be the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s). Since this mode uses just a single data stream, it uses a single pixel pipeline within the GMCH.

10.4.3 PCI Express* and Internal Graphics Simultaneous Operation (Intel® 82945G/82945GC GMCH Only)

10.4.3.1 Standard PCI Express* Cards and Internal Graphics

BIOS control of simultaneous operation is needed to ensure the PCI Express is configured appropriately.

10.4.3.2 ADD2+ Cards (Concurrent SDVO and PCI Express*)

SDVO lane reversal is supported. This functionality allows current SDVO ADD2 cards to work in current ATX and BTX systems instead of requiring a separate card. The 82945G GMCH allows SDVO and PCI Express to operate concurrently on the PCI Express port. The card that plugs into the x16 connector in this case is called an ADD2+ card. It uses 4 or 8 lanes for SDVO and up to 8 lanes of standard PCI Express.

Note: The only supported PCI Express width when SDVO is present is x1.

Note: The 82945GC supports only ADD2 cards and not ADD2+. The 945GC does not support concurrent SDVO and PCI Express*)

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing is always about the axis between PCI Express lanes 7 and 8.

Table 10-6. Concurrent SDVO / PCI Express* Configuration Strap Controls

Config #	Description	Slot Reversed Strap	SDVO Present Strap	SDVO/PCI Express* Concurrent Strap
1	PCI Express not reversed	—	—	—
2	PCI Express Reversed	Yes	—	—
3	SDVO (ADD2) not reversed	—	Yes	—
4	SDVO (ADD2) Reversed	Yes	Yes	—
5	SDVO and PCI Express (ADD2+) not reversed	—	Yes	Yes
6	SDVO and PCI Express (ADD2+) Reversed	Yes	Yes	Yes

NOTES:
1. The Configuration #s refer to the following figures (no intentional relation to validation configurations).
2. Configurations 4, 5, and 6 are new for the 82945G GMCH (required addition of SDVO/PCI Express Concurrent Strap).

Figure 10-3. Concurrent SDVO / PCI Express* Non-Reversed Configurations

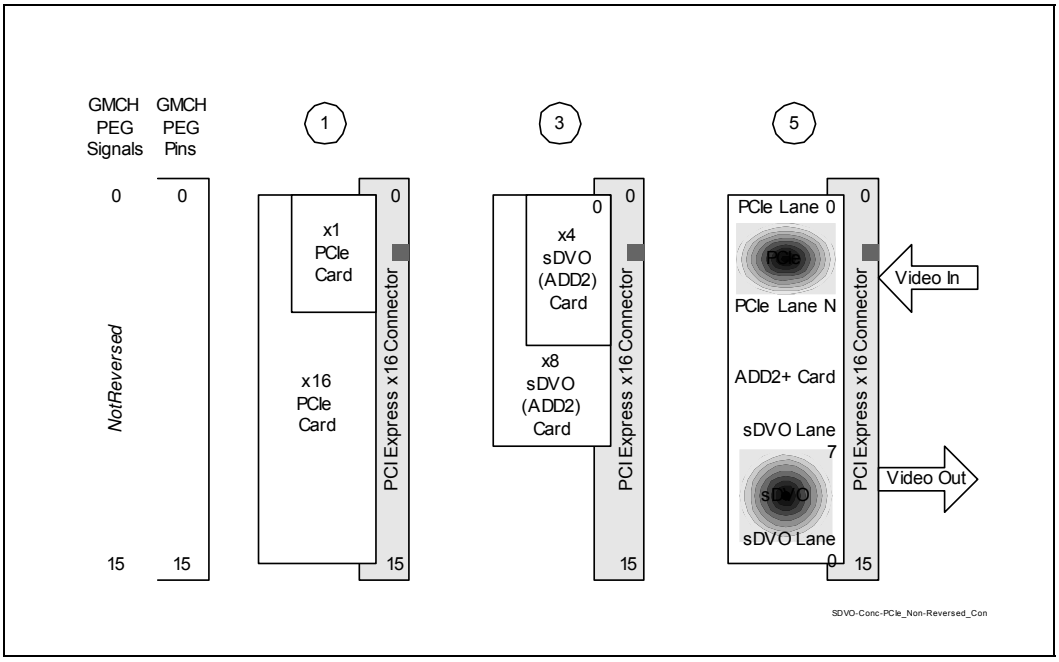


Figure 10-4. Concurrent SDVO / PCI Express* Reversed Configurations

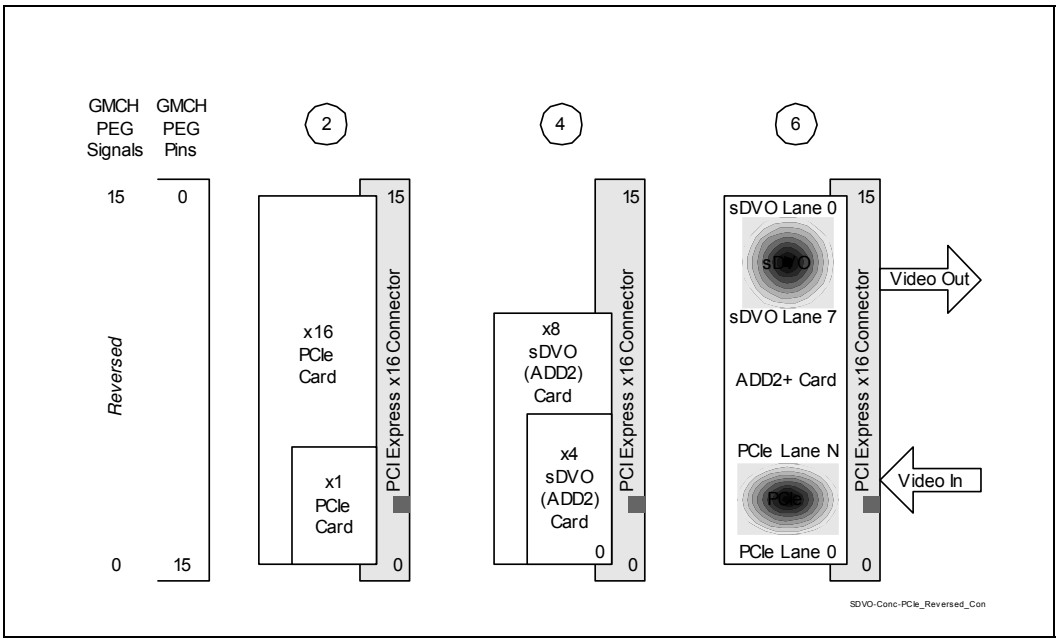
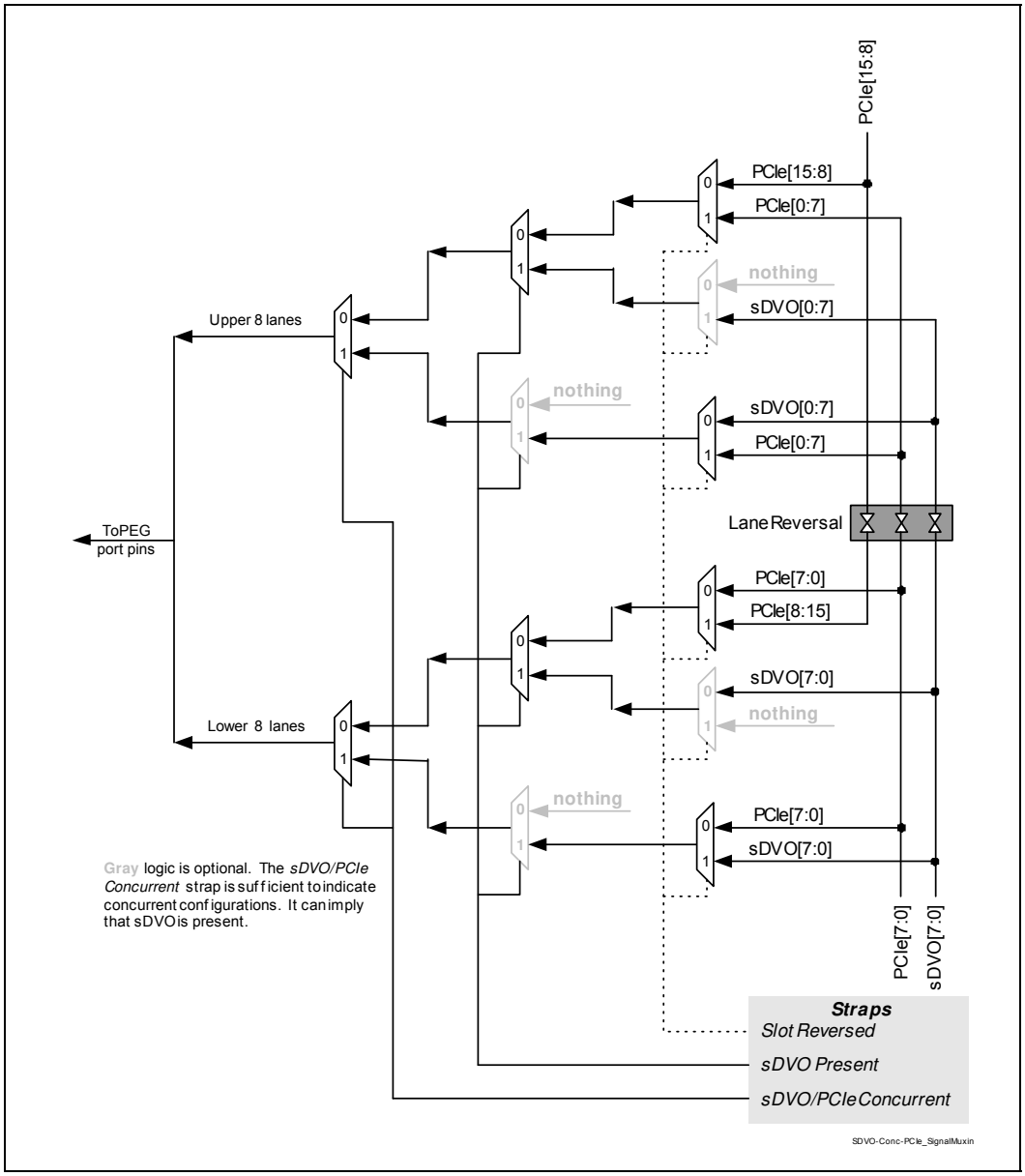


Figure 10-5. Concurrent SDVO / PCI Express* Signal Multiplexing



10.5 Integrated Graphics Device (Intel® 82945G/82945GC/82945GZ GMCH Only)

The major components in the Integrated Graphics Device (IGD) are the engines, planes, pipes and ports. The GMCH has a 3D/2D instruction processing unit to control the 3D and 2D engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The output of the engines are surfaces sent to memory that are then retrieved and processed by the GMCH planes.

The GMCH contains a variety of planes, such as display, overlay, cursor and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The GMCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe. The GMCH contains three display ports; 1 analog (DAC) and two digital (SDVO ports B and C). The ports will be explained in more detail later in this section .

The entire IGD is fed with data from its memory controller. The GMCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR2 533), the rest of the IGD will also be affected.

The rest of this section will focus on explaining the IGD components, their limitations, and dependencies.

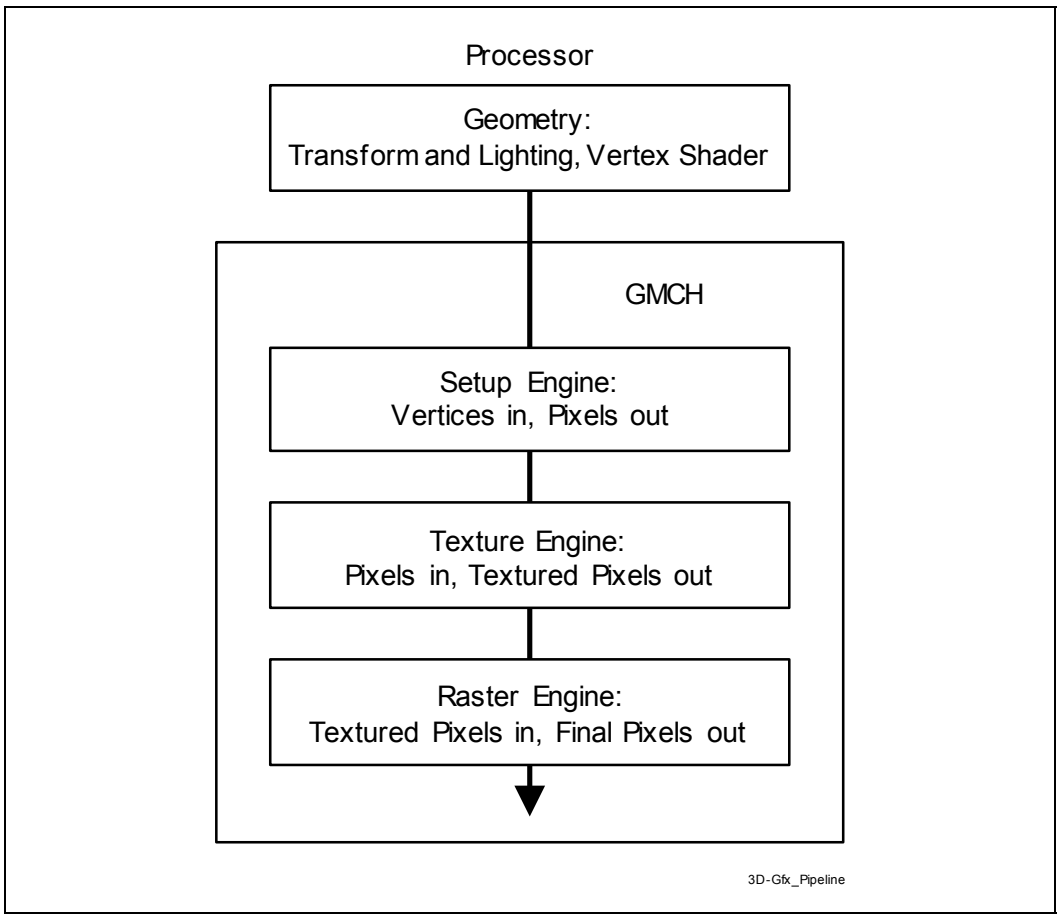
10.5.1 3D Graphics Pipeline

The GMCH graphics is the next step in the evolution of integrated graphics. In addition to running the graphics engine at 400 MHz, the GMCH graphics has four pixel pipelines that provide a 1.3 GB/s fill rate that enables an excellent consumer gaming experience.

The 3D graphics pipeline for the GMCH has a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. The 3D graphics pipeline is divided into four major stages: geometry processing, setup (vertex processing), texture application, and rasterization.

The GMCH graphics is optimized for use with current and future Intel® processors for advance software based transform and lighting techniques (geometry processing) as defined by the Microsoft Direct X* API. The other three stages of 3D processing are handled on the integrated graphics device. The setup stage is responsible for vertex processing; converting vertices to pixels. The texture application stage applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environmental affects to produce the final pixel value. From the rasterization stage, the final pixel value is written to the frame buffer in memory so it can be displayed.

Figure 10-6. Integrated 3D Graphics Pipeline



10.5.2 3D Engine

The 3D engine on the GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

10.5.3 4X Faster Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH maintains sub-pixel accuracy. For the 82945G/82945GC/82945GZ GMCH, it was redesigned to run at 1 cycle/attribute.

10.5.3.1 3D Primitives and Data Formats Support

The 3D primitives rendered by the GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans, and polygons. In addition to this, the GMCH supports the Microsoft DirectX Flexible Vertex Format (FVF) that enables the application to specify a variable length parameter list. This obviates the need for sending unused information to the hardware. Strips, Fans, and Indexed Vertices, as well as FVF, improve the vertex rate delivered to the setup engine significantly.

10.5.3.2 Pixel Accurate “Fast” Scissoring and Clipping Operation

The GMCH supports 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the scissor rectangle, avoiding processing pixels that fall outside the rectangle. The GMCH’s clipping and scissoring in hardware reduce the need for software to clip objects, and thus improve performance. During the setup stage, the GMCH clips objects to the scissor window.

A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle needs to be pixel accurate, and independent of line and point width. The GMCH supports a single scissor box rectangle that can be enabled or disabled. The rectangle is defined as an Inclusive box. Inclusive is defined as “draw the pixel if it is inside the scissor rectangle”.

10.5.3.3 Depth Bias

The GMCH supports source depth biasing in the setup engine The depth bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The depth bias value is added to the z or w value of the vertices. This is used for coplanar polygon priority. If two polygons are to be rendered that are coplanar, due to the inherent precision differences induced by unique x, y, and z values, there is no assurance of which polygon will be closer or farther. By using depth bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

10.5.3.4 Backface Culling

As part of the setup, the GMCH discards polygons from further processing, if they are facing away from or towards the user's viewpoint. This operation, referred to as "Backface Culling" is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

10.5.3.5 Scan Converter

Working on a per-polygon basis, the scan converter uses the vertex and edge information to identify all pixels affected by features being rendered.

10.5.3.6 Pixel Rasterization Rules

The GMCH supports both OpenGL and D3D pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry will be used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

10.5.3.7 Pixel Pipeline

The pixel pipeline function combines, for each pixel, the interpolated vertex components from the scan conversion function, texel values from the texture samplers, and the pixel's current values from the color and/or depth buffers. This combination is performed by a programmable pixel shader engine, followed by a pipeline for optional pixel operations performed in a specific order. The result of these operations can be written to the color and depth buffers.

10.5.3.8 Texture Samplers

A texture sampler takes a texture coordinate and its partial derivatives, access (samples) texture maps, applies filtering and other operations to the texel samples, and feeds the resultant per-pixel texel outputs to pixel shader registers. Sixteen texture samplers are supported.

10.5.3.9 2D Functionality

The stretch Block Level Transfer (BLT) function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

10.5.4 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, and bilinear interpolation), and YUV-to-RGB conversions.

10.5.4.1 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

10.5.4.2 Texture Formats and Storage

The GMCH supports up to 32 bits of color for textures.

10.5.4.3 Texture Decompression

DirectX supports texture compression to reduce the bandwidth required to deliver textures. As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism for compressing textures. Texture decompression formats supported include DXT1, DXT2, DXT3, DXT4, DXT5, and FXT1.

10.5.4.4 Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For " linear " texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

10.5.4.5 Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns that occur as a result of a very small number of pixels available on screen to contain the data of a high-resolution texture map. More subtle effects are observed in animation, where very small primitives blink in and out of view.

10.5.4.6 Texture Map Filtering

The GMCH supports many texture mapping modes. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. Textures need not be square. Included in the texture processor is a texture cache that provides efficient MIP-mapping.

The GMCH supports 7 types of texture filtering:

- Nearest (aka Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present).
- Linear (aka Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present).
- Nearest MIP Nearest (aka Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel is used.
- Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
- Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel is selected. The final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.
- Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used to minimize the visibility of LOD transitions across the polygon.
- Anisotropic MIP Nearest (Anisotropic Filtering): This is used if many LODs are present. The nearest LOD-1 level will be determined for each of four sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.

Both D3D (DirectX 6.0) and OGL (Revision 1.1) allow support for all these filtering modes.

10.5.4.7 Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP Maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

10.5.4.8 Pixel Shader

DX9 PS 2.0-compliant pixel shader. This includes perspective-correct diffuse and specular color interpolation via internal use of texcoords. In addition, there is support for non-perspective-correct texture coordinates as well as support for fog parameter separate from specular alpha.

10.5.4.9 Cube Map Textures

Multiple texture map surfaces arranged into a cubic environment map are supported. There is also support for CLAMP and CUBE texture address mode for Cubemaps.

10.5.4.10 4x4 Texture Filtering Includes Cube Maps

Compressed Cube Map Mip-amps

New format support for compressed cube maps that allows each mip/face to exist in its own compression block.

Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing processor load. There are several methods to generate environment maps (such as, spherical, circular, and cubic). The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic mapping requires a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection, or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

10.5.5 Raster Engine

The raster engine is where the color data (such as, fogging, specular RGB, texture map blending, etc.) is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the texture engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted that determine whether the frame and depth buffers will be updated with the new pixel values.

10.5.5.1 Texture Map Blending

Multiple textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports using a texture coordinate set to access multiple texture maps. State variables in multiple texture are bound to texture coordinates, texture map, or texture blending.

10.5.5.2 Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated “specular RGB” attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices that apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, RGB values from the output of the map blending are added to values for RS, GS, and BS on a component by component basis.

10.5.5.3 Color Shading Modes

The raster engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex’s attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

OpenGL and D3D use a different vertex to select the flat shaded color. This vertex is defined as the “provoking vertex”. In the case of strips/fans, after the first triangle, attributes on every vertex that define a primitive are used to select the flat color of the primitive. A state variable is used to select the “flat color” prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has a different value.

All the attributes can be selected independently from one of the shading modes by setting the appropriate value state variables.

10.5.5.4 Color Dithering

Color dithering helps to hide color quantization errors. Color dithering takes advantage of the human eye’s propensity to “average” the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5- or 6- bit components by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed on the components.

10.5.5.5 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects (such as low visibility conditions in flight simulator-type games). It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (fewer polygons); thereby, improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance. The higher the density the lower the visibility for distant objects.

There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon

to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations: vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit.

10.5.5.6 Alpha Blending (Frame Buffer)

Alpha blending adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color (RS, GS, BS) and alpha (AS) component with a destination pixel color (RD, GD, BD) and alpha (AD) component. For example, alpha blending could be used where there is glass surface on top (source) of a red surface (destination) allowing much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.

10.5.5.7 Microsoft Direct X* API and SGI OpenGL* Logic Ops

Both APIs provide a mode to use bitwise ops in place of alpha blending. This is used for rubber-banding (i.e., draw a rubber band outline over the scene using an XOR operation). Drawing it again restores the original image without having to do a potentially expensive redraw.

10.5.5.8 Color Buffer Formats: 8-, 16-, or 32-bits per Pixel (Destination Alpha)

The raster engine supports 8-bit, 16-bit, and 32-bit color buffer formats. The 8-bit format is used to support planar YUV420 format, which is used only in motion compensation and arithmetic stretch format. The bit format of color and Z will be allowed to mix.

The GMCH supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer of the GMCH contains at least two hardware buffers: the front buffer (display buffer) and the back buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing. This also speeds up the display process over a single buffer. Additionally, triple back buffering is also supported. The instruction set of the GMCH provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

10.5.5.9 Depth Buffer

The raster engine will be able to read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values, as opposed to only 64 K with a 16-bit Z buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when W (or eye-relative Z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, allowing applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point.

The GMCH supports a flexible format for the floating-point W buffer, wherein the number of exponent bits is programmable. This allows the driver to determine variable precision as a function of the dynamic range of the W (screen-space Z) parameter.

The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

10.5.5.10 Stencil Buffer

The raster engine will provide 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects (such as, decals, outlining, shadows and constructive solid geometry rendering).

10.5.5.11 Projective Textures

The GMCH supports two, simultaneous projective textures at full rate processing, and four textures at half rate. These textures require three floating point texture coordinates to be included in the Flexible Vertex Format (FVF). Projective textures enable special effects such as projecting spot light textures obliquely onto walls, etc.

10.5.6 2D Engine

The GMCH contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions (such as, Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs) make use of the 3D renderer.

10.5.6.1 GMCH VGA Registers

The 2D registers are a combination of registers defined by IBM when the Video Graphics Array (VGA) was first introduced and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

10.5.6.2 Logical 128-bit Fixed BLT and 256 Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit GMCH BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The GMCH can perform hardware clipping during BLTs.

10.5.7 Video Engine

10.5.7.1 Hardware Motion Compensation

The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward, or bidirectionally) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements motion compensation and subsequent steps in hardware. Performing motion compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The motion compensation functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally supports the following input format:

- YUV420 planar

4-Channel MPEG YUV

Improvements allow hardware MC output rate to be quadrupled.

10.5.7.2 Sub-Picture Support

Sub-picture is used for two purposes; one is Subtitles for movie captions, etc. (which are superimposed on a main picture), and the other is Menus used to provide some visual operation environments for the user of a content player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called "Subtitle" because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications; for example, as Subtitles in different languages or other information to be displayed.

There are two kinds of menus; the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title Menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can use four methods when dealing with sub-pictures. This flexibility enables the GMCH to work with all sub- picture formats.

10.5.8 Planes

A plane consists of a rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

10.5.8.1 Cursor Plane

The cursor planes are one of the simplest display planes. With a few exceptions, the cursor plan has a fixed size of 64x64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.

10.5.8.2 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external video capture device) or data delivered by the processor, with the graphics data on the screen. The source data can be mirrored horizontally or vertically or both.

Source/Destination Color Keying/ChromaKeying

Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color keying/ChromaKeying can be used to handle occluded portions of the overlay window on a pixel-by-pixel basis that is actually an underlay. Destination ChromaKeying would only be used for YUV passthrough to TV. Destination color keying supports a specific color (8- or 15-bit) mode as well as 32-bit alpha blending.

Source color keying/ChromaKeying is used to handle transparency based on the overlay window on a pixel-by-pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

Gamma Correction

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

YUV-to-RGB Conversion

The format conversion can be bypassed in the case of RGB source data. The format conversion assumes that the YUV data is input in the 4:4:4 format and uses the full range scale.

Maximum Resolution and Frequency

The maximum frequency supported by the overlay logic is 180 MHz. The maximum resolution is dependent on a number of variables.

Deinterlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.

10.5.8.3 Advanced Deinterlacing and Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to deinterlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as Weaving. This is the best solution for images with little motion; however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or "Bob" interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion; however, it will have reduced spatial resolution in areas that have no motion and introduces jaggies. In absence of any other deinterlacing, these form the baseline and are supported by the GMCH.

Scaling Filter and Control

The scaling filter has three vertical taps and five horizontal taps. Arbitrary scaling (per pixel granularity) for any video source (YUV422 or YUV420) format is supported.

The overlay logic can scale an input image up to 1600X1200 with no major degradation in the filter used as long as the maximum frequency limitation is met. Display resolution and refresh rate combinations where the dot clock is greater than the maximum frequency require the overlay to use pixel replication.

10.5.9 Pipes

The display consists of two pipes. The pipes can operate in a single-wide or "double-wide" mode at 2x graphics core clock though they are effectively limited by the respective display port. The display planes and the cursor plane will provide a "double wide" mode to feed the pipe.

10.5.9.1 Clock Generator Units (DPLL)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25–400 MHz. Accuracy for VESA timing modes is required to be within ±0.5%.

The DPLL can take a reference frequency from the external reference input (DREFCLKN/P) or the TV clock input (SDVO_TVCLKIN+/-).

10.6 Display Interfaces (Intel® 82945G/82945GC/82945GZ GMCH Only)

The GMCH has three display ports; one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure, and/or determine the capabilities of an external device.

The GMCH has one dedicated display port; the analog port. SDVO ports B and C are multiplexed with the PCI Express graphics interface and are not available if an external PCI Express graphics

device is in use. When a system uses a PCI Express graphics connector, SDVO ports B and C can be used via an ADD2/ADD2+ (Advanced Digital Display 2) card. Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

- The GMCH's analog port uses an integrated 400 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.
- The GMCH's SDVO ports are each capable of driving a 200-MP pixel rate. Each port is capable of driving a digital display up to 1600x1200 @ 60 Hz. When in dual-channel mode, the GMCH can drive a flat panel up to 2048x1536 @ 75 Hz or dCRT/HDTV up to 1920x1080 @ 85 Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

Table 10-7. Display Port Characteristics

Interface Protocol		Analog	Digital Port B	Digital Port C
		RGB DAC	DVO 1.0	DVO 1.0
Signals	HSYNC	Yes Enable/Polarity		
	VSYNC	Yes Enable/Polarity		
	BLANK	No	Yes(1)	Yes(1)
	STALL	No	Yes	Yes
	Field	No	Yes	Yes
	Display_Enable	No	—	No
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1		
Pixel Aspect Ratio		Square(1)		
Voltage		RGB 0.7 V p-p	PCI Express*	PCI Express
Clock		NA	Differential	
Max Rate		400 Mpixel	200/400 Mpixel	
Format		Analog RGB	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1/DDC2B	DDC2B	
External Device		No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-I	DVI/CVBS/S-Video/Component/SCART	

NOTES:
1. Single signal software selectable between display enable and Blank#.

10.6.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices (such as, LCD panels with analog inputs) may work satisfactorily but no functionality has been added to the signals to enhance that capability.

Table 10-8. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

10.6.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. The GMCH's integrated 400 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 75 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

10.6.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

10.6.1.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that sets the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

10.6.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDC_CLK and DDC_DATA signals to communicate with the analog monitor. The GMCH generates these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

10.6.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two SDVO ports. On the 82945G/82945GC GMCH these ports are multiplexed on the PCI Express interface. When an external PCI Express graphics accelerator is not present, the GMCH can use the multiplexed SDVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD2 card that is designed to plug into a PCI Express connector.

10.6.2.1 Multiplexed Digital Display Channels – Intel® SDVOB and Intel® SDVOC

The 82945G/82945GC/82945GZ GMCH has the capability to support digital display devices through two SDVO ports. For the 82945G/82945GC GMCH, when an external graphics accelerator is used via the multiplexed PCI Express port, these SDVO ports are not available.

The shared SDVO ports each support a pixel clock up to 200 MHz and can support a variety of transmission devices. When using a dual-channel external transmitter, it will be possible to pair the two SDVO ports in dual-channel mode to support a single digital display with higher resolutions and refresh rates. In this mode, the GMCH is capable of driving the pixel clock up to 400 MHz.

SDVO_CTRLDATA is an open-drain signal that acts as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an SDVO interface. When implementing SDVO, either via ADD2 cards or with a down device, a pull-up is placed on this line to signal to the GMCH to run in SDVO mode and for proper GMBus operation.

10.6.2.1.1 ADD2/ADD2+ Card

When a 945G/945GC Express chipset platform uses a PCI Express connector, the multiplexed SDVO ports may be used via an ADD2 card for 945GC and ADD2/ADD2+ card for 945G. The ADD2/ADD2+ card will be designed to fit a standard PCI Express (x16) connector.

10.6.2.1.2 TMDS Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display |(e.g., flat panel or digital CRT). When combining the two multiplexed SDVO ports, the GMCH can drive a flat panel up to 2048x1536 or a dCRT/HDTV up to 1920x1080. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver, or an external device, but has no native panel fitting capabilities. The GMCH will, however, provide unscaled mode where the display is centered on the panel.

10.6.2.1.3 LVDS Capabilities

The GMCH may use the SDVO ports to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver, or an external device, but has no native panel fitting capabilities. The GMCH will, however, provide unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the SDVO stall input pair.

10.6.2.1.4 TV-Out Capabilities

Although traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. The GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH generates the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed SDVO interface is a NTSC/PAL/SECAM display, the TV-Out port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided.

The TV-Out interface on the GMCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation will be that the overlay source data is in the YUV format and will bypass the conversion to RBG as it is sent to the TV port directly.

Sync Lock Support

Sync lock to the TV will be accomplished using the external encoders PLL combined with the display phase detector mechanism. The availability of this feature will be determined by which external encoder is in use.

Analog Content Protection

Analog content protection will be provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

Connectors

Target TV connectors support includes the CVBS, S-Video, Component, and SCART connectors. The external TV encoder in use will determine the method of support.

10.6.2.1.5 Control Bus

Communication to SDVO registers and if used, ADD2 PROMs and monitor DDCs, are accomplished by using the SDVO_CTRLDATA and SDVO_CTRLCLK signals through the SDVO device. These signals run up to 1 MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device datasheets for level shifting requirements of these signals.

Intel® SDVO Modes

The GMCH port can be dynamically configured in the Standard, Extended, and Dual Standard modes. Refer to Section 10.4.2 for details.

10.6.3 Multiple Display Configurations

Microsoft Windows* 2000 and Windows* XP operating systems have enabled support for multi-monitor display. Since the GMCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The GMCH (see note) supports Intel® Dual Display Clone, Intel Dual Display Twin, Intel Dual Display Zoom, and Extended Desktop.

Intel Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

Intel Dual Display Twin uses one of the display pipes to drive the same content, at the same resolution, color depth, and refresh rates to two different displays.

Intel Dual Display Zoom uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration results in a portion of the primary display to be zoomed in on and displayed on the secondary display.

Extended desktop uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows desktop by using both displays as a work surface.

Note: The 82945G/82945GC GMCH IGD is Not capable of operating in parallel with an external PCI Express graphics device. The GMCH can, however, work in conjunction with a PCI graphics adapter. Intel® Extended Desktop and Dual Display Zoom feature is supported with the 82945G GMCH only. Intel® Dual Display Clone and Dual Display Twin are supported with the 82945G, 82945GC, and the 82945GZ

10.7 Power Management

Power management feature List:

- ACPI 1.0b support
- ACPI S0, S1D, S3 (both Cold and Chipset Hot), S4, S5, C0, and C1. C2, C3, C4 states and corresponding Enhanced states- S3hot, C2, C3, and C4 are not used in the (G)MCH.
- Enhanced power management state transitions for increasing time processor spends in low power states
- Internal Graphics Display Device Control D0, D1, D2, D3
- Graphics Adapter States: D0, D3
- PCI Express Link States: L0, L0s (82945G/82945GC/82945P/82945PL Only)

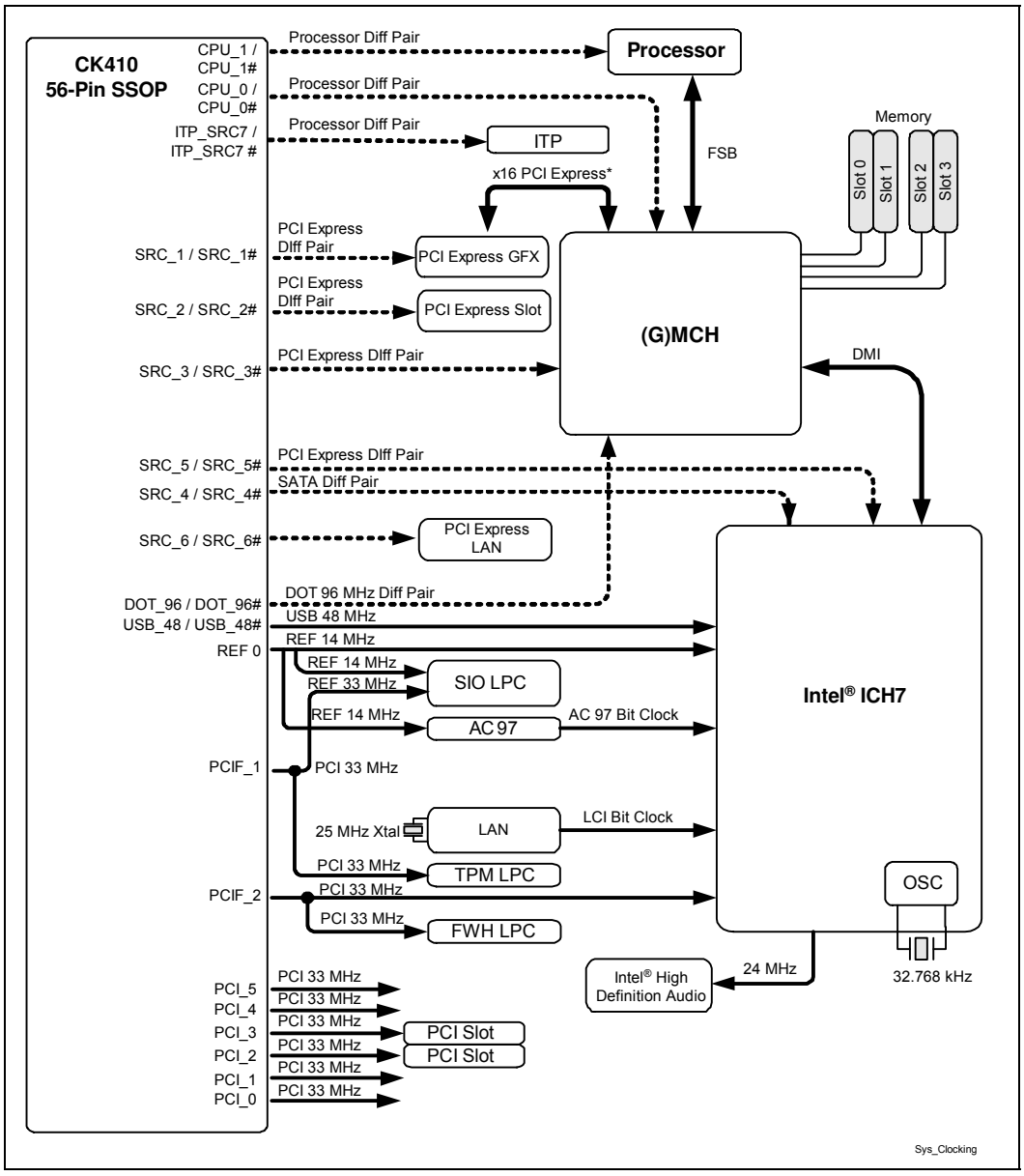
10.8 Clocking

The (G)MCH has a total of 5 PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL – This PLL generates the main core clocks in the host clock domain. The Host PLL can also be used to generate memory and internal graphics core clocks. It uses the Host clock (HCLKIN) as a reference.
- Memory PLL – This PLL can be used to generate memory and internal graphics core clocks, when not generated by the Host PLL. The memory PLL is not needed in all configurations, but exists to provide more flexible frequency combinations without an unreasonable VCO frequency. It uses the Host clock (HCLKIN) as a reference.
- PCI Express PLL – This PLL generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH7. The PCI Express PLL uses the 100 MHz (GCLKIN) as a reference.
- Display PLL A (82945G/82945GC/82945GZ GMCH Only) – This PLL generates the internal clocks for Display A. It uses DREFCLK as a reference.
- Display PLL B (82945G/82945GC/82945GZ GMCH Only) – This PLL generates the internal clocks for Display B. It uses DREFCLK as a reference.

Figure 10-7 illustrates the various clocks in the 945G Express chipset platform.

Figure 10-7. System Clocking Example



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11 Electrical Characteristics

This chapter contains the (G)MCH absolute maximum electrical ratings, power dissipation values, and DC characteristics.

Note: References to SDVO apply to the 82945G/82945GC/82945GZ GMCH only.

Note: References to 1066 MHz FSB apply to the 82945G/82945P only.

Note: References to DDR2-667 apply to the 82945G/82945GC/82945P only.

Note: References to the PCI Express Interface applies to the 82945G/82945GC/82945P/82945PL only.

11.1 Absolute Minimum and Maximum Ratings

Table 11-1 specifies the (G)MCH's absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the (G)MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 11-1. Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	-55	150	°C	1
(G)MCH Core					
VCC	1.5 V Core Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
Host Interface (533 MHz/800 MHz/1066 MHz) (1066 MHz on 82945G/82945P (G)MCH Only)					
VTT	System Bus Input Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_HPLL	1.5 V Host PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
DDR2 Interface (533 MHz/667 MHz) (667 MHz on 82945G/82945GC/82945P (G)MCH Only)					
VCCSM	1.8 V DDR2 System Memory Supply Voltage with respect to V_{SS}	-0.3	4.0	V	
VCCA_SMPLL	1.5 V System Memory PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
PCI Express*/SDVO/DMI Interface					
VCC_EXP	1.5 V PCI Express* and DMI Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_EXPPLL	1.5 V PCI Express PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
RGB/CRT DAC Display Interface (8 bit) (82945G/82945GC/82945GZ GMCH Only)					
VCCA_DAC	2.5 V Display DAC Analog Supply Voltage with respect to V_{SS}	-0.3	2.65	V	
VCCA_DPLLA	1.5 V Display PLL A Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_DPLLB	1.5 V Display PLL B Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
CMOS Interface					
VCC2	2.5 V CMOS Supply Voltage with respect to V_{SS}	-0.3	2.65	V	

NOTES:
1. Possible damage to the (G)MCH may occur if the (G)MCH temperature exceeds 150 °C. Intel does not warrant functionality for parts that have exceeded temperatures above 150 °C since this exceeds Intel's specification.

11.1.1 Power Characteristics

Table 11-2. Non Memory Power Characteristics

Symbol	Parameter	Signal Names	Min	Max	Unit	Notes
I_{VTT}	System Bus Supply Current	VTT	—	0.9	A	1, 4,5
I_{VCC}	1.5 V Core Supply Current (Integrated)	VCC	—	13.8	A	2,3,4,5
I_{VCC}	1.5 V Core Supply Current (Discrete)	VCC	—	8.9	A	2,3,4,5
I_{VCC_EXP}	1.5 V PCI Express and DMI Supply Current	VCC_EXP	—	1.5	A	5
I_{VCCA_DAC}	2.5 V Display DAC Analog Supply Current	VCCA_DAC	—	70	mA	5
I_{VCC2}	2.5 V CMOS Supply Current	VCC2	—	2.0	mA	5
I_{VCCA_EXPPLL}	1.5 V PCI Express and DMI PLL Analog Supply Current	VCCA_EXPPLL	—	45	mA	5
I_{VCCA_HPLL}	1.5 V Host PLL Supply Current	VCCA_HPLL	—	45	mA	5
I_{VCCA_DPLLA} I_{VCCA_DPLLB}	1.5 V Display PLL A and PLL B Supply Current (82945G/82945GC/82945GZ GMCH Only)	VCCA_DPLLA VCCA_DPLLB	—	55	mA	5

NOTES:
1. Estimate is only for maximum current coming through (G)MCH supply balls.
2. Rail includes DLLs and FSB sense amps.
3. Includes worst case leakage.
4. Calculated for highest frequencies.
5. I_{cc_max} values are determined on a per-interface basis. Maximum currents cannot occur simultaneously on all interfaces.

Table 11-3. DDR2 Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{VCCSM}	DDR2 System Memory Interface (1.8 V) Supply Current	—	4.0	A	1,2,3
I_{SUS_VCCSM}	DDR2 System Memory Interface (1.8 V) Standby Supply Current	—	25	mA	1
I_{SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current	—	2	mA	1
I_{SUS_SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current	—	10	µA	1
I_{TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	—	36	mA	1
I_{SUS_TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current	—	10	µA	1
I_{VCCA_SMPLL}	System Memory PLL Analog (1.5 V) Supply Current	—	66	mA	1

NOTES:
1. Estimate is only for max current coming through (G)MCH supply balls
2. Calculated for highest frequencies
3. I_{cc_max} values are determined on a per-interface basis. Maximum currents cannot occur simultaneously on all interfaces.

11.2 Signal Groups

The signal description includes the type of buffer used for the particular signal:

GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The (G)MCH integrates most GTL+ termination resistors.
DDR2	DDR2 System memory (1.8 V CMOS buffers)
PCI Express/SDVO	PCI Express interface signals. These signals are compatible with PCI Express 1.0a signaling environment AC specifications. The buffers are **not** 3.3 V tolerant.
Analog	Analog signal interface
Ref	Voltage reference signal
HVCMOS	2.5 V Tolerant High Voltage CMOS buffers
SSTL-1.8	1.8 V Tolerant Stub Series Termination Logic

Table 11-4. Signal Groups

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	GTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0], HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK#	
(b)	GTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HEDRDY#	
(c)	Asynchronous GTL+ Input	HPCREQ#	
(d)	Analog Host Interface Reference and Compensation Signals	HDVREF, HACCVREF, HSWING HRCOMP, HSCOMP	
(c1)	Miscellaneous CMOS Inputs	BSEL[2:0]	

Signal Group	Signal Type	Signals	Notes
PCI-Express* Graphics and Intel® SDVO Interface Signal Groups			
(e)	PCI Express*/ Intel SDVO Input	**PCI Express Interface (82945G/82945GC/82945P/82945PL Only):** EXP_RXN[15:0], EXP_RXP[15:0] **SDVO Interface (82945G/82945GC/82945GZ GMCH Only):** SDVO_TVCLKIN+, SDVO_TVCLKIN-, SDVOB_INT+, SDVOB_INT-, SDVO_STALL+, SDVO_STALL-, SDVOC_INT+, SDVOC_INT-	
(f)	PCI Express/ SDVO Output	**PCI Express Interface (82945G/82945GC/82945P/82945PL Only):** EXP_TXN[15:0], EXP_TXP[15:0] **SDVO Interface (82945G/82945GC/82945GZ GMCH Only):** SDVOB_RED+, SDVOB_RED-, SDVOB_GREEN+, SDVOB_GREEN-, SDVOB_BLUE+, SDVOB_BLUE-, SDVOB_CLK+, SDVOB_CLK-, SDVOC_RED+/SDVOB_ALPHA+, SDVOC_RED-/SDVOB_ALPHA-, SDVOC_GREEN+, SDVOC_GREEN-, SDVOC_BLUE+, SDVOC_BLUE-, SDVOC_CLK+, SDVOC_CLK-	
(g)	Analog PCI Express/SDVO Interface Compensation Signals	EXP_COMPO EXP_COMPI	
DDR2 Interface Signal Groups			
(h)	SSTL – 1.8 DDR2 CMOS I/O	SDQ_A[63:0], SDQ_B[63:0], SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0], SDQS_B[7:0]#	
(i)	SSTL – 1.8 DDR2 CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA_A[13:0], SMA_B[13:0] SBS_A[2:0], SBS_B[2:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(j)	DDR2 Reference Voltage	SMVREF[1:0]	
RGB/CRT DAC Display Signal Groups (82945G/82945GC/82945GZ GMCH Only)			
	Analog Current Outputs	RED, RED#, GREEN, GREEN#, BLUE, BLUE#	
	Analog/Ref DAC Miscellaneous	REFSET	1
	HVCMOS Type	HSYNC, VSYNC	
Clocks, Reset, and Miscellaneous Signal Groups			
(k)	HVCMOS Input	EXTTS#	

Signal Group	Signal Type	Signals	Notes
(l)	Miscellaneous Inputs	RSTIN#, PWROK	
	Miscellaneous HVCMOS Output	ICH_SYNC#	
(m)	Low Voltage Diff. Clock Input	HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN	
(n)	HVCMOS I/O (82945G/82945GC/82945GZ GMCH Only)	SDVO_CRTLCLK, SDVO_CTRLDATA, DDC_CLK, DDC_DATA	
I/O Buffer Supply Voltages			
(o)	System Bus Input Supply Voltage	VTT	
(p)	1.5 V SDVO, PCI Express Supply Voltages	VCC_EXP	
(q)	1.8 V DDR2 Supply Voltage	VCCSM	
(r)	1.5 V DDR2 PLL Analog Supply Voltage	VCC_SMPLL	
(s)	1.5 V (G)MCH Core Supply Voltage	VCC	
(t)	2.5 V CMOS Supply Voltage	VCC2	
(u)	2.5 V RGB/CRT DAC Display Analog Supply Voltage	VCCA_DAC	
(v)	PLL Analog Supply Voltages	VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	

NOTE:
1. Current Mode Reference pin. DC Specification not required

11.3 DC Characteristics

Table 11-5. DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage (AC Noise not included unless noted)							
VCCSM	(q)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	4
VCCA_SMPLL	(r)	DDR2 I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCC_EXP	(p)	SDVO, PCI-Express Supply Voltage	1.425	1.5	1.575	V	
VTT	(o)	System Bus Input Supply Voltage	1.14	1.2	1.26	V	
VCC	(s)	GMCH Core Supply Voltage	1.425	1.5	1.575	V	11
VCC2	(t)	CMOS Supply Voltage	2.375	2.5	2.625	V	
VCCA_DAC	(u)	CRT Display DAC Supply Voltage	2.375	2.5	2.625	V	
VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	(v)	Various PLLs' Analog Supply Voltages	1.425	1.5	1.575	V	
Reference Voltages							
HVREF	(d)	Host Address, Data, and Common Clock Signal Reference Voltage	0.63 x V_{TT} –2%	0.63 x V_{TT}	0.63 x V_{TT} +2%	V	
HSWING	(d)	Host Compensation Reference Voltage	0.22 x V_{TT} –2%	0.22 x V_{TT}	0.22 x V_{TT}+2%	V	
SMVREF	(j)	DDR2 Reference Voltage	0.49 x V_{CCSM}	0.50 x V_{CCSM}	0.51 x V_{CCSM}	V	
Host Interface							
V_{IL_H}	(a, c, c1)	Host GTL+ Input Low Voltage	-0.10	0	(0.63 x V_{TT}) – 0.1	V	
V_{IH_H}	(a, c, c1)	Host GTL+ Input High Voltage	(0.63 x V_{TT})+0.1	V_{TT}	V_{TT} +0.1	V	
V_{OL_H}	(a, b)	Host GTL+ Output Low Voltage	—	—	(0.22 x VTT)+0.1	V	
V_{OH_H}	(a, b)	Host GTL+ Output High Voltage	V_{TT} – 0.1	—	V_{TT}	V	
I_{OL_H}	(a, b)	Host GTL+ Output Low Current	—	—	V_{TTmax} *(1–0.22) / Rttmin	mA	Rtt_{min} = 54 Ω
I_{LEAK_H}	(a, c, c1)	Host GTL+ Input Leakage Current	—	—	20	µA	V_{OL}<Vpad< V_{TT}

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
C_{PAD}	(a, c, c1)	Host GTL+ Input Capacitance	2	—	2.5	pF	
C_{PCKG}	(a, c, c1)	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	
DDR2 Interface							
$V_{IL(DC)}$	(h)	DDR2 Input Low Voltage	—	—	SMVREF – 0.125	V	
$V_{IH(DC)}$	(h)	DDR2 Input High Voltage	SMVREF + 0.125	—	—	V	
$V_{IL(AC)}$	(h)	DDR2 Input Low Voltage	—	—	SMVREF – 0.250	V	
$V_{IH(AC)}$	(h)	DDR2 Input High Voltage	SMVREF + 0.250	—	—	V	
V_{OL}	(h, i)	DDR2 Output Low Voltage	—	—	0.3	V	1
V_{OH}	(h, i)	DDR2 Output High Voltage	1.5	—	—	V	1
I_{Leak}	(h)	Input Leakage Current	—	—	±20	µA	5
I_{Leak}	(h)	Input Leakage Current	—	—	±550	µA	6
$C_{I/O}$	(h, i)	DDR2 Input/Output Pin Capacitance	3.0	—	6.0	pF	
1.5V PCI Express* Interface 1.0a (includes PCI Express and SDVO)							
$V_{TX\text{-}DIFF\ P\text{-}P}$	(f)	Differential Peak to Peak Output Voltage	0.800	—	1.2	V	2
$V_{TX\_CM\text{-}ACp}$	(f)	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX\text{-}DIFF\text{-}DC}$	(f)	DC Differential TX Impedance	80	100	120	Ohms	
$V_{RX\text{-}DIFF\ p\text{-}p}$	(e)	Differential Peak to Peak Input Voltage	0.175	—	1.2	V	3
$V_{RX\_CM\text{-}ACp}$	(e)	AC Peak Common Mode Input Voltage	—	—	150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(k)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(k)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(k)	Input Leakage Current		—	± 20	µA	
C_{IN}	(k)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(m)	Input Low Voltage	- 0.150	0	—	V	
V_{IH}	(m)	Input High Voltage	0.660	0.700	0.850	V	
$V_{CROSS(abs)}$	(m)	Absolute Crossing Point	0.250	—	0.550	V	7, 9
$V_{CROSS(rel)}$	(m)	Relative Crossing Point	0.250 + 0.5 * (V_{Havg} – 0.700)	—	0.550 + 0.5 * (V_{Havg} – 0.770)	V	8, 9
ΔV_{CROSS}	(m)	Range of Crossing Points	—	—	0.140	V	10

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
C_{IN}	(m)	Input Capacitance	1	—	3	pF	
V_{OL}	(n)	Output Low Voltage (CMOS Outputs)	—	—	0.4	V	
V_{OH}	(n)	Output High Voltage (CMOS Outputs)	2.1	—	—	V	
I_{OL}	(n)	Output Low Current (CMOS Outputs)	—	—	1	mA	@V_{OL_HI} max
I_{OH}	(n)	Output High Current (CMOS Outputs)	-1	—	—	mA	@V_{OH_HI} min
V_{IL}	(n)	Input Low Voltage	—	—	1.1	V	
V_{IH}	(n)	Input High Voltage	1.4	—	—	V	
I_{LEAK}	(n)	Input Leakage Current	—	—	± 20	µA	
C_{IN}	(n)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(l)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(l)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(l)	Input Leakage Current	—	—	±100	µA	0<Vin<VCC3_3
C_{IN}	(l)	Input Capacitance	4.690	—	5.370	pF	

NOTES:

1. Determined with 2x GMCH DDR2 Buffer Strength Settings into a 50 Ω to 0.5xVCCSM test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI Express specification should be used as the RX device when taking measurements.
4. This is the DC voltage supplied at the (G)MCH and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the (G)MCH generated from any source other than the (G)MCH itself may not exceed the DC voltage range of 1.8 V ±100 mV.
5. Applies to the pin to V_{CC} or V_{SS} leakage current for the SDQ_A[63:0]# and SDQ_B[63:0]# signals.
6. Applies to the pin-to-pin leakage current between the SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0]#, and SDQS_B[7:0]# signals.
7. Crossing Voltage is defined as the instantaneous voltage value when the rising edge is equal to the falling edge.
8. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
9. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
10. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 7.
11. For all noise components ≤ 20 MHz, the sum of the DC voltage and AC noise component must be within the specified DC min/max operating range.

11.3.1 RGB/CRT DAC Display DC Characteristics (Intel® 82945G/82945GC/82945GZ GMCH Only)

Table 11-6. RGB/CRT DAC Display DC Characteristics: Functional Operating Range (VCCA_DAC = 2.5 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	8	—	—	Bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1, 2, 4 (white video level voltage)
Min Luminance	—	0.000	—	V	1, 3, 4 (black video level voltage)
LSB Current	—	73.2	—	µA	4, 5
Integral Linearity (INL)	-1.0	—	+1.0	LSB	1, 6
Differential Linearity (DNL)	-1.0	—	+1.0	LSB	1, 6
Video channel-channel voltage amplitude mismatch	—	—	6	%	7
Monotonicity	Ensured				

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Maximum steady-state amplitude
3. Minimum steady-state amplitude
4. Defined for a double 75-Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA Video Signal Standards.
7. Max full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).

§

12 Ballout and Package Information

This chapter provides the ballout and package information.

12.1 Ballout

Figure 12-1 through Figure 12-3 show the GMCH ballout for platforms using DDR2 system memory, as viewed from the top side of the package.

Note: Balls that are listed as RSV are reserved. Board traces should **Not** be routed to these balls.

Note: Some balls marked as reserved (RSV) are used in XOR testing. See Chapter 0 for details.

Note: Some balls marked as reserved (RSV) can be used as test points. These are marked as RSV_TPx.

Note: Balls that are listed as NC are No Connects.

Figure 12-1. Intel® 82945G GMCH Ballout Diagram (Top View – Columns 43–30)

	43	42	41	40	39	38	37	36	35	34	33	32	31	30	
BC	NC	NC		VCCSM		SMA_A13			VCCSM		SBS_A0		VCCSM		BC
BB	NC	VCCSM	VSS	SODT_A3	VSS	VCCSM	SCS_A0#		SWE_A#	VSS	VCCSM	SCLK_A0	SCLK_A3#	SMA_A2	BB
BA		VSS	SCS_B2#	SCS_B0#	SCS_A1#		SCAS_A#		SCS_A2#	SRAS_A#		SMA_A0	SCLK_A3	SMA_A3	BA
AY	VCCSM	SODT_B0	VCCSM		SODT_A1	SCS_A3#	SODT_A2			SBS_A1	SMA_A10	SCLK_A0#		SMA_A4	AY
AW		SMA_B13	SCS_B1#	SCS_B3#			SODT_A0		VCCSM	VCCSM		SMA_A1	VCCSM		AW
AV	SODT_B2	VCCSM		SODT_B1		SDQ_A34	VSS		SDQS_A4#	SDQ_A33		SDQ_A36	VCCSM		AV
AU		SDQ_A45	SDQ_A44	SODT_B3	SDQ_A35	SDQ_B45	SDQ_A39		SDQS_A4	VSS		VSS	SDQ_B39		AU
AT										SDM_A4		SDQ_A37	VSS		AT
AR	VSS	SDQ_A41	SDQ_A40		VSS	SDM_B5	VSS		SDQ_B44	SDQ_A38		VSS	SDQ_B34		AR
AP		SDQS_A5	SDQ_A46	SDQS_A5#	SDM_A5	VSS	SDQ_B41	SDQS_B5	SDQ_B40	VSS		SDQ_A32	SDQ_B38		AP
AN	SDQ_A42	VSS		SDQ_A47								SDQ_B42	VSS		AN
AM		SDQ_A53	SDQ_A52	SDQ_A43	VSS	SDQ_B46	VSS	VSS	SDQS_B5#	SDQ_B47	VSS		SDQ_B35		AM
AL	VSS	SDQ_A49	SDQ_A48		RSV	SCLK_B2	VSS	SCLK_B2#	SDQ_B43	SDQ_B48	VSS	VSS	SDQ_B52		AL
AK		SCLK_A2	SCLK_A2#	RSV										VSS	AK
AJ					SDM_B6	SCLK_B5	VSS	SCLK_B5#	VSS	SDQ_B49	VSS	SDQ_B53	VSS	VSS	AJ
AH	SCLK_A5#	VSS		SCLK_A5											AH
AG		SDQS_A6	SDQS_A6#	SDM_A6	VSS	VSS	VSS	VSS	SDQ_B54	SDQS_B6	VSS	SDQS_B6#	VSS	VSS	AG
AF	VSS	SDQ_A55	SDQ_A54		SDQ_A50	VSS	SDQ_B61	VSS	SDQ_B60	SDQ_B51	VSS	SDQ_B50	RSV	VCC	AF
AE		SDQ_A60	SDQ_A61	SDQ_A51											AE
AD	SDQ_A57	VSS		SDQ_A56	SDM_B7	SDQS_B7#	VSS	SDQS_B7	VSS	SDQ_B57	VSS	SDQ_B55	RSV	RSV	AD
AC		SDQS_A7	SDQS_A7#	SDM_A7	VSS	VSS	VSS	VSS	SDQ_B63	RSV	SDQ_B62	SDQ_B56	VSS	RSV	AC
AB	VSS	SDQ_A63	SDQ_A62												AB
AA		RSV	HBREQ0#	SDQ_A59	SDQ_A58	RSV	HA29#	VSS	RSV	RSV	VSS	SDQ_B59	VSS	RSV	AA
Y	HRS1#	VSS		HEDRDY#	VSS	HA28#	VSS	HA27#	VSS	HA31#	RSV	SDQ_B58	VSS	RSV	Y
W		HADS#	HHITM#	HTRDY#											W
V	VSS	HA25#	HDRDY#		VSS	VSS	VSS	VSS	HADSTB1#	VSS	HA22#	HA30#	RSV	RSV	V
U		HDBSY#	HHIT#	HLOCK#	HBNR#	VSS	HA19#	VSS	HA26#	HA23#	VSS	HA24#	VSS	RSV	U
T	HRS2#	VSS		HRS0#											T
R					VSS	HA21#	VSS	HA18#	HA20#	VSS	HA10#	HA17#	VSS	VSS	R
P		HD2	HD0	HDEFER#										VSS	P
N	VSS	HA14#	HD4		VSS	HA16#	HA15#	VSS	HA9#	HA12#	VSS	HA11#	VSS		N
M		HD3	HD7	HD5	HD1	HA13#	VSS	HADSTB0#	VSS	HA8#	HD33		HCLKP		M
L	HDSTBN0#	VSS		HD6								HD30	VSS		L
K		HD8	HDSTBP0#	HDINV0#	VSS	HA4#	VSS	HREQ2#	HA6#	VSS		VSS	HD34		K
J	VSS	HA5#	HD10		HA3#	VSS	HA7#		HD18	HD27		HD25	HD31		J
H										HD23		VSS	HD32		H
G		HD11	HD13	HD12	HD9	VSS	HREQ3#		VSS	HDSTBN1#		VSS	VSS		G
F	HD15	VSS		HD14		HPCREQ#	HD16		HDSTBP1#	VSS		HD29	HD37		F
E		HREQ4#	HREQ0#	HD50			HD17		NC	HDSTBP3#		VSS	HD48		E
D	VSS	HBPRI#	HREQ1#		HD19	HD53	HD51			HD56	HD54	HD61		HD63	D
C		NC	HD20	VSS	HD52		HD24		HD55	HD57		HD60	HD59	HCPURST#	C
B	NC	NC	NC	HD22	HD21	VSS	HDSTBN3#		HD26	HD28	VSS	HDINV3#	HD58	HD62	B
A	RSV	NC		VSS		HDINV1#			VSS		HD49		VSS		A
	43	42	41	40	39	38	37	36	35	34	33	32	31	30	

Figure 12-2. Intel® 82945G GMCH Ballout Diagram (Top View – Columns 29–16)

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
BC		SMA_A6		VCCSM		SCKE_A2		VCCSM		SMA_B4		VCCSM		RSV	BC
BB		VCCSM	SMA_A9	SMA_A12	SCKE_A0	VCCSM	SWE_B#	SMA_B0	SMA_B1	VCCSM	VSS	SMA_B9	SMA_B11	VCCSM	BB
BA			SMA_A5	SBS_A2	SCKE_A3		SRAS_B#	SMA_B10	SMA_B2		SMA_B8	SMA_B7	SMA_B12		BA
AY		SMA_A8	SMA_A7		SCKE_A1	SCAS_B#	SBS_B1		SMA_B3	SMA_B6	SMA_B5		SBS_B2	SCKE_B1	AY
AW	VCCSM		SMA_A11	NC		VCCSM	SBS_B0		VCCSM	VCCSM		RSV	RSV		AW
AV	SDQS_B4#		NC	NC		SDQ_B26	VCCSM		VCCSM	SDQ_A26		VCCSM	VSS		AV
AU	VSS		SDQ_B32	VSS		VSS	SDQS_B3		VSS	VSS		SDQS_A3	VSS		AU
AT	SDQS_B4		VSS	VSS		SDQ_B31	VSS		VSS	SDQ_A31		VSS	VSS		AT
AR	SDM_B4		SDQ_B37	SCLK_B3#		VSS	SDQS_B3#		SDQ_B29	VSS		SDQS_A3#	SDQ_A29		AR
AP	VSS		SDQ_B36	SCLK_B3		SDQ_B30	SDM_B3		SDQ_B28	SDQ_A30		SDM_A3	SDQ_A28		AP
AN	SDQ_B33		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		AN
AM	SCLK_B0		SCLK_B0#	SDQ_B27		SDQ_B24	SDQ_B25		SDQ_A27	SDQ_A24		SDQ_A25	SDQ_B19		AM
AL	RSV		VSS	RSV		VSS	VSS		VSS	RSV		VSS	RSV_TP1		AL
AK	VSS		RSV	VSS		VSS	RSV_TP2		RSV	VCC		RSV_TP3	RSV_TP0		AK
AJ	RSV		RSV	RSV		RSV	RSV		RSV	VCC		VCC	VCC		AJ
AH															AH
AG	RSV		RSV	RSV	RSV	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AG
AF	VCC		VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		AF
AE			VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		AE
AD	VSS		VSS	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		AD
AC	VSS		VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		AC
AB			VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AB
AA	VSS		VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC		AA
Y	VSS		VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		Y
W			VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC		W
V	VSS		VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC		V
U	VSS		RSV	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		U
T															T
R	VSS		RSV	VSS		VCC	VCC		VCC	VCC		VCC	VCC		R
P	VSS		VSS	VSS		VSS	VTT		VCC	VCC		VCC	VCC		P
N	VSS		VSS	VSS		VSS	VTT		RSV_TP6	DDC_CLK[1]		DDC_DATA[1]	VCC		N
M	HCLKN		HD35	HDSTBN2#		HD41	VTT		VSS	VSS		ICH_SYNC#	VCC		M
L	VSS		HD40	VSS		VSS	VTT		RSV_TP4	BSEL2		RSV_TP5	VSS		L
K	HD36		VSS	HD43		HD46	VTT		EXP_SLR	VSS		ALLZTEST	GREEN[1]		K
J	VSS		HDSTBP2#	HD42		VSS	VTT		VSS	EXTTS#		BLUE#[1]	GREEN#[1]		J
H	HD38		VSS	VSS		HD45	VTT		BSEL1	XORTEST		BLUE[1]	VSS		H
G	VSS		VSS	HD44		VSS	VTT		VSS	VSS		VSS	RED#[1]		G
F	HD39		VTT	VSS		HD47	VTT		BSEL0	EXP_EN		VSS	RED[1]		F
E	HDINV2#		VTT	VTT		VTT	VTT		VSS	VSS		VSS	VSS		E
D		HACCVREF	HDVREF		VTT	VTT	VTT		VSS	VSS	VCC2		HSYNC[1]	VSS	D
C			HSCOMP	VTT	VTT		VTT	VSS	VCCA_HPLL		VCCA_DPLLA[1]	VCCA_DAC	VSYNC[1]		C
B		VSS	HSWING	VTT	VTT	VTT	VTT	VSS	VSS	VCCA_SMPLL	VCCA_DPLLB[1]	VCCA_DAC	VCCA_EXPPLL	GCLKN	B
A		HRCOMP		VSS		VTT		VSS		REFSET[1]		VSSA_DAC		VSS	A
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

NOTES:

1. This analog display signal ball is reserved (RSV) on the 82945P/82945PL MCH component.

Figure 12-3. Intel® 82945G GMCH Ballout Diagram (Top View – Columns 15–1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
BC			VCCSM		SDQ_A22		VSS			SDQ_A14		VSS		NC	NC	BC
BB		VSS	SCKE_B3	SDQ_A19	VSS	SDM_A2	SDQ_A21		SDQ_A11	VSS	SCLK_A1#	SDQS_A1#	VSS	NC	NC	BB
BA		SCKE_B0	SCKE_B2	SDQ_A18		SDQS_A2#	SDQ_A20		SDQ_A10		SCLK_A4#	VSS	SDQS_A1	NC		BA
AY		RSV		SDQ_A23	SDQS_A2	SDQ_A17			SDQ_A15	SCLK_A4	SCLK_A1		SDQ_A9	SDM_A1	VSS	AY
AW	VCCSM		VCCSM	SDQ_A16		VSS	SCLK_B1#		SDM_B1			SDQ_A13	SDQ_A8	NC		AW
AV	SDQ_B18		SDQS_B2	SDQ_B10		VSS	SCLK_B1		SDQS_B1	SDQ_B9		SDQ_A3		VSS	SDQ_A12	AV
AU	VSS		VSS	VSS		SCLK_B4	VSS		SDQ_B8	VSS	SDQ_A6	SDQS_A0	SDQ_A2	SDQ_A7		AU
AT	SDQ_B23		SDQS_B2#	VSS		SCLK_B4#										AT
AR	VSS		SDQ_B21	SDQ_B14		SDQ_B15	SDQS_B1#		SDQ_B13	VSS	SDQ_B12		SDM_A0	SDQS_A0#	VSS	AR
AP	SDQ_B22		SDM_B2	VSS		VSS	SDQ_B3	SDQ_B2	VSS	SDQ_B7	VSS	SDQ_A5	SDQ_A0	SDQ_A1		AP
AN	VSS		VSS	SDQ_B20								VSS		VSS	SDQ_A4	AN
AM	SDQ_B16		SDQ_B17		SDQ_B11	SDQ_B6	VSS	SDQS_B0	VSS	SDQS_B0#	VSS	SMVREF0	SOCOMP1	SMVREF1		AM
AL	VSS		VSS	VSS	SDM_B0	VSS	SDQ_B5	SDQ_B1	VSS	SDQ_B0	SRCOMP0		VSS	VSS	VSS	AL
AK	VCC	VCC										VCC	VCC	VCC		AK
AJ	VCC	VCC	VCC	RSTIN#	SDQ_B4	VSS	PWROK	SOCOMP0	VSS	SRCOMP1	VCC					AJ
AH												VCC		VCC	VCC	AH
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AG
AF	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS		VSS	VSS	VSS	AF
AE												VCC_EXP	VCC_EXP	VCC_EXP		AE
AD	VCC	VCC	VSS	VCC_EXP	VSS	VCC_EXP	VSS	VCC_EXP	VSS	VCC_EXP	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	AD
AC	VCC	VSS	VCC_EXP	EXP_COMPO	EXP_COMPI	VSS	DMI_RXP3	DMI_RXN3	VSS	VCC_EXP	VCC_EXP	DMI_TXN3	VSS	VSS		AC
AB													DMI_TXP3	VSS	DMI_TXN1	AB
AA	VCC	VSS	VCC_EXP	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	DMI_RXN2	DMI_RXP2	VCC_EXP	DMI_TXN2	VSS	DMI_TXP1		AA
Y	VCC	VSS	VCC_EXP	VSS	EXP_RXN15	EXP_RXP15	VSS	DMI_RXN0	DMI_RXP0	VSS	VSS	DMI_TXP2		VSS	DMI_TXN0	Y
W												EXP_TXN15	VSS	DMI_TXP0		W
V	VCC	VSS	VCC_EXP	VSS	VSS	VCC_EXP	VCC_EXP	VSS	VCC_EXP	VCC_EXP	VCC_EXP		EXP_TXP15	VSS	EXP_TXN14	V
U	VCC	VSS	VCC_EXP	VSS	EXP_RXP12	EXP_RXN12	VSS	VCC_EXP	VCC_EXP	VCC_EXP	VSS	EXP_TXN13	VSS	EXP_TXP14		U
T												EXP_TXP13		VSS	EXP_TXN12	T
R	VCC	VSS	VCC_EXP	VSS	VCC_EXP	VCC_EXP	VSS	EXP_RXP13	EXP_RXN13	VSS	VCC_EXP					R
P	VSS	VSS										EXP_RXP14	VSS	EXP_TXP12		P
N	VSS		VSS	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VSS	VCC_EXP	VSS	VCC_EXP		EXP_RXN14	VSS	EXP_TXN11	N
M	RSV		VSS		RSV	VSS	VSS	VSS	EXP_RXN10	EXP_RXP10	VSS	EXP_TXN10	VSS	EXP_TXP11		M
L	RSV		VSS	VSS								EXP_TXP10		VSS	EXP_RXN11	L
K	VSS		VSS	VSS		VSS	EXP_RXP8	EXP_RXN8	VSS	VSS	VSS	EXP_TXN9	VSS	EXP_RXP11		K
J	DREFCLKP		EXP_RXP2	VSS		VSS	EXP_RXP4		VSS	EXP_RXN7	VSS		EXP_TXP9	VSS	EXP_TXN8	J
H	DREFCLKN		EXP_RXN2	VSS		EXP_RXN4										H
G	VSS		VSS	EXP_RXP0		VSS	VSS		VSS	EXP_RXP7	VSS	EXP_RXN9	VSS	EXP_TXP8		G
F	SDVO_CTRLDATA[1]		VSS	EXP_RXN0		EXP_RXN3	EXP_RXN5		EXP_RXP5	VSS		EXP_RXP9		VSS	EXP_TXN7	F
E	SDVO_CTRLCLK[1]		VSS	VSS		EXP_RXP3	VSS		VSS			VSS	VSS	EXP_TXP7		E
D		EXP_TXP0		EXP_RXN1	EXP_RXP1	VSS			EXP_TXP5	EXP_TXN5	VSS		EXP_RXN6	VSS	VSS	D
C		VSS	EXP_TXN0	VSS		EXP_TXP3	EXP_TXN3		VSS		VSS	EXP_RXP6	VSS	NC		C
B		GCLKP	VSS	EXP_TXN1	VSS	EXP_TXN2	VSS		EXP_TXN4	VSS	EXP_TXN6	VSS	NC	NC		B
A			EXP_TXP1		EXP_TXP2		EXP_TXP4			EXP_TXP6		VSS				A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

NOTES:

1. This analog display signal ball is reserved on the 82945P/82945PL MCH component.

12.2 Ballout Table

Table 12-1 lists the Intel® 82945G/82945GC/82945GZ GMCH and Intel® 82945P/82945PL MCH ballout in alphabetical order by signal name.

Table 12-1. Intel® 82945G//82945GZ/82945GC/82945P/82945PL (G)MCH Ballout Sorted by Signal Name

Intel® 82945G GMCH Signal Name	Intel® 82945GZ (82945GC) GMCH Signal Name	Intel® 82945P /82945PL MCH Signal Name	Ball #
ALLZTEST	ALLZTEST	ALLZTEST	K18
BLUE	BLUE	RSV	H18
BLUE#	BLUE#	RSV	J18
BSEL0	BSEL0	BSEL0	F21
BSEL1	BSEL1	BSEL1	H21
BSEL2	BSEL2	BSEL2	L20
DDC_CLK	DDC_CLK	RSV	N20
DDC_DATA	DDC_DATA	RSV	N18
DMI_RXN0	DMI_RXN0	DMI_RXN0	Y8
DMI_RXN1	DMI_RXN1	DMI_RXN1	AA10
DMI_RXN2	DMI_RXN2	DMI_RXN2	AA7
DMI_RXN3	DMI_RXN3	DMI_RXN3	AC8
DMI_RXP0	DMI_RXP0	DMI_RXP0	Y7
DMI_RXP1	DMI_RXP1	DMI_RXP1	AA9
DMI_RXP2	DMI_RXP2	DMI_RXP2	AA6
DMI_RXP3	DMI_RXP3	DMI_RXP3	AC9
DMI_TXN0	DMI_TXN0	DMI_TXN0	Y1
DMI_TXN1	DMI_TXN1	DMI_TXN1	AB1
DMI_TXN2	DMI_TXN2	DMI_TXN2	AA4
DMI_TXN3	DMI_TXN3	DMI_TXN3	AC4
DMI_TXP0	DMI_TXP0	DMI_TXP0	W2
DMI_TXP1	DMI_TXP1	DMI_TXP1	AA2
DMI_TXP2	DMI_TXP2	DMI_TXP2	Y4
DMI_TXP3	DMI_TXP3	DMI_TXP3	AB3
DREFCLKN	DREFCLKN	DREFCLKN	H15
DREFCLKP	DREFCLKP	DREFCLKP	J15
EXP_COMPI	RSV (EXP_COMPI)	EXP_COMPI	AC11
EXP_COMPO	RSV (EXP_COMP0)	EXP_COMPO	AC12
EXP_EN	EXP_EN	EXP_EN	F20
EXP_RXN0	RSV (EXP_RXN0)	EXP_RXN0	F12
EXP_RXN1	RSV (EXP_RXN1)	EXP_RXN1	D12

EXP_RXN2	RSV (EXP_RXN2)	EXP_RXN2	H13
EXP_RXN3	RSV (EXP_RXN3)	EXP_RXN3	F10
EXP_RXN4	RSV (EXP_RXN4)	EXP_RXN4	H10
EXP_RXN5	RSV (EXP_RXN5)	EXP_RXN5	F9
EXP_RXN6	RSV (EXP_RXN6)	EXP_RXN6	D3
EXP_RXN7	RSV (EXP_RXN7)	EXP_RXN7	J6
EXP_RXN8	RSV (EXP_RXN8)	EXP_RXN8	K8
EXP_RXN9	RSV (EXP_RXN9)	EXP_RXN9	G4
EXP_RXN10/ SDVOC_INT-	SDVOC_INT- (EXP_RXN10/ SDVOC_INT-)	EXP_RXN10	M7
EXP_RXN11	RSV (EXP_RXN11)	EXP_RXN11	L1
EXP_RXN12	RSV (EXP_RXN12)	EXP_RXN12	U10
EXP_RXN13/ SDVO_STALL-	SDVO_STALL- (EXP_RXN13/ SDVO_STALL-)	EXP_RXN13	R7
EXP_RXN14/ SDVOB_INT-	SDVOB_INT- (EXP_RXN14/ SDVOB_INT-)	EXP_RXN14	N3
EXP_RXN15/ SDVO_TVCLKIN-	SDVO_TVCLKIN- (EXP_RXN15/ SDVO_TVCLKIN-)	EXP_RXN15	Y11
EXP_RXP0	RSV (EXP_RXP0)	EXP_RXP0	G12
EXP_RXP1	RSV (EXP_RXP1)	EXP_RXP1	D11
EXP_RXP2	RSV (EXP_RXP2)	EXP_RXP2	J13
EXP_RXP3	RSV (EXP_RXP3)	EXP_RXP3	E10
EXP_RXP4	RSV (EXP_RXP4)	EXP_RXP4	J9
EXP_RXP5	RSV (EXP_RXP5)	EXP_RXP5	F7
EXP_RXP6	RSV (EXP_RXP6)	EXP_RXP6	C4
EXP_RXP7	RSV (EXP_RXP7)	EXP_RXP7	G6
EXP_RXP8	RSV (EXP_RXP8)	EXP_RXP8	K9
EXP_RXP9	RSV (EXP_RXP9)	EXP_RXP9	F4
EXP_RXP10/ SDVOC_INT+	SDVOC_INT+ (EXP_RXP10/ SDVOC_INT+)	EXP_RXP10	M6
EXP_RXP11	RSV (EXP_RXP11)	EXP_RXP11	K2
EXP_RXP12	RSV (EXP_RXP12)	EXP_RXP12	U11
EXP_RXP13/ SDVO_STALL+	SDVO_STALL+ (EXP_RXP13/ SDVO_STALL+)	EXP_RXP13	R8
EXP_RXP14/ SDVOB_INT+	SDVOB_INT+ (EXP_RXP14/ SDVOB_INT+)	EXP_RXP14	P4
EXP_RXP15/ SDVO_TVCLKIN+	SDVO_TVCLKIN+ (EXP_RXP15/ SDVO_TVCLKIN+)	EXP_RXP15	Y10

EXP_SLR	EXP_SLR	EXP_SLR	K21
EXP_TXN0	RSV (EXP_TXN0)	EXP_TXN0	C13
EXP_TXN1	RSV (EXP_TXN1)	EXP_TXN1	B12
EXP_TXN2	RSV (EXP_TXN2)	EXP_TXN2	B10
EXP_TXN3	RSV (EXP_TXN3)	EXP_TXN3	C9
EXP_TXN4	RSV (EXP_TXN4)	EXP_TXN4	B7
EXP_TXN5	RSV (EXP_TXN5)	EXP_TXN5	D6
EXP_TXN6	RSV (EXP_TXN6)	EXP_TXN6	B5
EXP_TXN7	RSV (EXP_TXN7)	EXP_TXN7	F1
EXP_TXN8/ SDVOC_CLK-	SDVOC_CLK- (EXP_TXN8/ SDVOC_CLK-	EXP_TXN8	J1
EXP_TXN9/ SDVOC_BLUE-	SDVOC_BLUE- (EXP_TXN9/ SDVOC_BLUE-)	EXP_TXN9	K4
EXP_TXN10/ SDVOC_GREEN-	SDVOC_GREEN- (EXP_TXN10/ SDVOC_GREEN-)	EXP_TXN10	M4
EXP_TXN11/ SDVOC_RED-/ SDVOB_ALPHA-	SDVOC_RED-/ SDVOB_ALPHA- (EXP_TXN11/ SDVOC_RED-/ SDVOB_ALPHA-)	EXP_TXN11	N1
EXP_TXN12/ SDVOB_CLK-	SDVOB_CLK- (EXP_TXN12/ SDVOB_CLK-)	EXP_TXN12	T1
EXP_TXN13/ SDVOB_BLUE-	SDVOB_BLUE- (EXP_TXN13/ SDVOB_BLUE-)	EXP_TXN13	U4
EXP_TXN14/ SDVOB_GREEN-	SDVOB_GREEN- (EXP_TXN14/ SDVOB_GREEN-)	EXP_TXN14	V1
EXP_TXN15/ SDVOB_RED-	SDVOB_RED- (EXP_TXN15/ SDVOB_RED-)	EXP_TXN15	W4
EXP_TXP0	RSV (EXP_TXP0)	EXP_TXP0	D14
EXP_TXP1	RSV (EXP_TXP1)	EXP_TXP1	A13
EXP_TXP2	RSV (EXP_TXP2)	EXP_TXP2	A11
EXP_TXP3	RSV (EXP_TXP3)	EXP_TXP3	C10
EXP_TXP4	RSV (EXP_TXP4)	EXP_TXP4	A9
EXP_TXP5	RSV (EXP_TXP5)	EXP_TXP5	D7
EXP_TXP6	RSV (EXP_TXP6)	EXP_TXP6	A6
EXP_TXP7	RSV (EXP_TXP7)	EXP_TXP7	E2
EXP_TXP8/ SDVOC_CLK+	SDVOC_CLK+ (EXP_TXP8/ SDVOC_CLK+)	EXP_TXP8	G2

EXP_TXP9/ SDVOC_BLUE+	SDVOC_BLUE+ (EXP_TXP9/ SDVOC_BLUE+)	EXP_TXP9	J3
EXP_TXP10/ SDVOC_GREEN+	SDVOC_GREEN+ (EXP_TXP10/ SDVOC_GREEN+)	EXP_TXP10	L4
EXP_TXP11/ SDVOC_RED+/ SDVOB_ALPHA+	SDVOC_RED+/ SDVOB_ALPHA+ (EXP_TXP11/ SDVOC_RED+/ SDVOB_ALPHA+)	EXP_TXP11	M2
EXP_TXP12/ SDVOB_CLK+	SDVOB_CLK+ (EXP_TXP12/ SDVOB_CLK+)	EXP_TXP12	P2
EXP_TXP13/ SDVOB_BLUE+	SDVOB_BLUE+ (EXP_TXP13/ SDVOB_BLUE+)	EXP_TXP13	T4
EXP_TXP14/ SDVOB_GREEN+	SDVOB_GREEN+ (EXP_TXP14/ SDVOB_GREEN+)	EXP_TXP14	U2
EXP_TXP15/ SDVOB_RED+	SDVOB_RED+ (EXP_TXP15/ SDVOB_RED+)	EXP_TXP15	V3
EXTTS#	EXTTS#	EXTTS#	J20
GCLKN	GCLKN	GCLKN	B16
GCLKP	GCLKP	GCLKP	B14
GREEN	GREEN	RSV	K17
GREEN#	GREEN#	RSV	J17
HA3#	HA3#	HA3#	J39
HA4#	HA4#	HA4#	K38
HA5#	HA5#	HA5#	J42
HA6#	HA6#	HA6#	K35
HA7#	HA7#	HA7#	J37
HA8#	HA8#	HA8#	M34
HA9#	HA9#	HA9#	N35
HA10#	HA10#	HA10#	R33
HA11#	HA11#	HA11#	N32
HA12#	HA12#	HA12#	N34
HA13#	HA13#	HA13#	M38
HA14#	HA14#	HA14#	N42
HA15#	HA15#	HA15#	N37
HA16#	HA16#	HA16#	N38
HA17#	HA17#	HA17#	R32
HA18#	HA18#	HA18#	R36
HA19#	HA19#	HA19#	U37
HA20#	HA20#	HA20#	R35

HA21#	HA21#	HA21#	R38
HA22#	HA22#	HA22#	V33
HA23#	HA23#	HA23#	U34
HA24#	HA24#	HA24#	U32
HA25#	HA25#	HA25#	V42
HA26#	HA26#	HA26#	U35
HA27#	HA27#	HA27#	Y36
HA28#	HA28#	HA28#	Y38
HA29#	HA29#	HA29#	AA37
HA30#	HA30#	HA30#	V32
HA31#	HA31#	HA31#	Y34
HACCVREF	HACCVREF	HACCVREF	D28
HADS#	HADS#	HADS#	W42
HADSTB0#	HADSTB0#	HADSTB0#	M36
HADSTB1#	HADSTB1#	HADSTB1#	V35
HBNR#	HBNR#	HBNR#	U39
HBPRI#	HBPRI#	HBPRI#	D42
HBREQ0#	HBREQ0#	HBREQ0#	AA41
HCLKN	HCLKN	HCLKN	M29
HCLKP	HCLKP	HCLKP	M31
HCPURST#	HCPURST#	HCPURST#	C30
HD0	HD0	HD0	P41
HD1	HD1	HD1	M39
HD2	HD2	HD2	P42
HD3	HD3	HD3	M42
HD4	HD4	HD4	N41
HD5	HD5	HD5	M40
HD6	HD6	HD6	L40
HD7	HD7	HD7	M41
HD8	HD8	HD8	K42
HD9	HD9	HD9	G39
HD10	HD10	HD10	J41
HD11	HD11	HD11	G42
HD12	HD12	HD12	G40
HD13	HD13	HD13	G41
HD14	HD14	HD14	F40
HD15	HD15	HD15	F43
HD16	HD16	HD16	F37
HD17	HD17	HD17	E37
HD18	HD18	HD18	J35
HD19	HD19	HD19	D39

HD20	HD20	HD20	C41
HD21	HD21	HD21	B39
HD22	HD22	HD22	B40
HD23	HD23	HD23	H34
HD24	HD24	HD24	C37
HD25	HD25	HD25	J32
HD26	HD26	HD26	B35
HD27	HD27	HD27	J34
HD28	HD28	HD28	B34
HD29	HD29	HD29	F32
HD30	HD30	HD30	L32
HD31	HD31	HD31	J31
HD32	HD32	HD32	H31
HD33	HD33	HD33	M33
HD34	HD34	HD34	K31
HD35	HD35	HD35	M27
HD36	HD36	HD36	K29
HD37	HD37	HD37	F31
HD38	HD38	HD38	H29
HD39	HD39	HD39	F29
HD40	HD40	HD40	L27
HD41	HD41	HD41	M24
HD42	HD42	HD42	J26
HD43	HD43	HD43	K26
HD44	HD44	HD44	G26
HD45	HD45	HD45	H24
HD46	HD46	HD46	K24
HD47	HD47	HD47	F24
HD48	HD48	HD48	E31
HD49	HD49	HD49	A33
HD50	HD50	HD50	E40
HD51	HD51	HD51	D37
HD52	HD52	HD52	C39
HD53	HD53	HD53	D38
HD54	HD54	HD54	D33
HD55	HD55	HD55	C35
HD56	HD56	HD56	D34
HD57	HD57	HD57	C34
HD58	HD58	HD58	B31
HD59	HD59	HD59	C31
HD60	HD60	HD60	C32

HD61	HD61	HD61	D32
HD62	HD62	HD62	B30
HD63	HD63	HD63	D30
HDBSY#	HDBSY#	HDBSY#	U42
HDEFER#	HDEFER#	HDEFER#	P40
HDINV0#	HDINV0#	HDINV0#	K40
HDINV1#	HDINV1#	HDINV1#	A38
HDINV2#	HDINV2#	HDINV2#	E29
HDINV3#	HDINV3#	HDINV3#	B32
HDRDY#	HDRDY#	HDRDY#	V41
HDSTBN0#	HDSTBN0#	HDSTBN0#	L43
HDSTBN1#	HDSTBN1#	HDSTBN1#	G34
HDSTBN2#	HDSTBN2#	HDSTBN2#	M26
HDSTBN3#	HDSTBN3#	HDSTBN3#	B37
HDSTBP0#	HDSTBP0#	HDSTBP0#	K41
HDSTBP1#	HDSTBP1#	HDSTBP1#	F35
HDSTBP2#	HDSTBP2#	HDSTBP2#	J27
HDSTBP3#	HDSTBP3#	HDSTBP3#	E34
HDVREF	HDVREF	HDVREF	D27
HEDRDY#	HEDRDY#	HEDRDY#	Y40
HHIT#	HHIT#	HHIT#	U41
HHITM#	HHITM#	HHITM#	W41
HLOCK#	HLOCK#	HLOCK#	U40
HPCREQ#	HPCREQ#	HPCREQ#	F38
HRCOMP	HRCOMP	HRCOMP	A28
HREQ0#	HREQ0#	HREQ0#	E41
HREQ1#	HREQ1#	HREQ1#	D41
HREQ2#	HREQ2#	HREQ2#	K36
HREQ3#	HREQ3#	HREQ3#	G37
HREQ4#	HREQ4#	HREQ4#	E42
HRS0#	HRS0#	HRS0#	T40
HRS1#	HRS1#	HRS1#	Y43
HRS2#	HRS2#	HRS2#	T43
HSCOMP	HSCOMP	HSCOMP	C27
HSWING	HSWING	HSWING	B27
HSYNC	HSYNC	RSV	D17
HTRDY#	HTRDY#	HTRDY#	W40
ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	M18
NC	NC	NC	BC43
NC	NC	NC	BC42
NC	NC	NC	BC2

NC	NC	NC	BC1
NC	NC	NC	BB43
NC	NC	NC	BB2
NC	NC	NC	BB1
NC	NC	NC	BA2
NC	NC	NC	AW26
NC	NC	NC	AW2
NC	NC	NC	AV27
NC	NC	NC	AV26
NC	NC	NC	E35
NC	NC	NC	C42
NC	NC	NC	C2
NC	NC	NC	B43
NC	NC	NC	B42
NC	NC	NC	B41
NC	NC	NC	B3
NC	NC	NC	B2
NC	NC	NC	A42
PWROK	PWROK	PWROK	AJ9
RED	RED	RSV	F17
RED#	RED#	RSV	G17
REFSET	REFSET	RSV	A20
RSTIN#	RSTIN#	RSTIN#	AJ12
RSV	RSV	RSV	V30
RSV	RSV	RSV	AG29
RSV	RSV	RSV	AJ29
RSV	RSV	RSV	AK27
RSV	RSV	RSV	AL26
RSV	RSV	RSV	AJ21
RSV	RSV	RSV	AL20
RSV	RSV	RSV	AL29
RSV	RSV	RSV	AJ26
RSV	RSV	RSV	AJ23
RSV	RSV	RSV	AK21
RSV	RSV	RSV	AC30
RSV	RSV	RSV	AA30
RSV	RSV	RSV	V31
RSV	RSV	RSV	U30
RSV	RSV	RSV	AD31
RSV	RSV	RSV	AF31
RSV	RSV	RSV	Y33

RSV	RSV	RSV	Y30
RSV	RSV	RSV	AC34
RSV	RSV	RSV	AD30
RSV	RSV	RSV	BC16
RSV	RSV	RSV	AY14
RSV	RSV	RSV	AW18
RSV	RSV	RSV	AW17
RSV	RSV	RSV	AL39
RSV	RSV	RSV	AK40
RSV	RSV	RSV	AJ27
RSV	RSV	RSV	AJ24
RSV	RSV	RSV	AG27
RSV	RSV	RSV	AG26
RSV	RSV	RSV	AG25
RSV	RSV	RSV	M11
RSV	RSV	RSV	A43
RSV	RSV	RSV	R27
RSV	RSV	RSV	U27
RSV	RSV	RSV	M15
RSV	RSV	RSV	L15
RSV	RSV	RSV	AA38
RSV	RSV	RSV	AA34
RSV	RSV	RSV	AA42
RSV	RSV	RSV	AA35
RSV_TP0	RSV_TP0	RSV_TP0	AK17
RSV_TP1	RSV_TP1	RSV_TP1	AL17
RSV_TP2	RSV_TP2	RSV_TP2	AK23
RSV_TP3	RSV_TP3	RSV_TP3	AK18
RSV_TP4	RSV_TP4	RSV_TP4	L21
RSV_TP5	RSV_TP5	RSV_TP5	L18
RSV_TP6	RSV_TP6	RSV_TP6	N21
SBS_A0	SBS_A0	SBS_A0	BC33
SBS_A1	SBS_A1	SBS_A1	AY34
SBS_A2	SBS_A2	SBS_A2	BA26
SBS_B0	SBS_B0	SBS_B0	AW23
SBS_B1	SBS_B1	SBS_B1	AY23
SBS_B2	SBS_B2	SBS_B2	AY17
SCAS_A#	SCAS_A#	SCAS_A#	BA37
SCAS_B#	SCAS_B#	SCAS_B#	AY24
SCKE_A0	SCKE_A0	SCKE_A0	BB25
SCKE_A1	SCKE_A1	SCKE_A1	AY25

SCKE_A2	SCKE_A2	SCKE_A2	BC24
SCKE_A3	SCKE_A3	SCKE_A3	BA25
SCKE_B0	SCKE_B0	SCKE_B0	BA14
SCKE_B1	SCKE_B1	SCKE_B1	AY16
SCKE_B2	SCKE_B2	SCKE_B2	BA13
SCKE_B3	SCKE_B3	SCKE_B3	BB13
SCLK_A0	SCLK_A0	SCLK_A0	BB32
SCLK_A0#	SCLK_A0#	SCLK_A0#	AY32
SCLK_A1	SCLK_A1	SCLK_A1	AY5
SCLK_A1#	SCLK_A1#	SCLK_A1#	BB5
SCLK_A2	SCLK_A2	SCLK_A2	AK42
SCLK_A2#	SCLK_A2#	SCLK_A2#	AK41
SCLK_A3	SCLK_A3	SCLK_A3	BA31
SCLK_A3#	SCLK_A3#	SCLK_A3#	BB31
SCLK_A4	SCLK_A4	SCLK_A4	AY6
SCLK_A4#	SCLK_A4#	SCLK_A4#	BA5
SCLK_A5	SCLK_A5	SCLK_A5	AH40
SCLK_A5#	SCLK_A5#	SCLK_A5#	AH43
SCLK_B0	SCLK_B0	SCLK_B0	AM29
SCLK_B0#	SCLK_B0#	SCLK_B0#	AM27
SCLK_B1	SCLK_B1	SCLK_B1	AV9
SCLK_B1#	SCLK_B1#	SCLK_B1#	AW9
SCLK_B2	SCLK_B2	SCLK_B2	AL38
SCLK_B2#	SCLK_B2#	SCLK_B2#	AL36
SCLK_B3	SCLK_B3	SCLK_B3	AP26
SCLK_B3#	SCLK_B3#	SCLK_B3#	AR26
SCLK_B4	SCLK_B4	SCLK_B4	AU10
SCLK_B4#	SCLK_B4#	SCLK_B4#	AT10
SCLK_B5	SCLK_B5	SCLK_B5	AJ38
SCLK_B5#	SCLK_B5#	SCLK_B5#	AJ36
SCS_A0#	SCS_A0#	SCS_A0#	BB37
SCS_A1#	SCS_A1#	SCS_A1#	BA39
SCS_A2#	SCS_A2#	SCS_A2#	BA35
SCS_A3#	SCS_A3#	SCS_A3#	AY38
SCS_B0#	SCS_B0#	SCS_B0#	BA40
SCS_B1#	SCS_B1#	SCS_B1#	AW41
SCS_B2#	SCS_B2#	SCS_B2#	BA41
SCS_B3#	SCS_B3#	SCS_B3#	AW40
SDM_A0	SDM_A0	SDM_A0	AR3
SDM_A1	SDM_A1	SDM_A1	AY2
SDM_A2	SDM_A2	SDM_A2	BB10

SDM_A3	SDM_A3	SDM_A3	AP18
SDM_A4	SDM_A4	SDM_A4	AT34
SDM_A5	SDM_A5	SDM_A5	AP39
SDM_A6	SDM_A6	SDM_A6	AG40
SDM_A7	SDM_A7	SDM_A7	AC40
SDM_B0	SDM_B0	SDM_B0	AL11
SDM_B1	SDM_B1	SDM_B1	AW7
SDM_B2	SDM_B2	SDM_B2	AP13
SDM_B3	SDM_B3	SDM_B3	AP23
SDM_B4	SDM_B4	SDM_B4	AR29
SDM_B5	SDM_B5	SDM_B5	AR38
SDM_B6	SDM_B6	SDM_B6	AJ39
SDM_B7	SDM_B7	SDM_B7	AD39
SDQ_A0	SDQ_A0	SDQ_A0	AP3
SDQ_A1	SDQ_A1	SDQ_A1	AP2
SDQ_A2	SDQ_A2	SDQ_A2	AU3
SDQ_A3	SDQ_A3	SDQ_A3	AV4
SDQ_A4	SDQ_A4	SDQ_A4	AN1
SDQ_A5	SDQ_A5	SDQ_A5	AP4
SDQ_A6	SDQ_A6	SDQ_A6	AU5
SDQ_A7	SDQ_A7	SDQ_A7	AU2
SDQ_A8	SDQ_A8	SDQ_A8	AW3
SDQ_A9	SDQ_A9	SDQ_A9	AY3
SDQ_A10	SDQ_A10	SDQ_A10	BA7
SDQ_A11	SDQ_A11	SDQ_A11	BB7
SDQ_A12	SDQ_A12	SDQ_A12	AV1
SDQ_A13	SDQ_A13	SDQ_A13	AW4
SDQ_A14	SDQ_A14	SDQ_A14	BC6
SDQ_A15	SDQ_A15	SDQ_A15	AY7
SDQ_A16	SDQ_A16	SDQ_A16	AW12
SDQ_A17	SDQ_A17	SDQ_A17	AY10
SDQ_A18	SDQ_A18	SDQ_A18	BA12
SDQ_A19	SDQ_A19	SDQ_A19	BB12
SDQ_A20	SDQ_A20	SDQ_A20	BA9
SDQ_A21	SDQ_A21	SDQ_A21	BB9
SDQ_A22	SDQ_A22	SDQ_A22	BC11
SDQ_A23	SDQ_A23	SDQ_A23	AY12
SDQ_A24	SDQ_A24	SDQ_A24	AM20
SDQ_A25	SDQ_A25	SDQ_A25	AM18
SDQ_A26	SDQ_A26	SDQ_A26	AV20
SDQ_A27	SDQ_A27	SDQ_A27	AM21

SDQ_A28	SDQ_A28	SDQ_A28	AP17
SDQ_A29	SDQ_A29	SDQ_A29	AR17
SDQ_A30	SDQ_A30	SDQ_A30	AP20
SDQ_A31	SDQ_A31	SDQ_A31	AT20
SDQ_A32	SDQ_A32	SDQ_A32	AP32
SDQ_A33	SDQ_A33	SDQ_A33	AV34
SDQ_A34	SDQ_A34	SDQ_A34	AV38
SDQ_A35	SDQ_A35	SDQ_A35	AU39
SDQ_A36	SDQ_A36	SDQ_A36	AV32
SDQ_A37	SDQ_A37	SDQ_A37	AT32
SDQ_A38	SDQ_A38	SDQ_A38	AR34
SDQ_A39	SDQ_A39	SDQ_A39	AU37
SDQ_A40	SDQ_A40	SDQ_A40	AR41
SDQ_A41	SDQ_A41	SDQ_A41	AR42
SDQ_A42	SDQ_A42	SDQ_A42	AN43
SDQ_A43	SDQ_A43	SDQ_A43	AM40
SDQ_A44	SDQ_A44	SDQ_A44	AU41
SDQ_A45	SDQ_A45	SDQ_A45	AU42
SDQ_A46	SDQ_A46	SDQ_A46	AP41
SDQ_A47	SDQ_A47	SDQ_A47	AN40
SDQ_A48	SDQ_A48	SDQ_A48	AL41
SDQ_A49	SDQ_A49	SDQ_A49	AL42
SDQ_A50	SDQ_A50	SDQ_A50	AF39
SDQ_A51	SDQ_A51	SDQ_A51	AE40
SDQ_A52	SDQ_A52	SDQ_A52	AM41
SDQ_A53	SDQ_A53	SDQ_A53	AM42
SDQ_A54	SDQ_A54	SDQ_A54	AF41
SDQ_A55	SDQ_A55	SDQ_A55	AF42
SDQ_A56	SDQ_A56	SDQ_A56	AD40
SDQ_A57	SDQ_A57	SDQ_A57	AD43
SDQ_A58	SDQ_A58	SDQ_A58	AA39
SDQ_A59	SDQ_A59	SDQ_A59	AA40
SDQ_A60	SDQ_A60	SDQ_A60	AE42
SDQ_A61	SDQ_A61	SDQ_A61	AE41
SDQ_A62	SDQ_A62	SDQ_A62	AB41
SDQ_A63	SDQ_A63	SDQ_A63	AB42
SDQ_B0	SDQ_B0	SDQ_B0	AL6
SDQ_B1	SDQ_B1	SDQ_B1	AL8
SDQ_B2	SDQ_B2	SDQ_B2	AP8
SDQ_B3	SDQ_B3	SDQ_B3	AP9
SDQ_B4	SDQ_B4	SDQ_B4	AJ11

SDQ_B5	SDQ_B5	SDQ_B5	AL9
SDQ_B6	SDQ_B6	SDQ_B6	AM10
SDQ_B7	SDQ_B7	SDQ_B7	AP6
SDQ_B8	SDQ_B8	SDQ_B8	AU7
SDQ_B9	SDQ_B9	SDQ_B9	AV6
SDQ_B10	SDQ_B10	SDQ_B10	AV12
SDQ_B11	SDQ_B11	SDQ_B11	AM11
SDQ_B12	SDQ_B12	SDQ_B12	AR5
SDQ_B13	SDQ_B13	SDQ_B13	AR7
SDQ_B14	SDQ_B14	SDQ_B14	AR12
SDQ_B15	SDQ_B15	SDQ_B15	AR10
SDQ_B16	SDQ_B16	SDQ_B16	AM15
SDQ_B17	SDQ_B17	SDQ_B17	AM13
SDQ_B18	SDQ_B18	SDQ_B18	AV15
SDQ_B19	SDQ_B19	SDQ_B19	AM17
SDQ_B20	SDQ_B20	SDQ_B20	AN12
SDQ_B21	SDQ_B21	SDQ_B21	AR13
SDQ_B22	SDQ_B22	SDQ_B22	AP15
SDQ_B23	SDQ_B23	SDQ_B23	AT15
SDQ_B24	SDQ_B24	SDQ_B24	AM24
SDQ_B25	SDQ_B25	SDQ_B25	AM23
SDQ_B26	SDQ_B26	SDQ_B26	AV24
SDQ_B27	SDQ_B27	SDQ_B27	AM26
SDQ_B28	SDQ_B28	SDQ_B28	AP21
SDQ_B29	SDQ_B29	SDQ_B29	AR21
SDQ_B30	SDQ_B30	SDQ_B30	AP24
SDQ_B31	SDQ_B31	SDQ_B31	AT24
SDQ_B32	SDQ_B32	SDQ_B32	AU27
SDQ_B33	SDQ_B33	SDQ_B33	AN29
SDQ_B34	SDQ_B34	SDQ_B34	AR31
SDQ_B35	SDQ_B35	SDQ_B35	AM31
SDQ_B36	SDQ_B36	SDQ_B36	AP27
SDQ_B37	SDQ_B37	SDQ_B37	AR27
SDQ_B38	SDQ_B38	SDQ_B38	AP31
SDQ_B39	SDQ_B39	SDQ_B39	AU31
SDQ_B40	SDQ_B40	SDQ_B40	AP35
SDQ_B41	SDQ_B41	SDQ_B41	AP37
SDQ_B42	SDQ_B42	SDQ_B42	AN32
SDQ_B43	SDQ_B43	SDQ_B43	AL35
SDQ_B44	SDQ_B44	SDQ_B44	AR35
SDQ_B45	SDQ_B45	SDQ_B45	AU38

SDQ_B46	SDQ_B46	SDQ_B46	AM38
SDQ_B47	SDQ_B47	SDQ_B47	AM34
SDQ_B48	SDQ_B48	SDQ_B48	AL34
SDQ_B49	SDQ_B49	SDQ_B49	AJ34
SDQ_B50	SDQ_B50	SDQ_B50	AF32
SDQ_B51	SDQ_B51	SDQ_B51	AF34
SDQ_B52	SDQ_B52	SDQ_B52	AL31
SDQ_B53	SDQ_B53	SDQ_B53	AJ32
SDQ_B54	SDQ_B54	SDQ_B54	AG35
SDQ_B55	SDQ_B55	SDQ_B55	AD32
SDQ_B56	SDQ_B56	SDQ_B56	AC32
SDQ_B57	SDQ_B57	SDQ_B57	AD34
SDQ_B58	SDQ_B58	SDQ_B58	Y32
SDQ_B59	SDQ_B59	SDQ_B59	AA32
SDQ_B60	SDQ_B60	SDQ_B60	AF35
SDQ_B61	SDQ_B61	SDQ_B61	AF37
SDQ_B62	SDQ_B62	SDQ_B62	AC33
SDQ_B63	SDQ_B63	SDQ_B63	AC35
SDQS_A0	SDQS_A0	SDQS_A0	AU4
SDQS_A0#	SDQS_A0#	SDQS_A0#	AR2
SDQS_A1	SDQS_A1	SDQS_A1	BA3
SDQS_A1#	SDQS_A1#	SDQS_A1#	BB4
SDQS_A2	SDQS_A2	SDQS_A2	AY11
SDQS_A2#	SDQS_A2#	SDQS_A2#	BA10
SDQS_A3	SDQS_A3	SDQS_A3	AU18
SDQS_A3#	SDQS_A3#	SDQS_A3#	AR18
SDQS_A4	SDQS_A4	SDQS_A4	AU35
SDQS_A4#	SDQS_A4#	SDQS_A4#	AV35
SDQS_A5	SDQS_A5	SDQS_A5	AP42
SDQS_A5#	SDQS_A5#	SDQS_A5#	AP40
SDQS_A6	SDQS_A6	SDQS_A6	AG42
SDQS_A6#	SDQS_A6#	SDQS_A6#	AG41
SDQS_A7	SDQS_A7	SDQS_A7	AC42
SDQS_A7#	SDQS_A7#	SDQS_A7#	AC41
SDQS_B0	SDQS_B0	SDQS_B0	AM8
SDQS_B0#	SDQS_B0#	SDQS_B0#	AM6
SDQS_B1	SDQS_B1	SDQS_B1	AV7
SDQS_B1#	SDQS_B1#	SDQS_B1#	AR9
SDQS_B2	SDQS_B2	SDQS_B2	AV13
SDQS_B2#	SDQS_B2#	SDQS_B2#	AT13
SDQS_B3	SDQS_B3	SDQS_B3	AU23

SDQS_B3#	SDQS_B3#	SDQS_B3#	AR23
SDQS_B4	SDQS_B4	SDQS_B4	AT29
SDQS_B4#	SDQS_B4#	SDQS_B4#	AV29
SDQS_B5	SDQS_B5	SDQS_B5	AP36
SDQS_B5#	SDQS_B5#	SDQS_B5#	AM35
SDQS_B6	SDQS_B6	SDQS_B6	AG34
SDQS_B6#	SDQS_B6#	SDQS_B6#	AG32
SDQS_B7	SDQS_B7	SDQS_B7	AD36
SDQS_B7#	SDQS_B7#	SDQS_B7#	AD38
SDVO_CTRLCLK	SDVO_CTRLCLK	RSV	E15
SDVO_CTRLDATA	SDVO_CTRLDATA	RSV	F15
SMVREF0	SMVREF0	SMVREF0	AM4
SMVREF1	SMVREF1	SMVREF1	AM2
SMA_A0	SMA_A0	SMA_A0	BA32
SMA_A1	SMA_A1	SMA_A1	AW32
SMA_A2	SMA_A2	SMA_A2	BB30
SMA_A3	SMA_A3	SMA_A3	BA30
SMA_A4	SMA_A4	SMA_A4	AY30
SMA_A5	SMA_A5	SMA_A5	BA27
SMA_A6	SMA_A6	SMA_A6	BC28
SMA_A7	SMA_A7	SMA_A7	AY27
SMA_A8	SMA_A8	SMA_A8	AY28
SMA_A9	SMA_A9	SMA_A9	BB27
SMA_A10	SMA_A10	SMA_A10	AY33
SMA_A11	SMA_A11	SMA_A11	AW27
SMA_A12	SMA_A12	SMA_A12	BB26
SMA_A13	SMA_A13	SMA_A13	BC38
SMA_B0	SMA_B0	SMA_B0	BB22
SMA_B1	SMA_B1	SMA_B1	BB21
SMA_B2	SMA_B2	SMA_B2	BA21
SMA_B3	SMA_B3	SMA_B3	AY21
SMA_B4	SMA_B4	SMA_B4	BC20
SMA_B5	SMA_B5	SMA_B5	AY19
SMA_B6	SMA_B6	SMA_B6	AY20
SMA_B7	SMA_B7	SMA_B7	BA18
SMA_B8	SMA_B8	SMA_B8	BA19
SMA_B9	SMA_B9	SMA_B9	BB18
SMA_B10	SMA_B10	SMA_B10	BA22
SMA_B11	SMA_B11	SMA_B11	BB17
SMA_B12	SMA_B12	SMA_B12	BA17
SMA_B13	SMA_B13	SMA_B13	AW42

SOCOMP0	SOCOMP0	SOCOMP0	AJ8
SOCOMP1	SOCOMP1	SOCOMP1	AM3
SODT_A0	SODT_A0	SODT_A0	AW37
SODT_A1	SODT_A1	SODT_A1	AY39
SODT_A2	SODT_A2	SODT_A2	AY37
SODT_A3	SODT_A3	SODT_A3	BB40
SODT_B0	SODT_B0	SODT_B0	AY42
SODT_B1	SODT_B1	SODT_B1	AV40
SODT_B2	SODT_B2	SODT_B2	AV43
SODT_B3	SODT_B3	SODT_B3	AU40
SRAS_A#	SRAS_A#	SRAS_A#	BA34
SRAS_B#	SRAS_B#	SRAS_B#	BA23
SRCOMP0	SRCOMP0	SRCOMP0	AL5
SRCOMP1	SRCOMP1	SRCOMP1	AJ6
SWE_A#	SWE_A#	SWE_A#	BB35
SWE_B#	SWE_B#	SWE_B#	BB23
VCC	VCC	VCC	AJ20
VCC	VCC	VCC	AJ18
VCC	VCC	VCC	AJ17
VCC	VCC	VCC	AJ15
VCC	VCC	VCC	AG24
VCC	VCC	VCC	AG23
VCC	VCC	VCC	AG22
VCC	VCC	VCC	AG21
VCC	VCC	VCC	AG20
VCC	VCC	VCC	AG19
VCC	VCC	VCC	AG18
VCC	VCC	VCC	AG17
VCC	VCC	VCC	AG15
VCC	VCC	VCC	AF29
VCC	VCC	VCC	AF27
VCC	VCC	VCC	AF26
VCC	VCC	VCC	AF25
VCC	VCC	VCC	AF23
VCC	VCC	VCC	AF21
VCC	VCC	VCC	AF19
VCC	VCC	VCC	AF17
VCC	VCC	VCC	AF15
VCC	VCC	VCC	AE27
VCC	VCC	VCC	AE26
VCC	VCC	VCC	AE24

VCC	VCC	VCC	AE22
VCC	VCC	VCC	AE20
VCC	VCC	VCC	AE18
VCC	VCC	VCC	AE17
VCC	VCC	VCC	AD26
VCC	VCC	VCC	AD25
VCC	VCC	VCC	AD23
VCC	VCC	VCC	AD21
VCC	VCC	VCC	AD19
VCC	VCC	VCC	AD17
VCC	VCC	VCC	AD15
VCC	VCC	VCC	AC27
VCC	VCC	VCC	AC26
VCC	VCC	VCC	AC24
VCC	VCC	VCC	AC20
VCC	VCC	VCC	AC18
VCC	VCC	VCC	AC17
VCC	VCC	VCC	AC15
VCC	VCC	VCC	AB27
VCC	VCC	VCC	AB26
VCC	VCC	VCC	AB25
VCC	VCC	VCC	AB24
VCC	VCC	VCC	AB20
VCC	VCC	VCC	AB19
VCC	VCC	VCC	AB18
VCC	VCC	VCC	AB17
VCC	VCC	VCC	AA26
VCC	VCC	VCC	AA24
VCC	VCC	VCC	AA20
VCC	VCC	VCC	AA19
VCC	VCC	VCC	AA18
VCC	VCC	VCC	AA17
VCC	VCC	VCC	AA15
VCC	VCC	VCC	Y27
VCC	VCC	VCC	Y25
VCC	VCC	VCC	Y23
VCC	VCC	VCC	Y21
VCC	VCC	VCC	Y19
VCC	VCC	VCC	Y18
VCC	VCC	VCC	Y17
VCC	VCC	VCC	Y15

VCC	VCC	VCC	W27
VCC	VCC	VCC	W26
VCC	VCC	VCC	W24
VCC	VCC	VCC	W22
VCC	VCC	VCC	W20
VCC	VCC	VCC	W19
VCC	VCC	VCC	W18
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VCC	VCC	VCC	V25
VCC	VCC	VCC	V23
VCC	VCC	VCC	V22
VCC	VCC	VCC	V21
VCC	VCC	VCC	V20
VCC	VCC	VCC	V19
VCC	VCC	VCC	V18
VCC	VCC	VCC	V17
VCC	VCC	VCC	V15
VCC	VCC	VCC	U26
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VCC	VCC	VCC	U24
VCC	VCC	VCC	U23
VCC	VCC	VCC	U22
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VCC	VCC	VCC	U20
VCC	VCC	VCC	U19
VCC	VCC	VCC	U18
VCC	VCC	VCC	U17
VCC	VCC	VCC	U15
VCC	VCC	VCC	R24
VCC	VCC	VCC	R23
VCC	VCC	VCC	R21
VCC	VCC	VCC	R20
VCC	VCC	VCC	R18
VCC	VCC	VCC	R17
VCC	VCC	VCC	R15
VCC	VCC	VCC	AK20
VCC	VCC	VCC	AK15
VCC	VCC	VCC	AK14
VCC	VCC	VCC	AK4
VCC	VCC	VCC	AK3

VCC	VCC	VCC	AK2
VCC	VCC	VCC	AJ14
VCC	VCC	VCC	AJ13
VCC	VCC	VCC	AJ5
VCC	VCC	VCC	AH4
VCC	VCC	VCC	AH2
VCC	VCC	VCC	AH1
VCC	VCC	VCC	AG14
VCC	VCC	VCC	AG13
VCC	VCC	VCC	AG12
VCC	VCC	VCC	AG11
VCC	VCC	VCC	AG10
VCC	VCC	VCC	AG9
VCC	VCC	VCC	AG8
VCC	VCC	VCC	AG7
VCC	VCC	VCC	AG6
VCC	VCC	VCC	AG5
VCC	VCC	VCC	AG4
VCC	VCC	VCC	AG3
VCC	VCC	VCC	AG2
VCC	VCC	VCC	AF30
VCC	VCC	VCC	AF14
VCC	VCC	VCC	AF13
VCC	VCC	VCC	AF12
VCC	VCC	VCC	AF11
VCC	VCC	VCC	AF10
VCC	VCC	VCC	AF9
VCC	VCC	VCC	AF8
VCC	VCC	VCC	AF7
VCC	VCC	VCC	AF6
VCC	VCC	VCC	AD14
VCC	VCC	VCC	AC22
VCC	VCC	VCC	AB23
VCC	VCC	VCC	AB22
VCC	VCC	VCC	AB21
VCC	VCC	VCC	AA22
VCC	VCC	VCC	P21
VCC	VCC	VCC	P20
VCC	VCC	VCC	P18
VCC	VCC	VCC	P17
VCC	VCC	VCC	N17

VCC	VCC	VCC	M17
VCC_EXP	VCC_EXP	VCC_EXP	AE4
VCC_EXP	VCC_EXP	VCC_EXP	AE3
VCC_EXP	VCC_EXP	VCC_EXP	AE2
VCC_EXP	VCC_EXP	VCC_EXP	AD12
VCC_EXP	VCC_EXP	VCC_EXP	AD10
VCC_EXP	VCC_EXP	VCC_EXP	AD8
VCC_EXP	VCC_EXP	VCC_EXP	AD6
VCC_EXP	VCC_EXP	VCC_EXP	AD5
VCC_EXP	VCC_EXP	VCC_EXP	AD4
VCC_EXP	VCC_EXP	VCC_EXP	AD2
VCC_EXP	VCC_EXP	VCC_EXP	AD1
VCC_EXP	VCC_EXP	VCC_EXP	AC13
VCC_EXP	VCC_EXP	VCC_EXP	AC6
VCC_EXP	VCC_EXP	VCC_EXP	AC5
VCC_EXP	VCC_EXP	VCC_EXP	AA13
VCC_EXP	VCC_EXP	VCC_EXP	AA5
VCC_EXP	VCC_EXP	VCC_EXP	Y13
VCC_EXP	VCC_EXP	VCC_EXP	V13
VCC_EXP	VCC_EXP	VCC_EXP	V10
VCC_EXP	VCC_EXP	VCC_EXP	V9
VCC_EXP	VCC_EXP	VCC_EXP	V7
VCC_EXP	VCC_EXP	VCC_EXP	V6
VCC_EXP	VCC_EXP	VCC_EXP	V5
VCC_EXP	VCC_EXP	VCC_EXP	U13
VCC_EXP	VCC_EXP	VCC_EXP	U8
VCC_EXP	VCC_EXP	VCC_EXP	U7
VCC_EXP	VCC_EXP	VCC_EXP	U6
VCC_EXP	VCC_EXP	VCC_EXP	R13
VCC_EXP	VCC_EXP	VCC_EXP	R11
VCC_EXP	VCC_EXP	VCC_EXP	R10
VCC_EXP	VCC_EXP	VCC_EXP	R5
VCC_EXP	VCC_EXP	VCC_EXP	N12
VCC_EXP	VCC_EXP	VCC_EXP	N11
VCC_EXP	VCC_EXP	VCC_EXP	N10
VCC_EXP	VCC_EXP	VCC_EXP	N9
VCC_EXP	VCC_EXP	VCC_EXP	N7
VCC_EXP	VCC_EXP	VCC_EXP	N5
VCC2	VCC2	VCC2	D19
VCCA_DAC	VCCA_DAC	VCCA_DAC	C18
VCCA_DAC	VCCA_DAC	VCCA_DAC	B18

VCCA_DPLLA	VCCA_DPLLA	RSV	C19
VCCA_DPLLB	VCCA_DPLLB	RSV	B19
VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	B17
VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	C21
VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	B20
VCCSM	VCCSM	VCCSM	BC40
VCCSM	VCCSM	VCCSM	AY43
VCCSM	VCCSM	VCCSM	BC35
VCCSM	VCCSM	VCCSM	BC31
VCCSM	VCCSM	VCCSM	BC26
VCCSM	VCCSM	VCCSM	BC22
VCCSM	VCCSM	VCCSM	BC18
VCCSM	VCCSM	VCCSM	BC13
VCCSM	VCCSM	VCCSM	BB42
VCCSM	VCCSM	VCCSM	BB38
VCCSM	VCCSM	VCCSM	BB33
VCCSM	VCCSM	VCCSM	BB28
VCCSM	VCCSM	VCCSM	BB24
VCCSM	VCCSM	VCCSM	BB20
VCCSM	VCCSM	VCCSM	BB16
VCCSM	VCCSM	VCCSM	AY41
VCCSM	VCCSM	VCCSM	AW35
VCCSM	VCCSM	VCCSM	AW34
VCCSM	VCCSM	VCCSM	AW31
VCCSM	VCCSM	VCCSM	AW29
VCCSM	VCCSM	VCCSM	AW24
VCCSM	VCCSM	VCCSM	AW21
VCCSM	VCCSM	VCCSM	AW20
VCCSM	VCCSM	VCCSM	AW15
VCCSM	VCCSM	VCCSM	AW13
VCCSM	VCCSM	VCCSM	AV42
VCCSM	VCCSM	VCCSM	AV31
VCCSM	VCCSM	VCCSM	AV23
VCCSM	VCCSM	VCCSM	AV21
VCCSM	VCCSM	VCCSM	AV18
VSS	VSS	VSS	BC4
VSS	VSS	VSS	AY1
VSS	VSS	VSS	AF24
VSS	VSS	VSS	AF22
VSS	VSS	VSS	AF20
VSS	VSS	VSS	AF18

VSS	VSS	VSS	AE25
VSS	VSS	VSS	AE23
VSS	VSS	VSS	AE21
VSS	VSS	VSS	AE19
VSS	VSS	VSS	AD29
VSS	VSS	VSS	AD27
VSS	VSS	VSS	AD24
VSS	VSS	VSS	AD22
VSS	VSS	VSS	AD20
VSS	VSS	VSS	AD18
VSS	VSS	VSS	AC29
VSS	VSS	VSS	AC25
VSS	VSS	VSS	AC19
VSS	VSS	VSS	AA29
VSS	VSS	VSS	AA27
VSS	VSS	VSS	AA25
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VSS	VSS	VSS	U29
VSS	VSS	VSS	R29
VSS	VSS	VSS	R26
VSS	VSS	VSS	D43
VSS	VSS	VSS	D1
VSS	VSS	VSS	A40
VSS	VSS	VSS	A4
VSS	VSS	VSS	BC9
VSS	VSS	VSS	BB41
VSS	VSS	VSS	BB39
VSS	VSS	VSS	BB34
VSS	VSS	VSS	BB19
VSS	VSS	VSS	BB14
VSS	VSS	VSS	BB11

VSS	VSS	VSS	BB6
VSS	VSS	VSS	BB3
VSS	VSS	VSS	BA42
VSS	VSS	VSS	BA4
VSS	VSS	VSS	AW10
VSS	VSS	VSS	AV37
VSS	VSS	VSS	AV17
VSS	VSS	VSS	AV10
VSS	VSS	VSS	AV2
VSS	VSS	VSS	AU34
VSS	VSS	VSS	AU32
VSS	VSS	VSS	AU29
VSS	VSS	VSS	AU26
VSS	VSS	VSS	AU24
VSS	VSS	VSS	AU21
VSS	VSS	VSS	AU20
VSS	VSS	VSS	AU17
VSS	VSS	VSS	AU15
VSS	VSS	VSS	AU13
VSS	VSS	VSS	AU12
VSS	VSS	VSS	AU9
VSS	VSS	VSS	AU6
VSS	VSS	VSS	AT31
VSS	VSS	VSS	AT27
VSS	VSS	VSS	AT26
VSS	VSS	VSS	AT23
VSS	VSS	VSS	AT21
VSS	VSS	VSS	AT18
VSS	VSS	VSS	AT17
VSS	VSS	VSS	AT12
VSS	VSS	VSS	AR43
VSS	VSS	VSS	AR39
VSS	VSS	VSS	AR37
VSS	VSS	VSS	AR32
VSS	VSS	VSS	AR24
VSS	VSS	VSS	AR20
VSS	VSS	VSS	AR15
VSS	VSS	VSS	AR6
VSS	VSS	VSS	AR1
VSS	VSS	VSS	AP38
VSS	VSS	VSS	AP34

VSS	VSS	VSS	AP29
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VSS	VSS	VSS	AP10
VSS	VSS	VSS	AP7
VSS	VSS	VSS	AP5
VSS	VSS	VSS	AN42
VSS	VSS	VSS	AN31
VSS	VSS	VSS	AN27
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VSS	VSS	VSS	AN24
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VSS	VSS	VSS	AN21
VSS	VSS	VSS	AN20
VSS	VSS	VSS	AN18
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VSS	VSS	VSS	AN15
VSS	VSS	VSS	AN13
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VSS	VSS	VSS	AN2
VSS	VSS	VSS	AM39
VSS	VSS	VSS	AM37
VSS	VSS	VSS	AM36
VSS	VSS	VSS	AM33
VSS	VSS	VSS	AM9
VSS	VSS	VSS	AM7
VSS	VSS	VSS	AM5
VSS	VSS	VSS	AL43
VSS	VSS	VSS	AL37
VSS	VSS	VSS	AL33
VSS	VSS	VSS	AL32
VSS	VSS	VSS	AL27
VSS	VSS	VSS	AL24
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VSS	VSS	VSS	AL21
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VSS	VSS	VSS	AL13
VSS	VSS	VSS	AL12
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VSS	VSS	VSS	AL3

VSS	VSS	VSS	AL2
VSS	VSS	VSS	AL1
VSS	VSS	VSS	AK30
VSS	VSS	VSS	AK29
VSS	VSS	VSS	AK26
VSS	VSS	VSS	AK24
VSS	VSS	VSS	AJ37
VSS	VSS	VSS	AJ35
VSS	VSS	VSS	AJ33
VSS	VSS	VSS	AJ31
VSS	VSS	VSS	AJ30
VSS	VSS	VSS	AJ10
VSS	VSS	VSS	AJ7
VSS	VSS	VSS	AH42
VSS	VSS	VSS	AG39
VSS	VSS	VSS	AG38
VSS	VSS	VSS	AG37
VSS	VSS	VSS	AG36
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VSS	VSS	VSS	AG31
VSS	VSS	VSS	AG30
VSS	VSS	VSS	AF43
VSS	VSS	VSS	AF38
VSS	VSS	VSS	AF36
VSS	VSS	VSS	AF33
VSS	VSS	VSS	AF5
VSS	VSS	VSS	AF3
VSS	VSS	VSS	AF2
VSS	VSS	VSS	AF1
VSS	VSS	VSS	AD42
VSS	VSS	VSS	AD37
VSS	VSS	VSS	AD35
VSS	VSS	VSS	AD33
VSS	VSS	VSS	AD13
VSS	VSS	VSS	AD11
VSS	VSS	VSS	AD9
VSS	VSS	VSS	AD7
VSS	VSS	VSS	AC39
VSS	VSS	VSS	AC38
VSS	VSS	VSS	AC37
VSS	VSS	VSS	AC36

VSS	VSS	VSS	AC31
VSS	VSS	VSS	AC23
VSS	VSS	VSS	AC21
VSS	VSS	VSS	AC14
VSS	VSS	VSS	AC10
VSS	VSS	VSS	AC7
VSS	VSS	VSS	AC3
VSS	VSS	VSS	AC2
VSS	VSS	VSS	AB43
VSS	VSS	VSS	AB2
VSS	VSS	VSS	AA36
VSS	VSS	VSS	AA33
VSS	VSS	VSS	AA31
VSS	VSS	VSS	AA23
VSS	VSS	VSS	AA21
VSS	VSS	VSS	AA14
VSS	VSS	VSS	AA12
VSS	VSS	VSS	AA11
VSS	VSS	VSS	AA8
VSS	VSS	VSS	AA3
VSS	VSS	VSS	Y42
VSS	VSS	VSS	Y39
VSS	VSS	VSS	Y37
VSS	VSS	VSS	Y35
VSS	VSS	VSS	Y31
VSS	VSS	VSS	Y14
VSS	VSS	VSS	Y12
VSS	VSS	VSS	Y9
VSS	VSS	VSS	Y6
VSS	VSS	VSS	Y5
VSS	VSS	VSS	Y2
VSS	VSS	VSS	W3
VSS	VSS	VSS	V43
VSS	VSS	VSS	V39
VSS	VSS	VSS	V38
VSS	VSS	VSS	V37
VSS	VSS	VSS	V36
VSS	VSS	VSS	V34
VSS	VSS	VSS	V14
VSS	VSS	VSS	V12
VSS	VSS	VSS	V11

VSS	VSS	VSS	V8
VSS	VSS	VSS	V2
VSS	VSS	VSS	U38
VSS	VSS	VSS	U36
VSS	VSS	VSS	U33
VSS	VSS	VSS	U31
VSS	VSS	VSS	U14
VSS	VSS	VSS	U12
VSS	VSS	VSS	U9
VSS	VSS	VSS	U5
VSS	VSS	VSS	U3
VSS	VSS	VSS	T42
VSS	VSS	VSS	T2
VSS	VSS	VSS	R39
VSS	VSS	VSS	R37
VSS	VSS	VSS	R34
VSS	VSS	VSS	R31
VSS	VSS	VSS	R30
VSS	VSS	VSS	R14
VSS	VSS	VSS	R12
VSS	VSS	VSS	R9
VSS	VSS	VSS	R6
VSS	VSS	VSS	P30
VSS	VSS	VSS	P29
VSS	VSS	VSS	P27
VSS	VSS	VSS	P26
VSS	VSS	VSS	P24
VSS	VSS	VSS	P15
VSS	VSS	VSS	P14
VSS	VSS	VSS	P3
VSS	VSS	VSS	N43
VSS	VSS	VSS	N39
VSS	VSS	VSS	N36
VSS	VSS	VSS	N33
VSS	VSS	VSS	N31
VSS	VSS	VSS	N29
VSS	VSS	VSS	N27
VSS	VSS	VSS	N26
VSS	VSS	VSS	N24
VSS	VSS	VSS	N15
VSS	VSS	VSS	N13

VSS	VSS	VSS	N8
VSS	VSS	VSS	N6
VSS	VSS	VSS	N2
VSS	VSS	VSS	M37
VSS	VSS	VSS	M35
VSS	VSS	VSS	M21
VSS	VSS	VSS	M20
VSS	VSS	VSS	M13
VSS	VSS	VSS	M10
VSS	VSS	VSS	M9
VSS	VSS	VSS	M8
VSS	VSS	VSS	M5
VSS	VSS	VSS	M3
VSS	VSS	VSS	L42
VSS	VSS	VSS	L31
VSS	VSS	VSS	L29
VSS	VSS	VSS	L26
VSS	VSS	VSS	L24
VSS	VSS	VSS	L13
VSS	VSS	VSS	L12
VSS	VSS	VSS	L2
VSS	VSS	VSS	K39
VSS	VSS	VSS	K37
VSS	VSS	VSS	K34
VSS	VSS	VSS	K32
VSS	VSS	VSS	K27
VSS	VSS	VSS	K20
VSS	VSS	VSS	K15
VSS	VSS	VSS	K13
VSS	VSS	VSS	K12
VSS	VSS	VSS	K10
VSS	VSS	VSS	K7
VSS	VSS	VSS	K6
VSS	VSS	VSS	K5
VSS	VSS	VSS	K3
VSS	VSS	VSS	J43
VSS	VSS	VSS	J38
VSS	VSS	VSS	J29
VSS	VSS	VSS	J24
VSS	VSS	VSS	J21
VSS	VSS	VSS	J12

VSS	VSS	VSS	J10
VSS	VSS	VSS	J7
VSS	VSS	VSS	J5
VSS	VSS	VSS	J2
VSS	VSS	VSS	H32
VSS	VSS	VSS	H27
VSS	VSS	VSS	H26
VSS	VSS	VSS	H17
VSS	VSS	VSS	H12
VSS	VSS	VSS	G38
VSS	VSS	VSS	G35
VSS	VSS	VSS	G32
VSS	VSS	VSS	G31
VSS	VSS	VSS	G29
VSS	VSS	VSS	G27
VSS	VSS	VSS	G24
VSS	VSS	VSS	G21
VSS	VSS	VSS	G20
VSS	VSS	VSS	G18
VSS	VSS	VSS	G15
VSS	VSS	VSS	G13
VSS	VSS	VSS	G10
VSS	VSS	VSS	G9
VSS	VSS	VSS	G7
VSS	VSS	VSS	G5
VSS	VSS	VSS	G3
VSS	VSS	VSS	F42
VSS	VSS	VSS	F34
VSS	VSS	VSS	F26
VSS	VSS	VSS	F18
VSS	VSS	VSS	F13
VSS	VSS	VSS	F6
VSS	VSS	VSS	F2
VSS	VSS	VSS	E32
VSS	VSS	VSS	E21
VSS	VSS	VSS	E20
VSS	VSS	VSS	E18
VSS	VSS	VSS	E17
VSS	VSS	VSS	E13
VSS	VSS	VSS	E12
VSS	VSS	VSS	E9

VSS	VSS	VSS	E7
VSS	VSS	VSS	E4
VSS	VSS	VSS	E3
VSS	VSS	VSS	D21
VSS	VSS	VSS	D20
VSS	VSS	VSS	D16
VSS	VSS	VSS	D10
VSS	VSS	VSS	D5
VSS	VSS	VSS	D2
VSS	VSS	VSS	C40
VSS	VSS	VSS	C22
VSS	VSS	VSS	C14
VSS	VSS	VSS	C12
VSS	VSS	VSS	C7
VSS	VSS	VSS	C5
VSS	VSS	VSS	C3
VSS	VSS	VSS	B38
VSS	VSS	VSS	B33
VSS	VSS	VSS	B28
VSS	VSS	VSS	B22
VSS	VSS	VSS	B21
VSS	VSS	VSS	B13
VSS	VSS	VSS	B11
VSS	VSS	VSS	B9
VSS	VSS	VSS	B6
VSS	VSS	VSS	B4
VSS	VSS	VSS	A35
VSS	VSS	VSS	A31
VSS	VSS	VSS	A26
VSS	VSS	VSS	A22
VSS	VSS	VSS	A16
VSS	VSS	VSS	L17
VSSA_DAC	VSSA_DAC	VSSA_DAC	A18
VSYNC	VSYNC	RSV	C17
VTT	VTT	VTT	P23
VTT	VTT	VTT	N23
VTT	VTT	VTT	M23
VTT	VTT	VTT	L23
VTT	VTT	VTT	K23
VTT	VTT	VTT	J23
VTT	VTT	VTT	H23

VTT	VTT	VTT	G23
VTT	VTT	VTT	F27
VTT	VTT	VTT	F23
VTT	VTT	VTT	E27
VTT	VTT	VTT	E26
VTT	VTT	VTT	E24
VTT	VTT	VTT	E23
VTT	VTT	VTT	D25
VTT	VTT	VTT	D24
VTT	VTT	VTT	D23
VTT	VTT	VTT	C26
VTT	VTT	VTT	C25
VTT	VTT	VTT	C23
VTT	VTT	VTT	B26
VTT	VTT	VTT	B25
VTT	VTT	VTT	B24
VTT	VTT	VTT	B23
VTT	VTT	VTT	A24
XORTEST	XORTEST	XORTEST	H20

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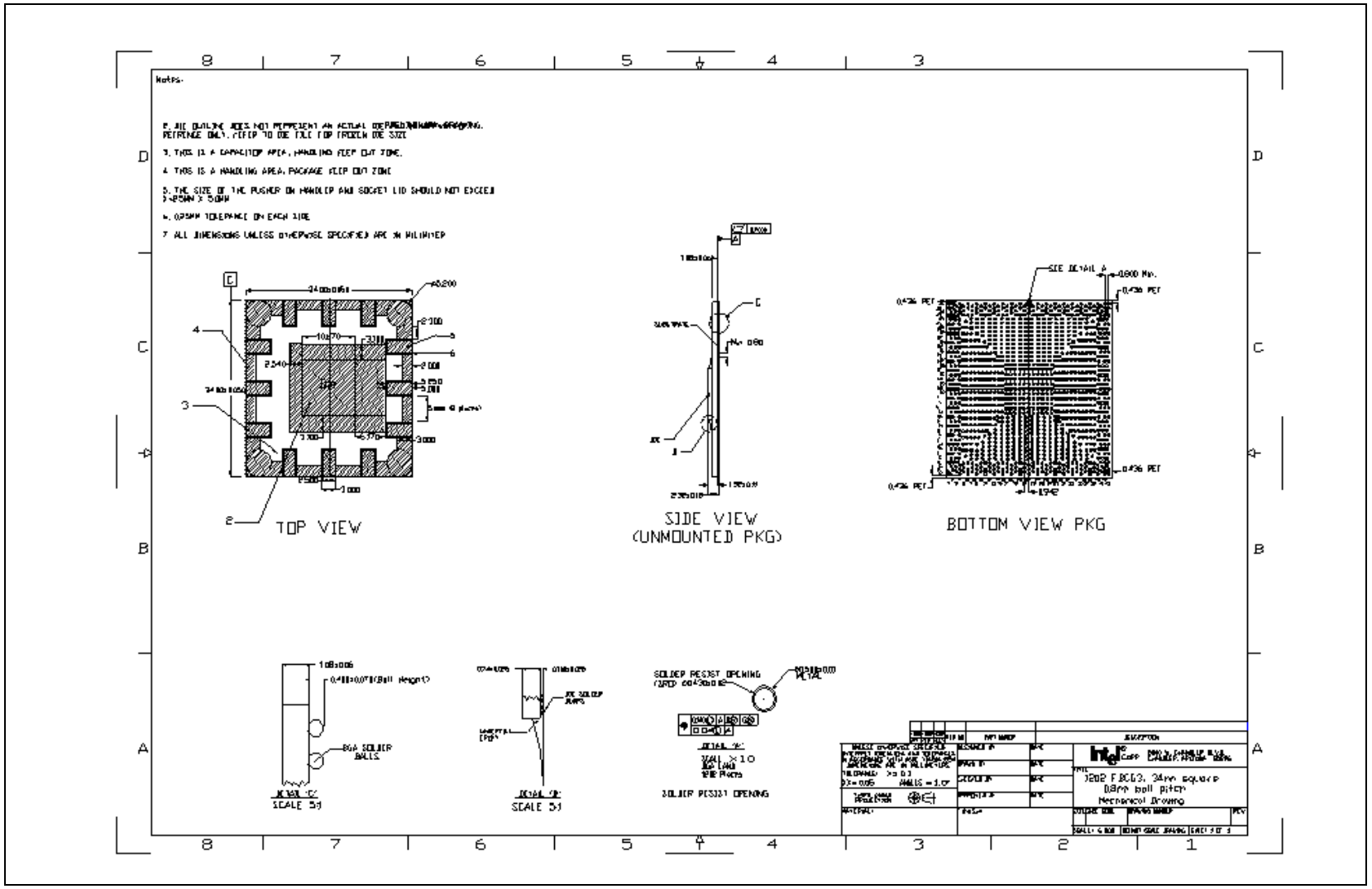
12.3 Package

The (G)MCH package measures 34 mm × 34 mm. The 1202 balls are located in a non-grid pattern. The package dimensions are shown in Figure 12-4.

Figure 12-4. (G)MCH Package Dimensions



13 Testability

In the (G)MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it.

13.1 Complimentary Pins

Table 13-1 contains pins that must remain complimentary while performing XOR testing. The first and third column contain the pin and its compliment. The second and fourth column specify which chain the associated pins are on.

Table 13-1. Complimentary Pins to Drive

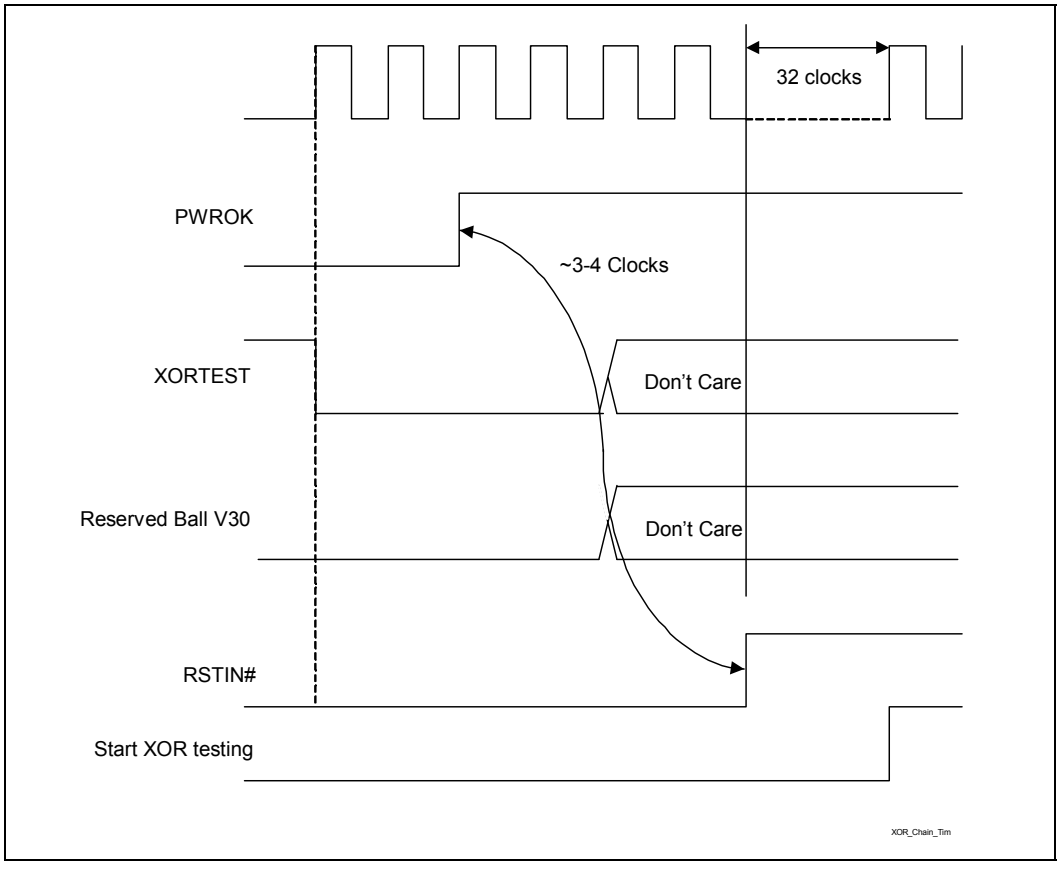
Complimentary Pin	XOR Chain	Complimentary Pin	XOR Chain
SDQS_A0	Not in XOR Chain	SDQS_A0#	4
SDQS_A1	Not in XOR Chain	SDQS_A1#	4
SDQS_A2	Not in XOR Chain	SDQS_A2#	4
SDQS A3	Not in XOR Chain	SDQS_A3#	4
SDQS_A4	Not in XOR Chain	SDQS_A4#	4
SDQS_A5	Not in XOR Chain	SDQS_A5#	4
SDQS_A6	Not in XOR Chain	SDQS_A6#	4
SDQS_A7	Not in XOR Chain	SDQS_A7#	4
SDQS_B0	Not in XOR Chain	SDQS_B0#	5
SDQS_B1	Not in XOR Chain	SDQS_B1#	5
SDQS_B2	Not in XOR Chain	SDQS_B2#	5
SDQS_B3	Not in XOR Chain	SDQS_B3#	5
SDQS_B4	Not in XOR Chain	SDQS_B4#	5
SDQS_B5	Not in XOR Chain	SDQS_B5#	5
SDQS_B6	Not in XOR Chain	SDQS_B6#	5
SDQS_B7	Not in XOR Chain	SDQS_B7#	5

13.2 XOR Test Mode Initialization

XOR test mode can be entered by pulling a Reserved ball (ball V30) and XORTEST (ball H20) low through the de-assertion of external reset (RSTIN# at ball AJ12). It was intended that no clocks should be required to enter this test mode; however, it is recommended that customers use the following sequence.

On power up, hold PWROK (ball AJ9), RSTIN# (ball AJ12), and a Reserved ball (ball V30) low and start external clocks. After a few clock cycles, pull PWROK high. After ~3–4 clocks, de-assert RSTIN# (pull it high). Release the Reserved ball (ball V30) and XORTEST. No external drive. Allow the clocks to run for an additional 32 clocks. Begin testing the XOR chains. Refer to Figure 13-1.

Figure 13-1. XOR Test Mode Initialization Cycles



13.3 XOR Chain Definition

The (G)MCH chipset has 10 XOR chains. The XOR chain outputs are driven out on the following output pins. During fullwidth testing, XOR chain outputs will be visible on both pins.

Table 13-2. XOR Chain Outputs

XOR Chain	Output Pins	Coordinate Location
xor_out0	BSEL2	L20
xor_out1	ALLZTEST	K18
xor_out2	XORTEST	H20
xor_out3	RSV_TP5	L18
xor_out4	EXP_SLR	K21
xor_out5	RSV_TP4	L21
xor_out6	EXP_EN	F20
xor_out7	RSV_TP6	N21
xor_out8	BSEL1	H21
xor_out9	BSEL0	F21

13.4 XOR Chains

Table 13-3 through Table 13-12 show the XOR chains. Section 13.5 has a pin exclusion list.

Table 13-3. XOR Chain 0

Pin Count	Ball #	Signal Name
1	M11	RSV_TP7[1]
2	N18	DDC_DATA[1]
3	E15	SDVO_CTRLCLK[1]
4	F15	SDVO_CTRLDATA[1]
5	N20	DDC_CLK[1]
6	M18	ICH_SYNC#
7	J20	EXTTS#
8	J26	HD42#
9	M24	HD41#
10	F24	HD47#
11	G26	HD44#
12	K26	HD43#
13	H24	HD45#
14	M27	HD35#
15	L27	HD40#
16	J27	HDSTBP2#
17	M26	HDSTBN2#
18	K24	HD46#
19	C30	HCPURST#
20	H29	HD38#
21	H31	HD32#
22	K31	HD34#
23	F31	HD37#
24	K29	HD36#
25	M33	HD33#
26	E29	HDINV2#
27	F29	HD39#
28	B31	HD58#
29	B32	HDINV3#
30	C39	HD52#
31	A33	HD49#
32	B30	HD62#
33	D32	HD61#
34	C31	HD59#

Table 13-3. XOR Chain 0

Pin Count	Ball #	Signal Name
35	C32	HD60#
36	D33	HD54#
37	C34	HD57#
38	E34	HDSTBP3#
39	B37	HDSTBN3#
40	D30	HD63#
41	D38	HD53#
42	E31	HD48#
43	E40	HD50#
44	D34	HD56#
45	C35	HD55#
46	D37	HD51#
47	B34	HD28#
48	A38	HDINV1#
49	B39	HD21#
50	F32	HD29#
51	H34	HD23#
52	J32	HD25#
53	C37	HD24#
54	E37	HD17#
55	F35	HDSTBP1#
56	G34	HDSTBN1#
57	B35	HD26#
58	B40	HD22#
59	J31	HD31#
60	D39	HD19#
61	J34	HD27#
62	C41	HD20#
63	L32	HD30#
64	J35	HD18#
65	F37	HD16#
66	F43	HD15#
67	K41	HDSTBP0#
68	G41	HD13#

Table 13-3. XOR Chain 0

Pin Count	Ball #	Signal Name
69	L40	HD6#
70	M39	HD1#
71	D41	HREQ1#
72	K38	HAB4#
73	J42	HAB5#
74	K35	HAB6#
75	N34	HAB12#
76	N37	HAB15#
77	P40	HDEFER#
78	U42	HDBSY#
79	Y40	HEDRDY#
80	D42	HBPRI#

NOTES:
1. Intel® 82945G/82945GC/82945GZ GMCH Only.

Table 13-4. XOR Chain 1

Pin Count	Ball #	Signal Name
1	G42	HD11#
2	F40	HD14#
3	K42	HD8#
4	G40	HD12#
5	L43	HDSTBN0#
6	G39	HD9#
7	P42	HD2#
8	M42	HD3#
9	M41	HD7#
10	P41	HD0#
11	N41	HD4#
12	M40	HD5#
13	K40	HDINV0#
14	J41	HD10#
15	G37	HREQ3#
16	J39	HAB3#
17	K36	HREQ2#
18	M36	HADSTB0#
19	E41	HREQ0#
20	J37	HAB7#

Table 13-4. XOR Chain 1

21	E42	HREQ4#
22	N42	HAB14#
23	M38	HAB13#
24	R33	HAB10#
25	M34	HAB8#
26	N32	HAB11#
27	N38	HAB16#
28	N35	HAB9#
29	F38	HPCREQ#
30	T43	HRS2#
31	T40	HRS0#
32	U41	HHIT#
33	V41	HDRDY#
34	W41	HHITM#
35	W42	HADS#
36	U40	HLOCK#
37	Y43	HRS1#
38	U39	HBNR#
39	W40	HTRDY#
40	R32	HAB17#
41	U37	HAB19#
42	R36	HAB18#
43	U35	HAB26#
44	R35	HAB20#
45	U34	HAB23#
46	R38	HAB21#
47	AA41	HBREQ0#
48	Y34	HAB31#
49	V35	HADSTB1#
50	V33	HAB22#
51	U32	HAB24#
52	V42	HAB25#
53	V32	HAB30#
54	Y36	HAB27#
55	Y38	HAB28#
56	AA37	HAB29#

Table 13-5. XOR Chain 2

Pin Count	Ball #	Signal Name
1	AC40	SDM_A7
2	AB41	SDQ_A62
3	AA39	SDQ_A58
4	AB42	SDQ_A63
5	AD40	SDQ_A56
6	AE41	SDQ_A61
7	AE42	SDQ_A60
8	AA40	SDQ_A59
9	AD43	SDQ_A57
10	AM42	SDQ_A53
11	AL41	SDQ_A48
12	AF42	SDQ_A55
13	AE40	SDQ_A51
14	AF39	SDQ_A50
15	AH43	SCLK_A5#
16	AK42	SCLK_A2
17	AR42	SDQ_A41
18	AP41	SDQ_A46
19	AN40	SDQ_A47
20	AP39	SDM_A5
21	AM40	SDQ_A43
22	BB40	SODT_A3
23	AW37	SODT_A0
24	AY38	SCS_A3#
25	AV38	SDQ_A34
26	AT34	SDM_A4
27	AV32	SDQ_A36
28	BC33	SBS_A0
29	BB37	SCS_A0#
30	BA39	SCS_A1#
31	BB35	SWE_A#
32	AY34	SBS_A1
33	BA35	SCS_A2#
34	AY28	SMA_A8
35	BA30	SMA_A3
36	BB26	SMA_A12
37	AY32	SCLK_A0#
38	AW27	SMA_A11
39	AY25	SCKE_A1

Table 13-6. XOR Chain 3

Pin Count	Ball #	Signal Name
1	AD34	SDQ_B57
2	Y32	SDQ_B58
3	AC33	SDQ_B62
4	AA32	SDQ_B59
5	AC32	SDQ_B56
6	AD39	SDM_B7
7	AF37	SDQ_B61
8	BB23	SWE_B#
9	AC35	SDQ_B63
10	AF35	SDQ_B60
11	AL36	SCLK_B2#
12	AF32	SDQ_B50
13	AL34	SDQ_B48
14	AJ34	SDQ_B49
15	AD32	SDQ_B55
16	AL31	SDQ_B52
17	BA41	SCS_B2#
18	AW41	SCS_B1#
19	AU40	SODT_B3
20	AV40	SODT_B1
21	AM38	SDQ_B46
22	AL35	SDQ_B43
23	AP35	SDQ_B40
24	AR35	SDQ_B44
25	AW42	SMA_B13
26	AR31	SDQ_B34
27	AU27	SDQ_B32
28	AU31	SDQ_B39
29	AR26	SCLK_B3#
30	BA22	SMA_B10
31	BA17	SMA_B12
32	AY21	SMA_B3
33	AY20	SMA_B6
34	AM26	SDQ_B27
35	AM24	SDQ_B24
36	AP21	SDQ_B28
37	BA14	SCKE_B0
38	BA13	SCKE_B2

Table 13-6. XOR Chain 3

Pin Count	Ball #	Signal Name
39	AT15	SDQ_B23
40	AM17	SDQ_B19
41	AR13	SDQ_B21
42	AV9	SCLK_B1

Table 13-7. XOR Chain 4

Pin Count	Ball #	Signal Name
1	AC41	SDQS_A7#
2	AG41	SDQS_A6#
3	AM41	SDQ_A52
4	AG40	SDM_A6
5	AL42	SDQ_A49
6	AF41	SDQ_A54
7	AH40	SCLK_A5
8	AK41	SCLK_A2#
9	AP40	SDQS_A5#
10	AN43	SDQ_A42
11	AU41	SDQ_A44
12	AU42	SDQ_A45
13	AR41	SDQ_A40
14	AY39	SODT_A1
15	AY37	SODT_A2
16	AV35	SDQS_A4#
17	AU39	SDQ_A35
18	AT32	SDQ_A37
19	AV34	SDQ_A33
20	BA34	SRAS_A#
21	BB31	SCLK_A3#
22	BC38	SMA_A13
23	BC28	SMA_A6
24	BB27	SMA_A9
25	BA27	SMA_A5
26	AY27	SMA_A7
27	BB25	SCKE_A0
28	AR18	SDQS_A3#
29	AM21	SDQ_A27
30	AM18	SDQ_A25

Table 13-7. XOR Chain 4

Pin Count	Ball #	Signal Name
31	AR17	SDQ_A29
32	AM20	SDQ_A24
33	BA10	SDQS_A2#
34	BA12	SDQ_A18
35	BB12	SDQ_A19
36	BB10	SDM_A2
37	AY6	SCLK_A4
38	BB5	SCLK_A1#
39	BC6	SDQ_A14
40	BA7	SDQ_A10
41	AW3	SDQ_A8
42	AY2	SDM_A1
43	BB4	SDQS_A1#
44	AR2	SDQS_A0#
45	AK17	RSV_TP0
46	AP4	SDQ_A5

Table 13-8. XOR Chain 5

Pin Count	Ball #	Signal Name
1	AD38	SDQS_B7#
2	AJ36	SCLK_B5#
3	AL38	SCLK_B2
4	AG35	SDQ_B54
5	AJ39	SDM_B6
6	AF34	SDQ_B51
7	AJ32	SDQ_B53
8	AG32	SDQS_B6#
9	BA40	SCS_B0#
10	AW40	SCS_B3#
11	AV43	SODT_B2
12	AY42	SODT_B0
13	AU38	SDQ_B45
14	AR38	SDM_B5
15	AM34	SDQ_B47
16	AP37	SDQ_B41
17	AN32	SDQ_B42
18	AM35	SDQS_B5#

Table 13-8. XOR Chain 5

Pin Count	Ball #	Signal Name
19	AM31	SDQ_B35
20	AR27	SDQ_B37
21	AR29	SDM_B4
22	AV29	SDQS_B4#
23	AM29	SCLK_B0
24	AY24	SCAS_B#
25	BA23	SRAS_B#
26	BB18	SMA_B9
27	AY17	SBS_B2
28	BB21	SMA_B1
29	BA18	SMA_B7
30	BA19	SMA_B8
31	AV24	SDQ_B26
32	AM23	SDQ_B25
33	AR21	SDQ_B29
34	AR23	SDQS_B3#
35	BB13	SCKE_B3
36	AP15	SDQ_B22
37	AM13	SDQ_B17
38	AM15	SDQ_B16
39	AT13	SDQS_B2#
40	AT10	SCLK_B4#
41	AV12	SDQ_B10
42	AM11	SDQ_B11
43	AR5	SDQ_B12
44	AR9	SDQS_B1#
45	AM6	SDQS_B0#
46	AJ11	SDQ_B4
47	AP6	SDQ_B7
48	AP8	SDQ_B2

Table 13-9. XOR Chain 6

Pin Count	Ball #	Signal Name
1	AU37	SDQ_A39
2	AR34	SDQ_A38
3	AP32	SDQ_A32
4	BA37	SCAS_A#

Table 13-9. XOR Chain 6

Pin Count	Ball #	Signal Name
5	BA31	SCLK_A3
6	AY33	SMA_A10
7	BA32	SMA_A0
8	AY30	SMA_A4
9	AW32	SMA_A1
10	BB32	SCLK_A0
11	BB30	SMA_A2
12	BA26	SBS_A2
13	BC24	SCKE_A2
14	BA25	SCKE_A3
15	AV20	SDQ_A26
16	AP20	SDQ_A30
17	AP18	SDM_A3
18	AT20	SDQ_A31
19	AP17	SDQ_A28
20	AW12	SDQ_A16
21	AY12	SDQ_A23
22	BC11	SDQ_A22
23	AY10	SDQ_A17
24	BB9	SDQ_A21
25	BA9	SDQ_A20
26	BA5	SCLK_A4#
27	AY5	SCLK_A1
28	AY7	SDQ_A15
29	BB7	SDQ_A11
30	AW4	SDQ_A13
31	AY3	SDQ_A9
32	AV1	SDQ_A12
33	AP3	SDQ_A0
34	AR3	SDM_A0
35	AV4	SDQ_A3
36	AU5	SDQ_A6
37	AN1	SDQ_A4
38	AU3	SDQ_A2
39	AU2	SDQ_A7
40	AP2	SDQ_A1

Table 13-10. XOR Chain 7

Pin Count	Ball #	Signal Name
1	AN29	SDQ_B33
2	AP31	SDQ_B38
3	AP27	SDQ_B36
4	AM27	SCLK_B0#
5	AP26	SCLK_B3
6	AW23	SBS_B0
7	AY23	SBS_B1
8	BC20	SMA_B4
9	BB22	SMA_B0
10	BB17	SMA_B11
11	BA21	SMA_B2
12	AY19	SMA_B5
13	AT24	SDQ_B31
14	AP24	SDQ_B30
15	AP23	SDM_B3
16	AY16	SCKE_B1
17	AV15	SDQ_B18
18	AP13	SDM_B2
19	AN12	SDQ_B20
20	AW9	SCLK_B1#
21	AU10	SCLK_B4
22	AU7	SDQ_B8
23	AR10	SDQ_B15
24	AR12	SDQ_B14
25	AW7	SDM_B1
26	AR7	SDQ_B13
27	AV6	SDQ_B9
28	AL11	SDM_B0
29	AL6	SDQ_B0
30	AL9	SDQ_B5
31	AM10	SDQ_B6
32	AP9	SDQ_B3
33	AL8	SDQ_B1

Table 13-11. XOR Chain 8

Pin Count	Ball #	Signal Name
1	F12	EXP_RXN0
2	C13	EXP_TXN0
3	D12	EXP_RXN1
4	B12	EXP_TXN1
5	H13	EXP_RXN2
6	B10	EXP_TXN2
7	F10	EXP_RXN3
8	C9	EXP_TXN3
9	H10	EXP_RXN4
10	B7	EXP_TXN4
11	F9	EXP_RXN5
12	D6	EXP_TXN5
13	D3	EXP_RXN6
14	B5	EXP_TXN6
15	J6	EXP_RXN7
16	F1	EXP_TXN7
17	K8	EXP_RXN8
18	J1	EXP_TXN8
19	G4	EXP_RXN9
20	K4	EXP_TXN9
21	M7	EXP_RXN10
22	M4	EXP_TXN10
23	L1	EXP_RXN11
24	N1	EXP_TXN11
25	U10	EXP_RXN12
26	T1	EXP_TXN12
27	R7	EXP_RXN13
28	U4	EXP_TXN13
29	N3	EXP_RXN14
30	V1	EXP_TXN14
31	Y11	EXP_RXN15
32	W4	EXP_TXN15
33	G12	EXP_RXP0
34	D14	EXP_TXP0
35	D11	EXP_RXP1
36	A13	EXP_TXP1
37	J13	EXP_RXP2
38	A11	EXP_TXP2
39	E10	EXP_RXP3

Table 13-11. XOR Chain 8

Pin Count	Ball #	Signal Name
40	C10	EXP_TXP3
41	J9	EXP_RXP4
42	A9	EXP_TXP4
43	F7	EXP_RXP5
44	D7	EXP_TXP5
45	C4	EXP_RXP6
46	A6	EXP_TXP6
47	G6	EXP_RXP7
48	E2	EXP_TXP7
49	K9	EXP_RXP8
50	G2	EXP_TXP8
51	F4	EXP_RXP9
52	J3	EXP_TXP9
53	M6	EXP_RXP10
54	L4	EXP_TXP10
55	K2	EXP_RXP11
56	M2	EXP_TXP11
57	U11	EXP_RXP12
58	P2	EXP_TXP12
59	R8	EXP_RXP13
60	T4	EXP_TXP13
61	P4	EXP_RXP14
62	U2	EXP_TXP14
63	Y10	EXP_RXP15
64	V3	EXP_TXP15

Table 13-12. XOR Chain 9

Pin Count	Ball #	Signal Name
1	Y8	DMI_RXN0
2	Y7	DMI_RXP0
3	Y1	DMI_TXN0
4	W2	DMI_TXP0
5	AA10	DMI_RXN1
6	AA9	DMI_RXP1
7	AB1	DMI_TXN1
8	AA2	DMI_TXP1
9	AA7	DMI_RXN2
10	AA6	DMI_RXP2
11	AA4	DMI_TXN2
12	Y4	DMI_TXP2
13	AC8	DMI_RXN3
14	AC9	DMI_RXP3
15	AC4	DMI_TXN3
16	AB3	DMI_TXP3

13.5 PADs Excluded from XOR Mode(s)

A large number of pads do not support XOR testing. The majority of the pads that fall into this category are analog related pins (see Table 13-13).

Table 13-13. XOR Pad Exclusion List

PCI Express*	FSB	SM	Misc
GCLKN	HCLKN	SRCOMP1	DREFCLKN
GCLKP	HCLKP	SRCOMP0	DREFCLKP
EXP_COMPO	HRCOMP	SMVREF1	BLUE
EXP_COMPI	HSCOMP	SMVREF0	BLUE#
	HVREF	SOCOMP1	GREEN
	HSWING	SOCOMP0	GREEN#
		SM_SLEWOUT1	RED
		SM_SLEWOUT0	RED#
		SM_SLEWIN1	RSTIN#
		SM_SLEWIN0	HSYNC
			VSYNC
			REFSET