

Super mini DIIPM Ver.5 Series APPLICATION NOTE

PS219Bx -S/-ST/-AS/-AST/-CS/CST

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CHAPTER 1 INTRODUCTION

1.1 Features of Super mini DIIPM Ver.5

Super Mini DIIPM Ver.5 (hereinafter called DIP Ver.5) is an ultra-small compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which make it easy for AC100-240V class low power motor inverter control. Current Super mini DIIPM Ver.4 series are most suitable for inverterized white goods because of our unique high efficiency power chips CSTBT, insulated sheet structure with very low thermal resistance and ultra small package. While the DIP Ver.5 keeps these features of Ver.4, it makes further progress. Main features of DIP Ver.5 are as below.

- **Newly developed 6th generation CSTBT are integrated for improving efficiency.**
- **Incorporating bootstrap diode with current limiting resistor for P-side gate driving supply**
- **Selectable new function for outputting package(control IC) temperature by analog signal**
- **Easy to replace from current Ver.4 due to high pin compatibility**

About detailed differences, please refer Section 1.5. Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.

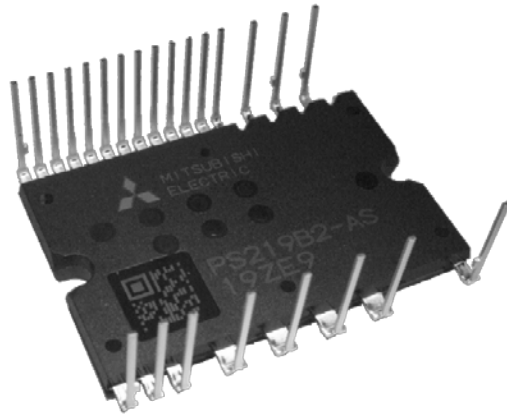


Fig.1-1-1 Package photograph

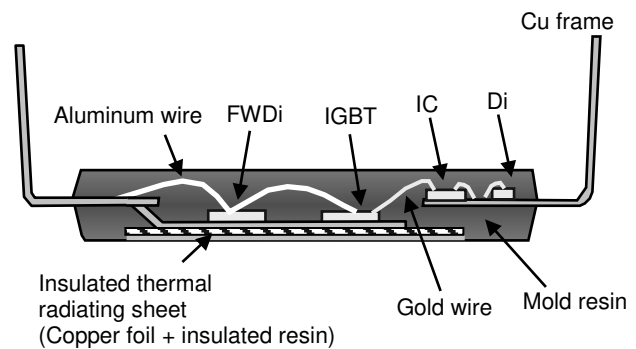


Fig.1-1-2 Internal cross-section structure

1.2 Functions

DIP Ver.5 has following functions and inner block diagram is described in Fig.1-2-1.

- For P-side IGBTs:
 - Drive circuit;
 - High voltage level shift circuit;
 - Control supply under voltage (UV) lockout circuit (without fault signal output).
 - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side IGBTs:
 - Drive circuit;
 - Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
 - Control supply under voltage (UV) lockout circuit (with fault signal output)
 - Over temperature (OT) protection by monitoring LVIC temperature. (-T series only)
 - Outputting LVIC temperature by analog signal (Need to select from this function or OT)
- Fault Signal Output
 - Corresponding to N-side IGBT SC, N-side UV and OT protection.
- IGBT Drive Supply
 - Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
 - Schmitt-triggered 3V,5V input compatible, high active logic.
- UL recognized : UL1557 File E323585

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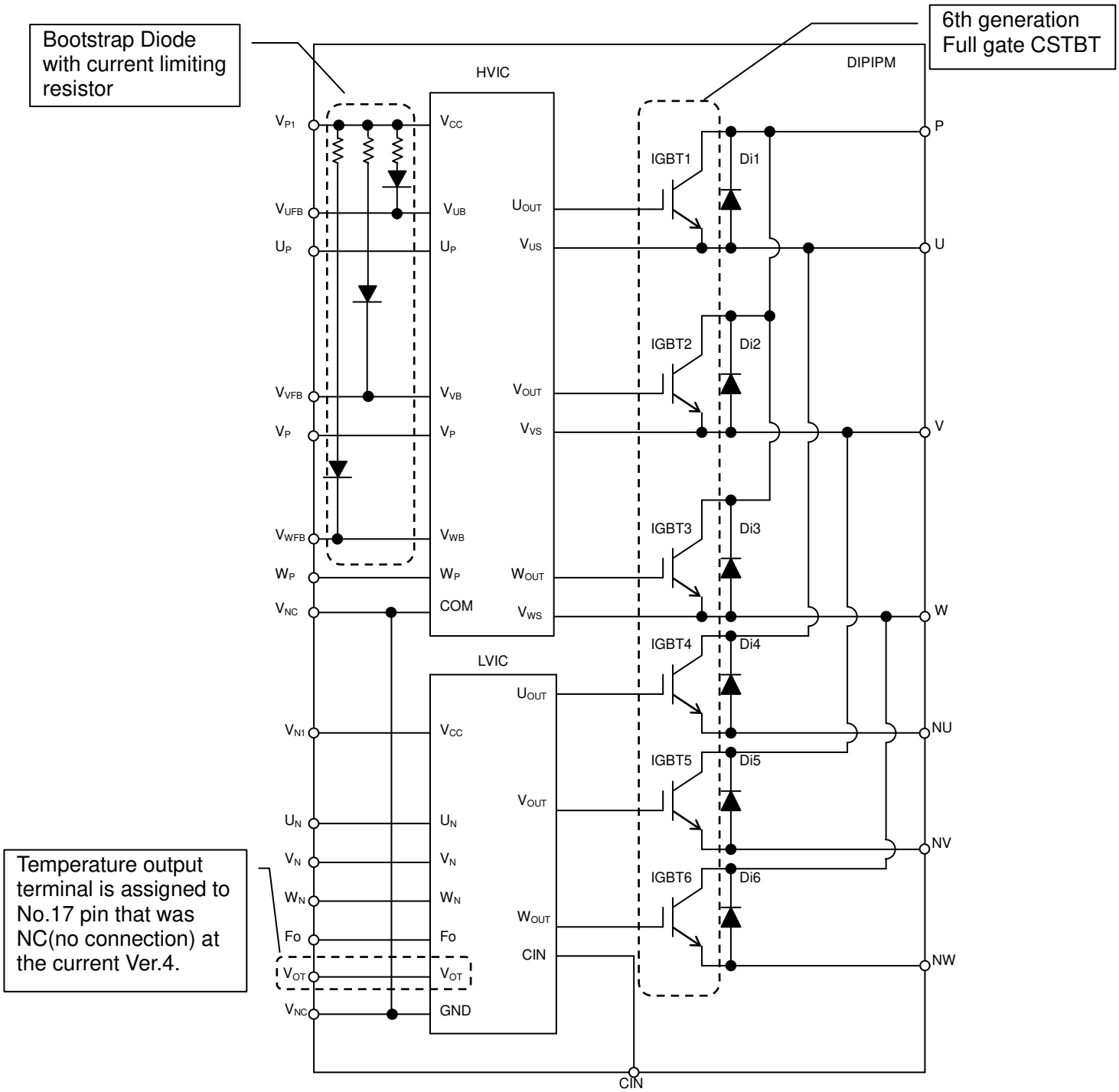


Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for household electric appliances, such as air conditioners, washing machines, refrigerators
 Low power industrial motor drive except automotive applications

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1.4 Product Line-up

Table 1-4-1 DIP Ver.5 Line-up **with temperature output function**

Type Name ^(Note 1)	IGBT Rating	Motor Rating ^(Note 2)	Isolation Voltage
PS219B2-S/-AS/-CS	5A/600V	0.4kW/220V _{AC}	V _{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS219B3-S/-AS/-CS	10A/600V	0.75kW/220V _{AC}	
PS219B4-S/-AS/-CS	15A/600V	0.75kW/220V _{AC}	

Table 1-4-2 DIP Ver.5 Line-up **with over temperature protection function**

Type Name ^(Note 1)	IGBT Rating	Motor Rating ^(Note 2)	Isolation Voltage
PS219B2-ST/-AST/-CST	5A/600V	0.4kW/220V _{AC}	V _{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS219B3-ST/-AST/-CST	10A/600V	0.75kW/220V _{AC}	
PS219B4-ST/-AST/-CST	15A/600V	0.75kW/220V _{AC}	

Note 1: Suffix 'A' indicates long pin type, 'C' indicates zigzag pin type, 'S' indicates N-side open emitter type and 'T' indicates built-in over temperature protect function type. Please refer to chapter 2 for details.

When selecting terminal shape for Super Mini DIIPM series, please contact Mitsubishi Electric Corporation or authorized Mitsubishi Semiconductor product distributors.

Note 2: The motor ratings are simulation results under following conditions: V_{AC}=220V, V_D=V_{DB}=15V, T_c=100°C, T_j=125°C, f_{PWM}=5kHz, P.F=0.8, motor efficiency=0.75, current ripple ratio=1.05, motor over load 150% 1min.

1.5 The Differences between Previous Series and This Series (PS219B*)

DIP Ver.5 has some differences against current DIP Ver.4 (PS2196* and PS219A*)

Main differences are described in Table 1-5-1 and Table 1-5-2.

Table 1-5-1 Differences of functions and outlines

Items	PS2196*	PS219A*	PS219B*	Ref.
	Ver.4	Ver.4 with BSD	Ver.5	
Built-in bootstrap diodes	-	Built-in ¹⁾	Built-in ¹⁾ with current limiting resistor	Section 4.2
Temperature protection	OT (-T)	OT (-T)	OT (-T) or Temperature output ²⁾	Section 2.2.4
Dummy terminal (Compare with PS2196*) ³⁾	-	Add one terminal (No. 1-B pin)	Add one terminal (No. 1-B pin)	Section 2.3
N-side IGBT emitter terminal	Common / Open	Common / Open	Open ⁴⁾	
Terminal shapes ⁴⁾	Total 5 types short, long, one side zigzag, both sides zigzag, short with 3 shunts	Total 5 types 5 types of PS2196* and long or one side zigzag with 3shunts	Total 3 types All types are 3 shunts short, long, one side zigzag	

(1) Built-in bootstrap diode (BSD) of DIP Ver.5 PS219B* incorporates current limiting resistor (typ. 100Ω). So there isn't any limitation about bootstrap capacitance like current PS219A* has (22μF or less in the case of one long pulse initial charging).

(2) Temperature protection function of DIP Ver.5 is selectable from two functions. (They have different model numbers as above.) One is conventional over temperature protection (OT), and the other is LVIC temperature output function (V_{OT}). OT function shutdowns all N-side IGBTs automatically when LVIC temperature exceeds specified value (typ.120 °C). But V_{OT} function cannot shutdown by itself in that case. So it is necessary for system controller to monitor this V_{OT} output and shutdown when the temperature reaches the protection level.

(3) Because of incorporating bootstrap diodes, a part of package was changed. (Just one dummy terminal was added) But its package size, pin assignment and pin number weren't changed, so the same PCB can be used with small modification when replacing from current Super min DIP Ver.4. (External bootstrap diodes and current limit resistors should be removed in the case of replacing from PS2196*. And also if N-side common emitter type was used in former PCB, it is necessary to change wiring from common emitter to open emitter wiring because of DIP Ver.5 has open emitter type only.)

(4) N-side IGBT emitter terminal of DIP Ver.5 is open emitter type only and terminal shapes are short (-S), long (-A) and one (control) side zigzag (-C) types.

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Table 1-5-2 Differences of specifications and recommended operating conditions

Items	Symbol	PS2196*	PS219A*	PS219B*
		Ver.4	Ver.4 with BSD	Ver.5
Circuit current for P-side driving	I_{DB}	Max. 0.55mA	Max. 0.10mA	Max. 0.10mA
Trip voltage for P-side control supply under voltage protection	UV_{DBt}	Min.10.0V	Min. 7.0V	Min. 7.0V
Trip voltage for P-side control supply under voltage protection	UV_{DBr}	Min.10.5V	Min. 7.0V	Min. 7.0V
Bootstrap Di forward voltage	V_F	-	Typ. 2.8V @100mA	Typ. 1.7V @10mA
Arm-shoot-through blocking time for 5~15A rating products	t_{dead}	Min. 1.5 μ s	Min. 1.0 μ s	Min. 1.0 μ s
Allowable minimum input pulse width	PWIN(on)	Min. 0.5 μ s	Min. 0.5 μ s	Min. 0.7 μ s
	PWIN(off)	Min. 0.5 μ s	Min. 0.5 μ s	Min. 0.7 μ s

For more detail and the other characteristics, please refer the datasheet or application note for each product.

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CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Super Mini DIIPM Ver.5 Specifications

DIP Ver.5 specifications are described below by using PS219B4 (15A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS219B4 are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$	15	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, less than 1ms	30	A
P_C	Collector dissipation	$T_C = 25^\circ\text{C}$, per 1 chip	33.3	W
T_j	Junction temperature	(Note)	-20~+150	$^\circ\text{C}$

Note: The maximum junction temperature rating of built-in power chips is $150^\circ\text{C} (@T_C \leq 100^\circ\text{C})$. However, to ensure safe operation of DIIPM, the average junction temperature should be limited to $T_j(\text{Ave}) \leq 125^\circ\text{C} (@T_C \leq 100^\circ\text{C})$.

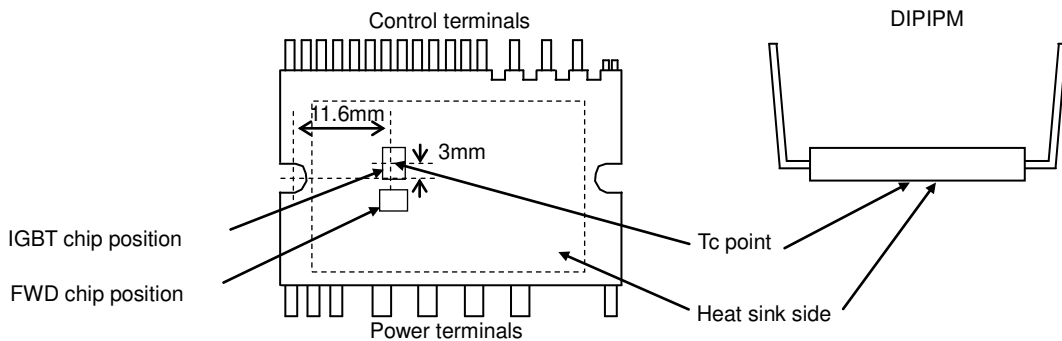
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-U, V_{VFB}-V, V_{WFB}-W$	20	V
V_{IN}	Input voltage	Applied between $U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}$	$-0.5-V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	$-0.5-V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	$-0.5-V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_j = 125^\circ\text{C}$, non-repetitive, less than $2\mu\text{s}$	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Fig.1	-20~+100	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

T_C measurement position



- (1) V_{CC} The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
- (2) $V_{CC(surge)}$ The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.
- (3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.
- (4) $\pm I_C$ The allowable current flowing into collect electrode ($@T_C=25^\circ\text{C}$).Pulse width and period are limited due to junction temperature T_j .
- (5) T_j The maximum junction temperature rating is 150°C . But for safe operation, it is recommended to limit the average junction temperature up to 125°C . Repetitive temperature variation ΔT_j affects the life time of power cycle, so refer life time curves for safety design.
- (6) $V_{CC(prot)}$ The maximum supply voltage for turning off IGBT safely in the case of an SC or OC fault. The power chip might be damaged if supply voltage exceeds this specification.

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(7) Isolation voltage Isolation voltage of Super mini DIIPM is the voltage between all shorted pins and copper surface of DIIPM. The maximum rating of isolation voltage of Super mini DIIPM is 1500Vrms. But if such as convex shape heat radiation fin will be used for enlarging clearance between outer terminals and heat radiation fin (2.5mm or more is recommended), it is able to correspond isolation voltage 2500Vrms. Super mini DIIPM is recognized by UL at the condition 2500Vrms with convex shape heat radiation fin

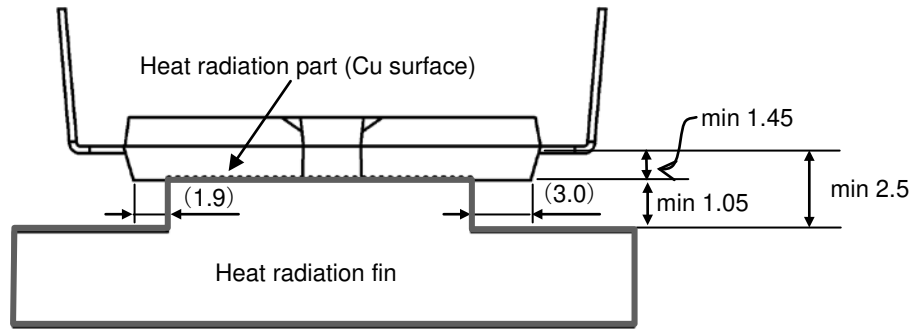


Fig.2-1-1 In the case of using convex heat sink (unit: mm)

(8) Tc position Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

[Power chip position]

Fig.2-1-2 indicates the position of the each power chips. (This figure is the view from laser marked side.)

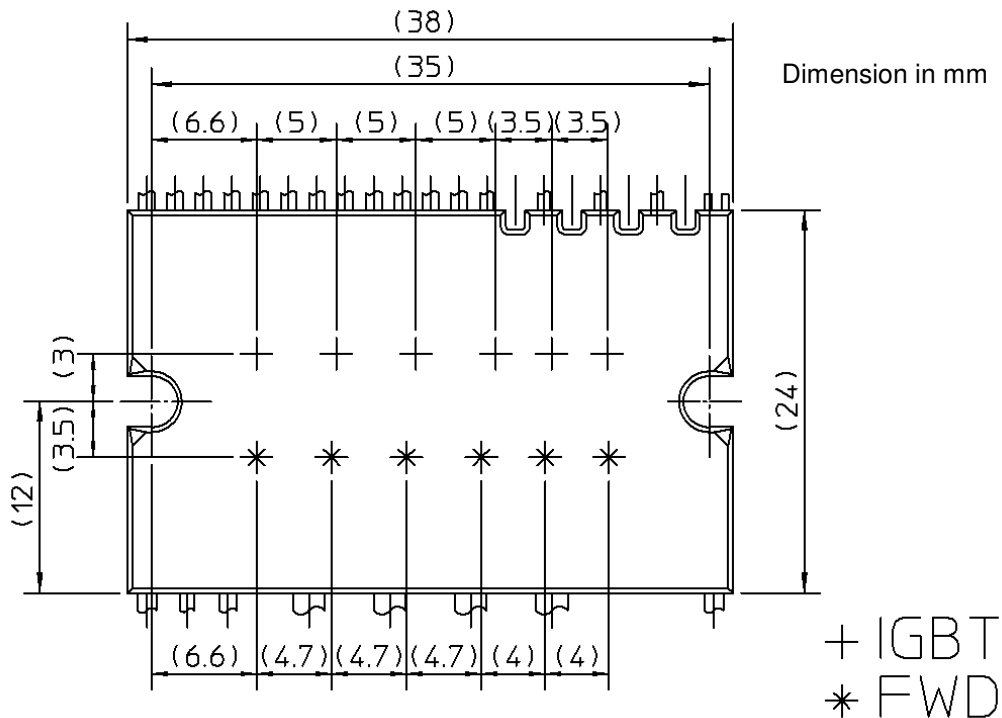


Fig.2-1-2 Power chip position

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2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance of PS219B4.

Table 2-1-2 Thermal resistance of PS219B4

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note)	Inverter IGBT part (per 1/6 module)	-	-	3.0	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	3.9	K/W

Note : Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-3. $Z_{th(j-c)}^*$ is the normalized value of the transient thermal impedance. $(Z_{th(j-c)}^* = Z_{th(j-c)} / R_{th(j-c)max})$

For example, the IGBT transient thermal impedance of PS219B4 in 0.3s is $3.0 \times 0.8 = 2.4K/W$.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock···)

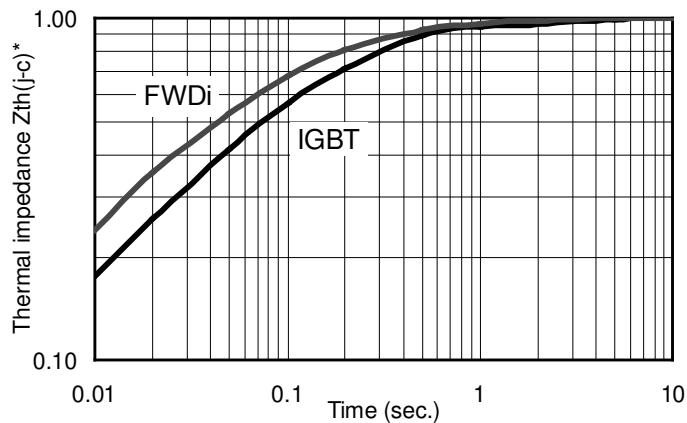


Fig.2-1-3 Typical transient thermal impedance

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2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PS219B4.

Table 2-1-3 Static characteristics and switching characteristics of PS219B4

INVERTER PART ($T_j = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}, V_{IN}= 5\text{V}, I_C= 15\text{A}$	$T_j= 25^\circ\text{C}$	-	1.50	2.00	V
			$T_j= 125^\circ\text{C}$	-	1.60	2.10	
V_{EC}	FWDi forward voltage	$V_{IN}= 0\text{V}, -I_C= 15\text{A}$	-	1.70	2.20	V	
t_{on}	Switching times	$V_{CC}= 300\text{V}, V_D= V_{DB}= 15\text{V}$ $I_C= 15\text{A}, T_j= 125^\circ\text{C}, V_{IN}= 0\leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)	-	0.85	2.05	μs	
$t_{C(on)}$			-	0.45	0.70	μs	
t_{off}			-	1.50	2.10	μs	
$t_{C(off)}$			-	0.35	0.60	μs	
t_{rr}			-	0.30	-	μs	
I_{CES}	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	$T_j= 25^\circ\text{C}$	-	-	1	mA
			$T_j= 125^\circ\text{C}$	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-4 and 2-1-5. Switching characteristics are measured by half bridge circuit with inductance load.

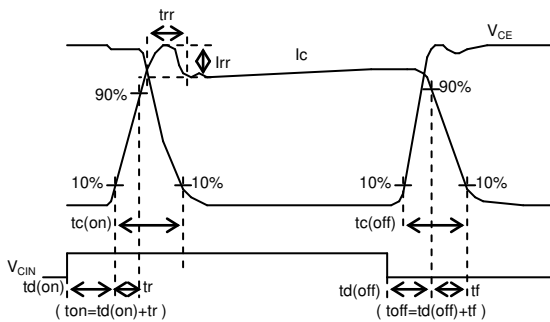


Fig.2-1-4 Switching time definition

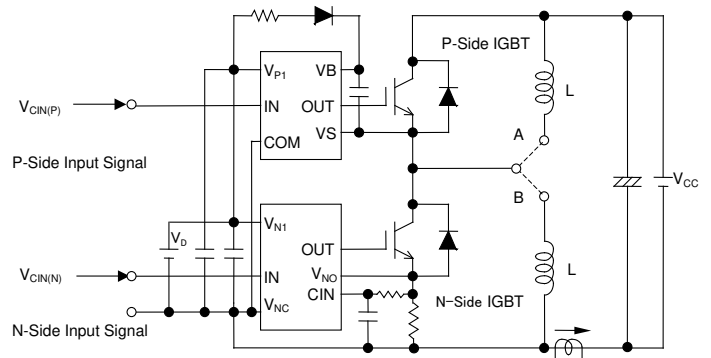


Fig.2-1-5 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

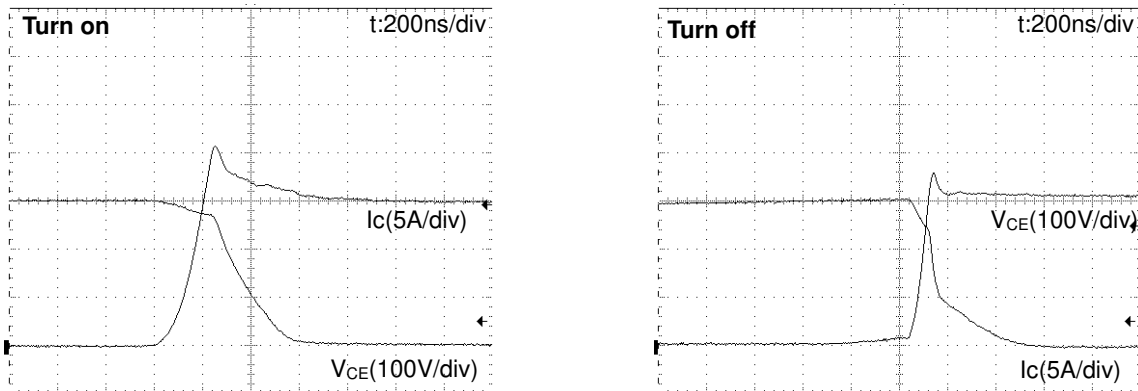


Fig.2-1-6 Typical switching waveform (PS219B4)

Conditions: $V_{CC}=300\text{V}, V_D=V_{DB}=15\text{V}, T_j=125^\circ\text{C}, I_C=15\text{A}$, Inductive load half-bridge circuit

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Table 2-1-4 shows the typical control part characteristics of PS219B4.

Table 2-1-4 Control (Protection) characteristics of PS219B4

CONTROL (PROTECTION) PART ($T_j = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I_D	Circuit current	Total of $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	$V_D=15\text{V}$, $V_{IN}=0\text{V}$	-	-	2.80	mA
			$V_D=15\text{V}$, $V_{IN}=5\text{V}$	-	-	2.80	
I_{DB}		Each part of $V_{UFB}-U$, $V_{VFB}-V$, $V_{WFB}-W$	$V_D=V_{DB}=15\text{V}$, $V_{IN}=0\text{V}$	-	-	0.10	
			$V_D=V_{DB}=15\text{V}$, $V_{IN}=5\text{V}$	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15\text{V}$ (Note 1)	0.43	0.48	0.53	V	
UV_{DBt}	P-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ\text{C}$	Trip level	7.0	10.0	12.0	V
UV_{DBr}			Reset level	7.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output* (-S/-AS/-CS only)	Pull down $R=5\text{k}\Omega$ (Note 2)	LVIC Temperature= 90°C	2.63	2.77	2.91	V
			LVIC Temperature= 25°C	0.88	1.13	1.39	V
OT_t	Overt temperature protection* (OT, -ST/-AST/-CST only) (Note3)	$V_D = 15\text{V}$ Detect LVIC temperature	Trip level	100	120	140	$^\circ\text{C}$
OT_{rh}			Hysteresis of trip-reset	-	10	-	$^\circ\text{C}$
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}$, F_o terminal pulled up to 5V by 10k Ω	4.9	-	-	V	
V_{FOL}		$V_{SC} = 1\text{V}$, $I_{FO} = 1\text{mA}$	-	-	0.95	V	
t_{FO}	Fault output pulse width	(Note 4)	20	-	-	μs	
I_{IN}	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
$V_{th(on)}$	ON threshold voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-	2.10	2.60	V	
$V_{th(off)}$	OFF threshold voltage		0.80	1.30	-		
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage		0.35	0.65	-		
V_F	Bootstrap Di forward voltage	$I_F=10\text{mA}$ including voltage drop by limiting resistor	1.1	1.7	2.3	V	
R	Built-in limiting resistance	Included in bootstrap Di	80	100	120	Ω	

- Note 1 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
 2 : DIIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIIPM.
 3 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and F_o outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIIPM. (There is a possibility that junction temperature of power chips exceeded maximum $T_j(150^\circ\text{C})$.
 4 : Fault signal F_o outputs when SC, UV or OT protection works. F_o pulse width is different for each protection modes. At SC failure, F_o pulse width is a fixed width (=minimum 20 μs), but at UV or OT failure, F_o outputs continuously until recovering from UV or OT state. (But minimum F_o pulse width is 20 μs .)

*) It is necessary to select from temperature output function or over temperature protection about temperature protection. Their part numbers are different. (e.g. PS219B4-S is the type with temperature output function and PS219B4-SI is the type with over temperature protection.)

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Recommended operating conditions of PS219B4 are given in Table 2-1-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIIPM safe operation.

Table 2-1-5 Recommended operating conditions of PS219B4

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V	
V_D	Control supply voltage	Applied between V_{P1} - V_{NC} , V_{N1} - V_{NC}	13.5	15.0	16.5	V	
V_{DB}	Control supply voltage	Applied between V_{UFB} -U, V_{VFB} -V, V_{WFB} -W	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/ μ s	
t_{dead}	Arm shoot-through blocking time	For each input signal	1.0	-	-	μ s	
f_{PWM}	PWM input frequency	$T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$	-	-	20	kHz	
I_O	Allowable r.m.s. current	$V_{CC} = 300\text{V}$, $V_D = 15\text{V}$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$ (Note1)	$f_{PWM} = 5\text{kHz}$	-	-	8.0	Arms
			$f_{PWM} = 15\text{kHz}$	-	-	5.0	
PWIN(on)	Minimum input pulse width	(Note 2)	0.7	-	-	μ s	
PWIN(off)			0.7	-	-		
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V	
T_j	Junction temperature		-20	-	+125	$^\circ\text{C}$	

Note 1: Allowable r.m.s. current depends on the actual application conditions.

2: DIIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

About Control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$$dV/dt \leq \pm 1\text{V}/\mu\text{s}, \quad V_{ripple} \leq 2\text{Vp-p}$$

2.1.4 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-1-6.

Please refer to Section 2.4 for the detailed mounting instruction of DIP Ver.5.

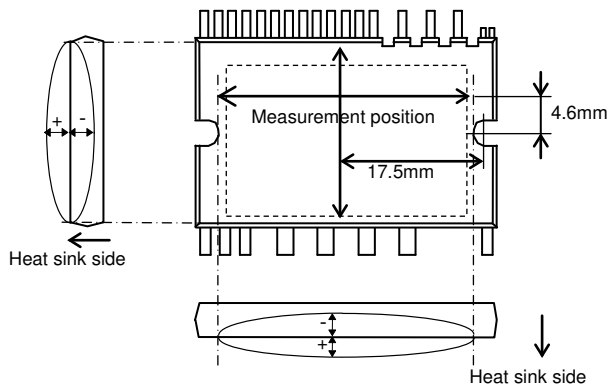
Table 2-1-6 Mechanical characteristics and ratings of PS219B4

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 1)	Recommended 0.69N·m	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat-sink flatness		(Note 2)	-50	-	100	μm

Note 1: Plain washers (ISO 7089~7094) are recommended.

Note 2: Measurement point of heat sink flatness



Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.2 Protective Functions and Operating Sequence

DIP Ver.5 has Short circuit (SC), Under Voltage of control supply (UV), Over Temperature (OT) and temperature output (VOT) for protection function. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

1. General

DIP Ver.5 uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection $V_{sc(ref)}$ is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent DIIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: $1.5\mu s \sim 2\mu s$) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

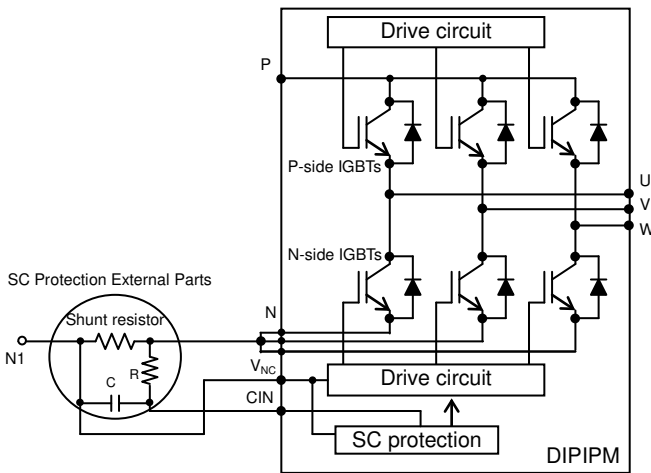


Fig.2-2-1 SC protecting circuit

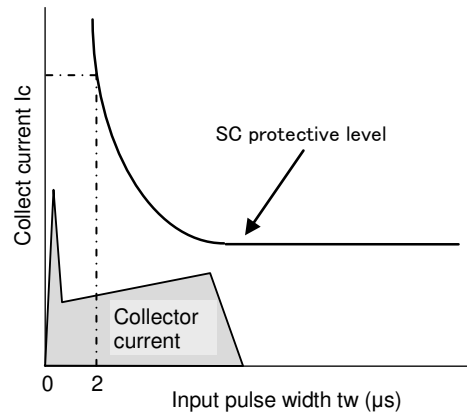


Fig.2-2-2 Filter time constant setting

2. SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
(It is recommended to set RC time constant $1.5 \sim 2.0\mu s$ so that IGBT shut down within $2.0\mu s$ when SC.)
- a3. All N-side IGBTs' gate are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo outputs for $t_{Fo} = \text{minimum } 20\mu s$.
- a6. Input = "L". IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

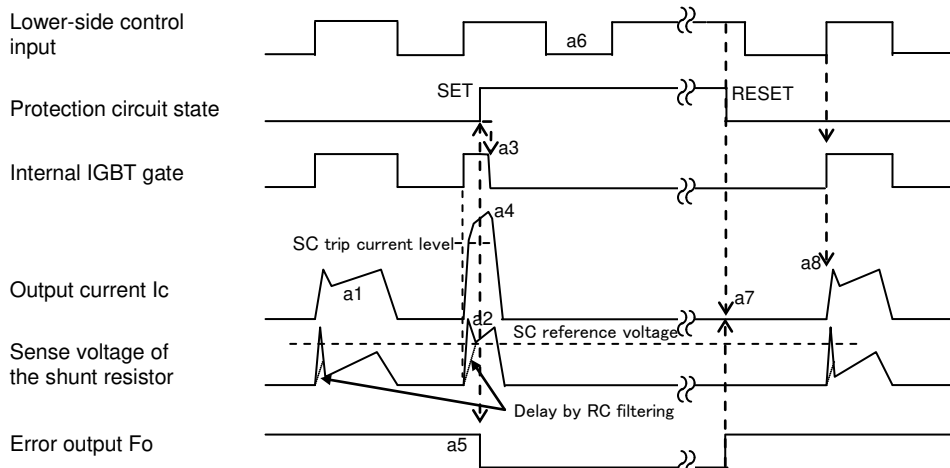


Fig.2-2-3 SC protection timing chart

3. Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)} / SC$$

where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum SC trip level SC(max) should be set less than the IGBT minimum saturation current which is 1.7 times as large as the rated current. For example, the SC(max) of PS219B4 should be set to $15 \times 1.7 = 25.5A$. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PS219B4, there is +/-0.05V dispersion in the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$ (unit: V)

Condition	Min	Typ	Max
at Tj=25°C, VD=15V	0.43	0.48	0.53

Then, the range of SC trip level can be calculated by the following expressions:

$$R_{Shunt(min)} = V_{SC(ref) max} / SC(max)$$

$$R_{Shunt(typ)} = R_{Shunt(min)} / 0.95^* \quad \text{then} \quad SC(typ) = V_{SC(ref) typ} / R_{Shunt(typ)}$$

$$R_{Shunt(max)} = R_{Shunt(typ)} \times 1.05^* \quad \text{then} \quad SC(min) = V_{SC(ref) min} / R_{Shunt(max)}$$

*) This is the case that shunt resistance dispersion is within +/-5%.

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range ($R_{Shunt} = 20.8m\Omega$ (min), 21.9mΩ (typ), 23.0mΩ(max))

Condition	min.	typ.	Max.
at Tj=25°C	18.7A	21.9A	25.5A

(e.g. $20.8m\Omega$ ($R_{shunt(min)} = 0.53V (=V_{SC(max)}) / 25.5A (=SC(max))$)

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - e^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc : the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	-	-	0.5	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

$$t_{TOTAL} = t1 + t2$$

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10µs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10µs after UV happened.

Table 2-2-4 DIIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0-UV _{Dt} (N), UV _{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV _{Dt} (N)-13.5V UV _{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N) 18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, V_{ripple} \leq 2V_{p-p}$$

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

[N-side UV Protection Sequence]

- a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a2. Normal operation: IGBT ON and carrying current.
- a3. V_D level dips to under voltage trip level. (UV_{Dt}).
- a4. All N-side IGBTs turn OFF in spite of control input condition.
- a5. F_o outputs for t_{Fo} =minimum $20\mu s$, but output is extended during V_D keeps below UV_{Dr} .
- a6. V_D level reaches UV_{Dr} .
- a7. Normal operation: IGBT ON and outputs current.

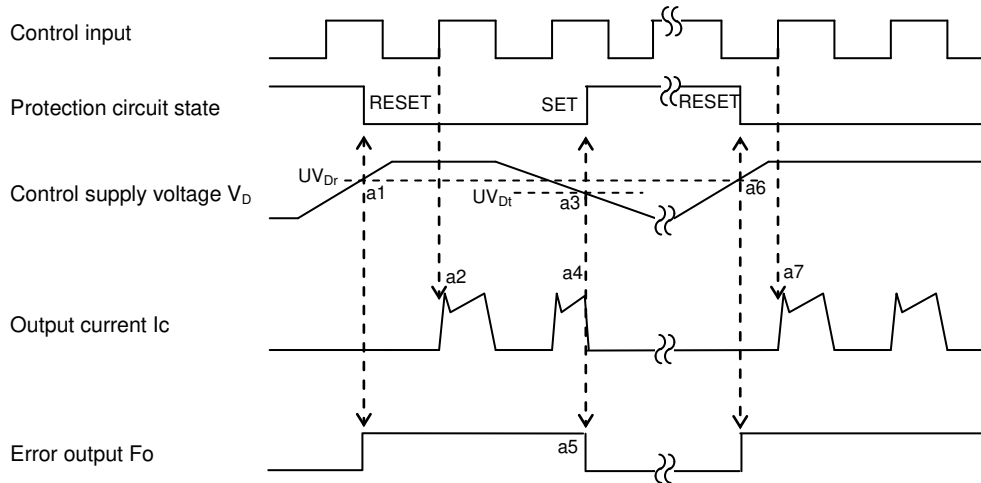


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

- a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal (L→H).
- a2. Normal operation: IGBT ON and outputs current.
- a3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
- a4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- a5. V_{DB} level reaches UV_{DBr} .
- a6. Normal operation: IGBT ON and outputs current.

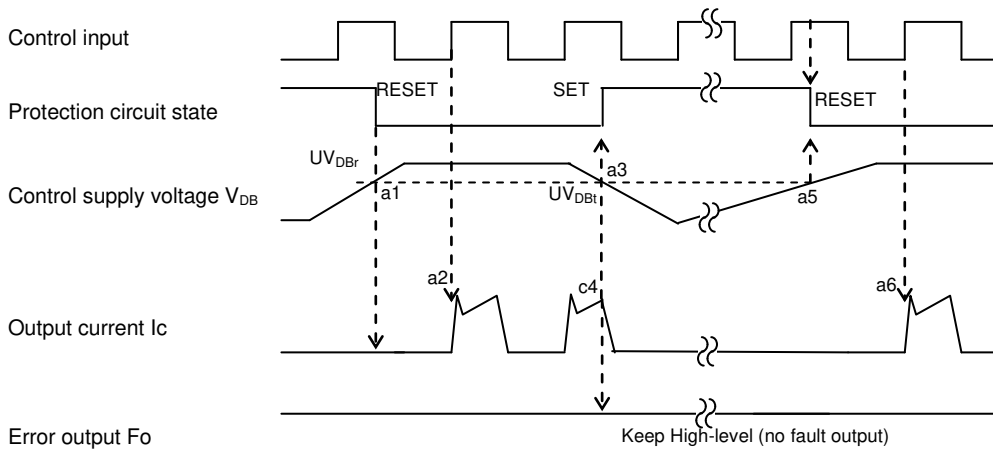


Fig.2-2-5 Timing Chart of P-side UV protection

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.2.3 OT Protection (PS219B*-ST/AST/CST only)

PS219B*-T series have OT (over temperature) protection function by monitoring LVIC temperature rise. While LVIC temperature exceeds and keeps over OT trip temperature, error signal Fo outputs and all N-side IGBTs are shut down without reference to input signal. (P-side IGBTs are not shut down)
 The specification of OT trip temperature and its sequence are described in Table 2-2-5 and Fig.2-2-6.

Table 2-2-5 OT trip temperature specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Over temperature protection	OT _t	V _D =15V, At temperature of LVIC	Trip level	100	120	140	°C
	OT _{rh}		Trip/reset hysteresis	-	10	-	

[OT Protection Sequence]

- a1. Normal operation: IGBT ON and outputs current.
 - a2. LVIC temperature exceeds over temperature trip level(OT_t).
 - a3. All N-side IGBTs turn OFF in spite of control input condition.
 - a4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
 - a5. LVIC temperature drops to over temperature reset level.
 - a6. Normal operation: IGBT turns on by next ON signal (L→H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)

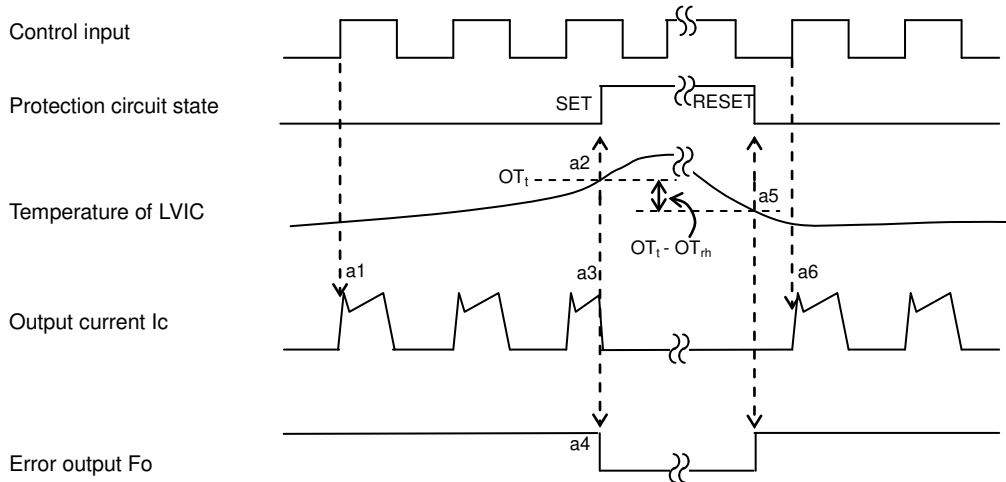


Fig.2-2-6 Timing Chart of OT protection

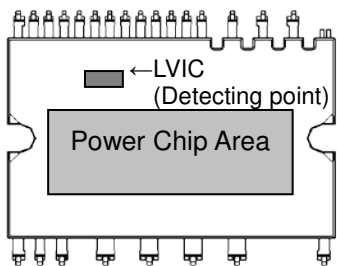


Fig.2-2-7 Temperature detecting point

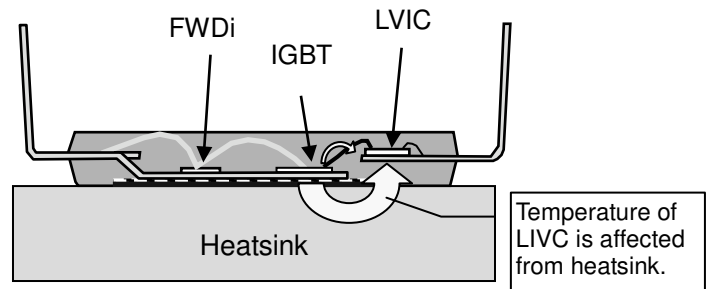


Fig.2-2-8 Thermal conducting from power chips

Precaution about this OT protection function

- (1) This OT protection will not work effectively in the case of rapid temperature rise like motor lock or over current. (This protection monitors LVIC temperature, so it cannot respond to rapid temperature rise of power chips.)
- (2) If the cooling system is abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fan stops) when OT protection works, can't reuse the DIIPM. (Because the junction temperature of power chips will exceed the maximum rating of T_j(150°C).)

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.2.4 Temperature output function V_{OT} (PS219B*-S/AS/CS only)

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC.

The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit) It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was mounted on outer heat sink currently)

[Note]

In this function, DIIPM cannot shutdown IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIIPM.

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-9, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-6. The characteristics of V_{OT} output vs. LVIC temperature is linear characteristics described in Fig.2-2-13. There are some cautions for using this function as below.

Table 2-2-6 Output capability
($T_c = -20^\circ\text{C} \sim 100^\circ\text{C}$)

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.

Sink : Current flow from outside to V_{OT} .

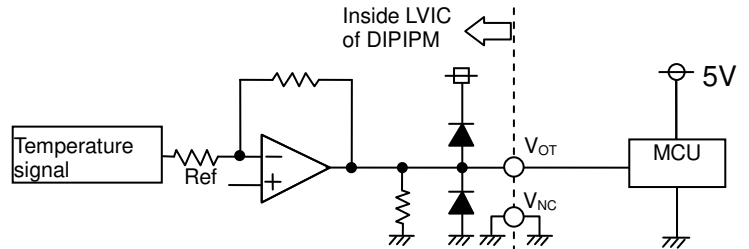


Fig.2-2-9 V_{OT} output circuit

• In the case of detecting lower temperature than room temperature

It is recommended to insert 5k Ω (5.1k Ω is recommended.) pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

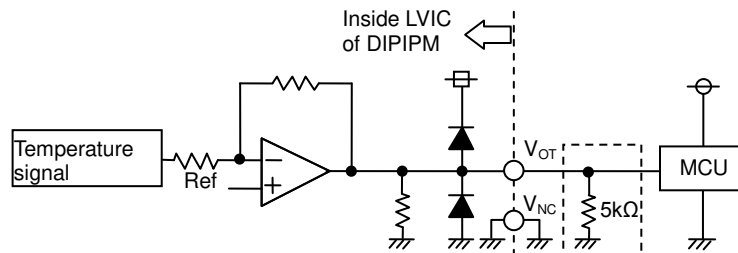


Fig.2-2-10 V_{OT} output circuit in the case of detecting low temperature

• In the case of using with low voltage controller(MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

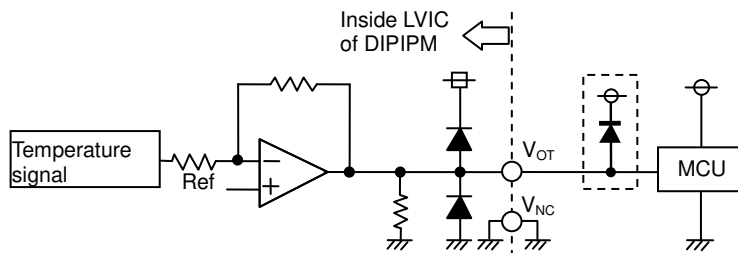


Fig.2-2-11 V_{OT} output circuit in the case of using with low voltage controller

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

- In the case that the protection level exceeds control supply of the controller

In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-2-12). In that case, sum of the resistances of divider circuit should be 5k Ω . About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clamp diode. But it should be judged by the divided output level finally.

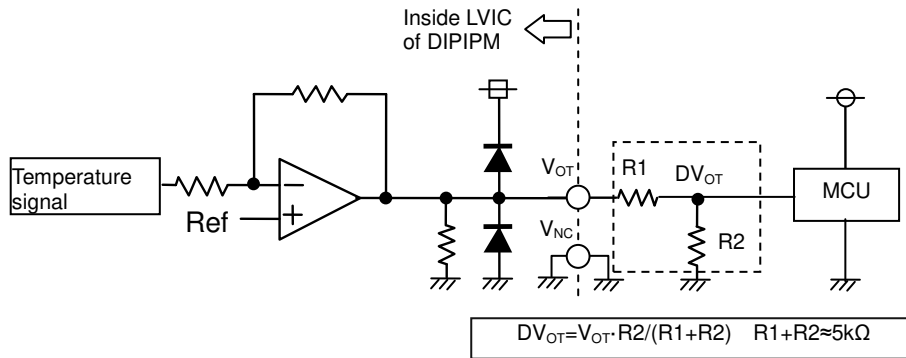


Fig.2-2-12 V_{OT} output circuit in the case with high protection level

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

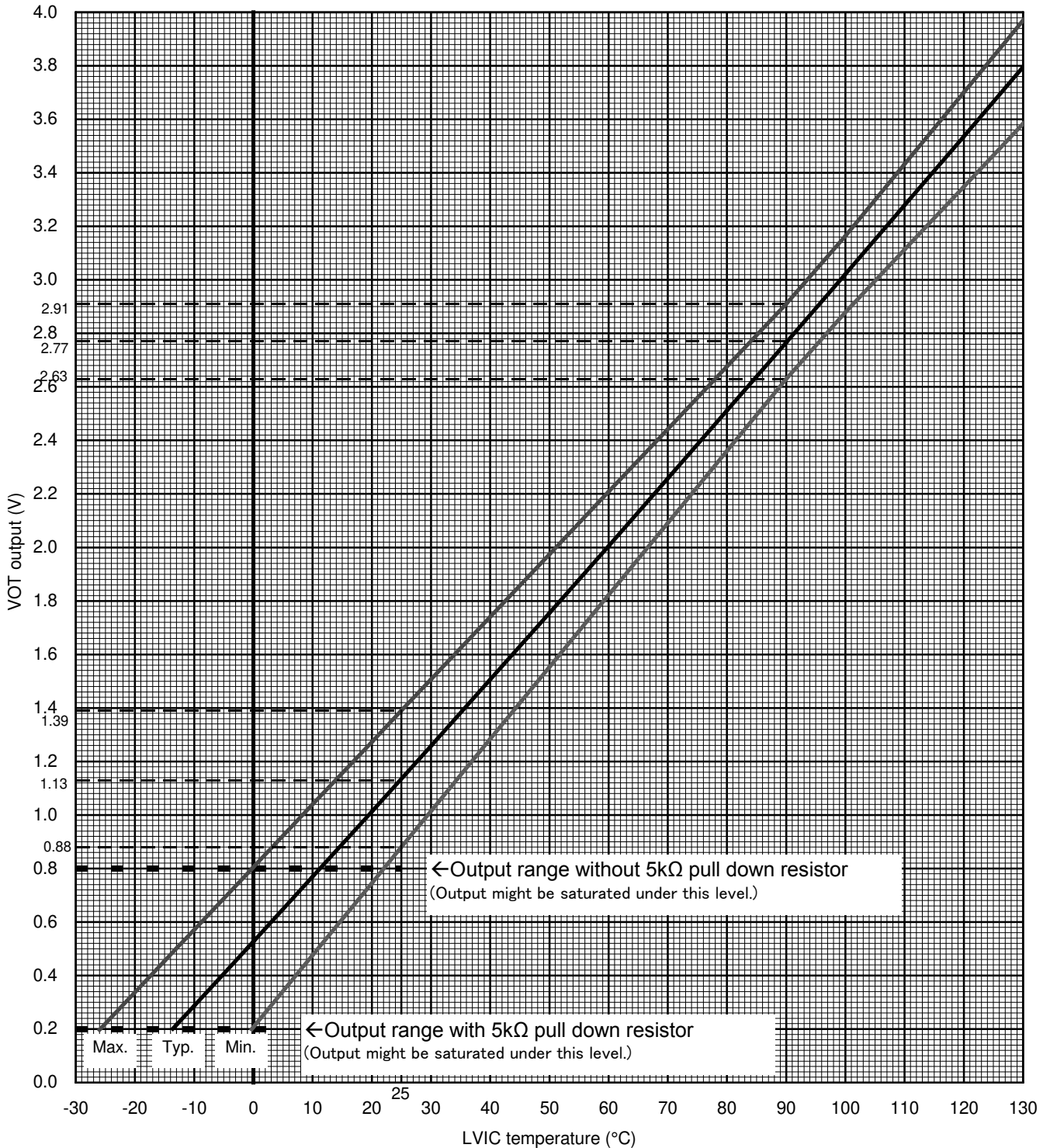


Fig.2-2-13 V_{OT} output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: $T_{ic}(=V_{OT} \text{ output})$, case temperature: T_c (under the chip defined on datasheet), and junction temperature: T_j depends on the system cooling condition, heat sink, control strategy, etc. For example, their relationship example in the case of using the heat sink (Table 2-2-7) is described in Fig.2-2-14. This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature T_{ic} , it is important to consider the protection temperature assures $T_c \leq 100^\circ\text{C}$ and $T_j \leq 150^\circ\text{C}$.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

Table 2-2-7 Outer heat sink

Heat sink size (W x D x H)	Thermal resistance Rth(f-a)
100 x 88 x 40 mm	2.20K/W

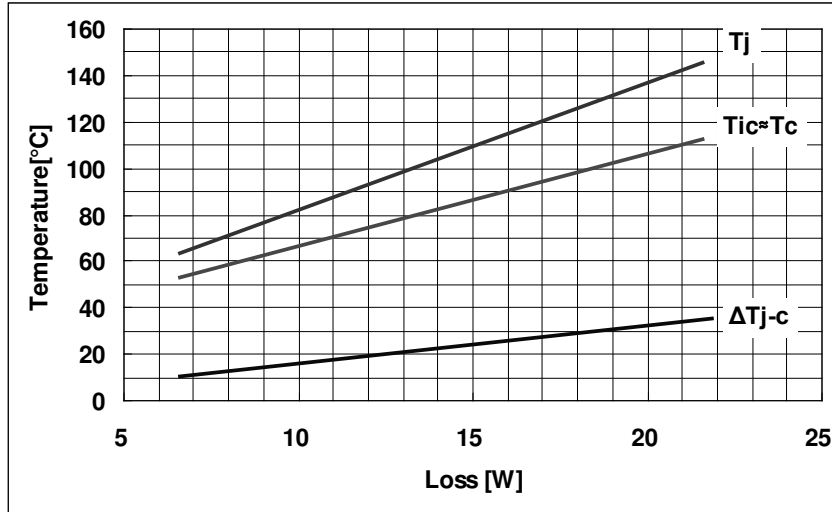
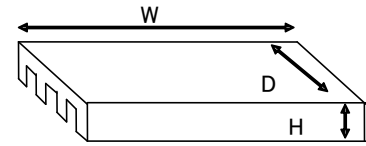


Fig.2-2-14 Example of relationship of Tj, Tc, Tic

(One IGBT chip turns on. DC current Ta=25°C, In this example, Tic and Tc are almost same temperature.)

Procedure about setting the protection level by using Fig.2-2-15 is described as below.

Table 2-2-8 Procedure for setting protection level

	Procedure	Setting value example
1)	Set the protection Tj temperature	Set Tj to 120°C as protection level.
2)	Get LVIC temperature Tic that matches to above Tj of the protection level from the relationship of Tj-Tic in Fig.2-2-15.	Tic=93°C (@Tj=120°C)
3)	Get VOT value from the VOT output characteristics in Fig.2-2-16 and the Tic value which was obtained at phase 2) .	VOT=2.84V (@Tic=93°C) is decided as the protection level.

As above procedure, the setting value for VOT output is decided to 2.84V. But VOT output has some data spread, so it is important to confirm whether the protection temperature fluctuation of Tj and Tc due to the data spread of VOT output is Tj≤150°C and Tc≤100°C. Procedure about the confirmation of temperature fluctuation is described in Table 2-2-9.

Table 2-2-9 Procedure for confirmation of temperature fluctuation

	Procedure	Confirmation example
4)	Confirm the region of Tic fluctuation at above VOT from Fig.2-2-16.	Tic=87°C~98.5°C (@VOT=2.84V)
5)	Confirm the region of Tj and Tc fluctuation at above region of Tic from Fig.2-2-15.	Tj=113°C~126°C (≤150°C No problem) Tc=87°C~98.5°C (≤100°C No problem) In this example, Tic and Tc are almost same temperature, so Tc fluctuation is also same that of Tic

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

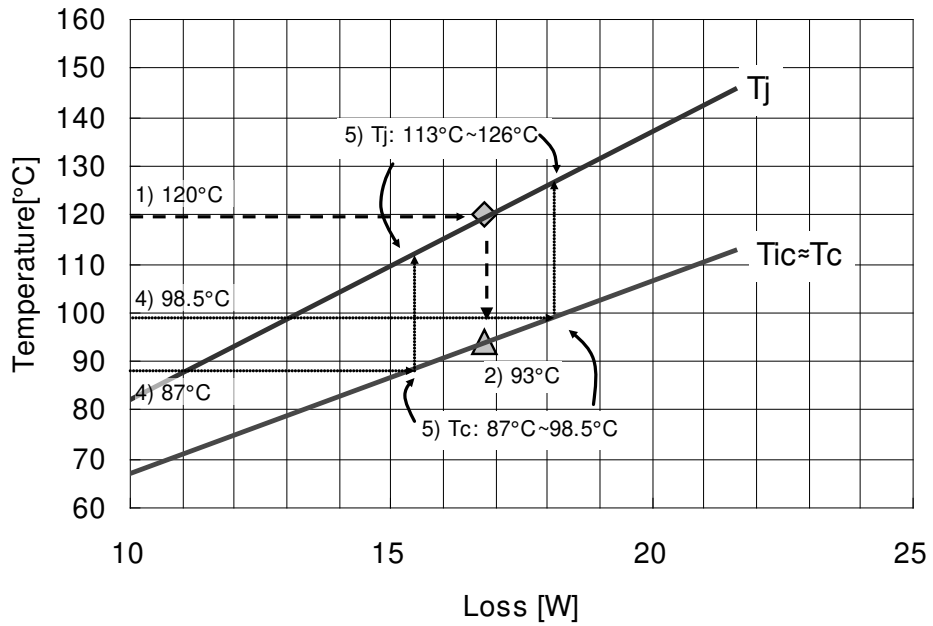


Fig.2-2-15 Relationship of T_j , T_c , T_{ic} (Enlarged graph of Fig.2-2-14)

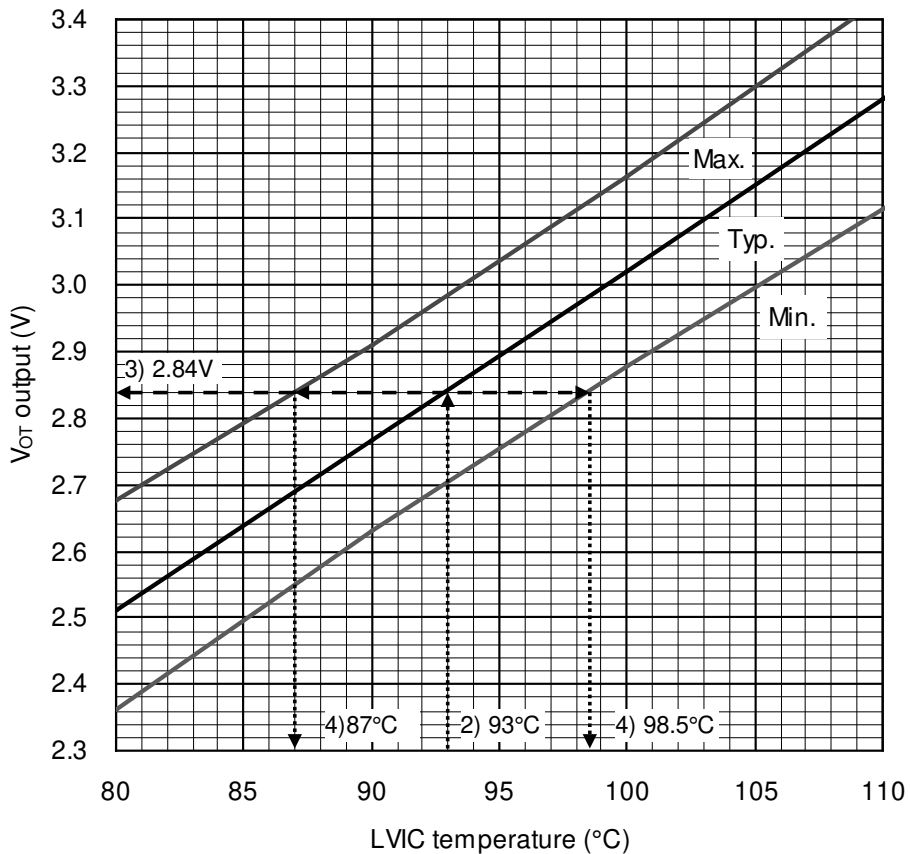


Fig.2-2-16 V_{OT} output vs. LVIC temperature (Enlarged graph of Fig.2-2-13)

As mentioned above, the relationship between T_{ic} , T_c and T_j depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.3 Package Outlines

2.3.1 Package outlines

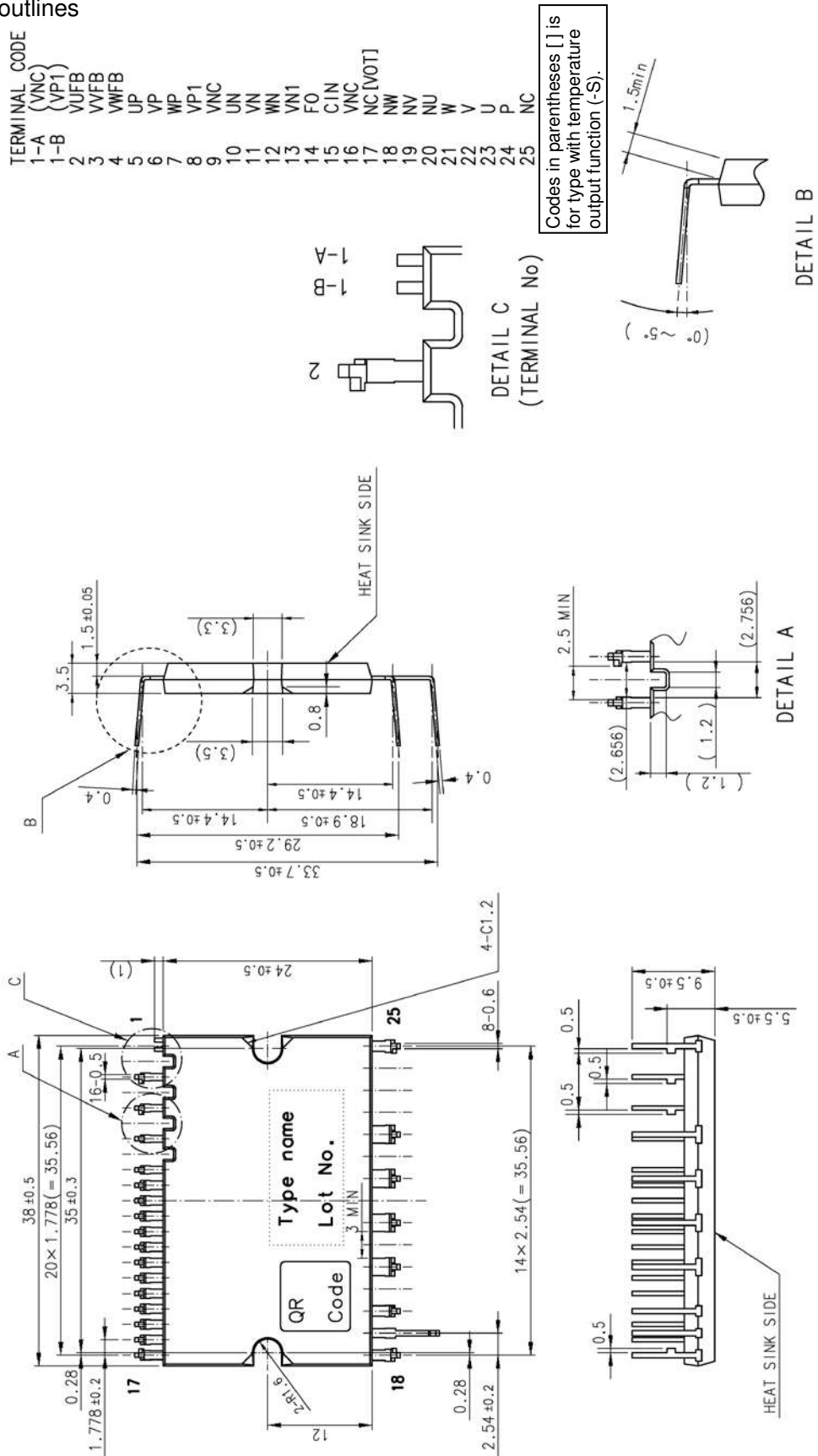


Fig.2-3-1 Short pin type package (-S/-ST) outline drawing

Dimensions in mm

(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

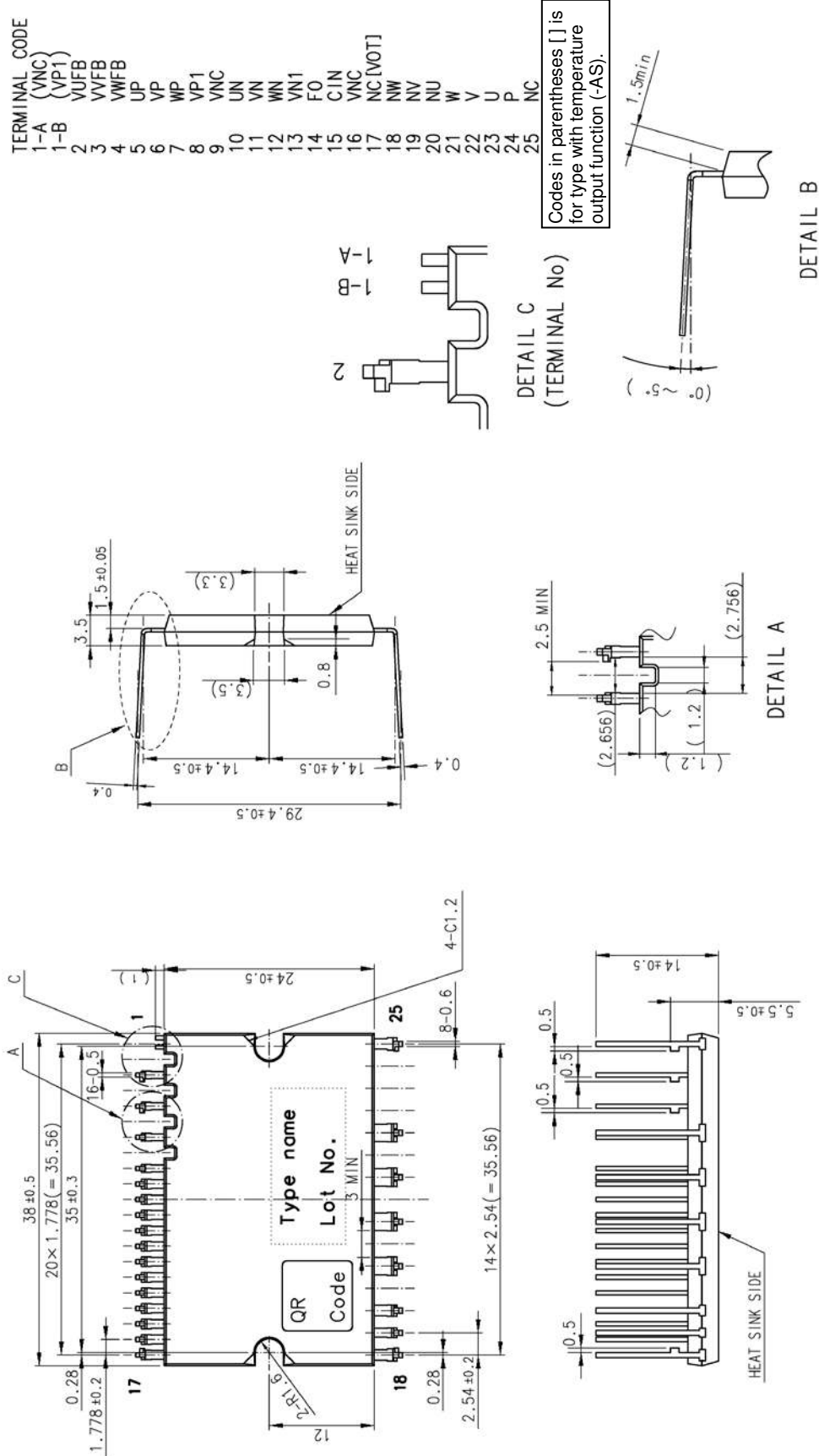


Fig.2-3-2 Long pin type package(-AS/-AST) outline drawing

Dimensions in mm

(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

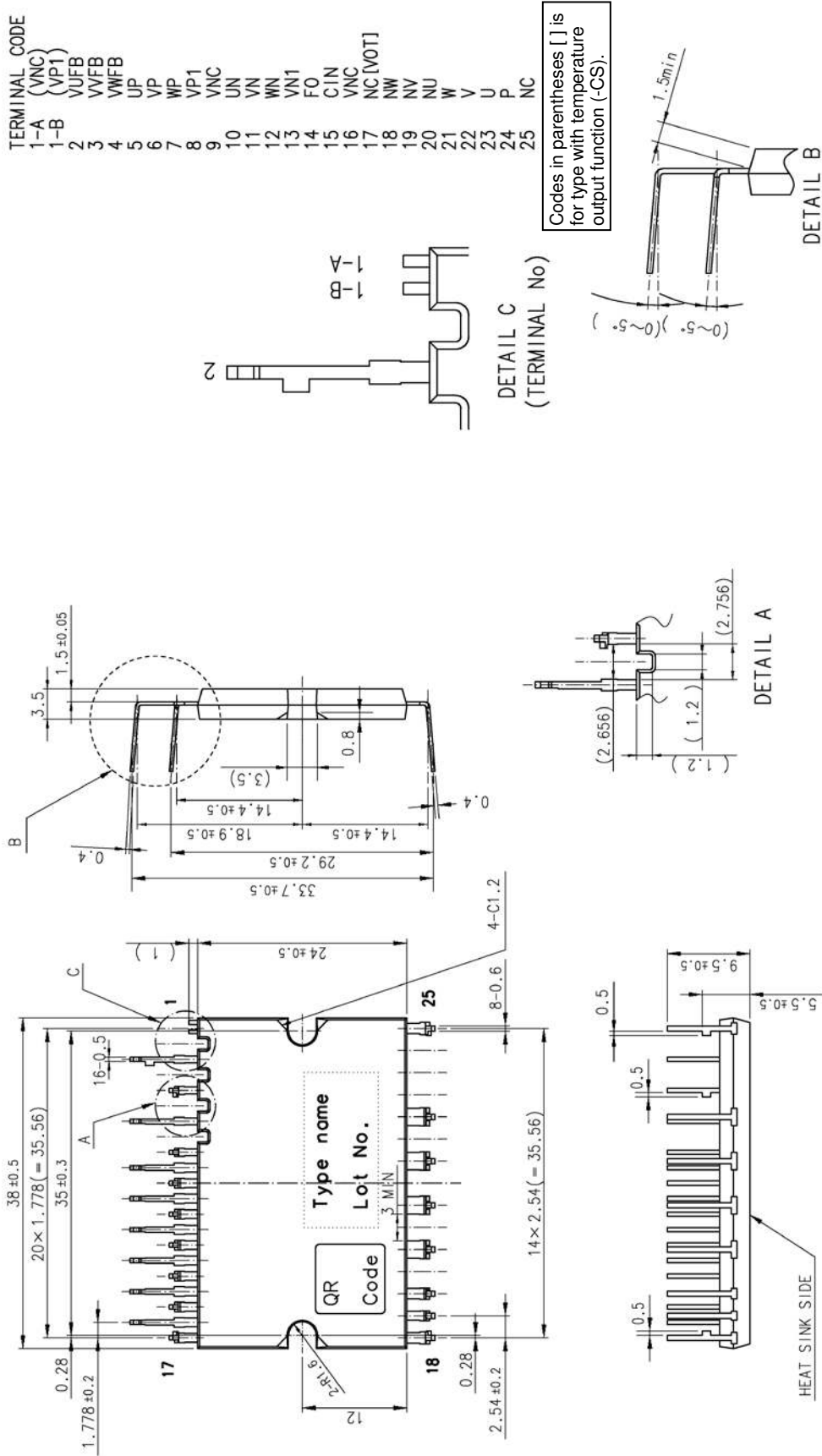


Fig.2-3-3 Zigzag pin type package(-CS/-CST) outline drawing

Dimensions in mm

(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.3.2 Marking

The laser marking specification of DIP Ver.5 is described in Fig.2-3-4. Mitsubishi Corporate crest, Type name, Lot number, and QR code mark are marked in the upper side of module.

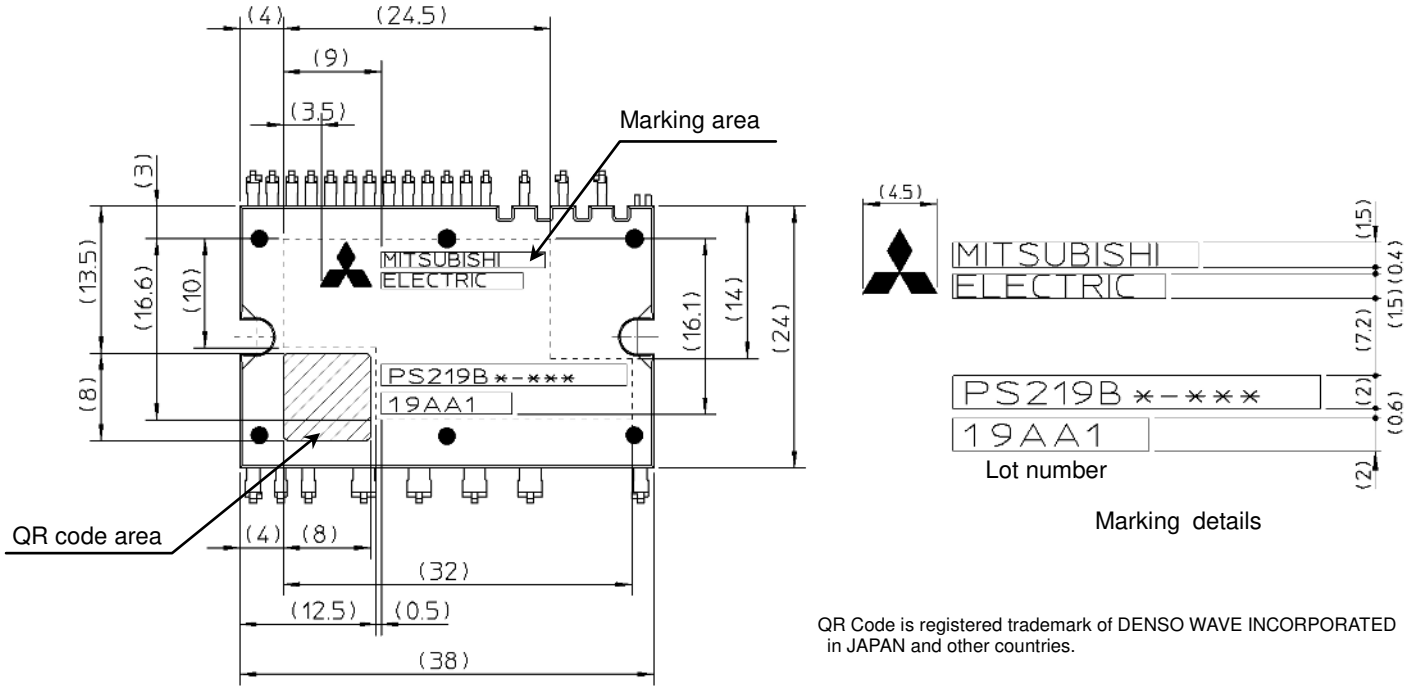
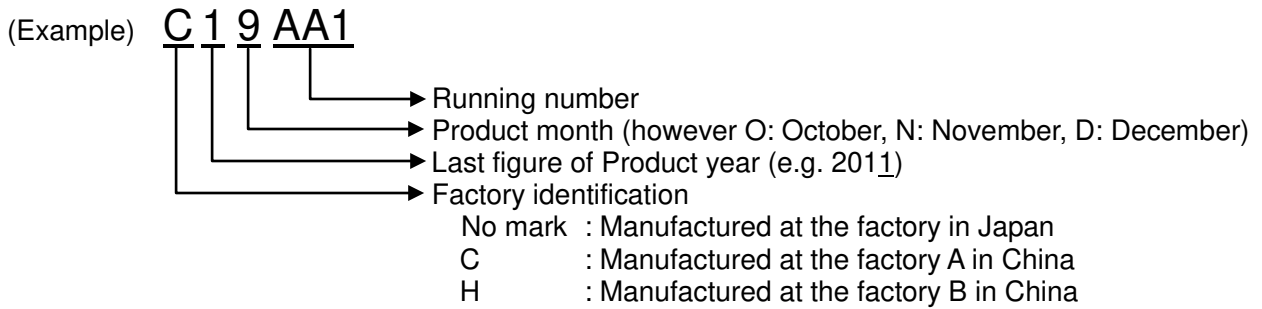


Fig.2-3-4 Laser marking view

The Lot number indicates production year, month, running number and country of origin. The detailed is described as below.



Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.3.3 Terminal Description

Table 2-3-1 Terminal description

Pin	PS219B*-S/AS/CS(with temperature output function)		PS219B*-ST/AST/CST(with OT protection function)	
	Name	Description	Name	Description
1-A	(V _{NC}) ^{*2}	Inner used terminal It has control GND potential, so it should be left no connection.	(V _{NC}) ^{*2}	Same in the left
1-B	(V _{P1}) ^{*2}	Inner used terminal It has control supply potential, so it should be left no connection.	(V _{P1}) ^{*2}	Same in the left
2	V _{UFB}	U-phase P-side drive supply positive terminal	V _{UFB}	Same in the left
3	V _{VFB}	V-phase P-side drive supply positive terminal	V _{VFB}	Same in the left
4	V _{WFB}	W-phase P-side drive supply positive terminal	V _{WFB}	Same in the left
5	U _P	U-phase P-side control input terminal	U _P	Same in the left
6	V _P	V-phase P-side control input terminal	V _P	Same in the left
7	W _P	W-phase P-side control input terminal	W _P	Same in the left
8	V _{P1}	P-side control supply positive terminal	V _{P1}	Same in the left
9	V _{NC} ^{*1}	P-side control supply GND terminal	V _{NC} ^{*1}	Same in the left
10	U _N	U-phase N-side control input terminal	U _N	Same in the left
11	V _N	V-phase N-side control input terminal	V _N	Same in the left
12	W _N	W-phase N-side control input terminal	W _N	Same in the left
13	V _{N1}	N-side control supply positive terminal	V _{N1}	Same in the left
14	F _O	Fault signal output terminal	F _O	Same in the left
15	CIN	SC trip voltage detecting terminal	CIN	Same in the left
16	V _{NC} ^{*1}	N-side control supply GND terminal	V _{NC} ^{*1}	Same in the left
17	V _{OT}	Temperature output	NC	No connection (There isn't any connection inside DIIPM.)
18	NW	WN-phase IGBT emitter	NW	Same in the left
19	NV	VN-phase IGBT emitter	NV	Same in the left
20	NU	UN-phase IGBT emitter	NU	Same in the left
21	W	W-phase output terminal(W-phase drive supply GND)	W	Same in the left
22	V	V-phase output terminal (V-phase drive supply GND)	V	Same in the left
23	U	U-phase output terminal (U-phase drive supply GND)	U	Same in the left
24	P	Inverter DC-link positive terminal	P	Same in the left
25	NC	No connection (There isn't any connection inside DIIPM.)	NC	Same in the left

*1) Connect only one V_{NC} terminal to the system GND and leave another one open.

*2) No.1-A,1-B are inner used terminals, so it is necessary to leave no connection.

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Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB-U} V_{VFB-V} V_{WFB-W}	<ul style="list-style-type: none"> • Drive supply terminals for P-side IGBTs. • By mounting bootstrap capacitor, individual isolated power supplies are not needed for the P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply when potential of output terminal is almost GND level. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability due to ripple or surge. In order to prevent malfunction, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	<ul style="list-style-type: none"> • Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	<ul style="list-style-type: none"> • Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences. • Connect only one V_{NC} terminal (9 or 16pin) to the GND, and leave another one open.
Control input terminal	U_P, V_P, W_P U_N, V_N, W_N	<ul style="list-style-type: none"> • Control signal input terminals. Voltage input type. • These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIIPM from noise interference. • Use RC filter in case of signal oscillation. (Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Short-circuit trip voltage detecting terminal	CIN	<ul style="list-style-type: none"> • For inverter part SC protection, input the potential of shunt resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F _O	<ul style="list-style-type: none"> • Fault signal output terminal. • Fo signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limiting the Fo sink current I_{Fo} up to 1mA.) Normally 10kΩ is recommended.
Temperature output terminal	V _{OT}	<ul style="list-style-type: none"> • LVIC temperature is output by analog signal. • This terminal is connected to the output of OP amplifier internally. • It is recommended to connect 5kΩ pulldown resistor if output linearity is necessary under room temperature.
Inverter DC-link positive terminal	P	<ul style="list-style-type: none"> • DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be located very closely to the P and N terminal of DIIPM. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU, NV, NW	<ul style="list-style-type: none"> • Open emitter terminal of each N-side IGBT • Usually, these terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	<ul style="list-style-type: none"> • Inverter output terminals for connection to inverter load (e.g. motor). • Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1 μ s/div. Please ensure the voltage (including surge) not exceed the specified limitation.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of DIP Ver.5.

2.4.1 Electric Spacing

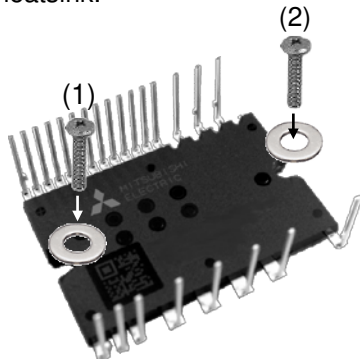
The electric spacing specification of DIP Ver.5 is shown in Table 2-4-1

Table 2-4-1 Minimum insulation distance of DIP Ver.5

	Clearance (mm)	Creepage (mm)
Between live terminals with high potential	2.50	3.00
Between terminals and heat sink	1.45	1.50

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-1. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention to the foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIIPM with the heatsink.



Temporary fastening
(1)→(2)
Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating. Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-1 Recommended screw fastening order

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 0.69N·m, Screw : M3	0.59	-	0.78	N·m
Flatness of outer heat sink	Refer Fig.2-4-2	-50	-	+100	μm

Note : Recommend to use plain washer (ISO7089-7094) in fastening the screws.

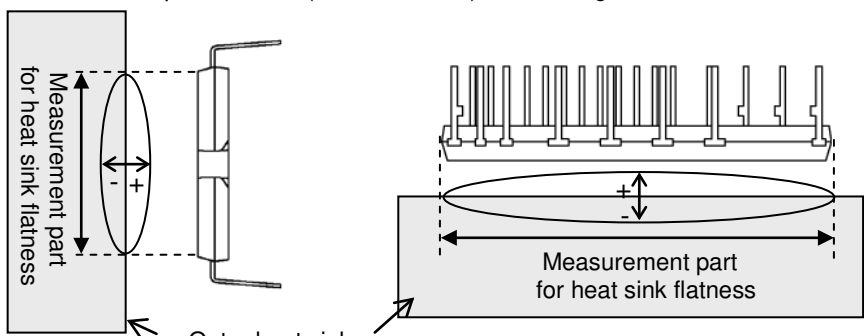


Fig.2-4-2 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

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2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
 (Note: The reflow soldering cannot be recommended for DIIPM.)

(1) Flow (wave) Soldering

DIIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-4-3 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: DIP Ver.5 (Short lead type)

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 350/400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

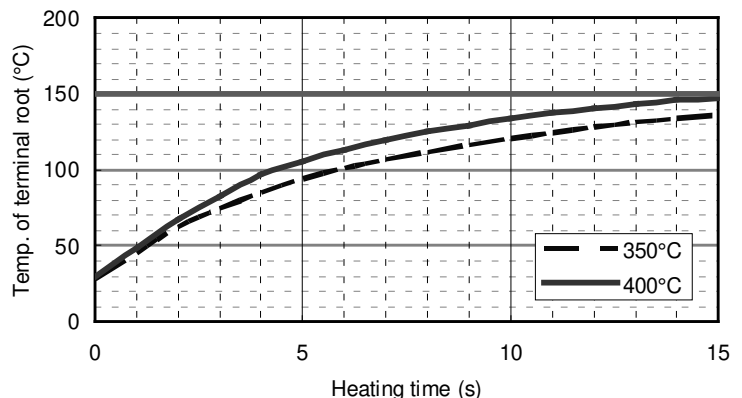
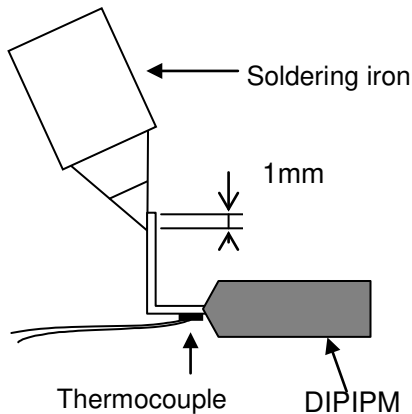


Fig.2-4-3 Heating and measuring point

Fig.2-4-4 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

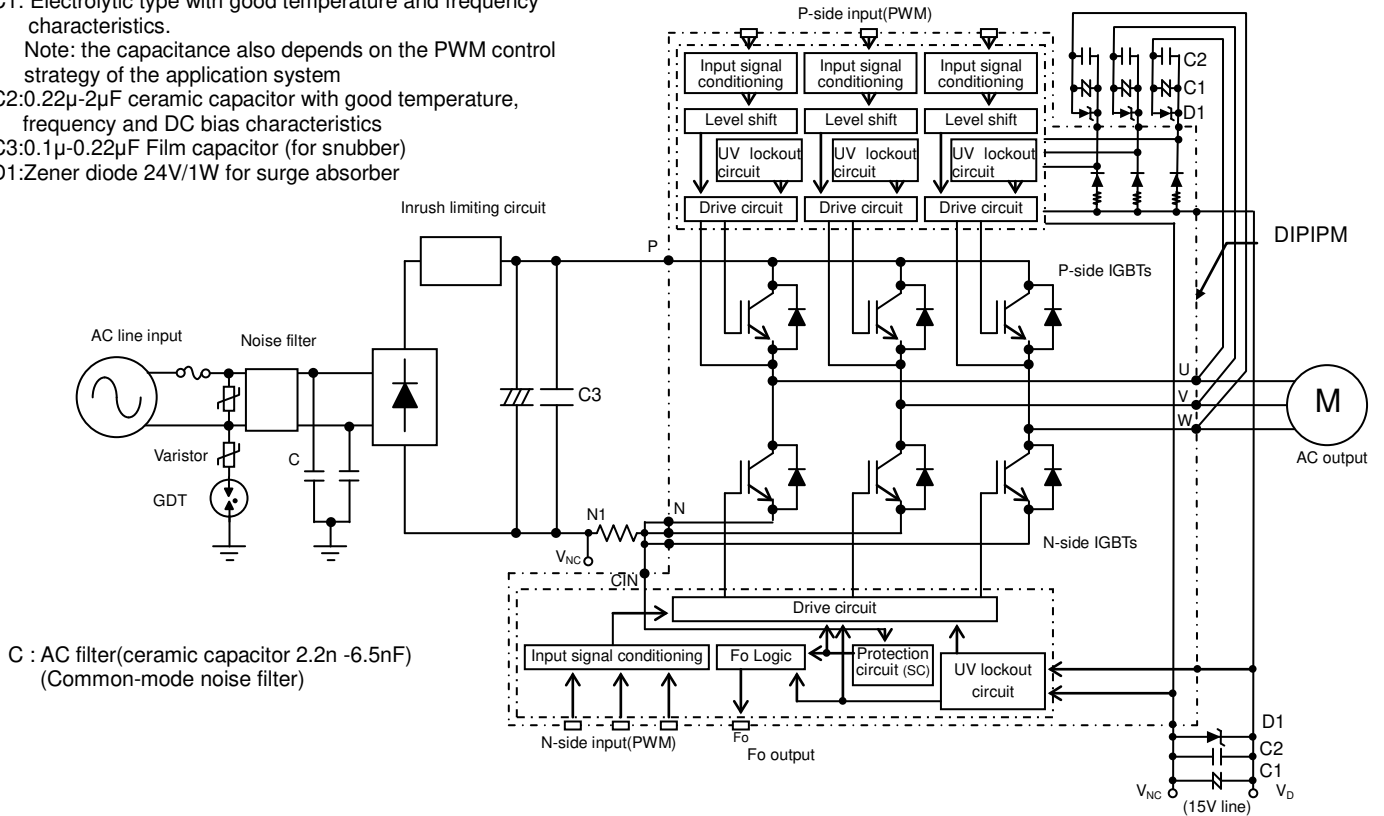
CHAPTER 3 SYSTEM APPLICATION GUIDANCE

3.1 Application Guidance

This chapter states the DIP Ver.5 application method and interface circuit design hints.

3.1.1 System connection

- C1: Electrolytic type with good temperature and frequency characteristics.
- Note: the capacitance also depends on the PWM control strategy of the application system
- C2: 0.22 μ -2 μ F ceramic capacitor with good temperature, frequency and DC bias characteristics
- C3: 0.1 μ -0.22 μ F Film capacitor (for snubber)
- D1: Zener diode 24V/1W for surge absorber



C : AC filter(ceramic capacitor 2.2n -6.5nF)
(Common-mode noise filter)

Fig.3-1-1 Application System block diagram

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3.1.2 Interface Circuit (Direct Coupling Interface example for using one shunt resistor)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU, DSP).

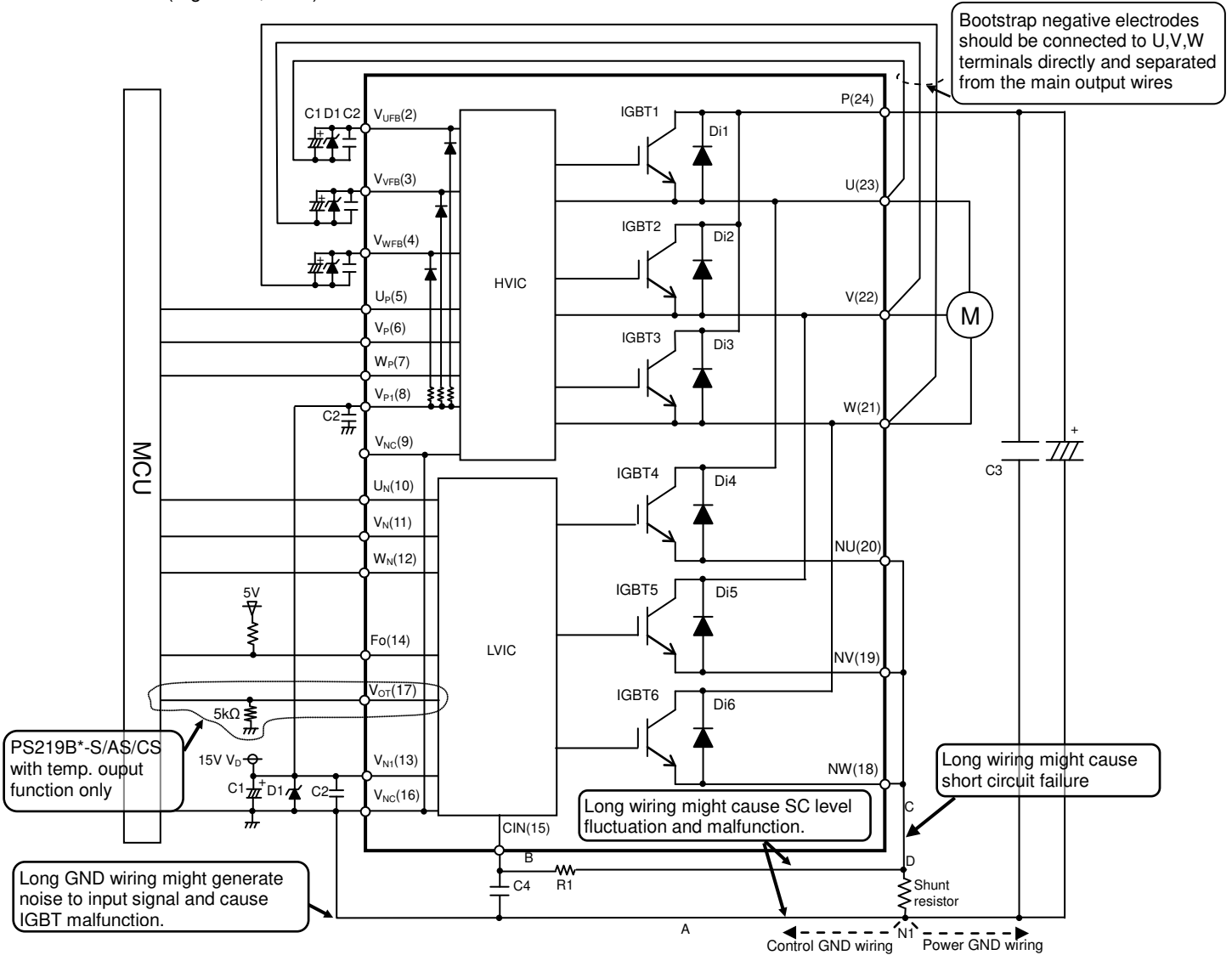


Fig.3-1-2 Interface circuit example except for common emitter type

- (1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
- (2) It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- (3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
- (4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
- (5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- (6) The point D at which the wiring to C_{IN} filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
- (7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- (8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- (9) F_o output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{Fo} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
- (10) Thanks to built-in HVIC, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- (11) Two V_{NC} terminals (9 & 16 pin) are connected inside DIIPM, please connect either one to the 15V power supply GND outside and leave another one open.
- (12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, V_{ripple}≤2Vp-p.

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3.1.3 Interface Circuit (Example of Opto-coupler Isolated Interface)

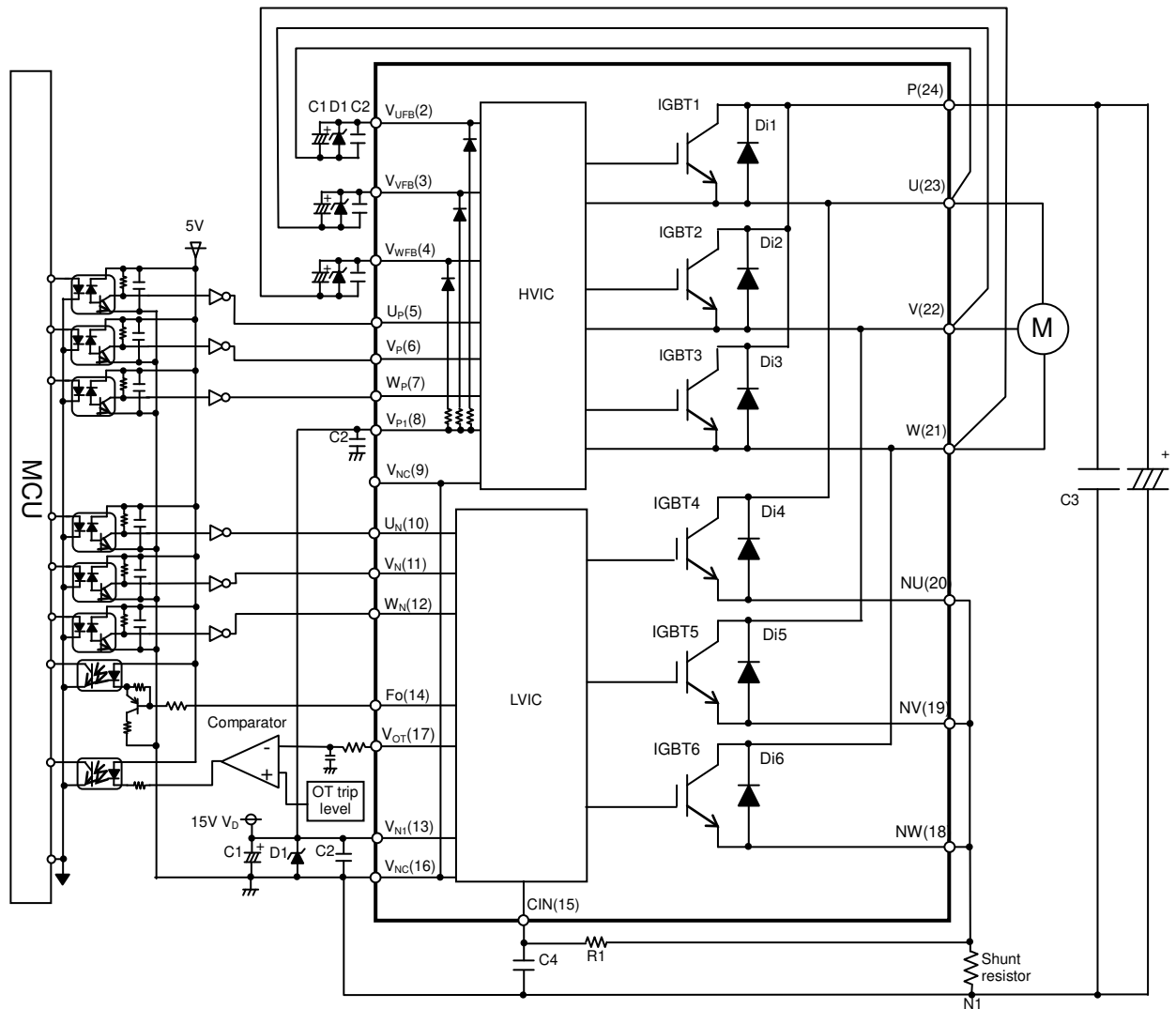


Fig.3-1-3 Interface circuit example with opto-coupler

Note:

- (1) High speed (high CMR) opto-coupler is recommended.
- (2) F_o terminal sink current for inverter part is max. 1 mA.
- (3) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

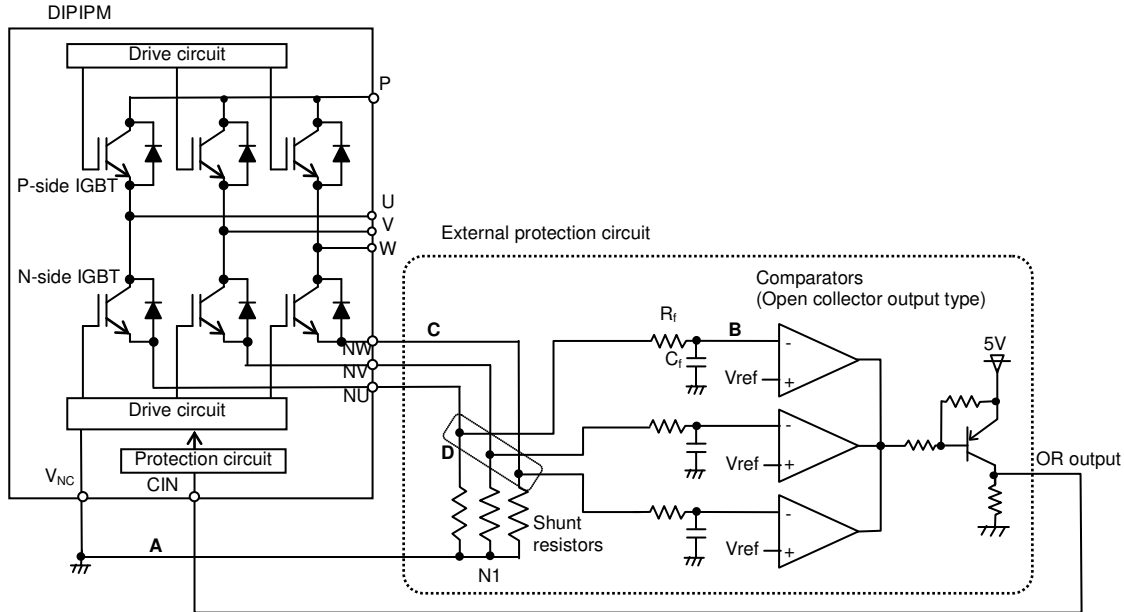


Fig.3-1-4 Interface circuit example

Note:

- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stop within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) The threshold voltage V_{ref} should be set up the same rating of short circuit trip level ($V_{sc(ref)}$ typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value.
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- (6) OR output high level should be over 0.53V (=maximum $V_{sc(ref)}$).

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIIPM is high-active input logic.

A $3.3k\Omega$ (min) pull-down resistor is built-in each input circuits of the DIIPM as shown in Fig.3-1-5, so external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1-1, a direct coupling to 3V class microcomputer or DSP becomes possible.

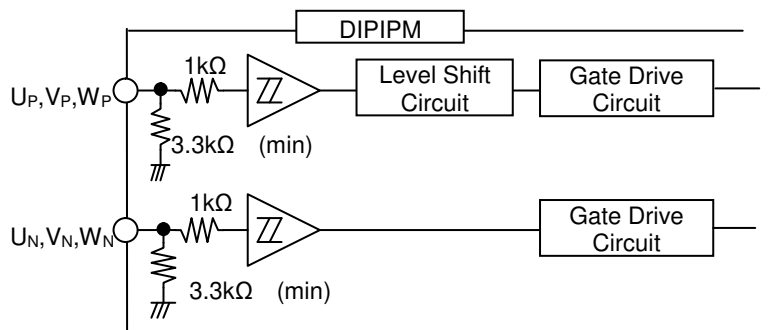


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings($T_j=25^\circ C$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	$V_{th(on)}$	$U_P, V_P, W_P - V_{NC}$ terminals $U_N, V_N, W_N - V_{NC}$ terminals	-	2.1	2.6	V
Turn-off threshold voltage	$V_{th(off)}$		0.8	1.3	-	
Threshold voltage hysteresis	$V_{th(hys)}$		0.35	0.65	-	

Note: There are specifications for the minimum input pulse width in DIIPM Ver.5. DIIPM might make no response if the input signal pulse width (both on and off) is less than the specified value. Please refer to the datasheet for the specification.

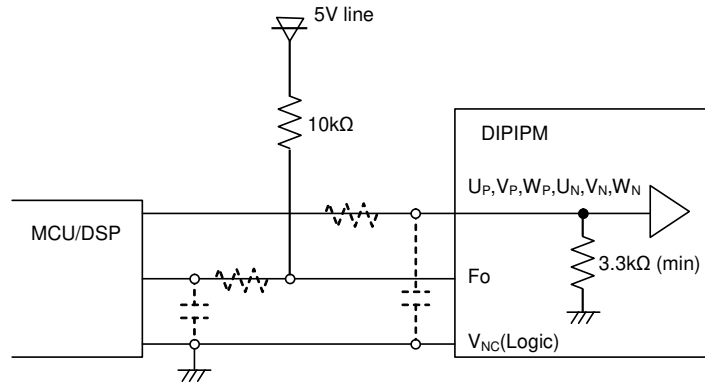


Fig.3-1-6 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

The DIIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

(2) Internal Circuit of F_o Terminal

F_o terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-1-6. Fig.3-1-7 shows the typical V-I characteristics of F_o terminal. The maximum sink current of F_o terminal is 1mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-1-2 Electric characteristics of F_o terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V _{FOH}	V _{SC} =0V, F _o =10kΩ, 5V pulled-up	4.9	-	-	V
	V _{FOL}	V _{SC} =1V, F _o =1mA	-	-	0.95	V

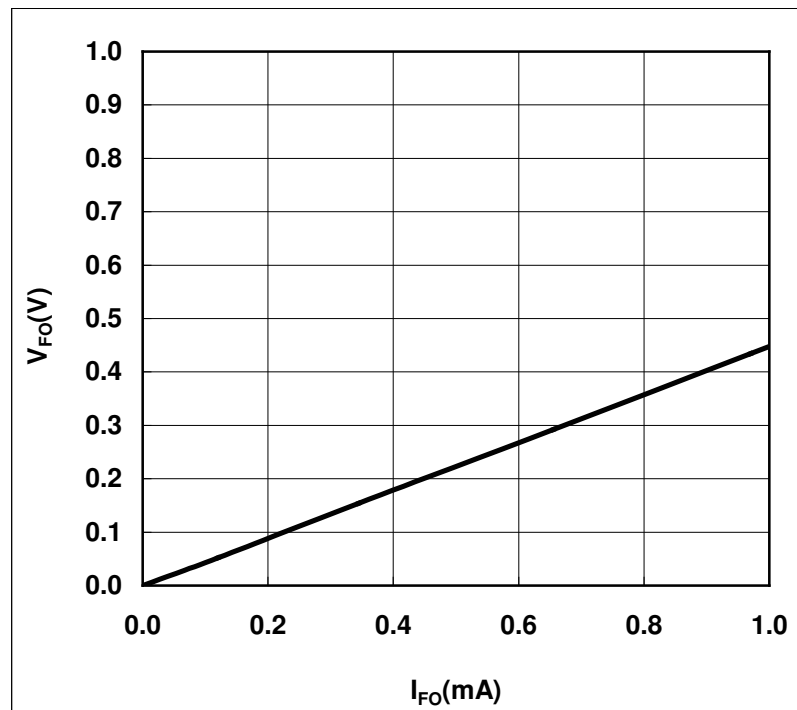


Fig.3-1-7 F_o terminal typical V-I characteristics (V_D=15V, T_J=25°C)

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3.1.6 Snubber Circuit

In order to prevent DIIPM from destruction by extra surge, the wiring length between the smoothing capacitor and DIIPM P terminal – N1 points (shunt resistor terminal) should be as short as possible. Also, a $0.1\mu\sim 0.22\mu\text{F}/630\text{V}$ snubber capacitor should be mounted in the DC-link and near to P, N1.

There are two positions ((1) or (2)) to mount a snubber capacitor as shown in Fig.3-1-8. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) and part-B should be as small as possible. A better wiring example is shown in location (3).

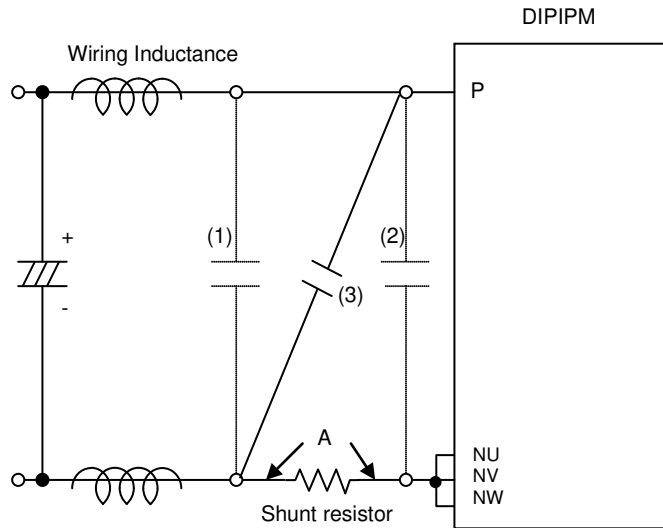


Fig.3-1-8 Recommended snubber circuit location

3.1.7 Recommended Wiring Method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and DIIPM causes so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt resistor and DIIPM should be as short as possible and using low inductance type resistor such as SMD resistor instead of long-lead type resistor.

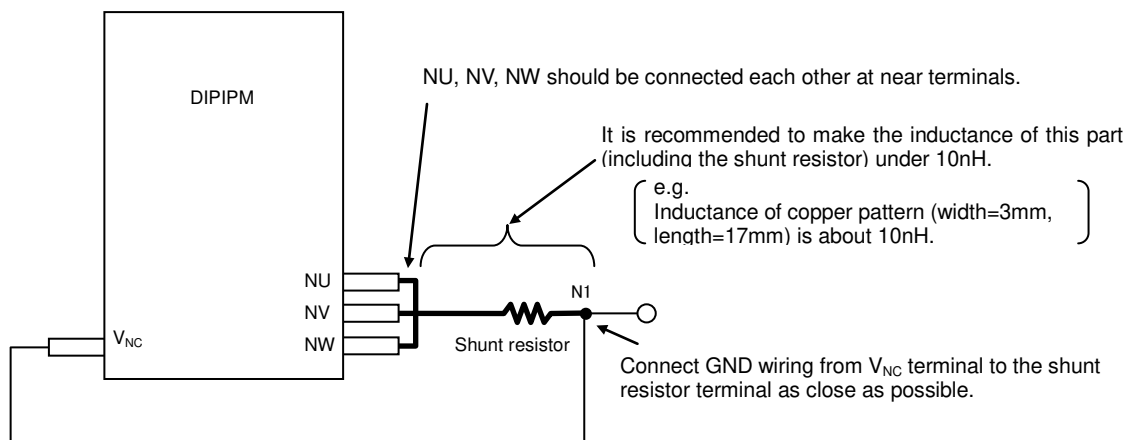


Fig.3-1-9 Wiring instruction (In the case of using with one shunt resistor)

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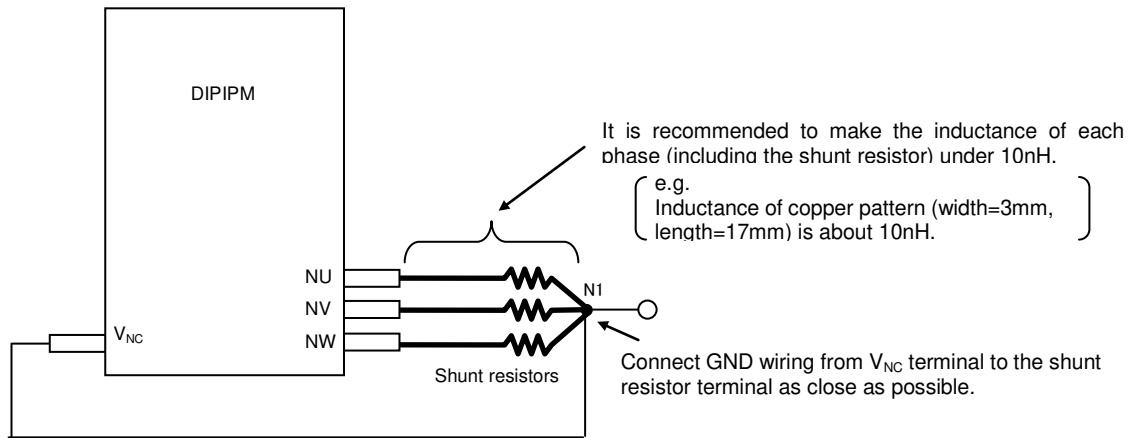


Fig.3-1-10 Wiring instruction for type '-S'

Influence of pattern wiring around the shunt resistor is shown below.

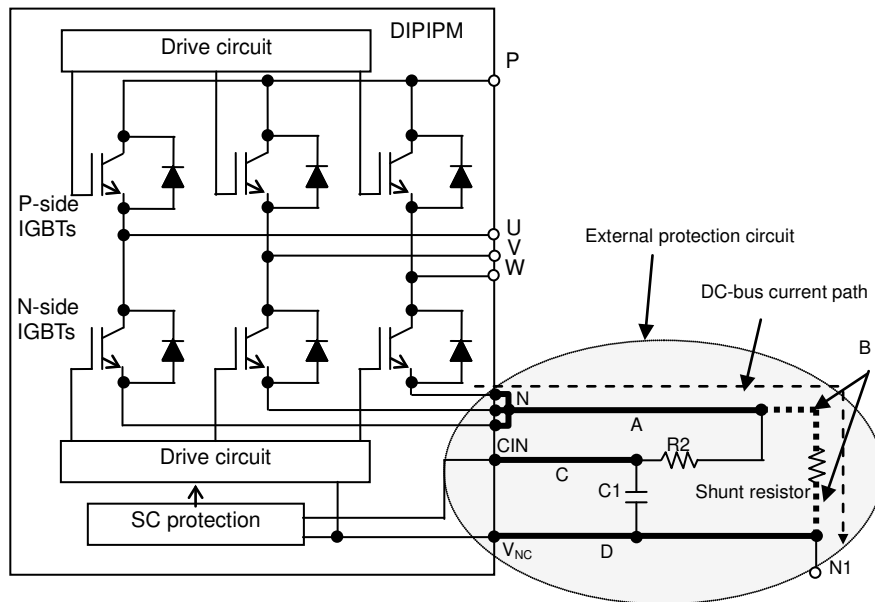


Fig.3-1-11 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side IGBT gate is V_{NC} . If part-A wiring pattern in Fig.3-1-11 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by detecting the voltage of the C1N terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect C1N and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. It is necessary to install the C1R2 filter near C1N, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

3.1.8 Precaution for Wiring on PCB

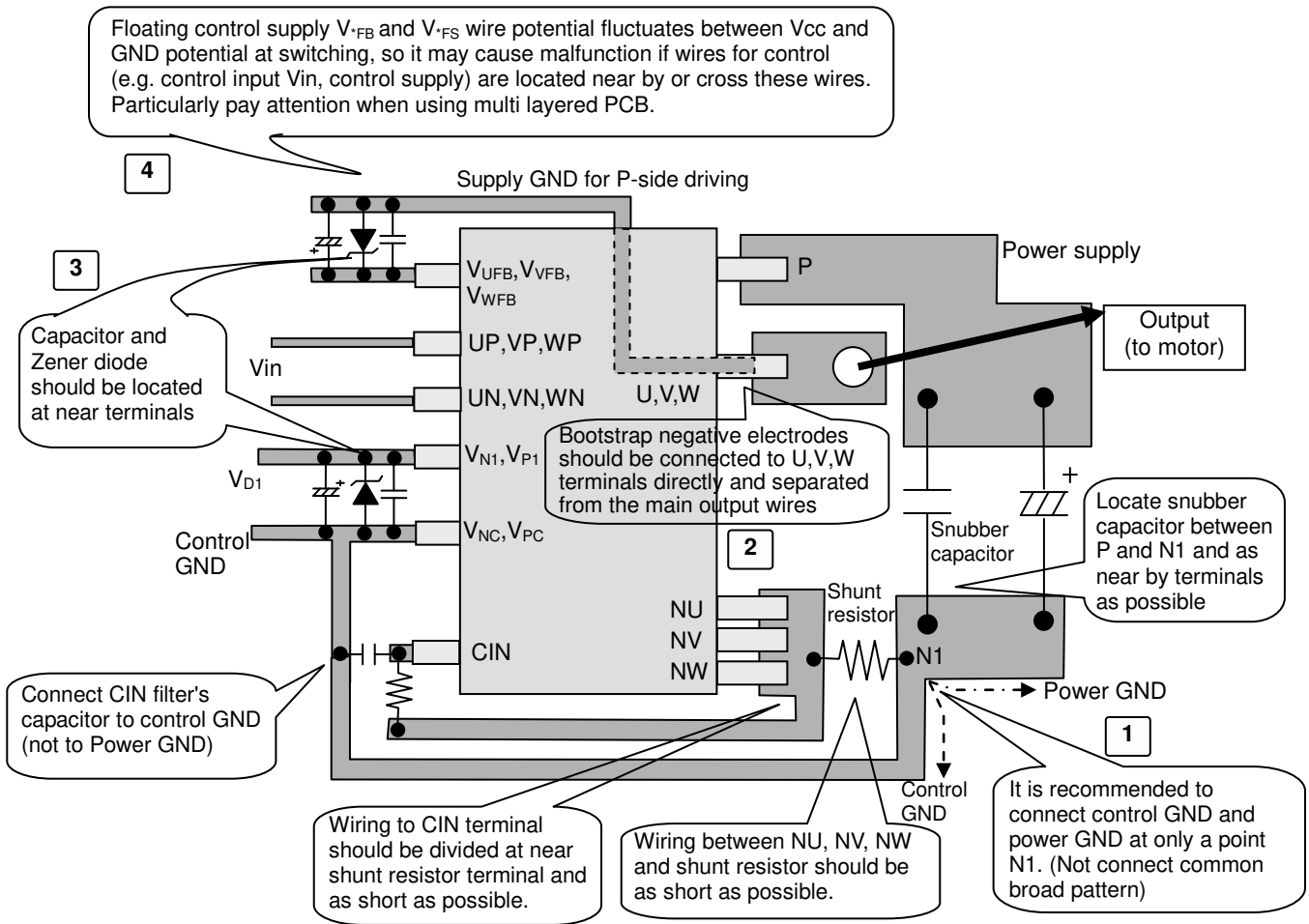


Fig.3-1-12 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Large inductance of wiring between N and N1 terminal	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occur.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIIPM. Then incorrect signals are input to DIIPM input, and arm short (short circuit) might occur.

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3.1.9 Parallel operation of DIIPM

Fig.3-1-13 shows the circuitry of parallel connection of two DIIPMs. Route (1) and (2) indicate the gate charging path of low-side IGBT in DIIPM No.1 & 2 respectively. In the case of DIIPM 1, the parasitic inductance becomes large by long wiring and it might have a negative effect on DIIPM's switching operation. (Chare operation of bootstrap capacitor for high-side might be affected too.) Also, such a wiring makes DIIPM be affected by noise easily, then it might lead to malfunction. If more DIIPMs are connected in parallel, GND pattern becomes longer and the influence to other circuit (protection circuit etc.) by the fluctuation of GND potential is conceivable, therefore parallel connection is not recommended.

Because DIIPM doesn't consider the fluctuation of characteristics between each phases definitely, it cannot be recommended to drive same load by parallel connection with other phase IGBT or IGBT of other DIIPM.

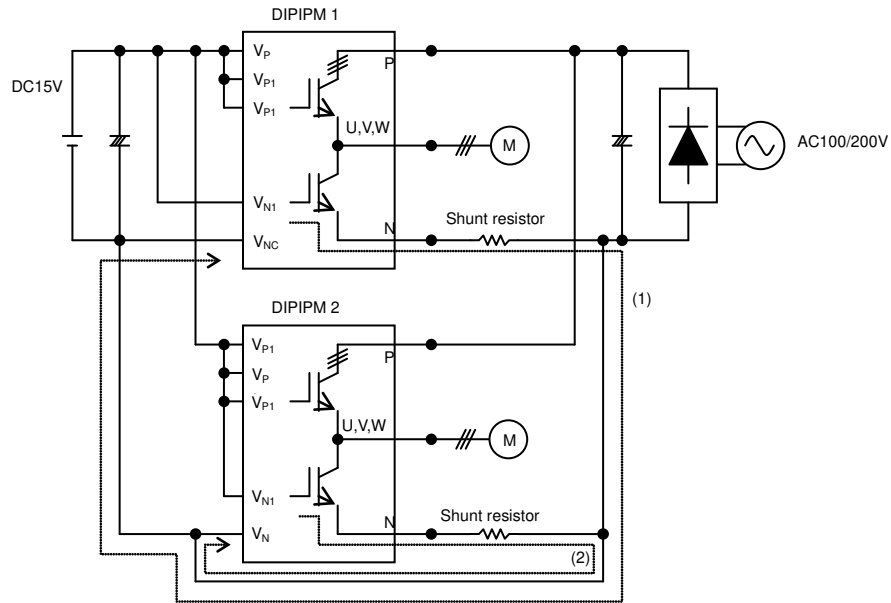


Fig.3-1-13 Parallel operation

3.1.10 SOA of DIP Ver.5

The following describes the SOA (Safety Operating Area) of the DIP Ver.5.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: Total amount of V_{CC} and surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(prot)}$: DC-link voltage that DIIPM can protect itself.

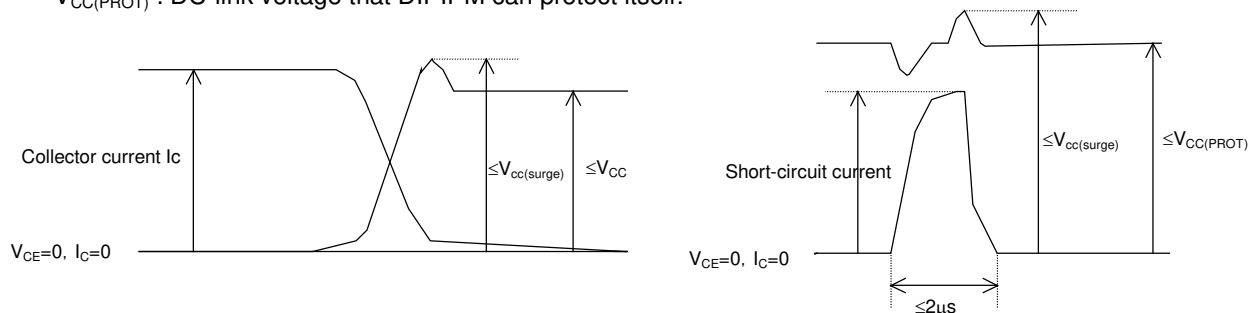


Fig.3-1-14 SOA at switching mode and short-circuit mode

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC} , that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC} , that is, 400V.

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3.1.11 SCSOA

Fig.3-1-15~17 show the typical SCSOA performance curves of PS219B2, PS219B3 and PS219B4.

(Conditions: $V_{CC}=400V$, $T_j=125^{\circ}C$ at initial state, $V_{CC}(\text{surge})\leq 500V$ (surge included), non-repetitive, 2m load.)

In the case of PS219B4, it can shutdown safely an SC current that is about 8.6 times of its current rating under the conditions only if the IGBT conducting period is less than $3.2\mu s$. Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

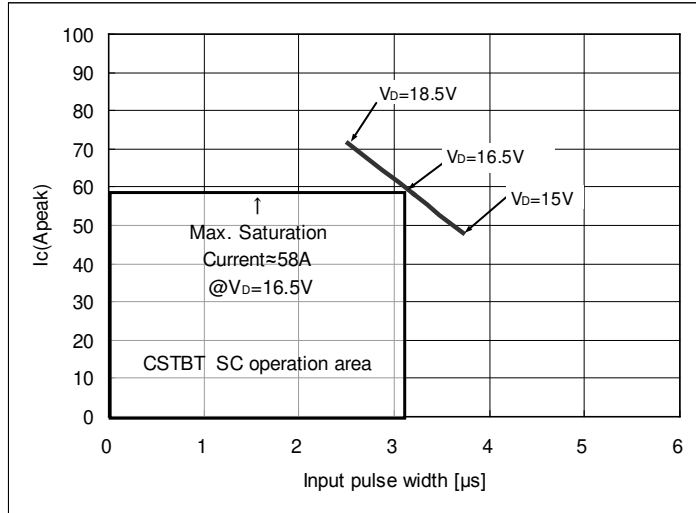


Fig.3-1-15 Typical SCSOA curve of PS219B2

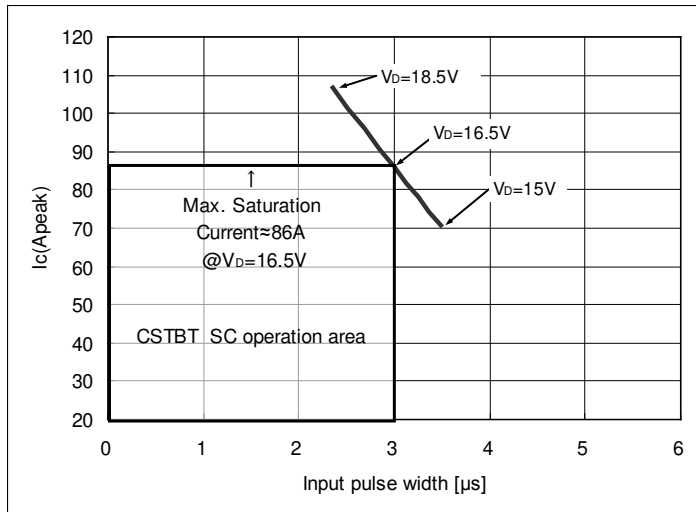


Fig.3-1-16 Typical SCSOA curve of PS219B3

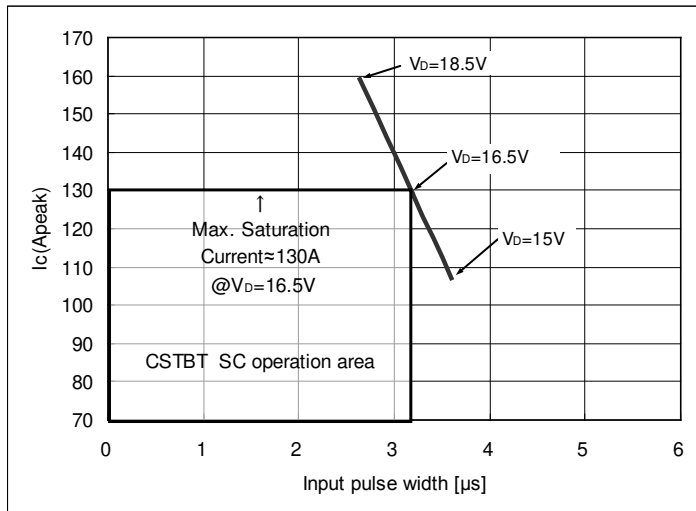


Fig.3-1-17 Typical SCSOA curve of PS219B4

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

3.1.12 Power Life Cycles

When DIIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔT_j). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-18 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔT_j). (The curve is a regression curve based on 3 points of $\Delta T_j=46, 88, 98K$ with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

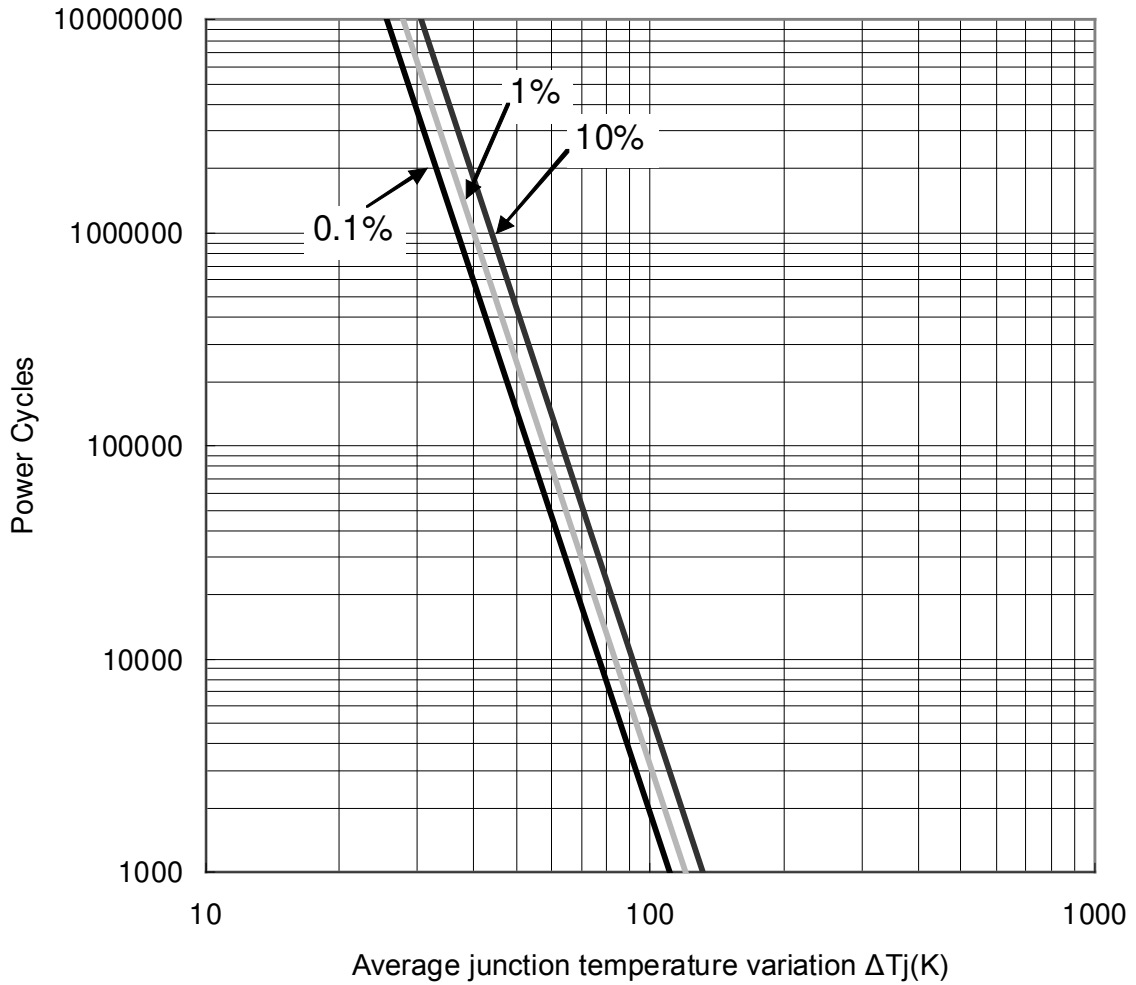


Fig.3-1-18 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

- (1) PWM controlled VVVF inverter with sinusoidal output;
- (2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
- (3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
- (4) Output current varies with $I_{cp} \cdot \sin x$ and it does not include ripple.
- (5) Power factor of load output current is $\cos\theta$, ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+D \times \sin x}{2}$ which is equivalent to the output voltage variation. From the power factor $\cos\theta$, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$\begin{aligned} \text{Output current} &= I_{cp} \times \sin x \\ \text{PWM Duty} &= \frac{1 + D \times \sin(x + \theta)}{2} \end{aligned}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$\begin{aligned} V_{ce(sat)} &= V_{ce(sat)}(@ I_{cp} \times \sin x) \\ V_{ec} &= (-1) \times V_{ec}(@ I_{cp} \times \sin x) \end{aligned}$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi} \int_0^\pi (I_{cp} \times \sin x) \times V_{ce(sat)}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi} \int_\pi^{2\pi} ((-1) \times I_{cp} \times \sin x) \times (-1) \times V_{ec}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi} \int_0^\pi (P_{sw(on)}(@ I_{cp} \times \sin x) + P_{sw(off)}(@ I_{cp} \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

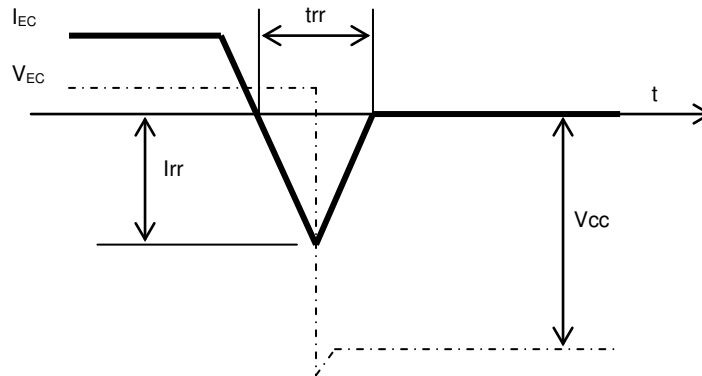


Fig.3-2-1 Ideal FWDi recovery characteristics curve

$$P_{SW} = \frac{I_{rr} \times V_{CC} \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{CC} \times trr(@ I_{cp} \times \sin x)}{4} \times fc \cdot dx \\ & = \frac{1}{8} \int_{\rho}^{2\pi} I_{rr}(@ I_{cp} \times \sin x) \times V_{CC} \times trr(@ I_{cp} \times \sin x) \times fc \cdot dx \end{aligned}$$

- Attention of applying the power loss simulation for inverter designs
 - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC} , and P_{sw} corresponding to the output current. The worst condition is most important.
 - PWM duty depends on the signal generating way.
 - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
 - $V_{CE(sat)}$, V_{EC} and $P_{sw}(on, off)$ should be the values at $T_j=125^{\circ}C$.

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3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: $V_{CC}=300V$, $V_D=V_{DB}=15V$, $V_{CE(sat)}=Typ.$, Switching loss=Typ., $T_j=125^\circ C$, $T_f=100^\circ C$, $R_{th(j-c)}=Max.$, $R_{th(c-f)}=0.3^\circ C/W$ (per 1/6 module), P.F=0.8, 3-phase PWM modulation, 60Hz sine waveform output

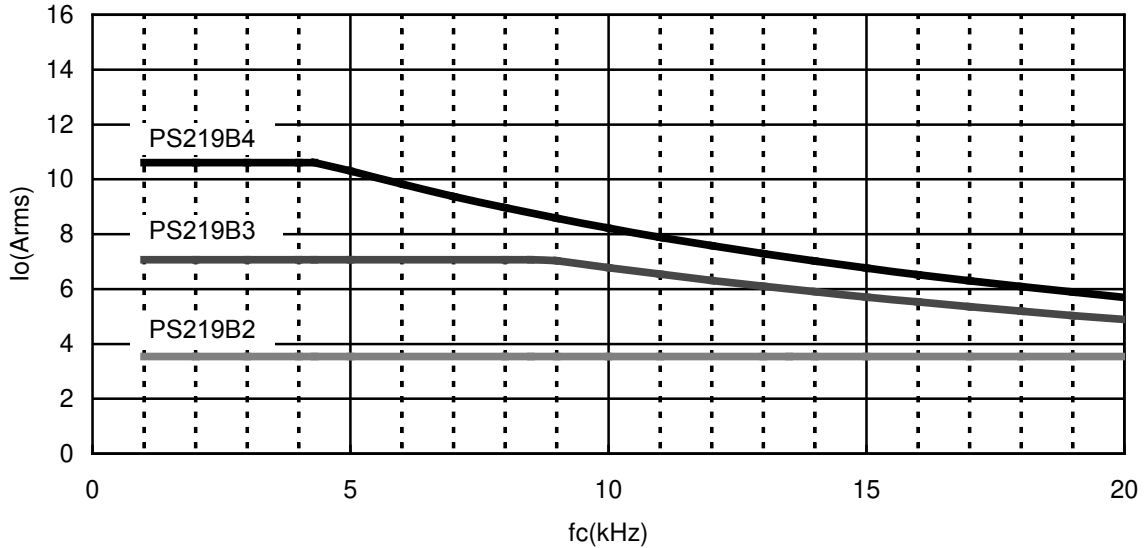


Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ($T_f=100^\circ C$, $T_j=125^\circ C$). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously. The inverter loss can be calculated by the free power loss simulation software. The software can be downloaded at Mitsubishi Electric web site.

URL: <http://www.mitsubishielectric.com/semiconductors/>

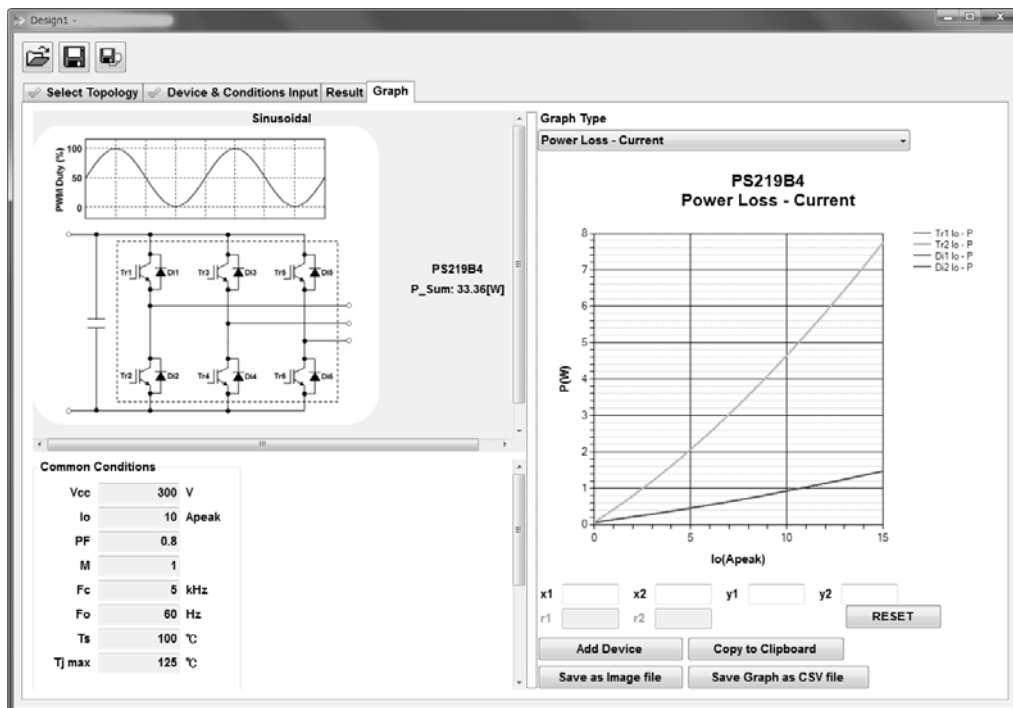


Fig.3-2-3 Loss simulator screen image

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

DIP Ver.5 series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

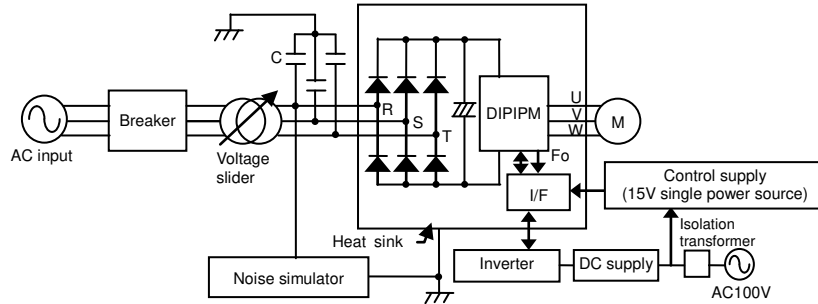


Fig.3-3-1 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

$V_{CC}=300V$, $V_D=15V$, $T_a=25^{\circ}C$, no load

Scheme of applying noise: From AC line (R, S, T), Period $T=16ms$, Pulse width $t_w=0.05-1\mu s$, input in random.

3.3.2 Countermeasures and Precautions

DIIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

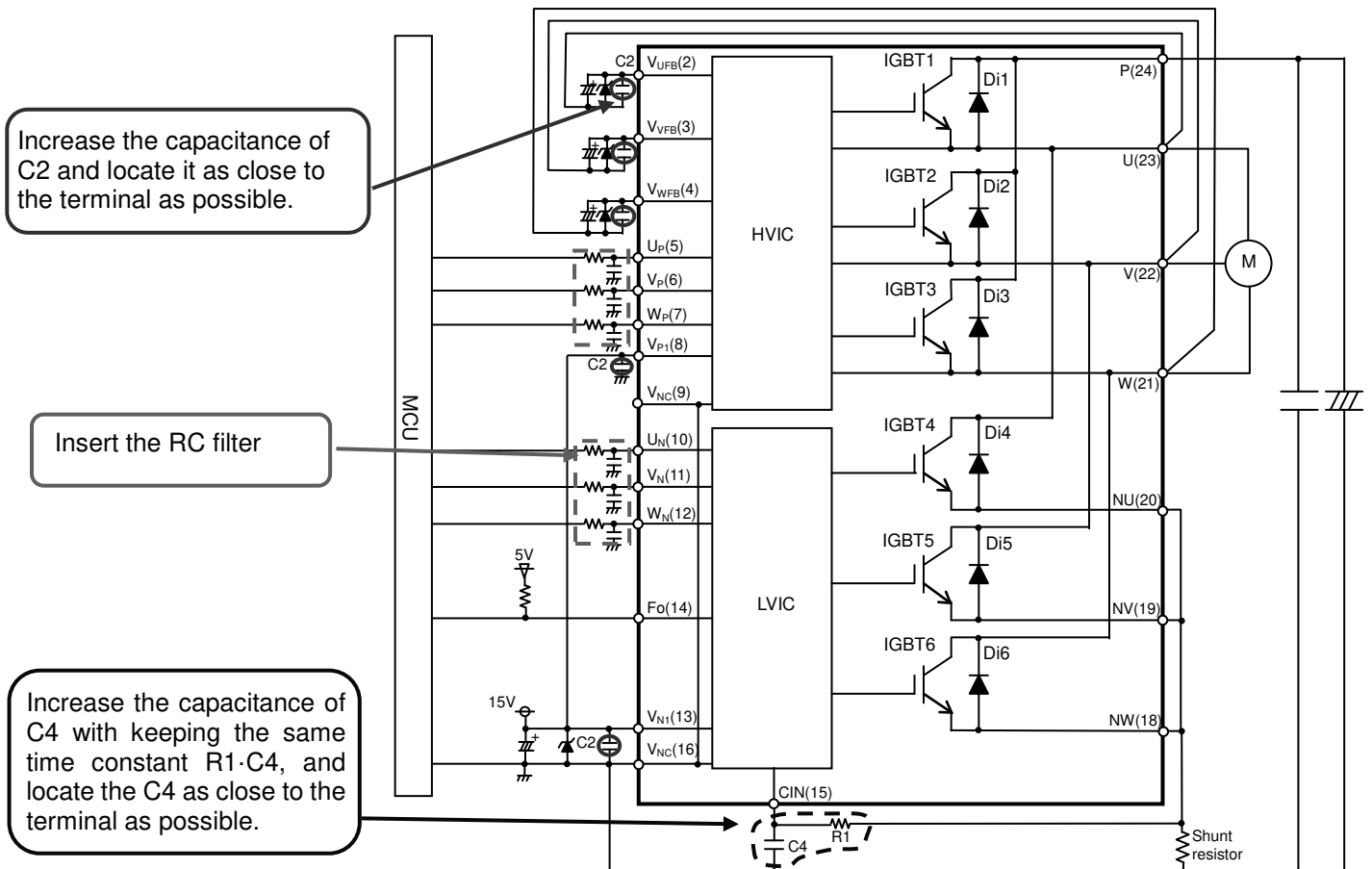


Fig.3-3-2 Example of countermeasures for inverter part

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

3.3.3 Static Electricity Withstand Capability

DIIPM has been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-3-3, 4. The results (typical data) are described in Table 3-3-1.

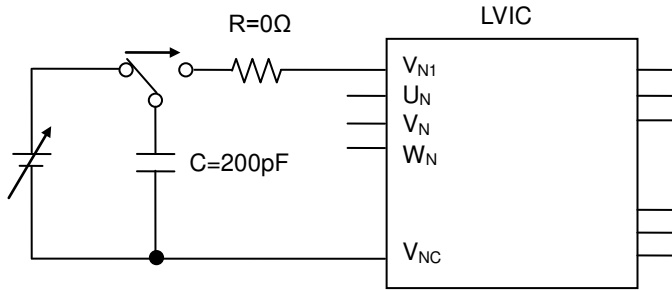


Fig.3-3-3 LVIC terminal Surge Test circuit

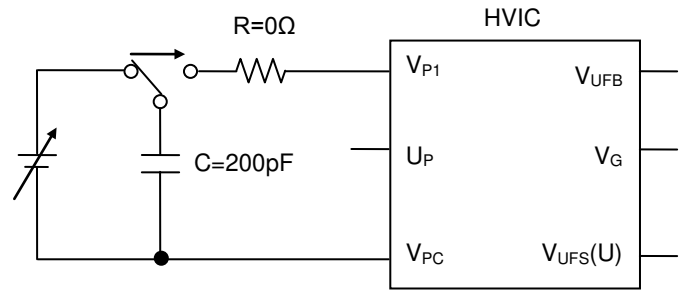


Fig.3-3-4 HVIC terminal Surge Test circuit

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage. (Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-3-1 Typical ESD capability

[Control terminal part] Common data for PS219B2/3/4 because of all types have same interface circuit.

Terminals	+	-
UP, VP, WP-V _{NC}	0.6	0.7
V _{P1} - V _{NC}	1.3	1.1
V _{UFB} -U, V _{VFB} -V, V _{WFB} -W	1.5	1.9
UN, VN, WN-V _{NC}	0.6	0.6
V _{N1} -V _{NC}	4.0 or more	2.8
CIN-V _{NC}	0.3	0.5
F0-V _{NC}	0.5	1.1
V _{OT} -V _{NC} *	0.9	0.9

*) The type with temperature output only (PS219B-S/AS/CS)

[Power terminal part]

PS219B4

Terminals	+	-
P-NU, NV, NW	3.4	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

PS219B3

Terminals	+	-
P-NU, NV, NW	2.0	4.0 or more
U-NU, V-NV, W-NW	3.6	4.0 or more

PS219B2

Terminals	+	-
P-NU, NV, NW	1.4	4.0 or more
U-NU, V-NV, W-NW	3.0	4.0 or more

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. (Super mini DIIPM Ver.5 series integrates BSD and limiting resistor and can make bootstrap circuit by adding outer BSC only.) It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

The BSD characteristics for Super mini DIIPM Ver.5 series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

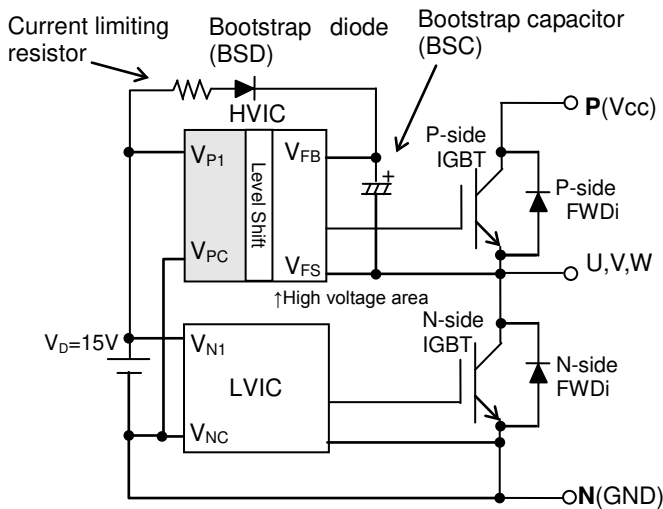


Fig.4-1-1 Bootstrap Circuit Diagram

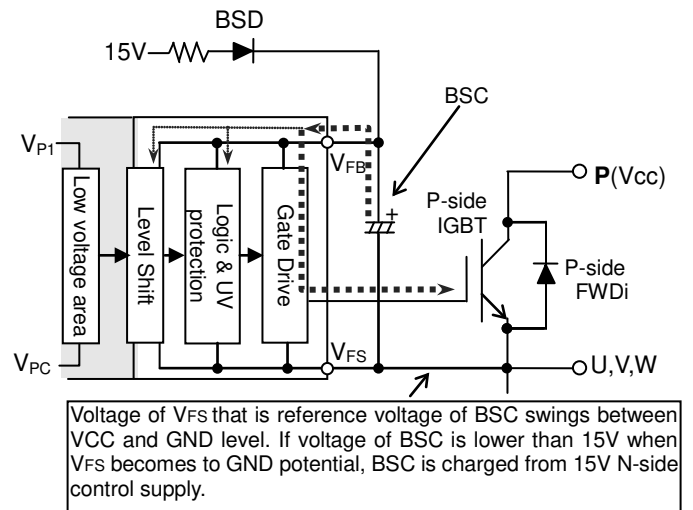


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.1mA for PS219B* series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current exceeds 0.1mA and increases proportional to carrier frequency. For reference, Fig.4-2-1~3 show I_{DB} - carrier frequency f_c characteristics for PS219B2, PS219B3 and PS219B4. (Conditions: $V_D=V_{DB}=15V$, $T_j=125^\circ C$ at which I_{DB} becomes larger, IGBT ON Duty=10, 30, 50, 70, 90%)

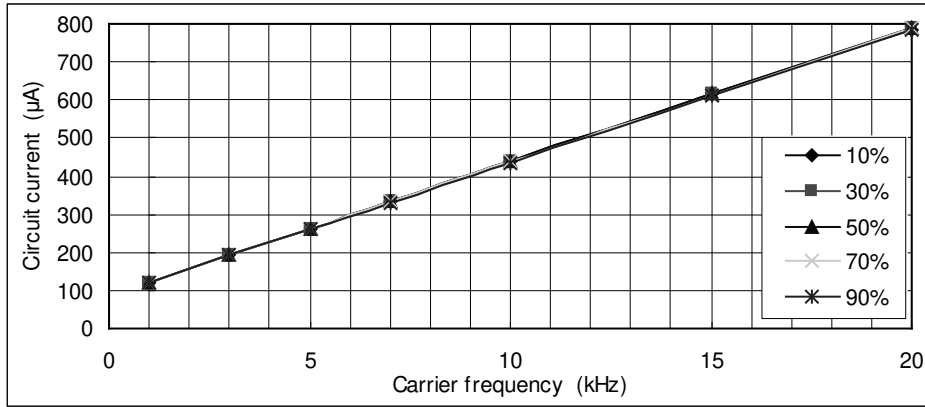


Fig.4-2-1 I_{DB} vs. Carrier frequency for PS219B2

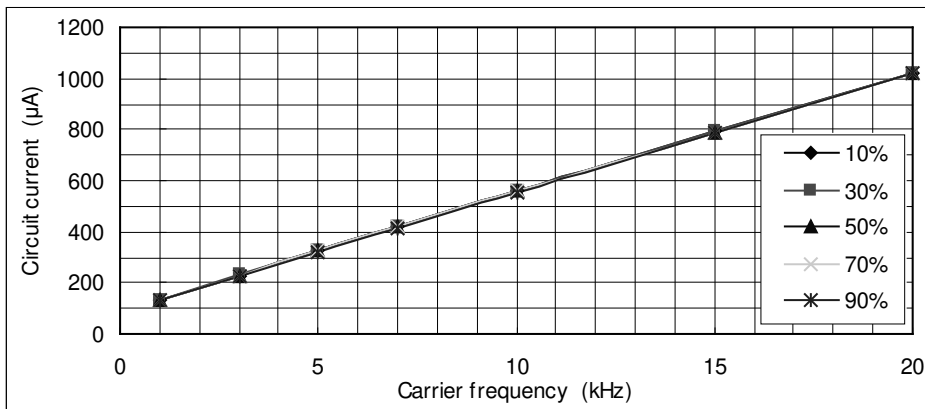


Fig.4-2-2 I_{DB} vs. Carrier frequency for PS219B3

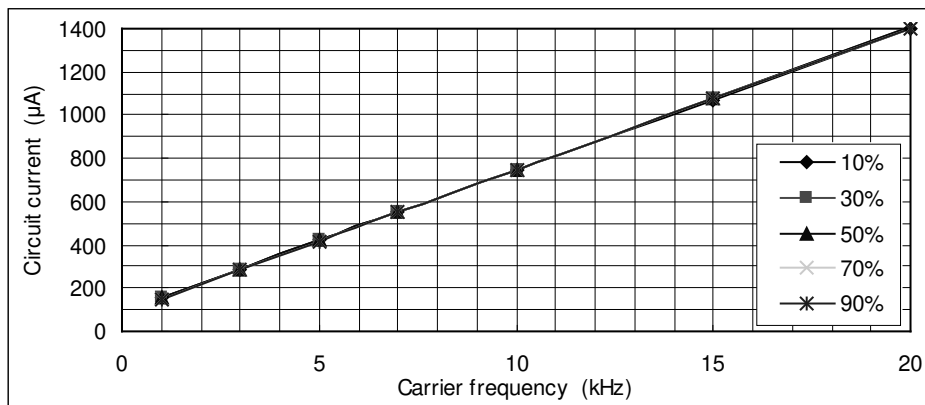


Fig.4-2-3 I_{DB} vs. Carrier frequency for PS219B4

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4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "Bootstrap Circuit Design Manual"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-3-1.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta: -20~ 85°C)	<ul style="list-style-type: none"> Aluminum type: Low temp.: -10% High temp: +10% Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10% 	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

DIP Ver.5 integrates bootstrap diode for P-side driving supply. This BSD incorporates current limiting resistor (typ. 100Ω). So there isn't any limitation about bootstrap capacitance like former PS219A* has (22μF or less in the case of one long pulse initial charging). The VF-IF characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-3-1 and Table 4-3-2.

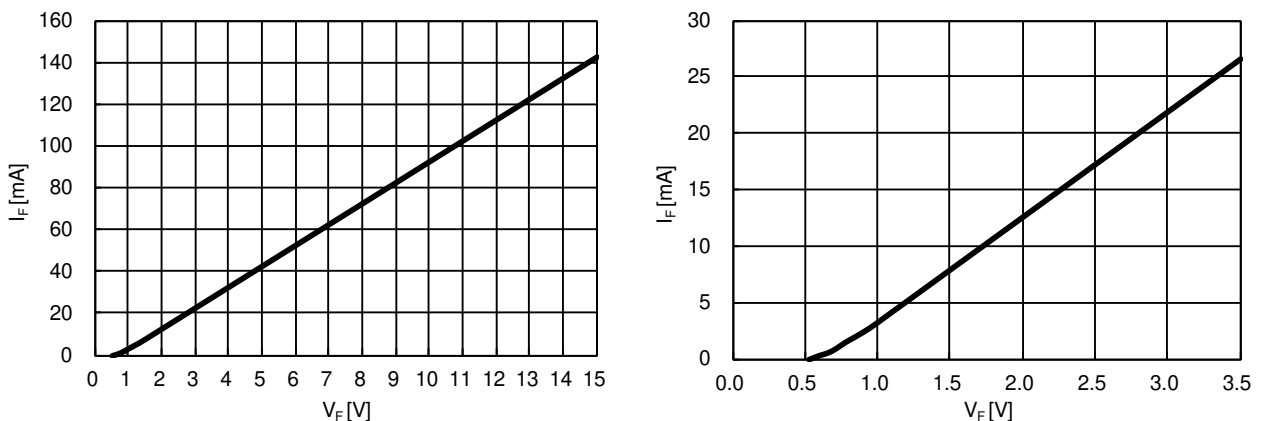


Fig.4-3-1 VF-IF curve for bootstrap Diode (The right figure is enlarged view)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	$I_F=10mA$ including voltage drop by limiting resistor	1.1	1.7	2.3	V
Built-in limiting resistance	R	Included in bootstrap Di	80	100	120	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

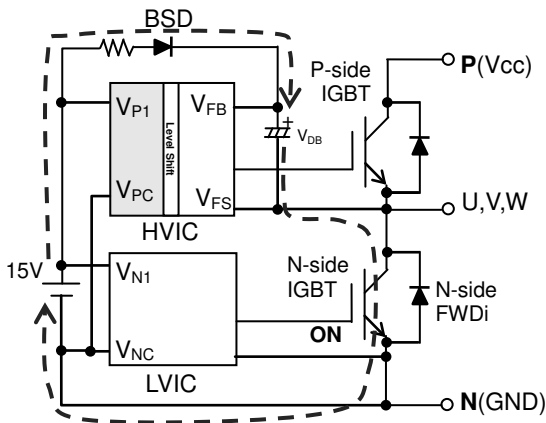


Fig.4-4-1 Initial charging root

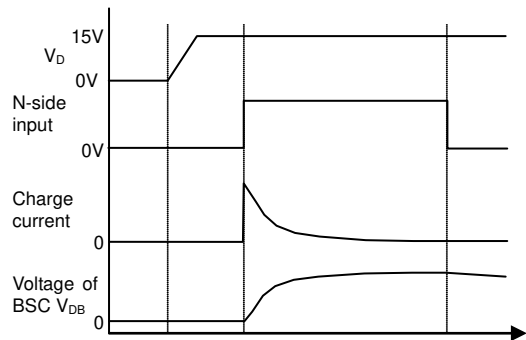


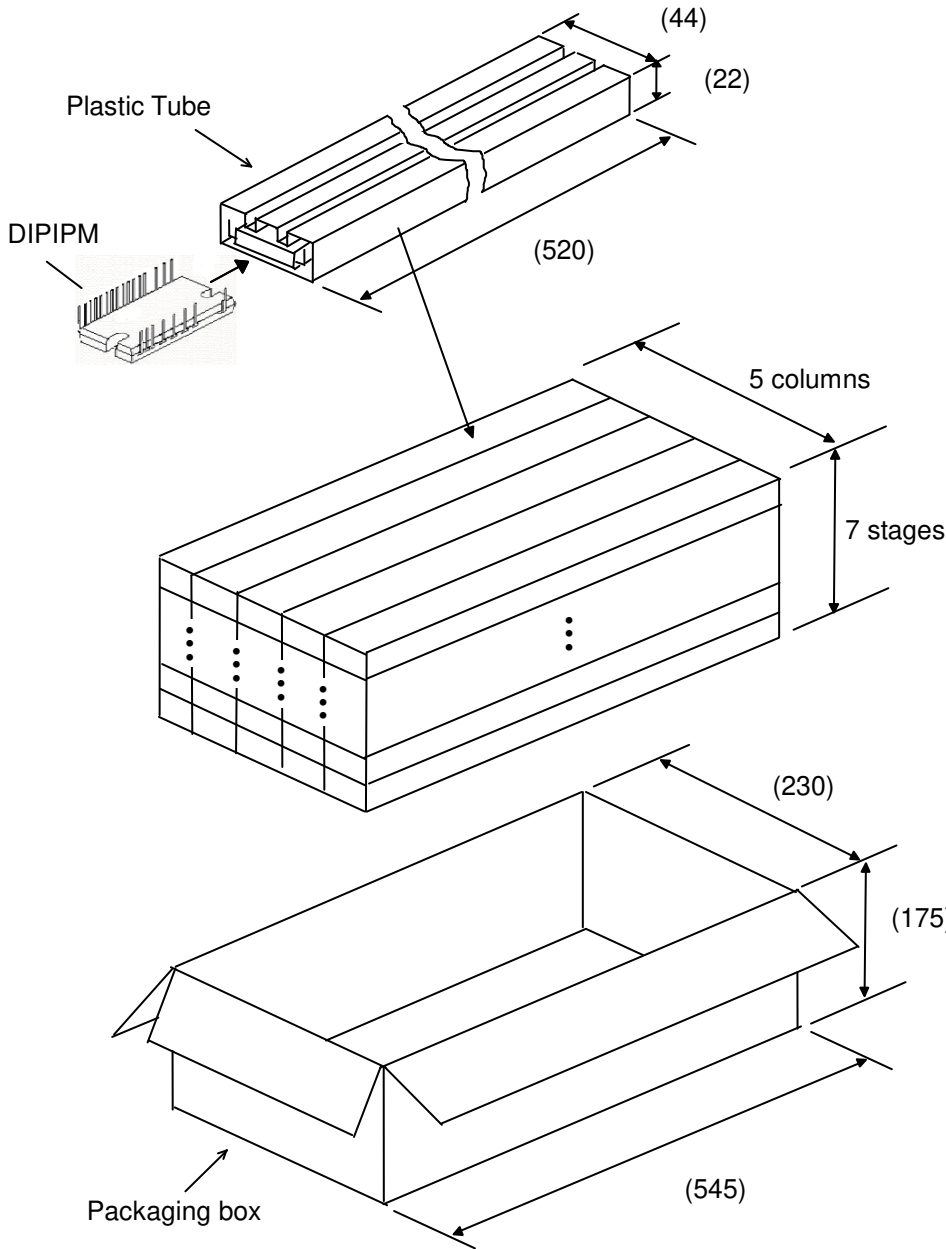
Fig.4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for the reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 0.7μs or more for Super mini DIIPM Ver.5. Refer the datasheet for each product.)

CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification



Quantity:

12pcs per 1 tube

Total amount in one box (max):

Tube Quantity: $5 \times 7 = 35$ pcs
IPM Quantity: $35 \times 12 = 420$ pcs

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.


Weight (max):

About 8.5g per 1 pcs of DIIPM
About 200g per 1 tube
About 8.3kg per 1 box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

 <h1>Cautions</h1>	
Transportation	<ul style="list-style-type: none">·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.·Throwing or dropping the packaging boxes might cause the devices to be damaged.·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	<ul style="list-style-type: none">·We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	<ul style="list-style-type: none">·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	<ul style="list-style-type: none">·Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	<ul style="list-style-type: none">·The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	<ul style="list-style-type: none">·ICs and power chips with MOS gate structure are used for the DIIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. <p>(1)Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none">·Containers that charge static electricity easily should not be used for transit and for storage.·Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands.·Should not be taking out DIIPM from tubes until just before using DIIPM and never touch terminals with bare hands.·During assembly and after taking out DIIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats.·When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board.·If using a soldering iron, earth its tip. <p>(2)Notice when the control terminals are open</p> <ul style="list-style-type: none">·When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.·Short the terminals before taking a module off.

Super Mini DIIPM Ver.5 Series APPLICATION NOTE

Revision Record

Rev.	Date	Points
-	15/10/2012	New
1	15/12/2013	2.1.1 Description of (7) Isolation voltage is revised.
2	1/ 5/2014	<ul style="list-style-type: none">· Revise Section 2.4.2· Revise Fig.3-2-3· Add section 4.4

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