

# FAN6555

## 2A DDR Bus Termination Regulator

### Features

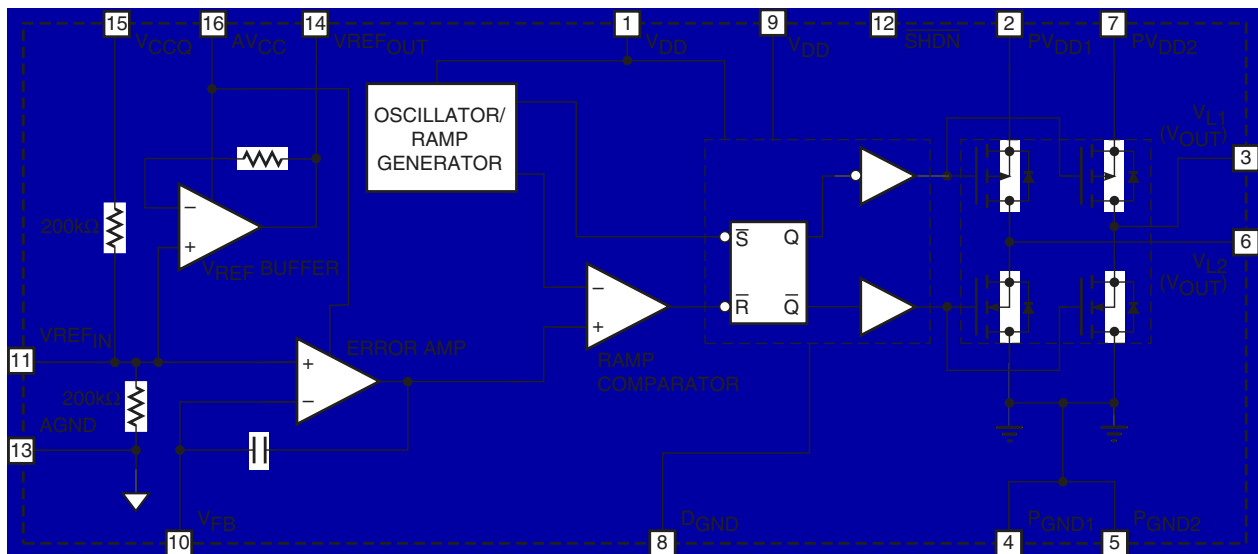
- Can source and sink up to 2A continuous, 3A peak
- No heatsink required
- Integrated Power MOSFETs
- Generates termination voltages for DDR SDRAM
- $V_{REF}$  input available for external voltage divider
- Separate voltages for  $V_{CCQ}$  and  $PV_{DD}$
- Buffered  $V_{REF}$  output
- $V_{OUT}$  of  $\pm 3\%$  or less at 2A
- Minimum external components
- 16-pin SOIC package
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  operating temperature range
- Shutdown for standby or suspend mode operation
- Thermal Shutdown  $\approx 130^{\circ}\text{C}$

### Description

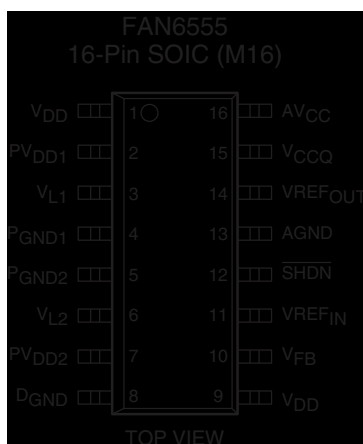
The FAN6555 switching regulator is designed to convert voltage supplies ranging from 2.3V to 4V into a desired output voltage or termination voltage for DDR SDRAM memory. The FAN6555 can be implemented to produce regulated output voltages in two different modes. In the default mode, when the  $V_{REF}$  pin is open, the FAN6555 output voltage is 50% of the voltage applied to  $V_{CCQ}$ . The FAN6555 can also be used to produce various user-defined voltages by forcing a voltage on the  $V_{REFIN}$  pin. In this case, the output voltage follows the input  $V_{REFIN}$  voltage. The switching regulator is capable of sourcing or sinking up to 2A of current while regulating an output  $V_{TT}$  voltage to within 3% or less. Transient output currents of  $\pm 3\text{A}$  can also be accommodated.

The FAN6555 can also be used in conjunction with series termination resistors to provide an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

### Block Diagram



## Pin Configuration



## Pin Description

Pin	Name	Function
1	V <sub>DD</sub>	Digital supply voltage
2	PV <sub>DD1</sub>	Voltage supply for internal power transistors
3	V <sub>L1</sub>	Output voltage/ inductor connection
4	P <sub>GND1</sub>	Ground for output power transistors
5	P <sub>GND2</sub>	Ground for output power transistors
6	V <sub>L2</sub>	Output voltage/inductor connection
7	PV <sub>DD2</sub>	Voltage supply for internal power transistors
8	D <sub>GND</sub>	Digital ground
9	V <sub>DD</sub>	Digital supply voltage
10	V <sub>FB</sub>	Input for external compensation feedback
11	VREF <sub>IN</sub>	Input for external reference voltage
12	SHDN	Shutdown active low. CMOS input level
13	AGND	Ground for internal reference voltage divider
14	VREF <sub>OUT</sub>	Reference voltage output
15	V <sub>CCQ</sub>	Voltage reference for internal voltage divider
16	AV <sub>CC</sub>	Analog voltage supply

## Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
$PV_{DD}$		4.5	V
Voltage on Any Other Pin	GND – 0.3	$V_{IN} + 0.3$	V
Average Switch Current ( $I_{AVG}$ )		2.0	A
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Thermal Resistance: Junction to Case ( $\theta_{JC}$ )		30	°C/W
Junction to Ambient ( $\theta_{JA}$ )		88	
Output Current, Source or Sink (peak)		3.0	A

## Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range	-40	+85	°C
$PV_{DD}$ Operating Range	2.0	4.0	V
$V_{CCQ}$ Operating Range	1.4	4.0	V

## Electrical Characteristics

Unless otherwise specified,  $AV_{CC} = V_{DD} = PV_{DD} = 3.3V \pm 10\%$ ,  $T_A$  = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Switching Regulator</b>							
$V_{TT}$	Output Voltage, $V_{TT}$ (See Figure 1)	$I_{OUT} = 0$ , $V_{REF} = \text{open}$ Note 2	$V_{CCQ} = 2.3V$	1.12	1.15	1.18	V
			$V_{CCQ} = 2.5V$	1.22	1.25	1.28	V
			$V_{CCQ} = 2.7V$	1.32	1.35	1.38	V
		$I_{OUT} = \pm 2A$ , $V_{REF} = \text{open}$ $T_A = 25^\circ C$ Note 2	$V_{CCQ} = 2.3V$	1.09	1.15	1.21	V
			$V_{CCQ} = 2.5V$	1.19	1.25	1.31	V
			$V_{CCQ} = 2.7V$	1.28	1.35	1.42	V
$V_{REF_{OUT}}$	Internal Resistor Divider	$I_{OUT} = 0$ Note 2	$V_{CCQ} = 2.3V$	1.139	1.15	1.162	V
			$V_{CCQ} = 2.5V$	1.238	1.25	1.263	V
			$V_{CCQ} = 2.7V$	1.337	1.35	1.364	V
$Z_{IN}$	$V_{REF}$ Reference Pin Input Impedance	Note 2	$V_{CCQ} = 0$		100		k $\Omega$
				Switching Frequency		650	
$\Delta V_{OFFSET}$	Offset Voltage $V_{TT} - V_{REF_{OUT}}$	$AV_{CC} = 2.5V$ No Load	$V_{CCQ} = 2.5$	-20		20	mV
<b>Supply</b>							
$I_Q$	Quiescent Current	$I_{OUT} = 0$ , no load $V_{CCQ} = 2.5V$	$I_{VCCQ}$		6	10	$\mu A$
			$I_{AVCC}$		0.5	1.0	mA
			$I_{AVCC SD}$		0.2	0.5	mA
			$I_{VDD}$		0.25	1.0	mA
			$I_{VDD SD}$		0.2	1.0	mA
			$I_{PVDD}$		100	250	$\mu A$
<b>Buffer</b>							
$I_{REF}$	Output Current Capability			3			mA

### Notes

- Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
- $AV_{CC}$ ,  $PV_{DD} = 3.3V \pm 10\%$

## Functional Description

The FAN6555 integrates two power MOSFETs that can be used to source and sink 2A of current while maintaining a tight voltage regulation. Using the external feedback, the output can be regulated well within 3% or less, depending on the external components chosen. Separate voltage supply inputs have been added to accommodate applications with various power supplies for the databus and power buses.

### Outputs

The output voltage pins ( $V_{L1}$ ,  $V_{L2}$ ) are tied to the databus, address, or clock lines via an external inductor. See the Applications section for recommendations. Output voltage is determined by the  $V_{CCQ}$  or  $VREF_{IN}$  inputs.

### Inputs

The input voltage pins ( $V_{CCQ}$  or  $VREF_{IN}$ ) determine the output voltages ( $V_{L1}$  or  $V_{L2}$ ). In the default mode, where the  $VREF_{IN}$  pin is floating, the output voltage is 50% of the  $V_{CCQ}$  input.  $V_{CCQ}$  can be the reference voltage for the databus.

Output voltage can also be selected by forcing a voltage at the  $VREF_{IN}$  pin. In this case, the output voltage follows the voltage at the  $VREF_{IN}$  input. Simple voltage dividers can be used in this case to produce a wide variety of output voltages between 0.7V and  $V_{DD}-0.7V$ .

### VREF Input and Output

The  $VREF_{IN}$  input can be used to force a voltage at the outputs (Inputs section, above). The  $VREF_{OUT}$  pin is an output pin that is driven by a small output buffer to provide the  $VREF$  signal to other devices in the system. The output buffer is capable of driving several output loads. The output buffer can handle 3mA.

### Other Supply Voltages

Several inputs are provide for the supply voltages:  $PV_{DD1}$ ,  $PV_{DD2}$ ,  $AV_{CC}$ , and  $V_{DD}$ .

The  $PV_{DD1}$  and  $PV_{DD2}$  provide the power supply to the power MOSFETs.  $V_{DD}$  provides the voltage supply to the digital sections, while  $AV_{CC}$  supplies the voltage for the analog sections. Again, see the Applications section for recommendations.

### Feedback Input

The  $V_{FB}$  pin is an input that can be used for closed loop compensation. This input is derived from the voltage output. See Application section for recommendation.

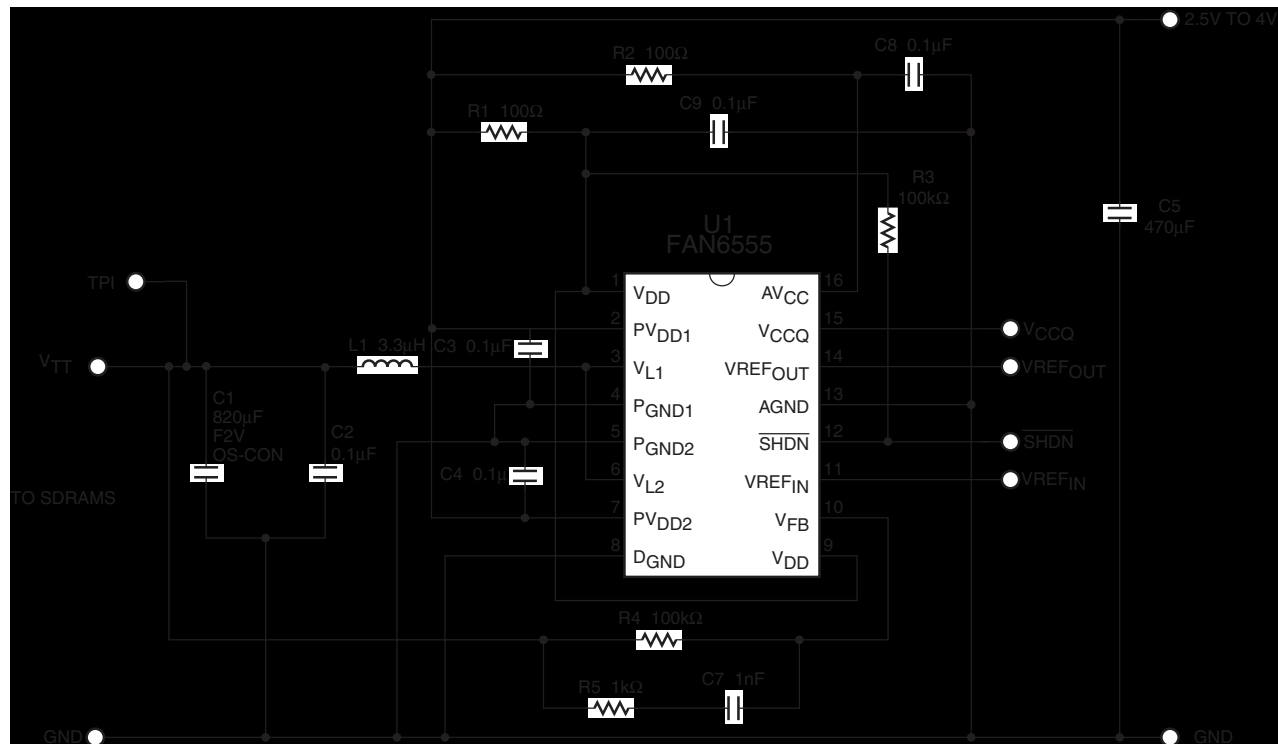


Figure 1.

## Applications

### Using the FAN6555 for DDR Bus Termination

The circuit schematic in Figure 1 shows a recommended approach for constructing a bus terminating solution for a DDR bus. This circuit can be used in PC memory and Graphics memory applications as shown in Figures 3 and 4. Note that the FAN6555 can provide the voltage reference ( $V_{REF}$ ) and terminating voltages ( $V_{TT}$ ). Using the layout as shown in Figures 5, 6, and 7, and measuring the  $V_{TT}$  performance using the test setup as described in Figure 8, the FAN6555 delivered a  $V_{TT} \pm 20mV$  for 1A to 2A loads (see Figure 9). Table 1 provides a recommended parts list.

An alternate application circuit for the FAN6555 is shown in Figure 2. The number of external components is reduced

compared to the circuit in Figure 1. This is achieved by replacing four, 0.1 $\mu F$  bypass capacitors with one, low ESR, 10 $\mu F$  ceramic capacitor placed right next to U1. Two 100 $\Omega$  resistors are also eliminated. High value, surface-mount MLC capacitors were not available when the original application circuit (Figure 1) was developed. Both application circuits offer the same electrical performance but the circuit shown in Figure 2 has a reduced bill-of-materials. Table 2 shows the recommended parts list for the circuit of Figure 2.

### Bus Termination Solutions for Others Buses

Table 3 provides a summary of various bus termination  $V_{REF}$  &  $V_{TT}$  requirements. The FAN6555 can be used for those applications.

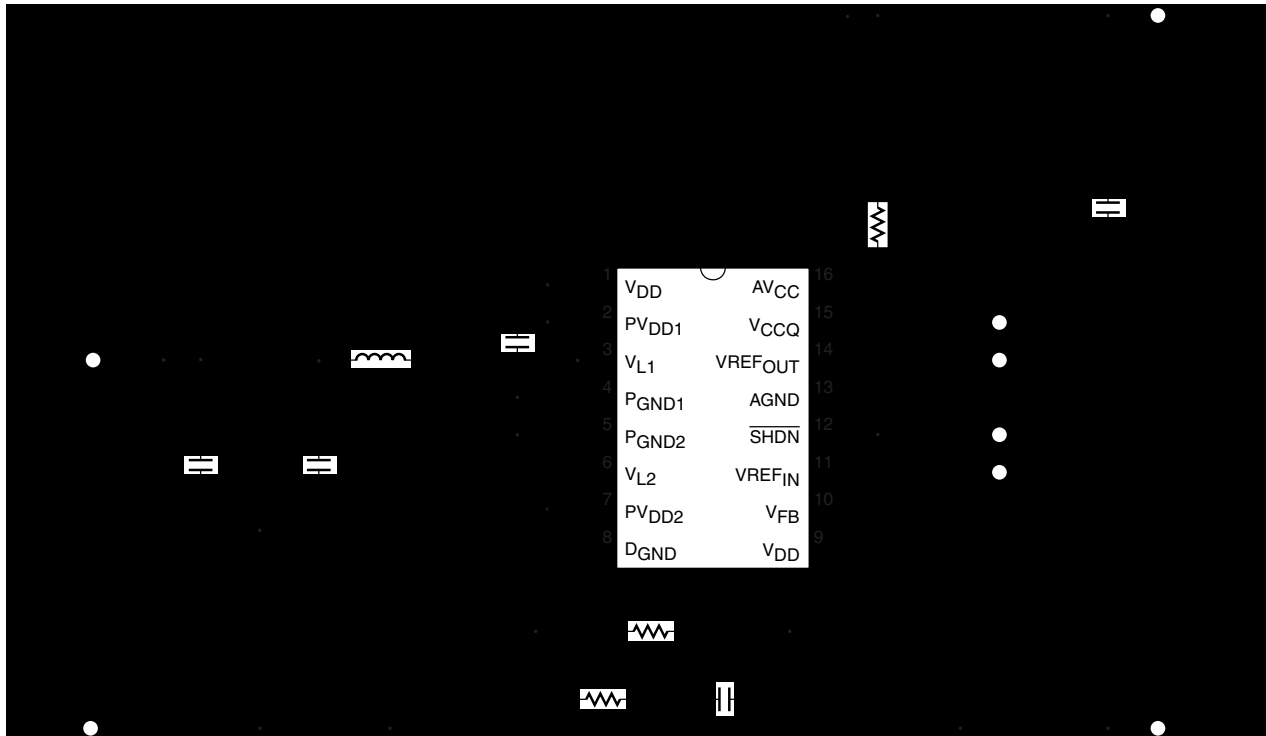


Figure 2. Alternate Application Circuit

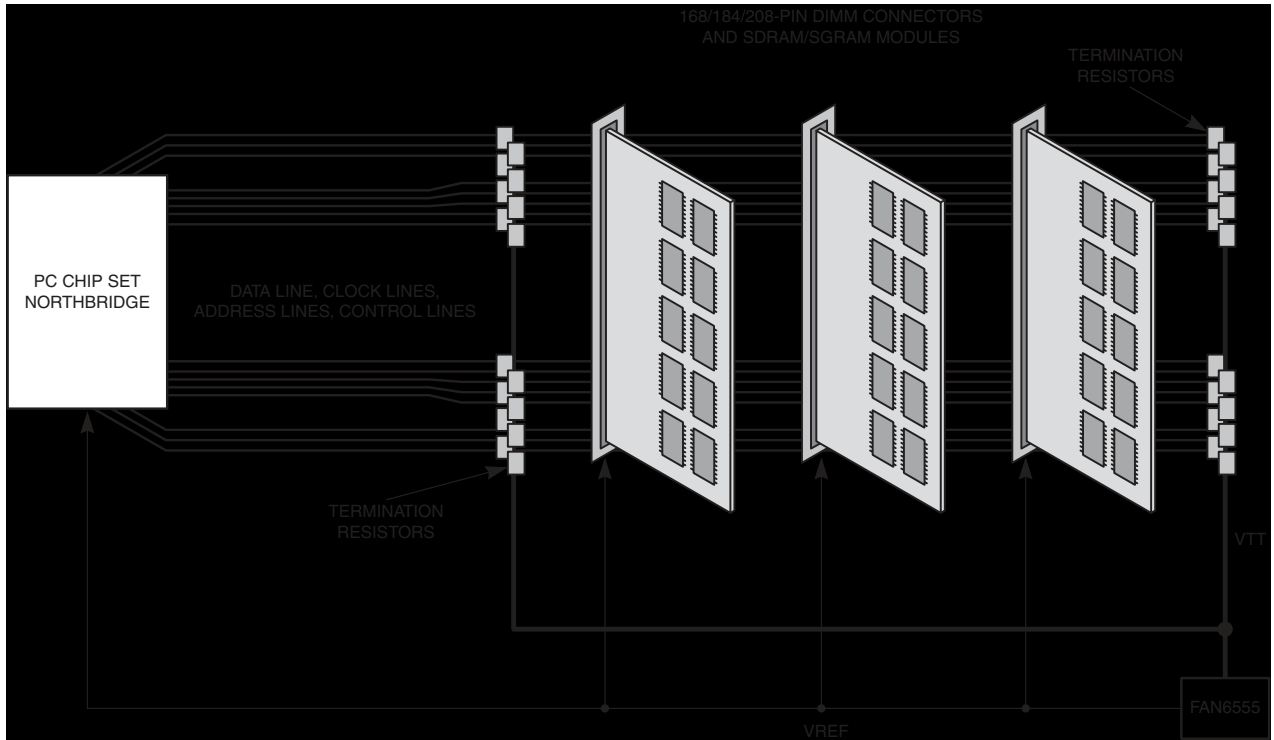


Figure 3. Complete Termination Solution PC Main Memory (PC Motherboard)

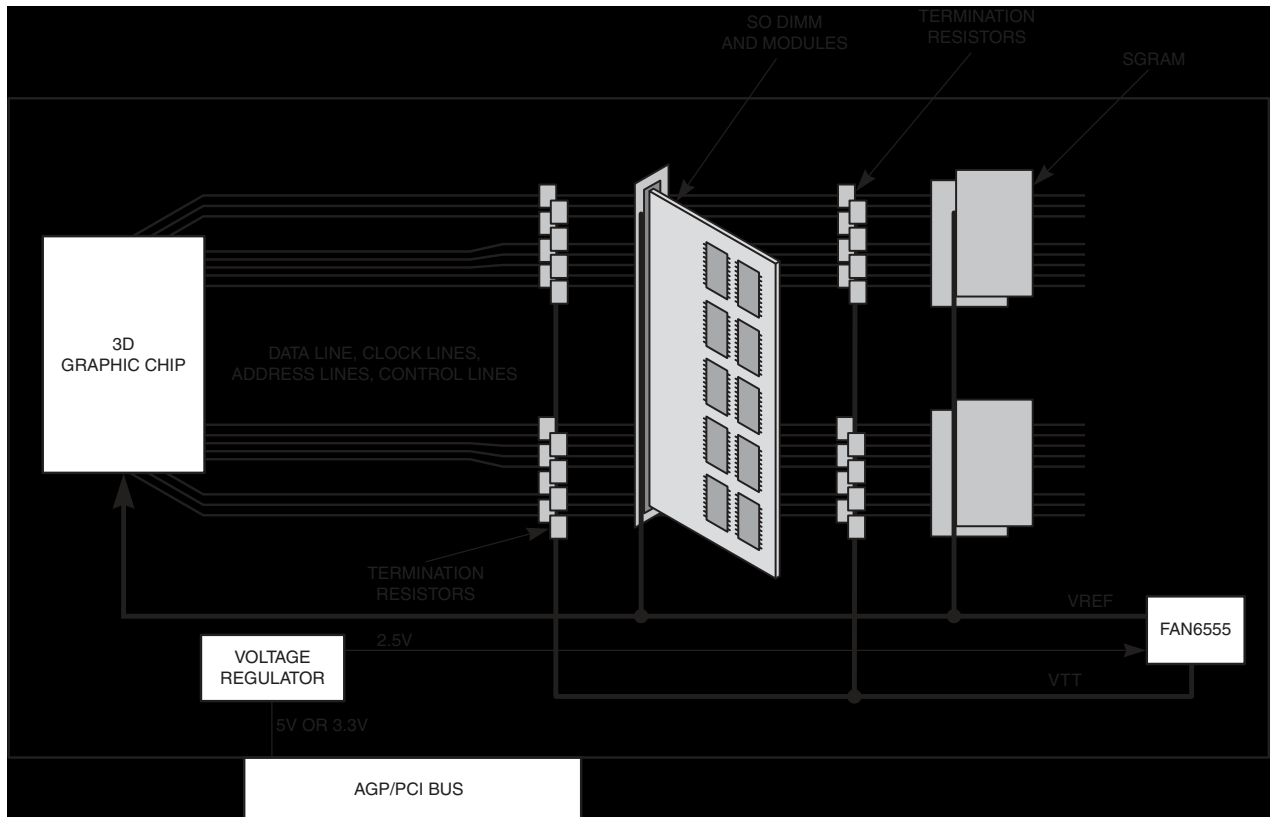


Figure 4. Complete Termination Solution Graphics Memory Bus – AGP Graphics Cards

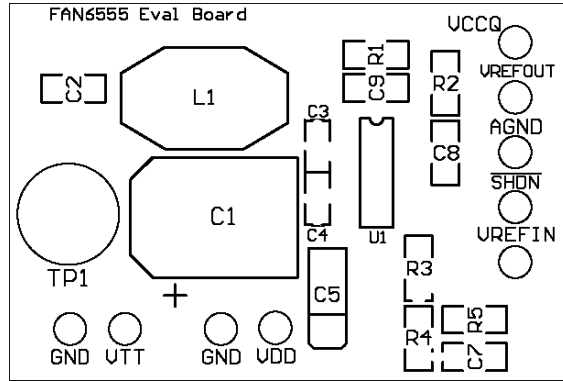


Figure 5. Top Silk

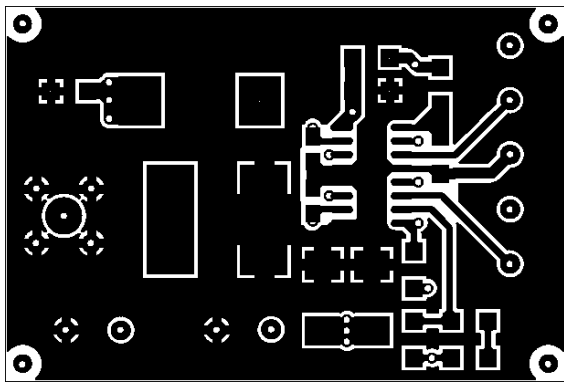


Figure 6. Top Layer

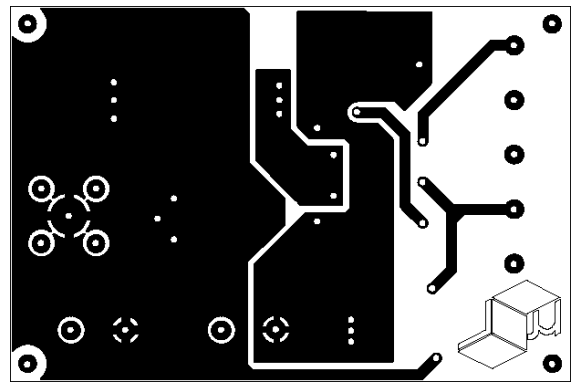
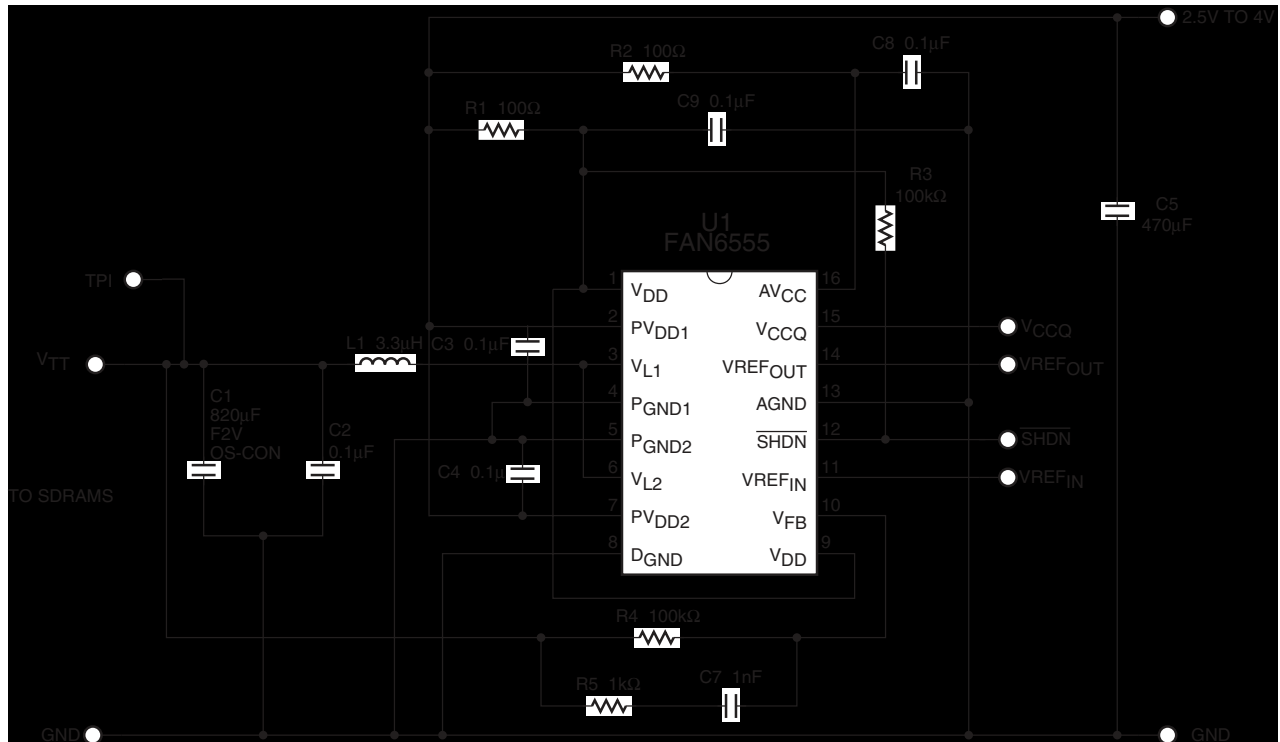


Figure 7. Bottom Layer



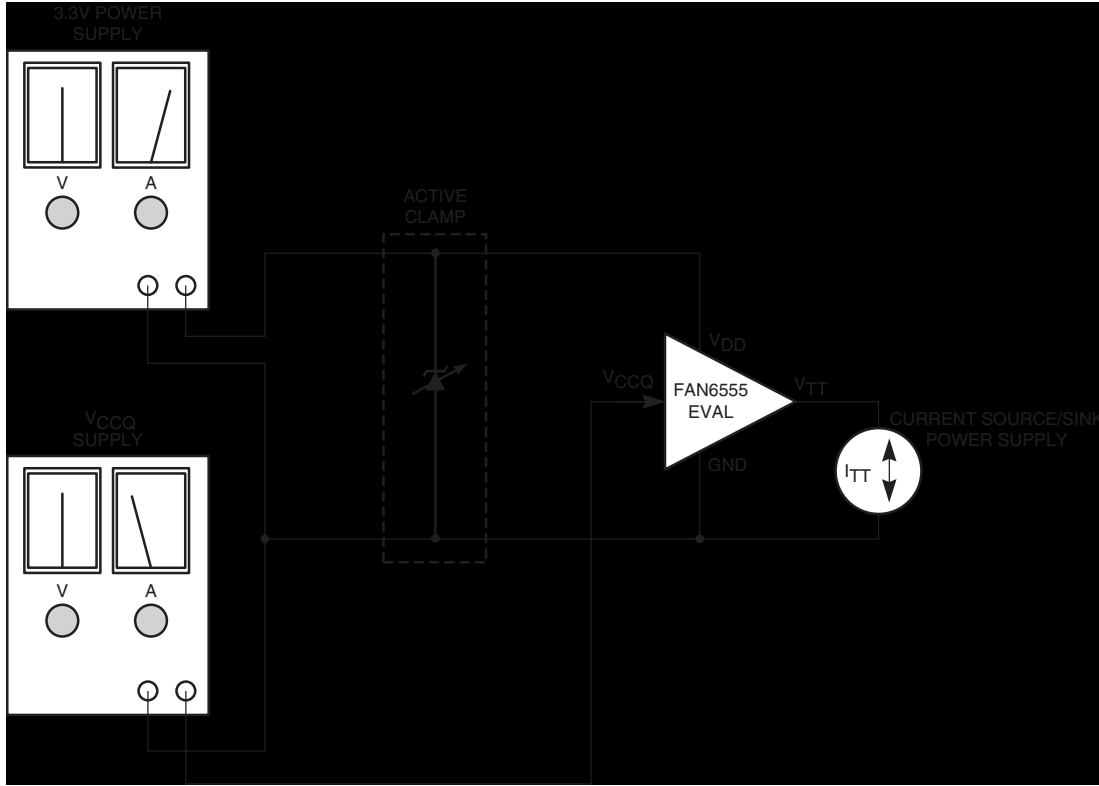


Figure 8. Test Circuit Setup

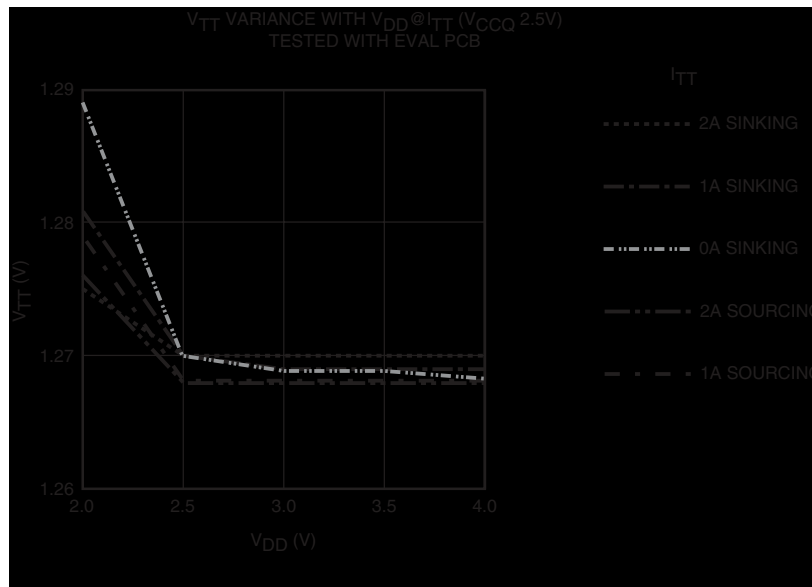


Figure 9. VTT Performance for DDR Bus



Table 1. Recommend Parts List for Figure 1.

Item	Qty	Description	Manufacturer / Part Number	Designator
<b>Resistors</b>				
1	2	100Ω1210 SMD	Panasonic/ERJ-8ENF1000V	R1, R2
2	1	1kΩ 1210 SMD	Panasonic/ERJ-8ENF1001V	R5
3	2	100kΩ1210 SMD	Panasonic/ERJ-8ENF1003V	R3, R4
<b>Capacitors</b>				
4	3	0.1μF 1210 Film SMD	Panasonic/ECV3VB1E104K Panasonic/ECU-V1H104KBW	C2, C8, C9
5	1	820μF 2V Solid Elect. SMD	Sanyo/2SV820M Os Con	C1
6	1	470μF 6.3V Solid Elect. SMD	Sanyo/6SVP470M Os Con	C5
7	1	1nF 1210 Film SMD	Panasonic/ECU-V1H102KBM	C7
8	2	0.1μF 0805 Film	Panasonic/ECJ-2VF1C104Z	C3, C4
<b>ICs</b>				
9	1	FAN6555 Bus Terminator	FAN6555M	U1
<b>Magnetics</b>				
10	1	3.3μH 5A inductor SMD	Coilcraft/D03316P-332HC Pulse Eng./ P0751.332T Gowanda/SMP3316-331M XFMRs inc./XF0046-S4	L1
<b>Other</b>				
11	1	Scope probe socket	Tektronics/131-4353-00	TP1
12	1	12 Pin breakaway strip	Sullins/PTC36SAAN (36 PINS)	I/O, standoffs

Table 2. Recommend Parts List for Figure 2.

Item	Qty	Description	Manufacturer / Part Number	Designator
<b>Resistors</b>				
1	2	100kΩ 0805 SMD	Panasonic/ERJ-8ENF1000V	R1, R3
2	1	1kΩ 0805 SMD	Panasonic/ERJ-8ENF1000V	R2
<b>Capacitors</b>				
3	1	0.1μF, 1210 Film SMD	Panasonic/ECV3VB1E104K Panasonic/ECU-V1H104KBW	C2
4	1	820μF 2V Solid Elect. SMD	Sanyo/2SV820M Os Con	C1
5	1	470μF 6.3V Solid Elect. SMD	Sanyo/6SVP470M Os Con	C5
6	1	1nF 1210 Film SMD	Panasonic/ECU-V1H102KBM	C4
7	1	10μF 6.3V Ceramic	TDK/C2012X5R0J106M	C3
<b>ICS</b>				
8	1	FAN6555 Bus Terminator	FAN6555M	U1
<b>Magnetics</b>				
9	1	3.3μH 5A inductor SMD	Coilcraft/D03316P-332HC Pulse Eng./ P0751.332T Gowanda/SMP3316-331M XFMRs inc./XF0046-S4	L1
<b>Other</b>				
10	1	Scope probe socket	Tektronics/131-4353-00	TP1
11	1	12 Pin breakaway strip	Sullins/PTC36SAAN (36 PINS)	I/O, standoffs

**Vendor List**

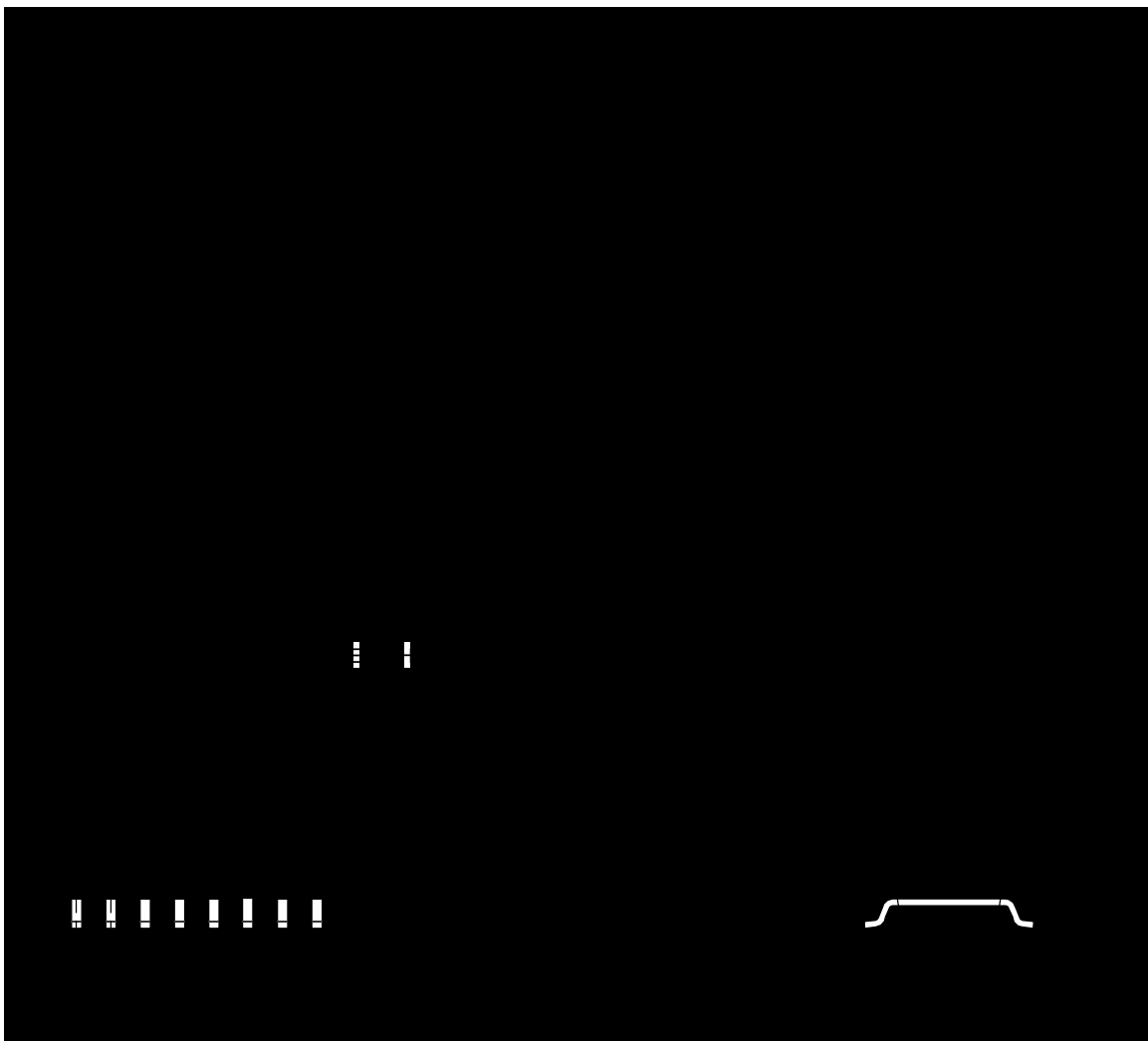
1. AVX (207) 282-5111
2. Sanyo (619) 661-6835
3. Tektronix (408) 496-0800
4. Coilcraft (847) 639-6400
5. Pulse (800) 797-8573
6. Gowanda (716) 532-2234
7. Xfmrs Inc. (317) 834-1066
8. Panasonic (714) 373-7366
9. Digikey (800) 344-4539

**Table 3. Termination Solutions Summary By Bus Type**

Bus	Description	Driving Method	VDDQ	VTT	V <sub>REF</sub>	Fairchild Solutions	Industry System Components
GTL+	Gunning Transceiver Bus Plus	Open Drain	3.3V	1.5V±10%	1.0V±2%	FAN6555; Mode: V <sub>REF</sub> Input = 1.5V, V <sub>CC</sub> = 3.3V	300 to 500MHz Processor; PC Chipsets; GTL+ 16xxx Buffers; Fairchild, Texas Instr.
DDR (SSTL-2)	Series Stub Terminated Logic for 2V	Symmetric Drive, Series Resistance	2.5V±10%	0.5x (V <sub>DDQ</sub> ) ±3%	2.5V	FAN6555, ML6554CU, or ML6553CS; Mode: V <sub>REF</sub> Input = Floating or Forced, V <sub>CC</sub> = 3.3V	DDR SDRAM; Hitachi, Fujitsu, NEC, Micro, Mitsubishi
RAMBUS	RAMBUS Signaling Logic	Open Drain	None Specified	2.5V	2.0V	ML6553CS; Mode: V <sub>REF</sub> Input = Open, V <sub>CC</sub> = V <sub>DDQ</sub>	nDRAM, RAMBUS, Intel, Toshiba
LV-TTL	Low Voltage TTL Logic or PECL or 3.3V VME	Symmetric Drive	3.3±10%	V <sub>DDQ</sub> /2	3.3V	ML6553CS; Mode: V <sub>REF</sub> Input = Open, V <sub>CC</sub> = V <sub>DDQ</sub>	Processors or backplanes; LV-TTL SDRAM, EDO RAM

# Mechanical Dimensions Inches (Millimeters)

Package: M16 16-Pin SOIC



## Ordering Information

Part Number	Temperature Range	Package
FAN6555M	-40°C to +85°C	16-Pin SOIC (M16)
FAN6555MX	-40°C to +85°C	16-Pin SOIC in tape-and-reel

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