

### Features

- Frequency range : 25MHz to 312.5MHz
- SMD seam sealing ceramic package
- Supply voltage : 2.5V, 3.3V
- LVDS output
- Low phase noise and phase jitter
- Tri-state function available
- External dimensions (mm)  
L : 7.0 x W : 5.0 x H : 1.4
- RoHS compliant & Pb free

### Applications

- Networking, Telecommunication, Data communication, Switch, Server, Storage
- Fibre channel, Ethernet, SONET, SATA, SAS, PCI-Express
- Optical module
- Microprocessor, DSP, FPGA, Clock source for ADC and DAC
- Test and measurement

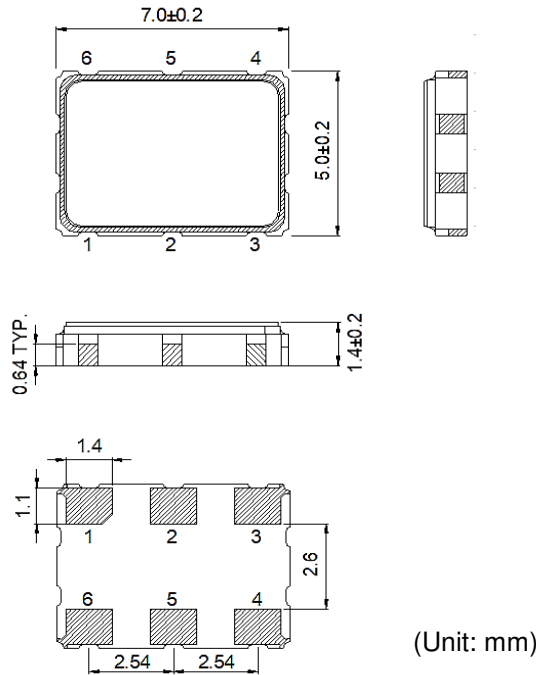
### Electrical Characteristics

Item	QTM750D	Conditions
Frequency Range ( $F_0$ )	25MHz ~ 312.5MHz	
Frequency Stability ( $F_{stab}$ ) over Operating Temperature Range ( $T_{OTR}$ )	$\pm 50$ ppm, $\pm 25$ ppm	-40°C ~ +85°C, Note [1]
	$\pm 50$ ppm	-40°C ~ +105°C, Note [1]
Operating Temperature Range ( $T_{OTR}$ )	-40°C ~ +85°C	
	-40°C ~ +105°C	
Supply Voltage ( $V_{DD}$ )	2.5V, 3.3V	$V_{DD} \pm 10\%$
Current Consumption ( $I_{DD}$ )	50 mA Max.	
Output Type	LVDS	
Output Load	100 $\Omega$	
Output Voltage High ( $V_{OH}$ )	1.43V Typ. / 1.6V Max.	
Output Voltage Low ( $V_{OL}$ )	0.9V Min. / 1.1V Typ.	
Offset Voltage	1.125V Min. / 1.25V Typ. / 1.375V Max.	
Differential Output Voltage	247mV Min. / 330mV Typ. / 454mV Max.	
Rise & Fall Time ( $T_r / T_f$ )	0.6 ns Max.	20%~80% of output swing
Duty Cycle	45% ~ 55%	
Start-up Time	5 ms Max.	
Enable Voltage High, Logic "1"	70% VDD Min.	Input to OE pin Note [2]
Enable Voltage Low, Logic "0"	30% VDD Max.	
Phase Jitter	$F_0 = 156.25$ MHz	12kHz ~ 20MHz, RMS
	$F_0 = 312.5$ MHz	
Aging ( $F_{aging}$ )	$\pm 3$ ppm Max.	at 25°C $\pm$ 3°C, first year
Storage Temperature Range ( $T_{STR}$ )	-55°C ~ +125°C	

**Notes:**

- [1] Inclusive of frequency tolerance at 25°C, variations over temperature, supply voltage and vibration.
- [2] Output will be enabled if OE is Logic "1" or Open; Output will be disabled if OE is Logic "0".
- [3] The standard testing environment except temperature test is 25°C±5°C, 40%~70% relative humidity.

**Dimensions**

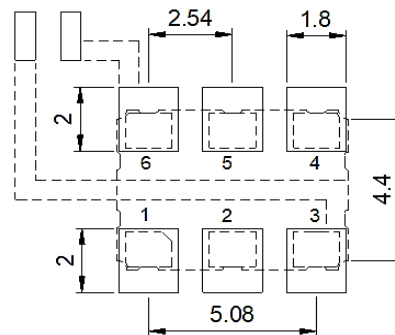


\* Pad dimension tolerance is ±0.2mm

**Pin function**

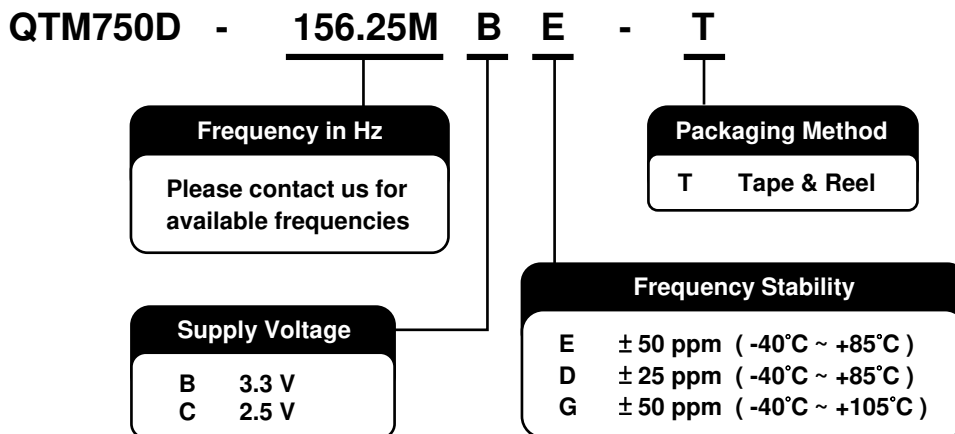
Pin 1	OE
Pin 2	NC
Pin 3	GND
Pin 4	OUT
Pin 5	$\overline{\text{OUT}}$
Pin 6	V <sub>DD</sub>

**Recommended pad layout**

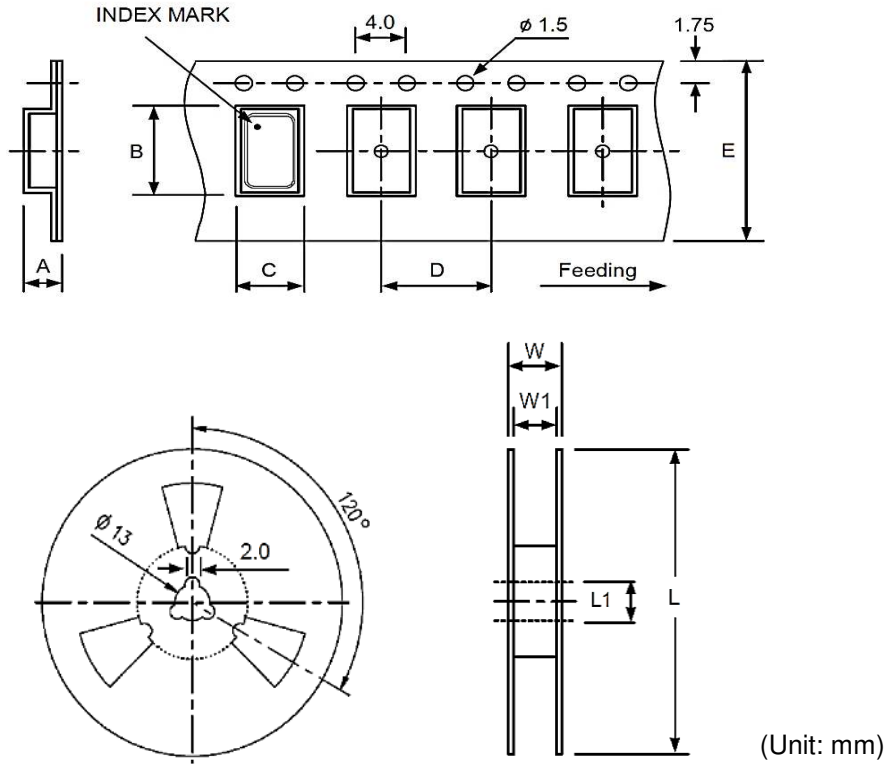


\* Power supply decoupling capacitor is required.

**Ordering Information**



### Packing



DIMENSIONS	A	B	C	D	E	L	L1	W	W1
	2.00	7.90	5.45	8.00	16.0	180.0	13.0	20.5	16.0

### Reflow Profile

Solder melting point : 220°C ± 10°C, 60 sec. Min., 200 sec. Max.  
 Peak temperature : 260°C ± 10°C, 10 sec. Min., 30 sec. Max.

