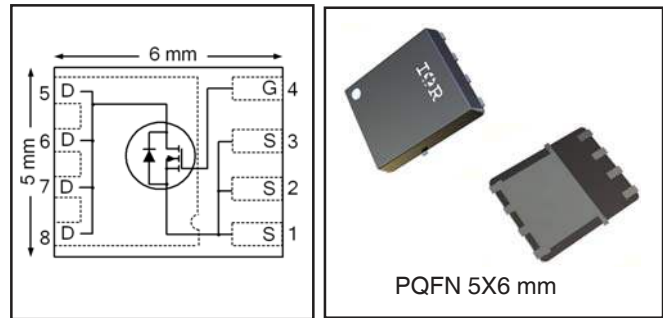


V_{DS}	30	V
$V_{GS\ max}$	± 20	V
$R_{DS(on)\ max}$ (@ $V_{GS} = 10V$)	2.1	mΩ
(@ $V_{GS} = 4.5V$)	3.2	
$Q_g\ typ.$	30	nC
I_D (@ $T_{c(Bottom)} = 25^\circ C$)	80 ⑦	A

HEXFET® Power MOSFET



Applications

- Synchronous MOSFET for high frequency buck converters

Features and Benefits

Features

Low Thermal Resistance to PCB (< 1.3°C/W)
Low Profile (<1.2mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in
 ⇒

Benefits

Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable part number	Note
		Form	Quantity		
IRFH8311TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH8311TRPBF	
IRFH8311TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	IRFH8311TR2PBF	EOL notice #259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	32	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	26	
$I_D @ T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	169⑥ ⑦	
$I_D @ T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	107⑥ ⑦	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	80⑦	
I_{DM}	Pulsed Drain Current ①	400	W
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	3.6	
$P_D @ T_{c(Bottom)} = 25^\circ C$	Power Dissipation ⑤	96	
	Linear Derating Factor ⑤	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑦ are on page 9

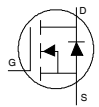
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.021	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	1.70	2.10	mΩ	V _{GS} = 10V, I _D = 20A ③
		—	2.60	3.20		V _{GS} = 4.5V, I _D = 16A ③
V _{GS(th)}	Gate Threshold Voltage	1.35	1.8	2.35	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.6	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	83	—	—	S	V _{DS} = 10V, I _D = 20A
Q _g	Total Gate Charge	—	66	—	nC	V _{GS} = 10V, V _{DS} = 15V, I _D = 20A
Q _g	Total Gate Charge	—	30	—	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 20A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	9.7	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	3.9	—		
Q _{gd}	Gate-to-Drain Charge	—	8.6	—		
Q _{godr}	Gate Charge Overdrive	—	7.8	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	12.5	—		
Q _{oss}	Output Charge	—	21	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	0.6	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	21	—	ns	V _{DD} = 15V, V _{GS} = 4.5V I _D = 20A R _G = 1.8Ω
t _r	Rise Time	—	26	—		
t _{d(off)}	Turn-Off Delay Time	—	21	—		
t _f	Fall Time	—	12	—		
C _{iss}	Input Capacitance	—	4960	—	pF	V _{GS} = 0V V _{DS} = 10V f = 1.0MHz
C _{oss}	Output Capacitance	—	1065	—		
C _{rss}	Reverse Transfer Capacitance	—	455	—		

Avalanche Characteristics

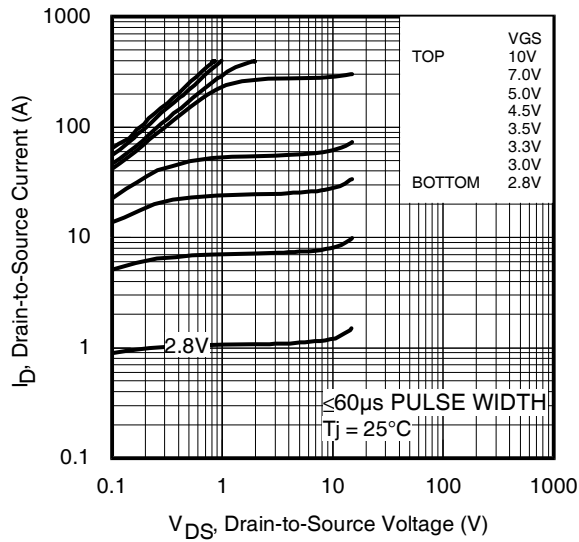
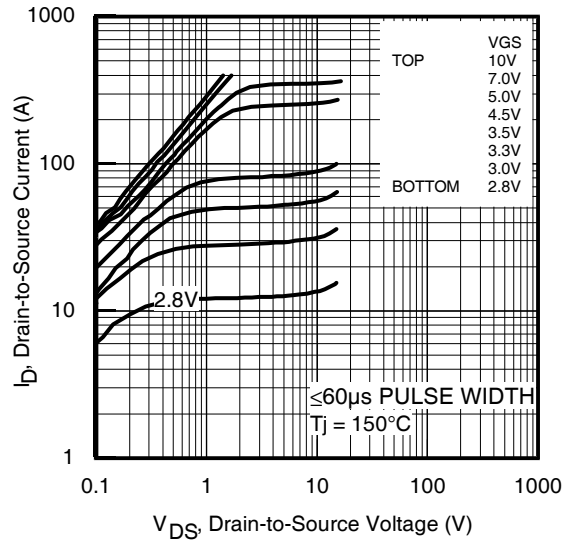
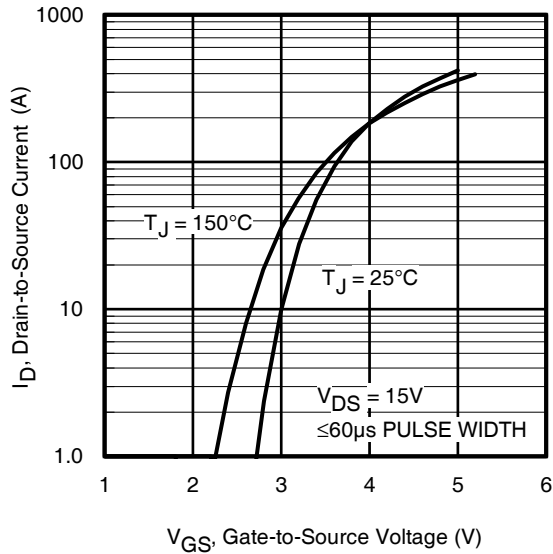
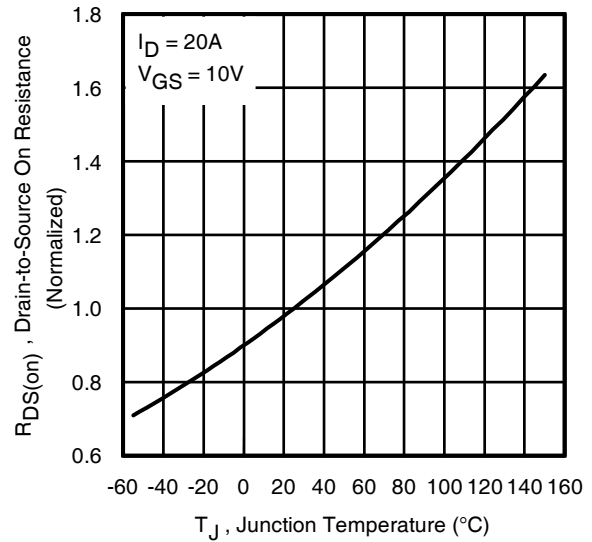
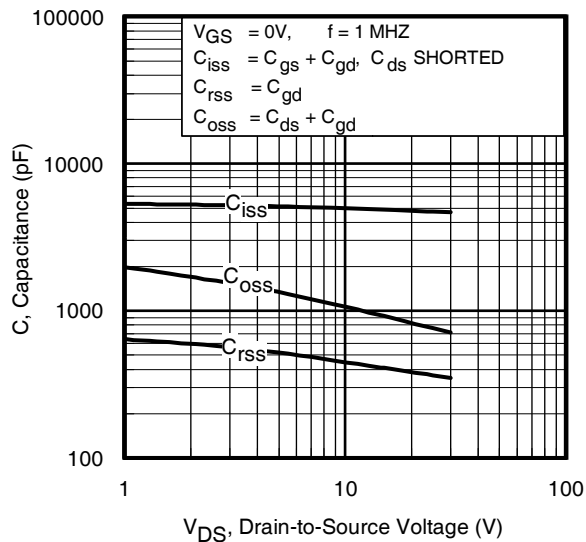
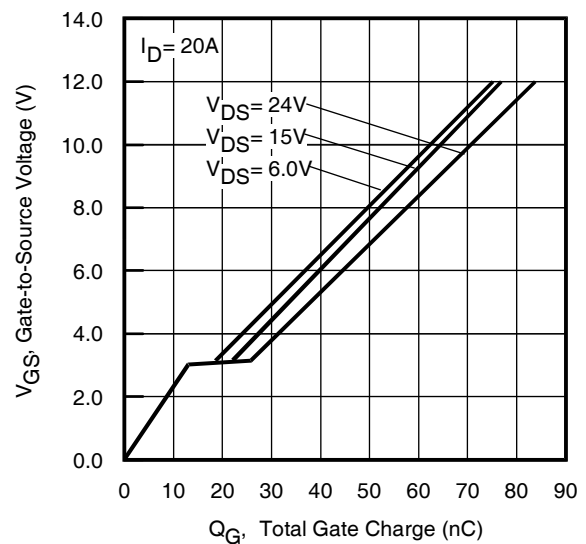
	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	326	mJ
I _{AR}	Avalanche Current ①	—	20	A

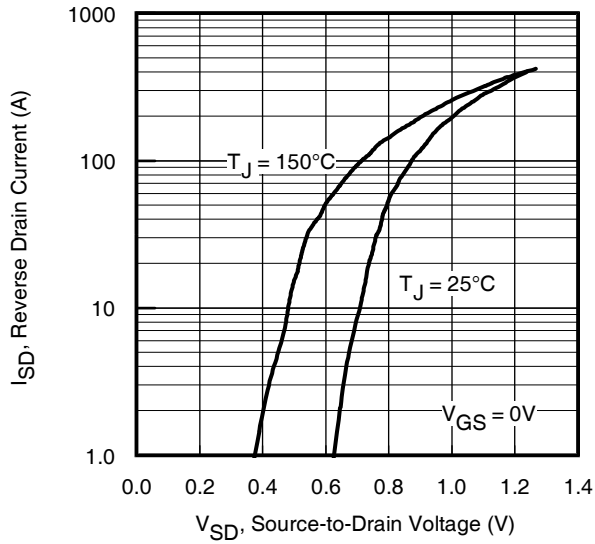
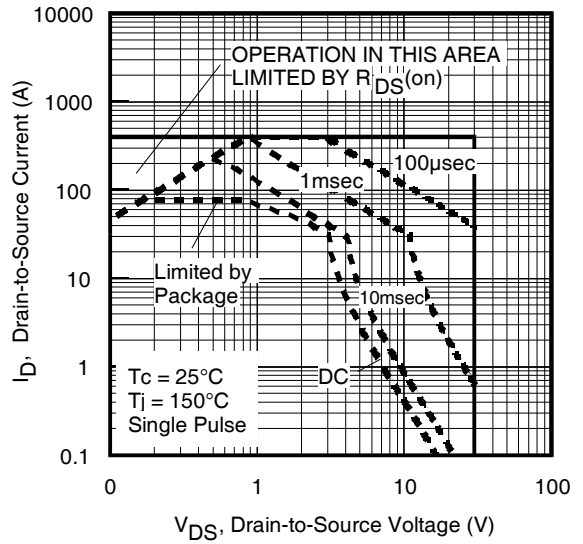
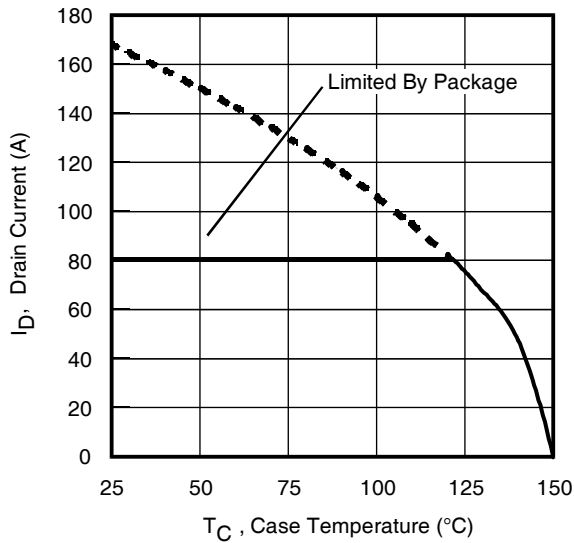
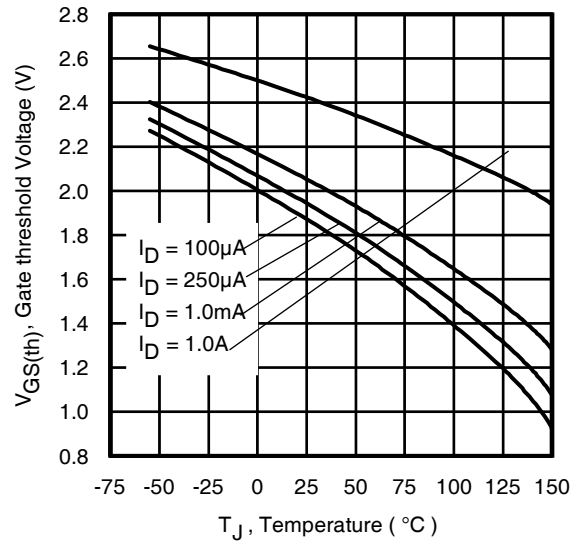
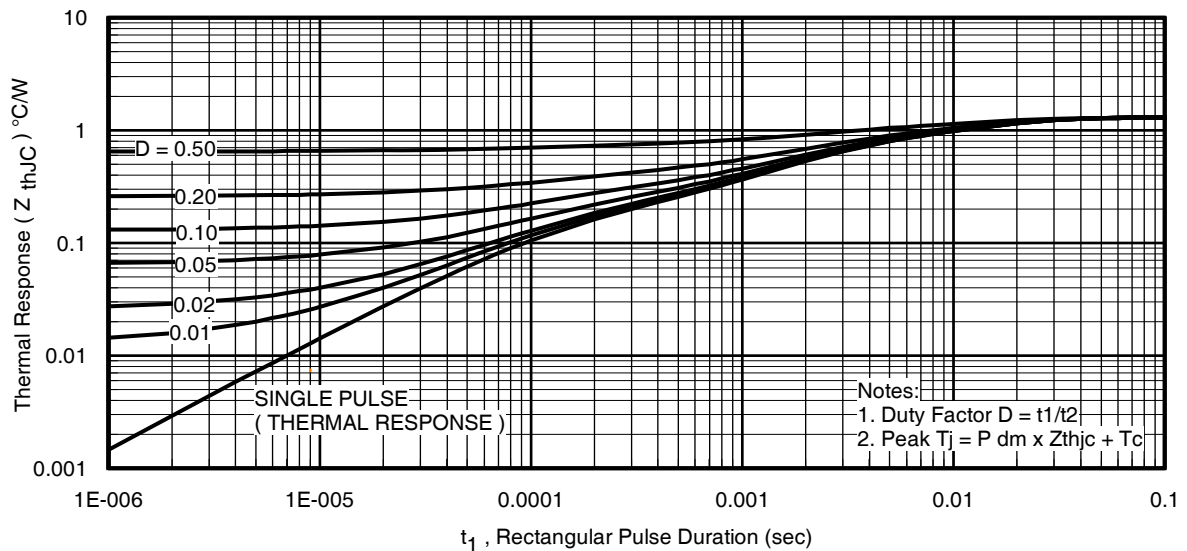
Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	80 ②	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	22	33	ns	T _J = 25°C, I _F = 20A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	47	71	nC	di/dt = 390 A/μs ③
t _{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ④	—	1.3	°C/W
R _{θJC} (Top)	Junction-to-Case ④	—	30	
R _{θJA}	Junction-to-Ambient ⑤	—	35	
R _{θJA} (<10s)	Junction-to-Ambient ⑤	—	0.99	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

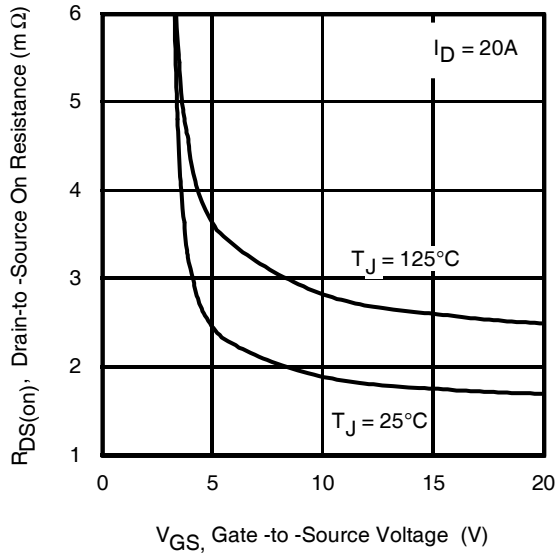


Fig 12. On-Resistance vs. Gate Voltage

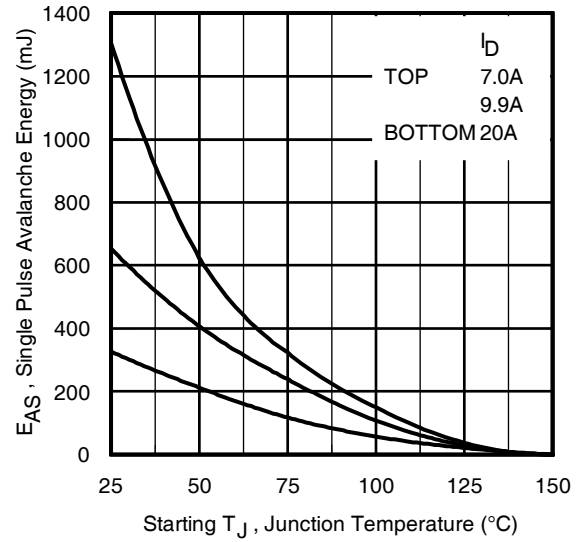


Fig 13. Maximum Avalanche Energy vs. Drain Current

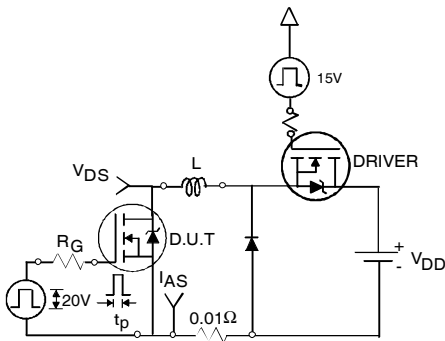


Fig 14a. Unclamped Inductive Test Circuit

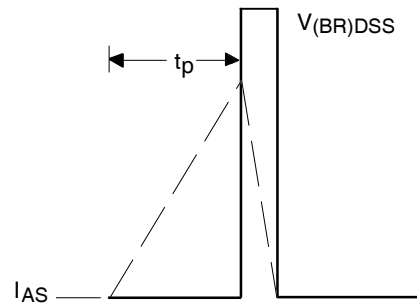


Fig 14b. Unclamped Inductive Waveforms

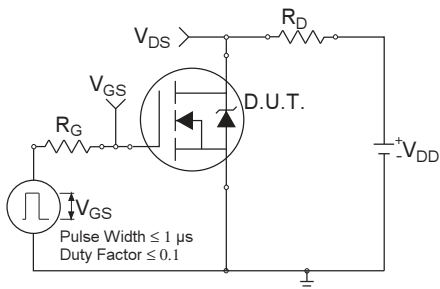


Fig 15a. Switching Time Test Circuit

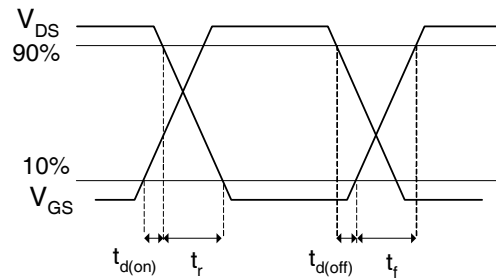


Fig 15b. Switching Time Waveforms

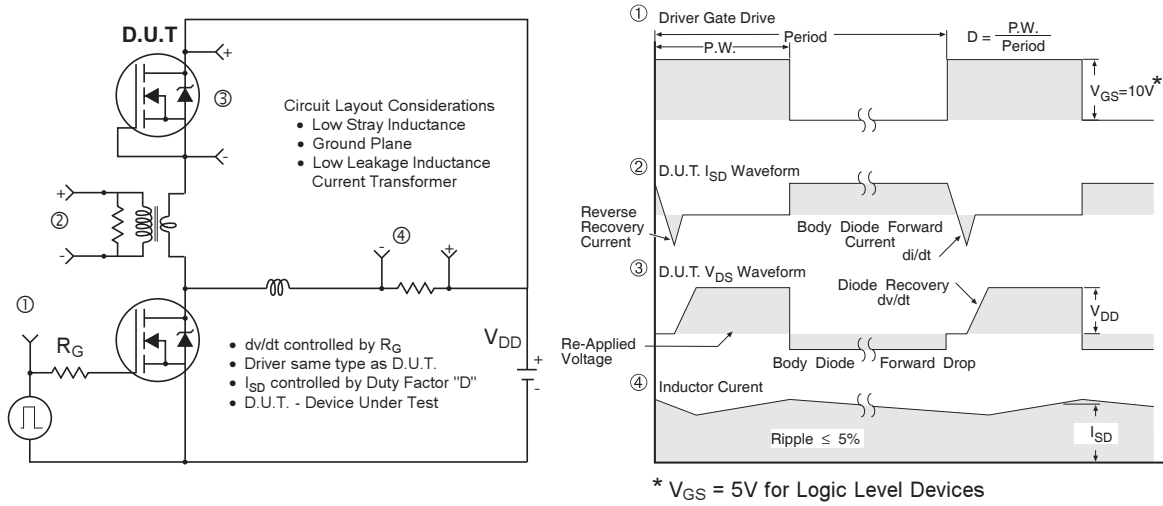


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

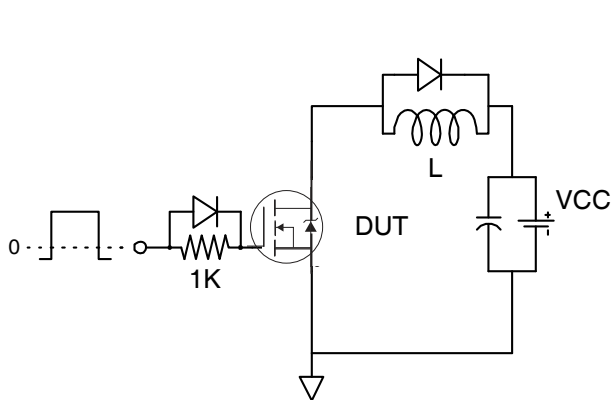


Fig 17. Gate Charge Test Circuit

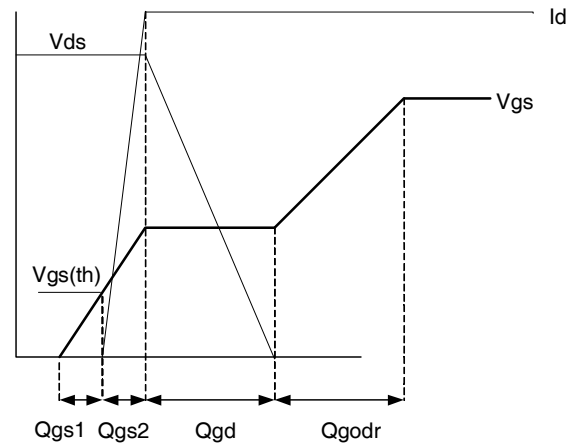
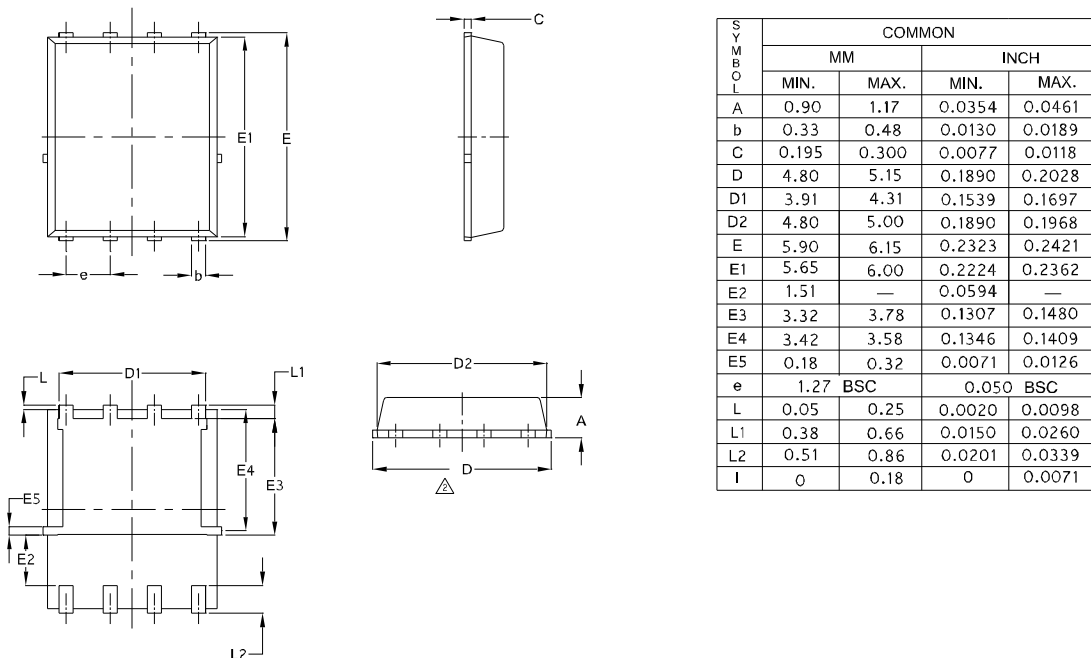
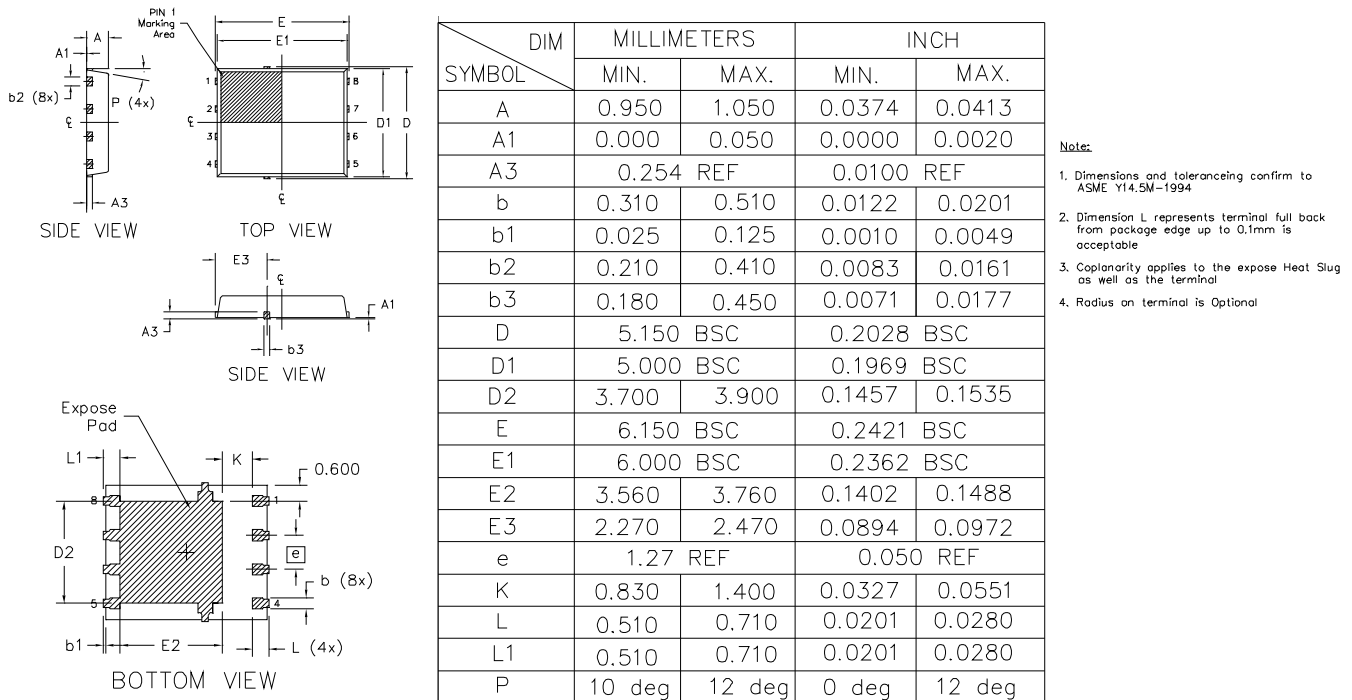


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "E" Package Details



PQFN 5x6 Outline "G" Package Details



For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

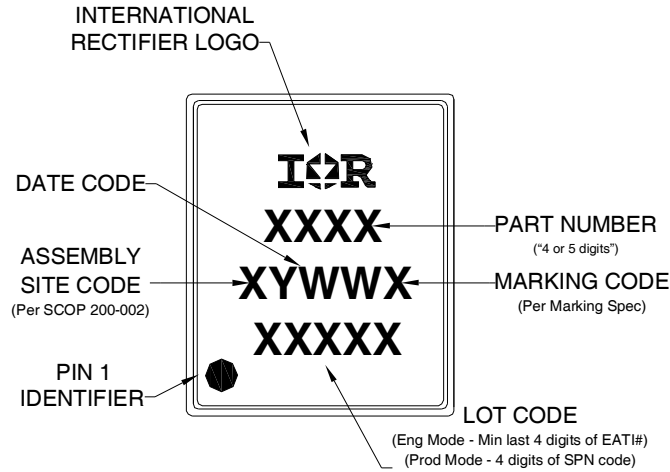
<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

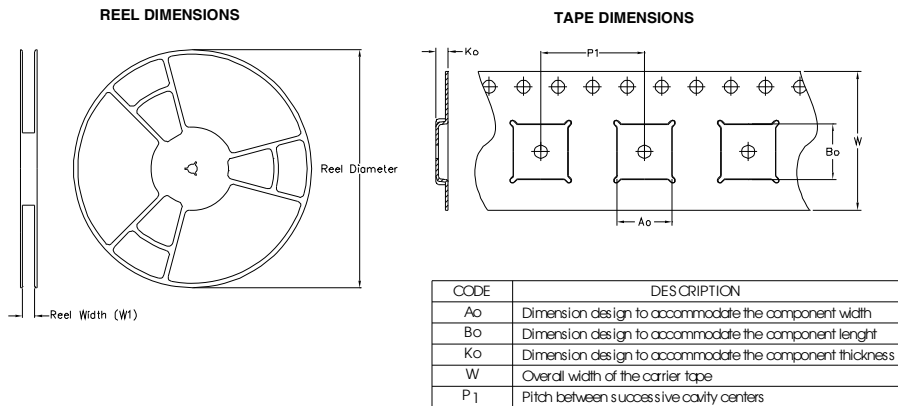
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Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

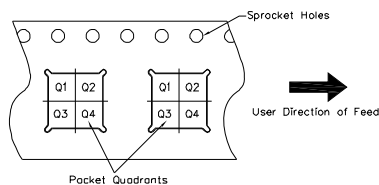
PQFN 5x6 Part Marking



PQFN 5x6 Tape and Reel



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.
 Please contact your International Rectifier sales representative for further information:
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.63\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 80A by source bonding technology.

Revision History

Date	Comment
3/26/2010	• Idss limits at $T_J 25^\circ\text{C}$ is changed to 500 μA max and at $T_J 125^\circ\text{C}$ it is changed to 5.0mA max. All other parameters remain unchanged.
1/7/2014	• Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259). • Updated data sheet with the new IR corporate template.
6/2/2015	• Updated package outline for “option E” and added package outline for “option G” on page 7. • Updated “IFX” logo on page 1 & 9. • Updated tape and reel on page 8.

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