TPS650002-Q1 2.25-MHz Step-Down Converter With Dual LDOs

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 2: –40°C to +105°C, T_A
- Step-down converters:
  - V_{IN} range from 2.3 V to 6 V
  - 2.25-MHz Fixed-frequency operation
  - 600-mA Output current
- LDOs:
  - V_{IN} Range From 1.6 V to 6 V
  - Up to 300-mA output current
  - Separate power inputs and enables
- 3-mm × 3-mm 16-Pin WQFN

2 Applications

- Automotive camera module
- Automotive infotainment
- Automotive cluster
- Automotive sensor fusion

3 Description

The TPS650002-Q1 device is a single-chip power-management IC (PMIC) for automotive applications. This device combines a single step-down converter with two low-dropout regulators. The step-down converter enters a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications, the device can be forced into fixed-frequency PWM using the MODE pin. The step-down converter allows the use of a small inductor and capacitors to achieve a small solution size. A power-good status output can be used for sequencing. The LDOs can supply 300 mA, and can operate with an input voltage range from 1.6 V to 6 V, thus allowing them to be supplied from the step-down converter. The step-down converter and the LDOs have separate voltage inputs and enables, thus allowing for design and sequencing flexibility.

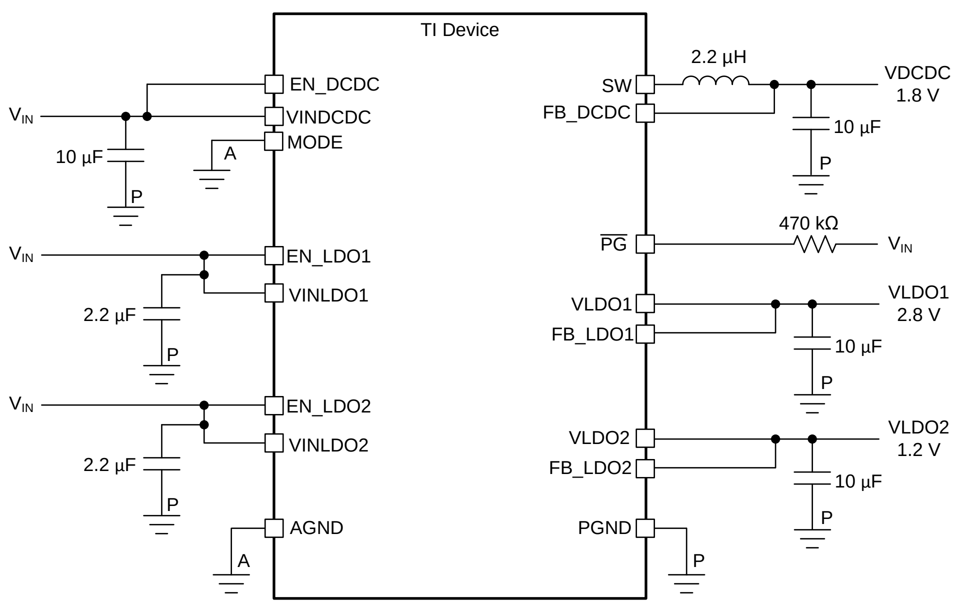
The TPS650002-Q1 device is available in a 16-pin leadless package (3-mm × 3-mm WQFN).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS650002-Q1	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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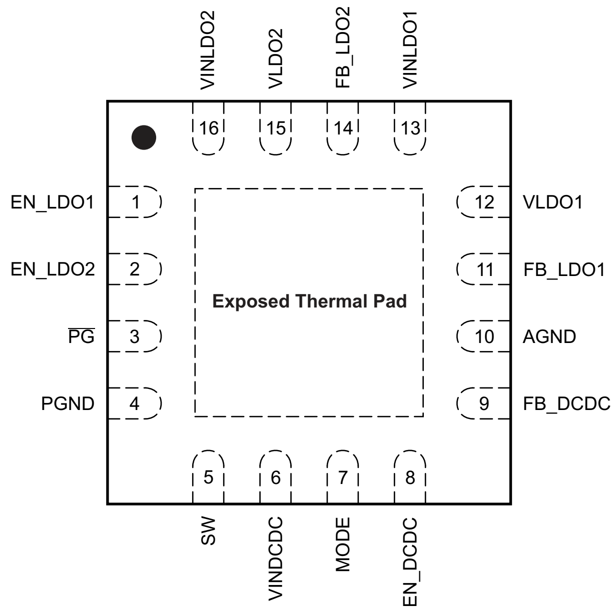
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2019	*	Initial release.

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	10	—	Analog ground – Star back to PGND as close to the IC as possible
EN_DCDC	8	I	Enable DC-DC converter
EN_LDO1	1	I	Enable LDO1
EN_LDO2	2	I	Enable LDO2
FB_DCDC	9	I	Voltage to DC-DC error amplifier
FB_LDO1	11	I	Voltage to LDO1 error amplifier
FB_LDO2	14	I	Voltage to LDO2 error amplifier
MODE	7	I	Selects forced-PWM or PWM-to-PFM automatic-transition mode
$\overline{PG}$	3	O	Open-drain active-low power-good output
PGND	4	—	Power ground – connected to the thermal pad
SW	5	O	Switch pin – connect inductor here
VINDCDC	6	I	Input voltage to DC-DC converter and all other control blocks
VINLDO1	13	I	Input voltage to LDO1
VINLDO2	16	I	Input voltage to LDO2
VLDO1	12	O	LDO1 output voltage
VLDO2	15	O	LDO2 output voltage
EP		—	Exposed thermal pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	On all pins except AGND, PGND, EN_DCDC, FB_LDO1, FB_LDO2, pins with respect to AGND	–0.3	7	V
	On EN_DCDC with respect to AGND	–0.3	V_{IN} + 0.3, ≤ 7	
	FB_LDO1, FB_LDO2	-0.3	3.6	
Output voltage	On VLDO1, VLDO2,	–0.3	3.6	V
Output voltage	/PG	-0.3	7	V
Output voltage	SW	-0.6	7	V
Output voltage	SW for 20ns transients	-2	10	V
Current	VINDCDC, SW, PGND,		1800	mA
	VINLDO1, VINLDO2, VLDO1, VLDO1, AGND		800	mA
	At all other pins		1	mA
Operating free-air temperature, T_A		–40	105	°C
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VINDCDC		2.3		6.0	V
VINLDO1, VINLDO2		1.6		VINDCDC	V
MODE		0		VINDCDC	V
EN_DCDC , EN_LDO1, EN_LDO2		0		VINDCDC	V
L1	SW pin inductor	1.5	2.2	3.3	µH
C_I	Input capacitor at VINDCDC	10			µF
	Input capacitor at VINLDO1, VINLDO2	2.2			µF
C_O	Output capacitor for VDCDC	10		22	µF
	Output capacitor for LDO1, LDO2	2.2			µF
I_O	DC-DC converter output current			600	mA
	LDO1 output current			300	mA
	LDO2 output current			300	mA
T_A	Operating ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS650002-Q1s RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
V_{IN}	Input voltage for VINDCDC of DC-DC converter		2.3		6	V
	Input voltage for LDO1 (VINLDO1)	See [(1)]	1.6		6	V
	Input voltage for LDO2 (VINLDO2)	See [(1)]	1.6		6	V
	Internal undervoltage (UVLO) lockout threshold	V_{CC} falling	1.72	1.77	1.82	V
	Internal undervoltage (UVLO) lockout hysteresis			160		mV
SUPPLY CURRENT						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1, EN_LDO2 low, I_{OUT} = 0 mA and no switching		23	32	µA
		MODE low, EN_DCDC low, EN_LDO1, EN_LDO2 high, I_{OUT} = 0 mA I_{OUT} = 0 mA and no switching		50	57	µA
		EN_DCDC high, MODE high, EN_LDO1, EN_LDO2 low, I_{OUT} = 0 mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		0.16	2.2	µA
DIGITAL PINS (EN_DCDC, EN_LDO1, EN_LDO2, MODE, $\overline{PG}$						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	$\overline{PG}$ pins only, I_O = –100 µA			0.4	V
I_{lkg}	Input leakage current	MODE, EN_DCDC, EN_LDO1, EN_LDO2 tied to GND or VINDCDC,		0.01	0.1	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		2.01	2.25	2.41	MHz
STEP-DOWN CONVERTER POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET ON-resistance	VINDCDC = V_{GS} = 3.6 V		240	480	mΩ
	Low-side MOSFET ON-resistance	VINDCDC = V_{GS} = 3.6 V		185	380	mΩ
I_O	DC output current	2.3 V ≤ VINDCDC ≤ 2.5 V			300	mA
		2.5 V ≤ VINDCDC ≤ 6 V			600	mA
I_{LIMF}	Forward current limit, PMOS and NMOS	2.3 V ≤ VINDCDC ≤ 6 V	800	1000	1400	mA

(1) The design principle allows only VINDCDC to be the highest supply in the system. If separate input voltage supplies are used for the DC-DC converter and LDOs, then choose VINDCDC ≥ VINLDO1 and VINDCDC ≥ VINLDO2.

Electrical Characteristics (continued)

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STEP-DOWN CONVERTER POWER SWITCH (continued)						
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		30		°C
STEP-DOWN CONVERTER OUTPUT VOLTAGE						
VDCDC	Fixed output voltage, VDCDC			1.825		V
VDCDC	Output-voltage DC accuracy (PWM mode)(2)	MODE = high, 2.3 ≤ VINDCDC ≤ 6 V	-1.5%		+1.5%	
	Output-voltage DC accuracy (PFM mode)	MODE low +1% voltage positioning active		1%		
	Load regulation (PWM mode)	MODE high		0.5		%/A
R_{DIS}	Internal discharge resistance at SW	EN_DCDC low		450		Ω
LOW-DROPOUT REGULATORS						
V_I	Input voltage for LDOx (VINLDOx)		1.6		6	V
V_{LDO1}	Fixed output voltage, LDO1 (VLDO1)(3)			2.8		V
V_{LDO2}	Fixed output voltage, LDO2 (VLDO2)(3)			1.2		V
I_O	Continuous-pass FET current				300	mA
I_{SC}	Short-circuit current limit	2.3 V ≤ VINLDOx	340		825	mA
		VINLDOx < 2.3 V	210		825	
V_{DO}	Dropout voltage (4)	VINLDOx ≥ 2.3 V, I_{OUT} = 250 mA			370	mV
		VINLDOx < 2.3 V, I_{OUT} = 175 mA			370	mV
	Output voltage accuracy	I_O = 1 mA to 300 mA, VINLDOx = 2.3 V–6 V, VLDOx = 1.2 V	–3.5%		3.5%	
		I_O = 1 mA to 175 mA, VINLDOx = 1.6 V–6 V, VLDOx = 1.2 V	–3.5%		3.5%	
	Load regulation	I_O = 1 mA to 300 mA, VINLDOx = 3.6 V VLDOx = 1.2 V	–1.5%		1.5%	
	Line regulation	VINLDOx = 1.6 V–6 V, VLDOx = 1.2 V at I_O = 1 mA	–0.5%		0.5%	
PSRR	Power-supply rejection ratio	f_{NOISE} ≤ 10 kHz, C_{OUT} ≥ 2.2 µF, V_{IN} = 2.3 V, V_{OUT} = 1.3 V, I_{OUT} = 10 mA		40		dB
R_{DIS}	Internal discharge resistance at VLDOx	EN_LDOx low		450		Ω
T_{SD}	Thermal shutdown	Increasing temperature		150		°C
	Thermal shutdown hysteresis	Decreasing temperature		30		°C

(2) For VINDCDC = VDCDC + 1 V
(3) Maximum output voltage VLDOx = 3.6 V.
(4) V_{DO} = VINLDOx – VLDOx, where VINLDOx = VLDOx(nom) – 100 mV

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STEP-DOWN CONVERTER OUTPUT VOLTAGE						
t_{Start}	Start-up time	EN_DCDC to start of switching (10%)		250		µs
t_{Ramp}	VDCDC ramp-up time	VDCDC ramp from 10% to 90%		250		µs
LOW-DROPOUT REGULATORS						
t_{RAMP}	VLDOx ramp time	VLDOx ramp from 10% to 90%		200		µs

6.7 Typical Characteristics

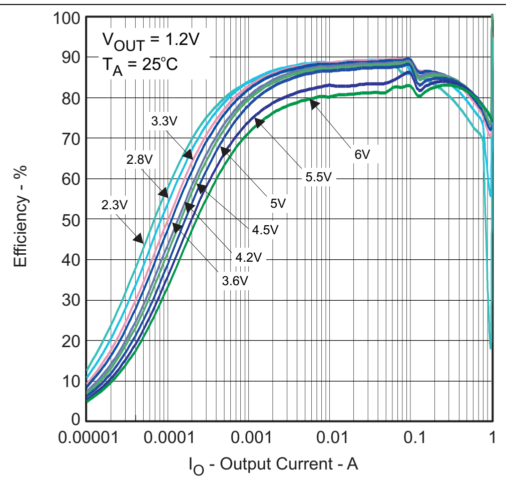


Figure 1. Efficiency (DC-DC 600-mA PFM Mode) vs Output Current

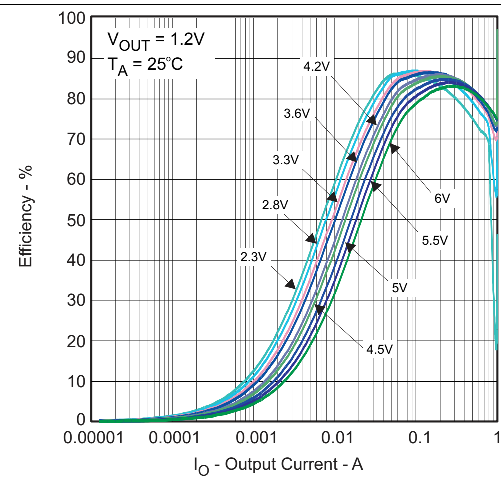


Figure 2. Efficiency (DC-DC 600-mA PWM Mode) vs Output Current

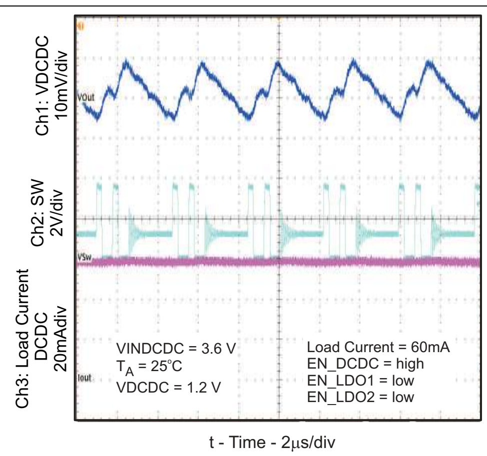


Figure 3. Output Voltage Ripple (DC-DC PFM Mode)

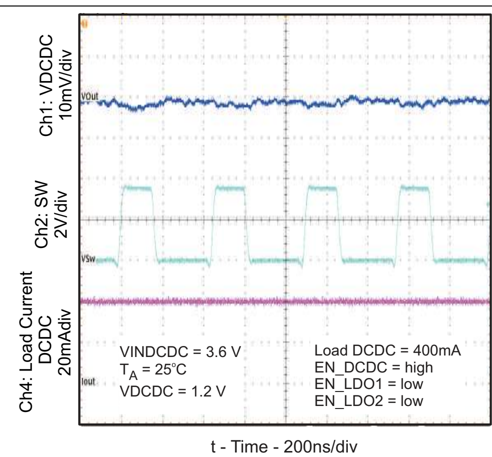


Figure 4. Output Voltage Ripple (DC-DC PWM Mode)

Typical Characteristics (continued)

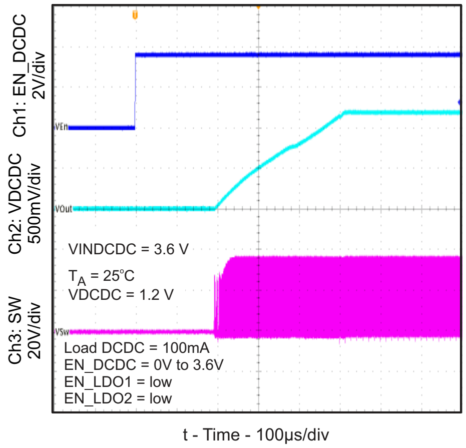


Figure 5. Start-Up Timing (DC-DC)

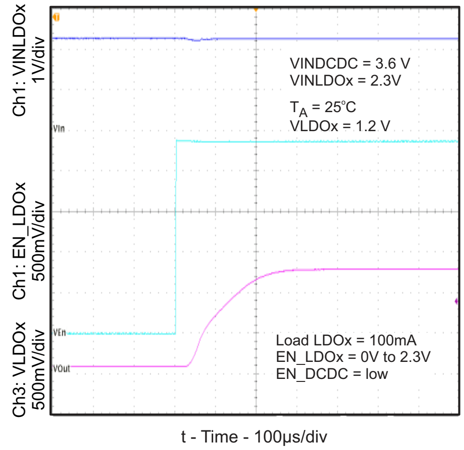


Figure 6. Start-Up Timing (LDOx)

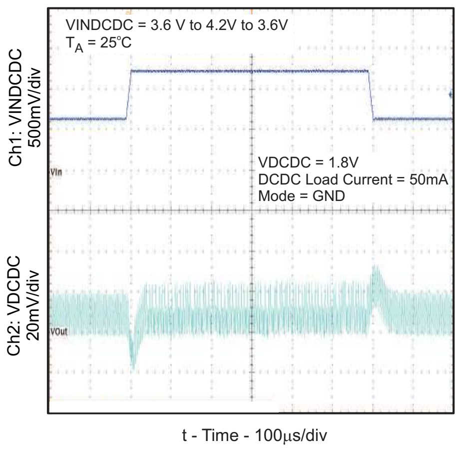


Figure 7. Line Transient Response (DC-DC PFM Mode)

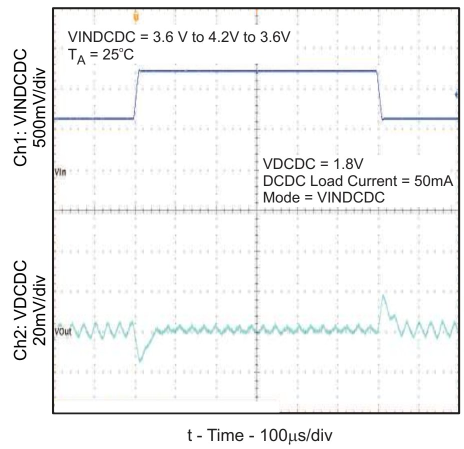


Figure 8. Line Transient Response (DC-DC PWM Mode)

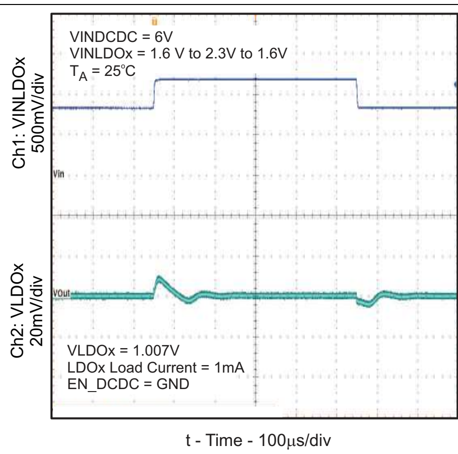


Figure 9. Line Transient Response (LDOx)

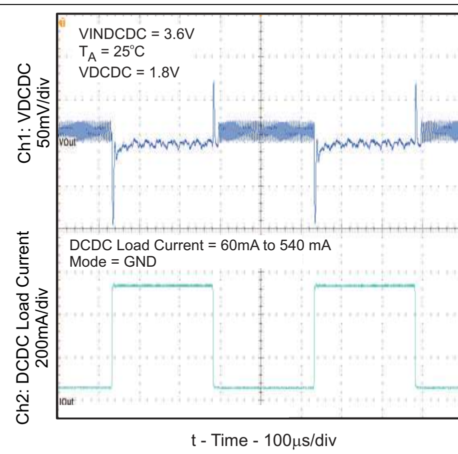


Figure 10. Load Transient Response (DC-DC PFM Mode)

Typical Characteristics (continued)

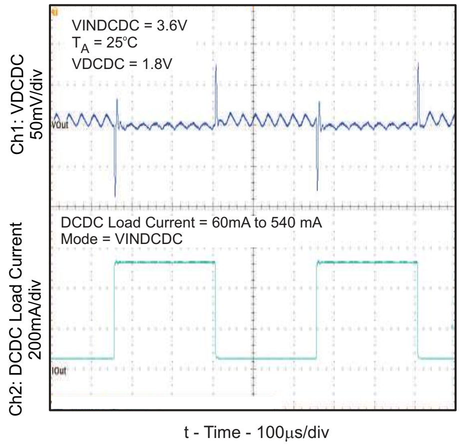


Figure 11. Load Transient Response (DC-DC PWM Mode)

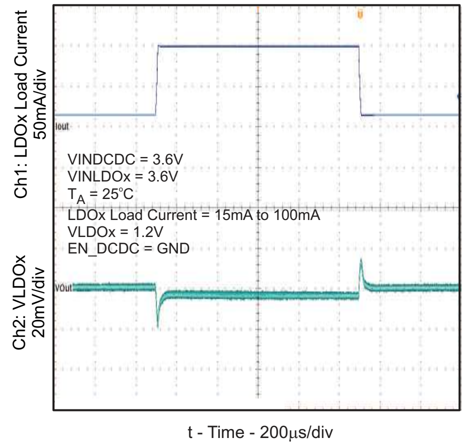


Figure 12. Load Transient Response (LDOx)

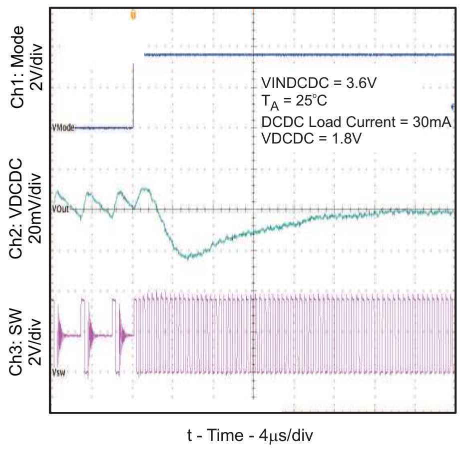


Figure 13. PFM to PWM Transition (DC-DC)

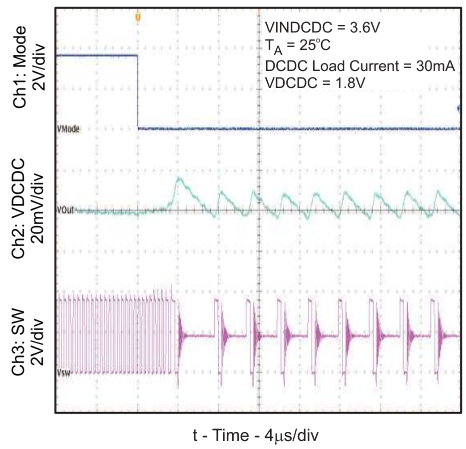


Figure 14. PWM to PFM Transition (DC-DC)

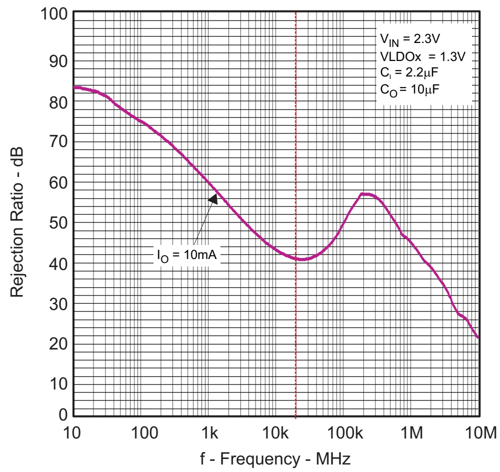


Figure 15. Power-Supply Rejection Ratio (LDOx) vs Frequency

7 Detailed Description

7.1 Overview

The TPS650002-Q1 device has one step-down converter, and two low dropout regulators. The device has an input voltage range of 2.3 V to 6 V. This device is intended for (but not limited to) powering automotive camera modules.

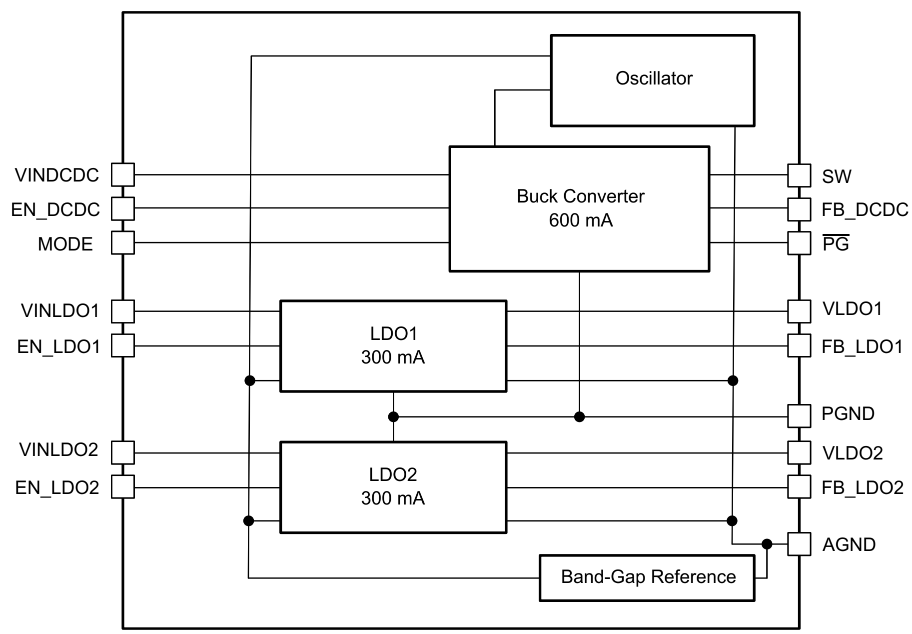
To maximize efficiency, there are two modes of operation based on load conditions: PWM or PFM. By pulling the MODE pin high, forced PWM can be achieved. Pulling this pin low results in an automatic adjustment between PFM and PWM modes.

The two general-purpose low-dropout regulators each have their own separate enables and voltage inputs. The inputs can be tied to the output of the step-down converter or to a separate voltage source.

The switching frequency of the step-down converter is handled by the oscillator, with a typical frequency of 2.25 MHz.

The TPS650002-Q1 device also provides a power good signal to monitor the condition of the DC-DC and both LDOs. The DC-DC and LDOs are only monitored if their enable signal is high. If all enabled resources are in regulation, the pin is pulled low. If one or more of the enabled resources are out of regulation, the pin is placed in Hi-Z.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Step-Down Converter

The step-down converter is intended to allow maximum flexibility in the end equipment. Figure 16 shows the necessary connections.

Feature Description (continued)

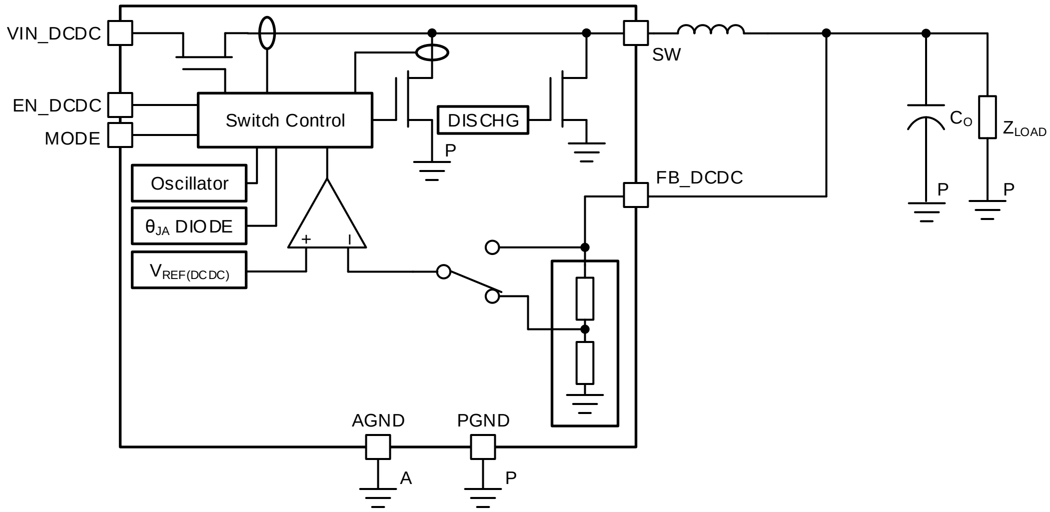


Figure 16. DC-DC Converter Block Diagram

Externally adjustable output voltages and additional current-limit options are also possible. Contact TI for further information.

The step-down converter has two modes of operation to maximize efficiency at different load conditions. At moderate to heavy load currents, the device operates in a fixed-frequency pulse-width modulation (PWM) mode that results in small output ripple and high efficiency. Pulling the MODE pin to a DC-high level results in PWM mode over the entire load range.

At light load currents, the device operates in a pulsed frequency-modulation (PFM) mode to improve efficiency. The transition to this mode occurs when the inductor current through the low-side FET becomes zero, indicating discontinuous conduction. PFM mode also results in the output voltage increasing by 1% from the PWM mode value. This voltage positioning is intended to minimize both the voltage undershoot of a load step from light to heavy loads, as when a processor moves from sleep to active modes, and the voltage overshoot at load removal. shows the voltage positioning behavior for a light-to-heavy load step.

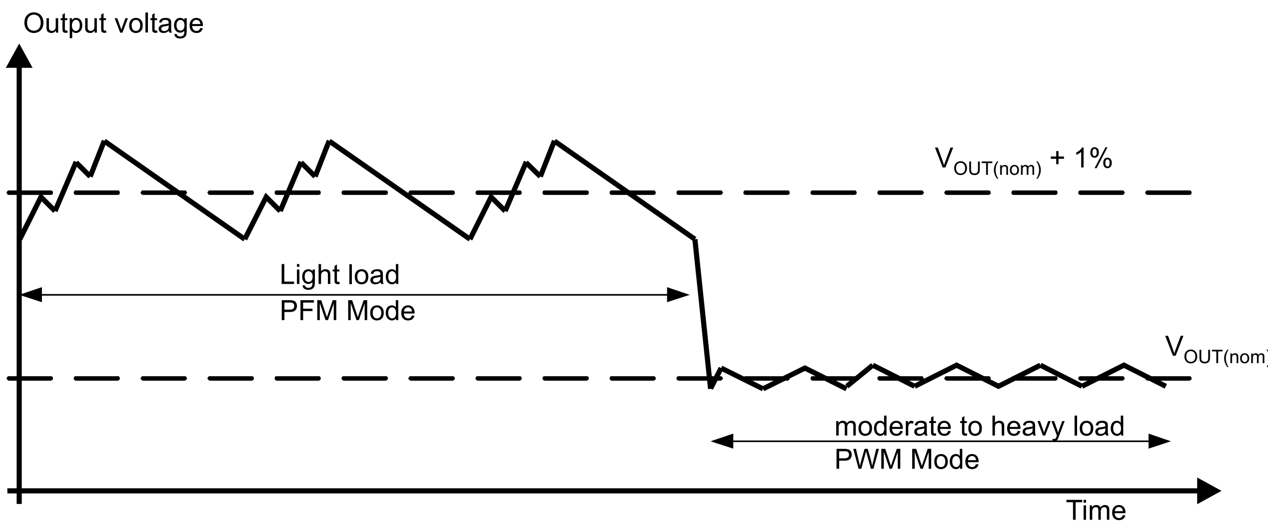


Figure 17. PFM Voltage Positioning

Pulling the MODE pin to DC ground results in an automatic transition between PFM and PWM modes to maximize efficiency.

Feature Description (continued)

The DC-DC converter output automatically discharges to ground through an internal 450-Ω load when EN_DCDC goes low or when the UVLO condition is met.

7.3.2 Soft Start

The step-down converter has an internal soft-start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp-up is controlled as shown in Figure 18.

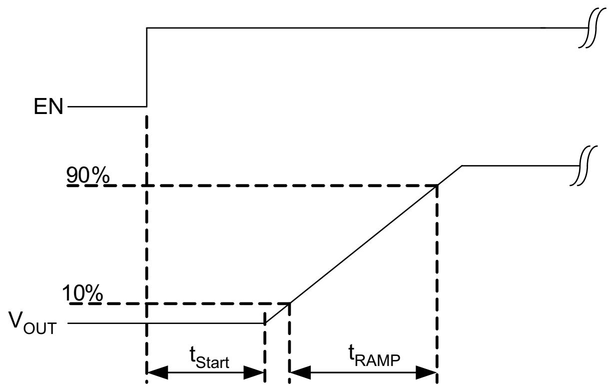


Figure 18. Soft Start

7.3.3 Linear Regulators

The two linear dropout regulators (LDOs) in the TPS650002-Q1 are designed to provide flexibility in system design. Each LDO has a separate voltage input and enable signal. The input can be tied to the output of the step-down converter or the output of another voltage source. Each LDO output discharges to ground automatically when EN_LDOx goes low.

The LDOs are general-purpose devices that can handle inputs from 6 V down to 1.6 V. Figure 19 shows the necessary connections for LDO1. The same architecture applies to LDO2.

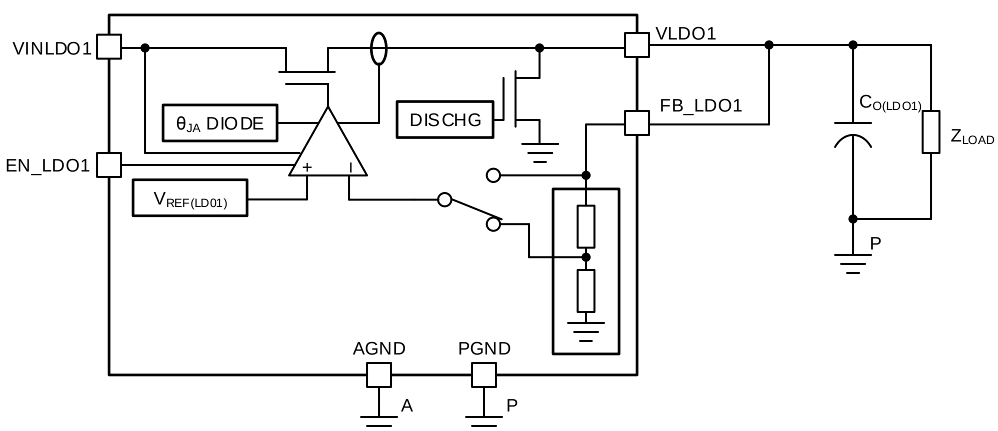


Figure 19. LDO Block Diagram

7.3.4 Power Good

The open-drain $\overline{PG}$ output is used to indicate the condition of the step-down converter and each LDO. This is a combined output, with the outputs being compared when the appropriate enable signal is high. The pin is pulled low when all enabled outputs are greater than 95%of the target voltage, and it is pulled into Hi-Z when an enabled output is less than 90% of its intended value or when all the enable signals are pulled low.

Feature Description (continued)

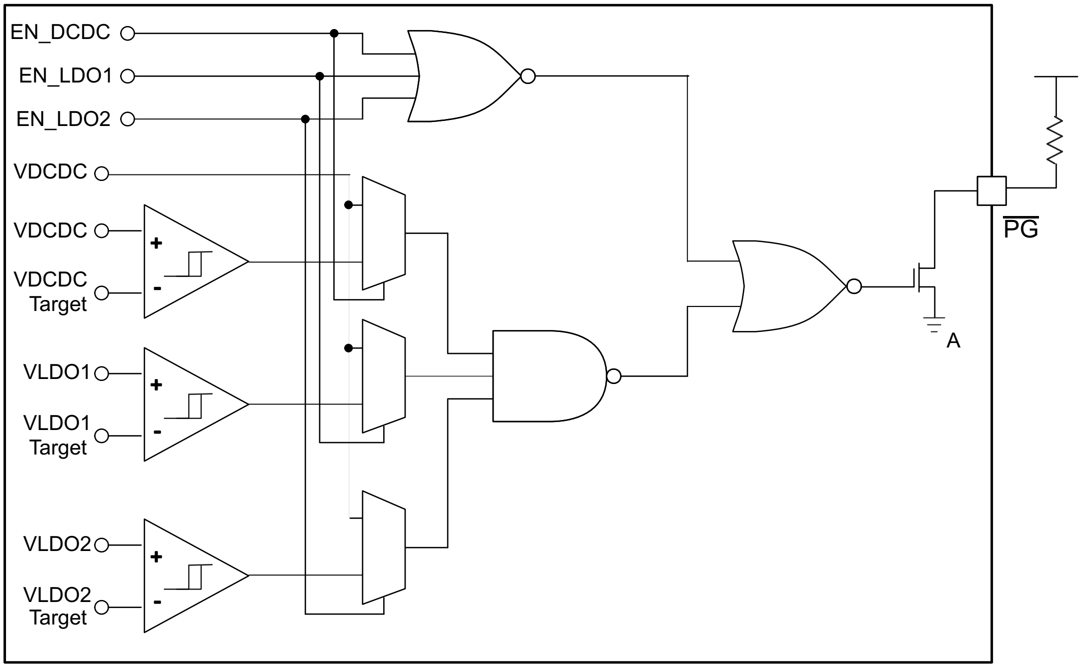


Figure 20. Power-Good Functionality

7.4 Device Functional Modes

The step-down converter has two modes of operation to maximize efficiency:

1. PFM
   - For light loads
   - For automatic transition between this mode and PWM mode when MODE pin is pulled low over all load ranges
2. PWM
   - For moderate to heavy loads
   - For a small output ripple
   - For maintaining the specified switching frequency variation by pulling the MODE pin high which places the device in a forced PWM mode over the entire load range.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS650002-Q1 can be used in an automotive-camera sensor module to generate the AVDD, DVDD, and IOVDD voltage rails. For noise immunity, one of the LDOs should be used to generate the AVDD voltage rail. To minimize power dissipation, the DC-DC converter should be used to power the DVDD rail because the DVDD rail normally has a lower operating voltage and higher current consumption.

8.2 Typical Application

Regulators with fixed voltage outputs do not require external feedback resistors. Feedback pins must externally connect to the output capacitors.

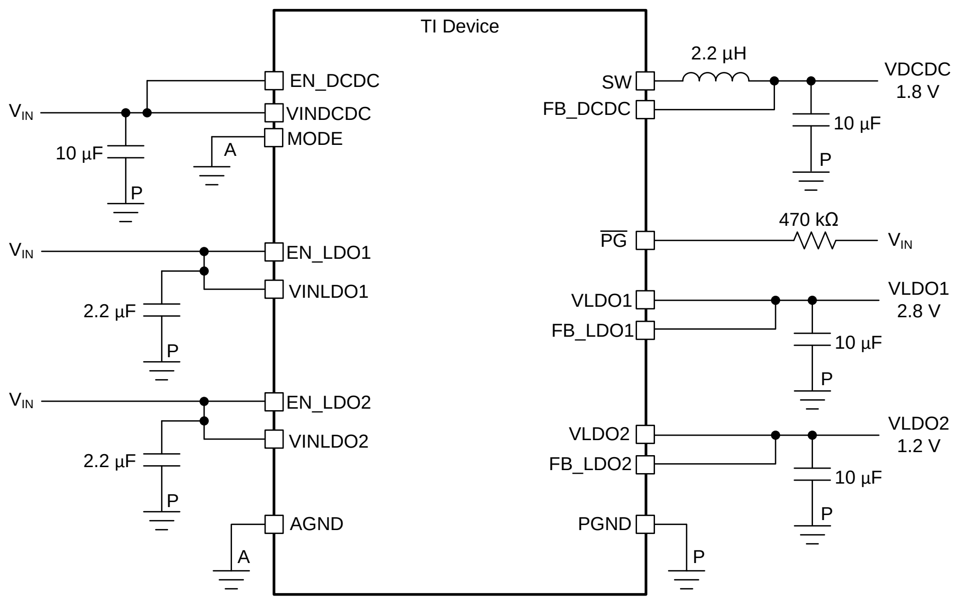


Figure 21. Typical Fixed Voltage Application Schematic

8.2.1 Design Requirements

For this example, the fixed voltage TPS650002-Q1 device operates with the parameters listed in Table 1.

Table 1. Design Parameters

RESOURCES	VOLTAGE
SW	1.8 V
VLDO1	2.8 V
VLDO2	1.2 V

8.2.2 Detailed Design Procedure

8.2.2.1 Output Filter Design (Inductor and Output Capacitor)

8.2.2.1.1 Inductor Selection

The typical value for the converter inductor is 2.2-µH output inductor. Larger or smaller inductor values in the range of 1.5 µH to 3.3 µH can optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly. An inductor with lowest DC resistance must be selected for highest efficiency. For more information on inductor selection, refer to the *Choosing Inductors and Capacitors for DC/DC Converters* application report.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. TI recommends this because during heavy load transient, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- f = Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak Inductor Ripple Current (1)

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = Maximum Inductor Current (2)

The highest inductor current occurs at maximum V_{IN}.

Open-core inductors have a soft saturation characteristic and can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consider that the core material from inductor to inductor differs and impacts the efficiency especially at high-switching frequencies.

The step down converter has internal loop compensation. TI designed the internal loop compensation to work with a certain output filter corner frequency calculated as in Equation 3:

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}} \text{ with } L = 2.2\mu H,\ C_{OUT} = 10\mu F \quad (3)$$

The selection of external L-C filter must be consistent with Equation 3. The product of L × C_{OUT} must be constant while selecting smaller inductor or increasing output capacitor value.

8.2.2.1.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 22 μF, without having large output voltage under and overshoots during heavy load transients. TI recommends ceramic capacitors with low ESR values because they result in lowest output voltage ripple. See for the TI-recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. The RMS ripple current is calculated as in Equation 4:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor as calculated in Equation 5:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (5)$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.2.2 Input Capacitor Selection

Due to the DC-DC converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high-input voltage spikes . Place the input capacitor as close as possible to the VINDCDC pin with the clean GND connection. Do the same for the output capacitor and the inductor. The converters require a ceramic input capacitor, a 10 μF is recommended . The input capacitor can increase without any limit for better input voltage filtering.

8.2.3 Application Curves

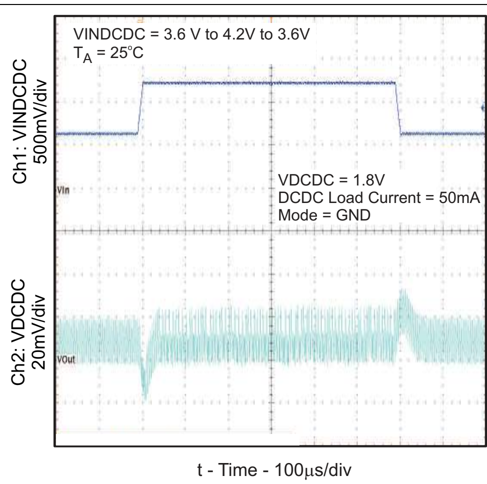


Figure 22. Line Transient Response (DC-DC PFM Mode)

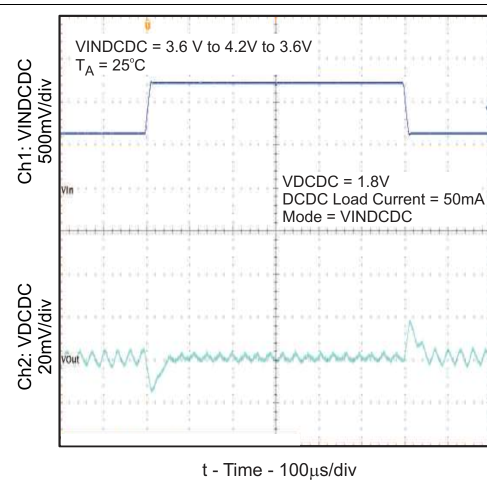


Figure 23. Line Transient Response (DC-DC PWM Mode)

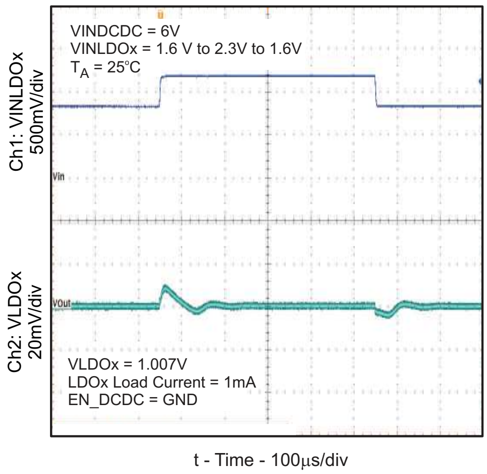


Figure 24. Line Transient Response (LDOx)

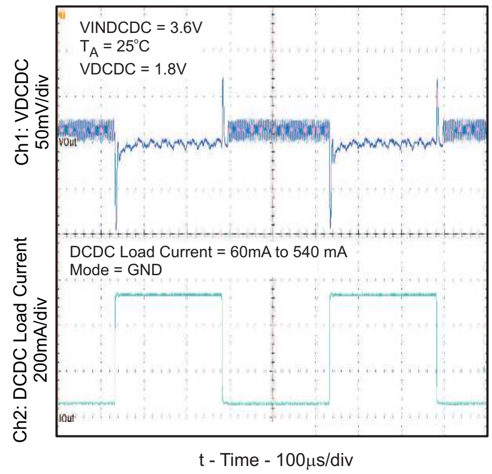


Figure 25. Load Transient Response (DC-DC PFM Mode)

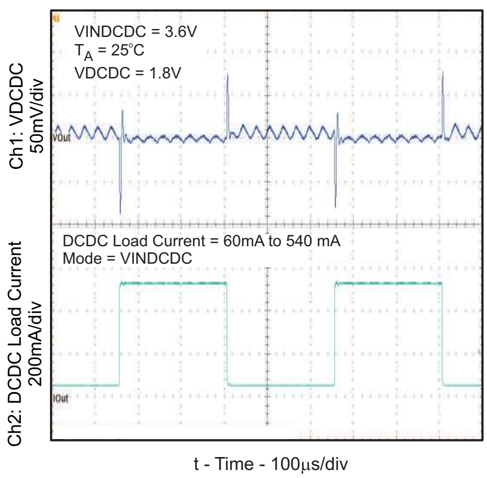


Figure 26. Load Transient Response (DC-DC PWM Mode)

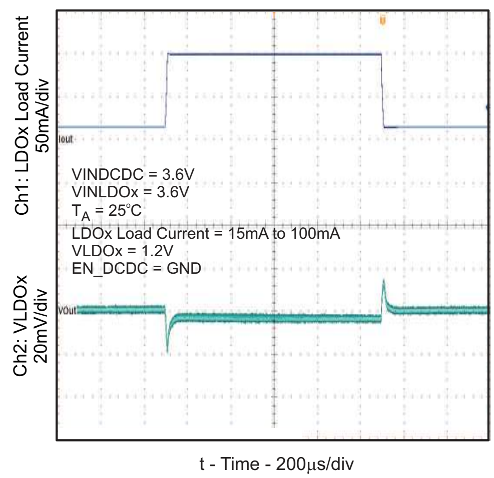


Figure 27. Load Transient Response (LDOx)

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 1.6 V to 6 V. This input supply can be from a DC supply, or other externally regulated supply. If the input supply is located more than a few inches from the TPS650002-Q1, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- The VINDCDC and VINLDOx pins must be bypassed to ground with a low-ESR ceramic bypass capacitor. TI recommends the typical bypass capacitance is 10 µF and 2.2 µF with a X5R dielectric.
- The optimum placement is closest to the VINDCDCx and VINLDOx pins of the device. Minimize the loop area formed by the bypass capacitor connection, the VINDCDC and VINLDO pins, and the thermal pad of the device.
- The thermal pad must be tied to the PCB ground plane with multiple vias.
- The traces of the VLDOx and VDCDCx pins (feedback pins) must be routed away from any potential noise source to avoid coupling.
- VODC output capacitance must be placed immediately at the VODC pin. Excessive distance between the capacitance and DCDCx pin may cause poor converter performance.
- AGND star back to PGND as close to the device as possible.
- DGND connect to the thermal pad

10.2 Layout Examples

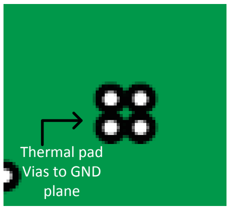


Figure 28. Layout Recommendation

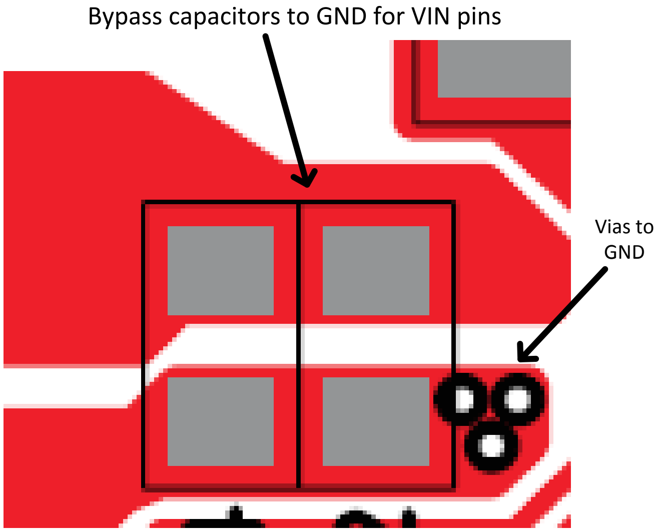


Figure 29. Bypass Capacitor and Via Placement Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Choosing Inductors and Capacitors for DC/DC Converters* application report
- Texas Instruments, *Using the TPS65000EVM 2.25 MHz Step-Down Converter with Dual LDO* user's guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650002TRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SJO2	Samples
TPS650002TRTETQ1	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SJO2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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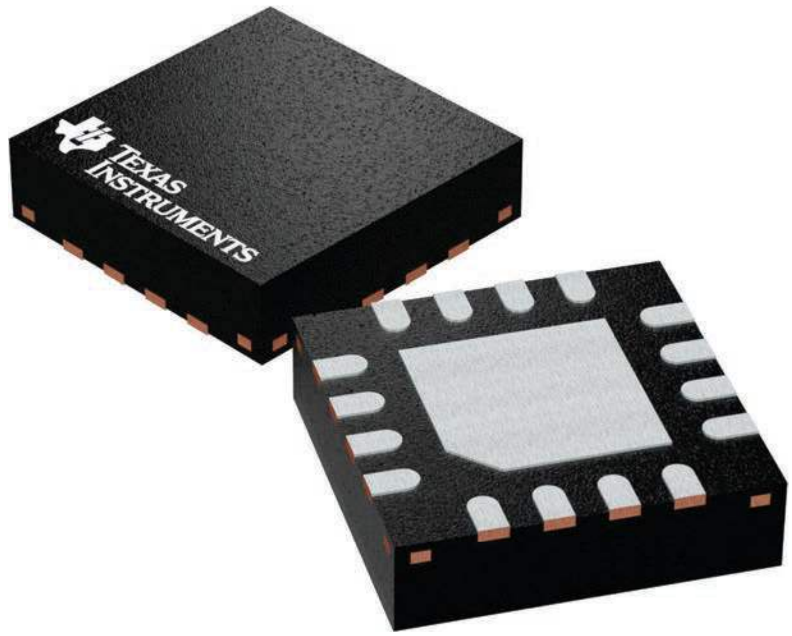
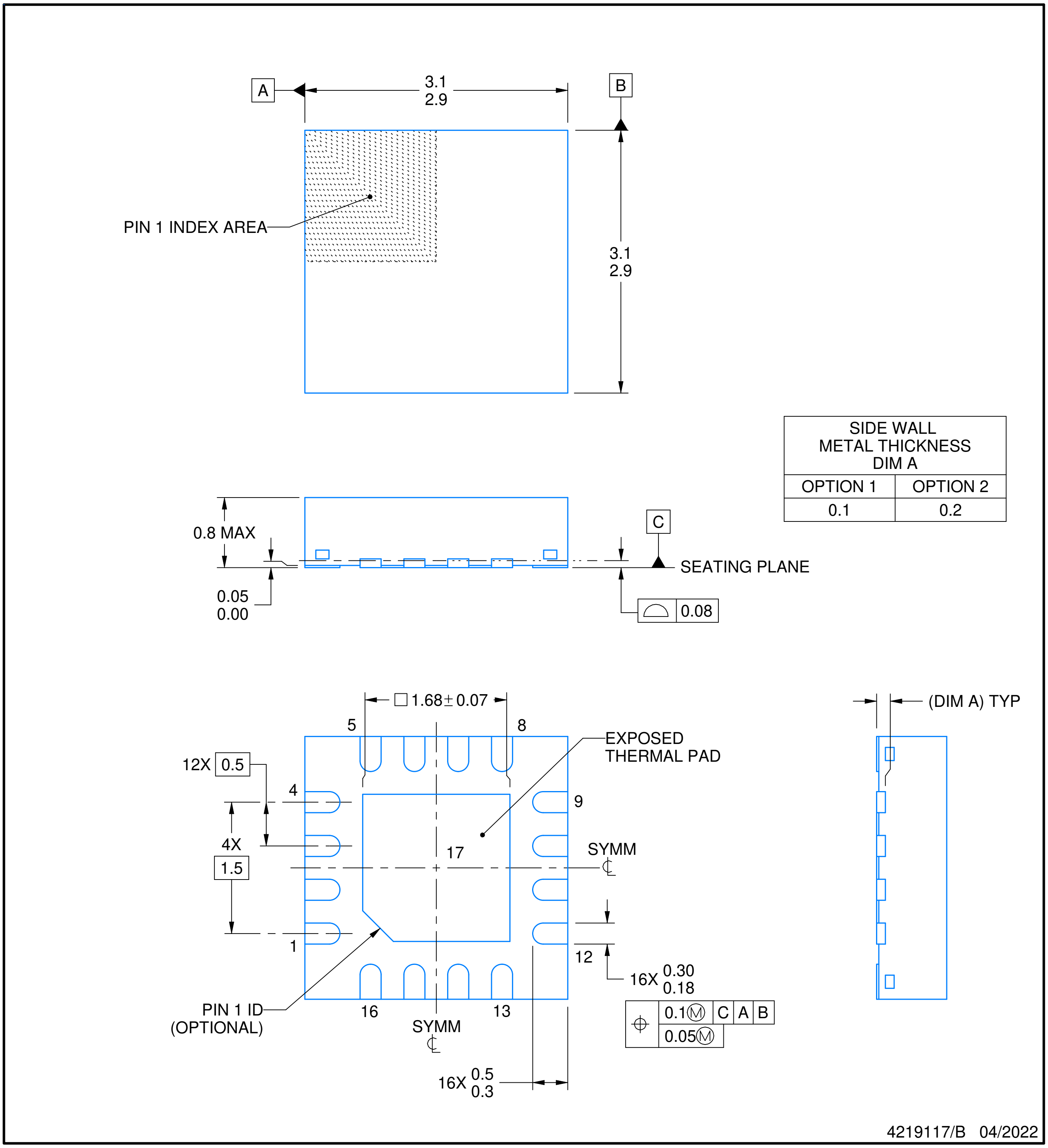
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

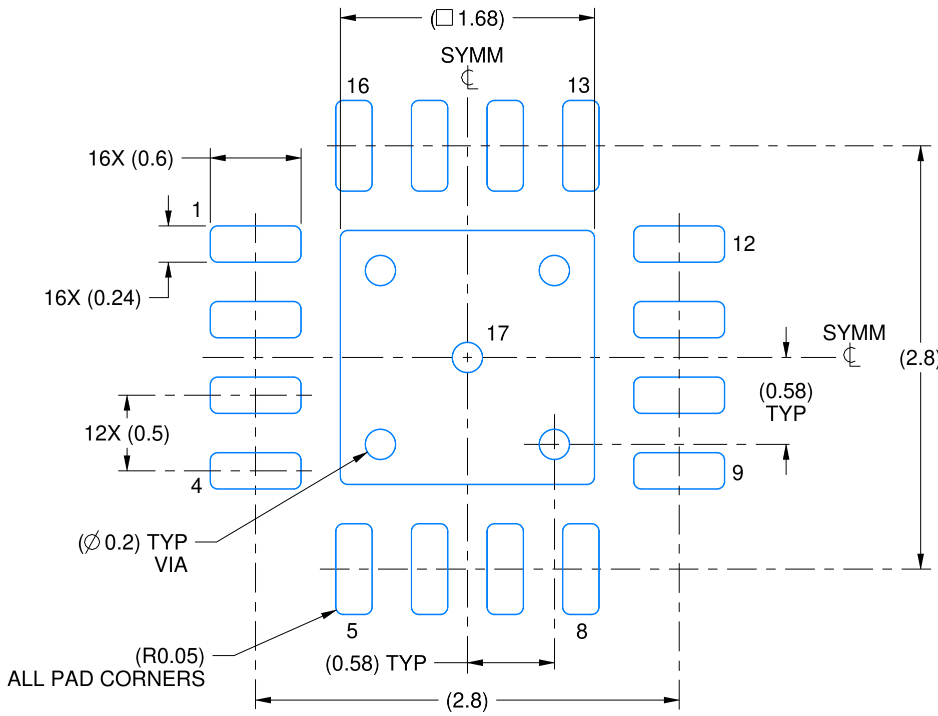
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



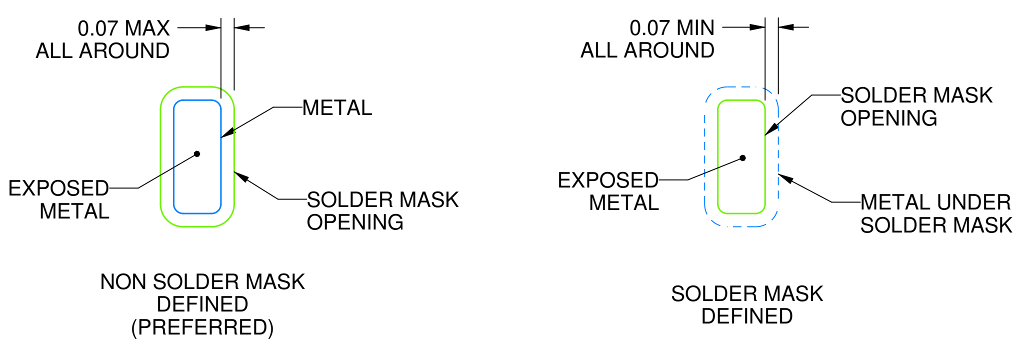


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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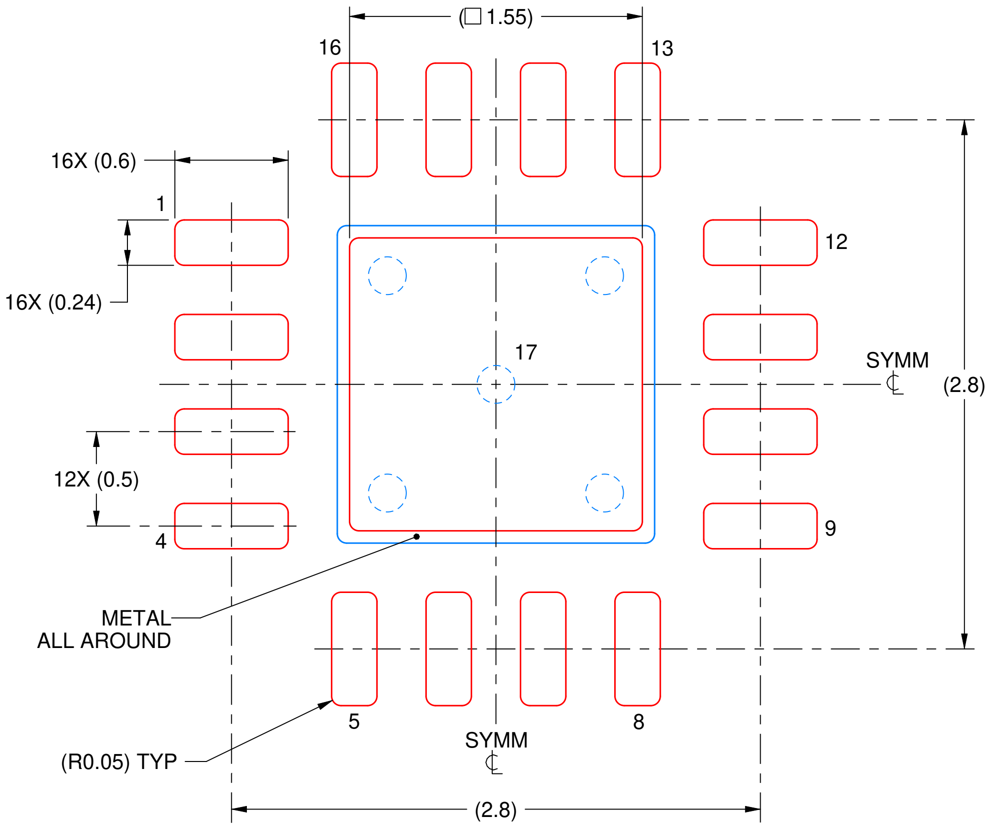
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.