# Programmable Gamma-Voltage Generator and High Slew Rate $V_{COM}$ with Integrated Two-Bank Memory plus 1/2 AVDD Topology

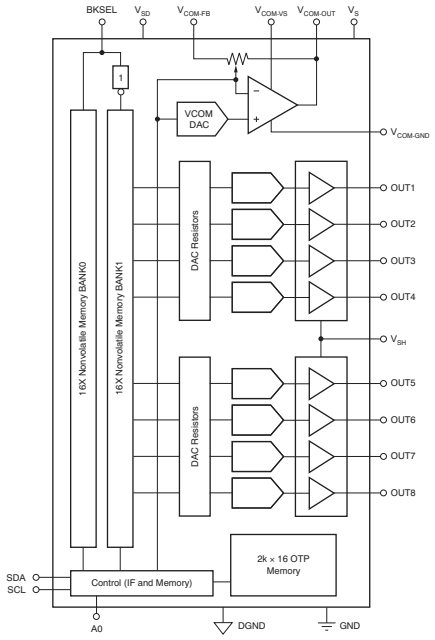
**Check for Samples: BUF08630**

## FEATURES

- **10-Bit Resolution**
- **8-Channel P-Gamma**
- **1-Channel P-$V_{COM}$**
- **High Slew Rate $V_{COM}$: 45 V/µs**
- **16x Rewritable Nonvolatile Memory**
- **Two Independent Pin-Selectable Memory Banks**
- **Rail-to-Rail Output:**
  - **300 mV Min Swing-to-Rail (10 mA)**
  - **> 300 mA Max $I_{OUT}$**
- **Low Supply Current**
- **Supply Voltage: 9 V to 20 V**
- **Digital Supply: 2 V to 5.5 V**
- **Two-Wire Interface:**
  - **Supports 400 kHz and 3.4 MHz**
- **1/2 AVDD Capability**

## APPLICATIONS

- **TFT-LCD Reference Drivers**




## DESCRIPTION

The BUF08630 offers eight programmable gamma channels and one programmable $V_{COM}$ channel.

The final gamma and $V_{COM}$ values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08630 supports up to 16 write operations to the on-chip memory.

The BUF08630 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma and $V_{COM}$ channels offer a rail-to-rail output that typically swings to within 150 mV of either supply rail with a 10-mA load. All channels are programmed using a two-wire interface that supports standard operations up to 400 kHz, and high-speed data transfers up to 3.4 MHz.

The BUF08630 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20V. The BUF08630 is available in a 20-pin QFN package, and is specified from –40°C to +95°C.

### RELATED PRODUCTS

| FEATURES | PRODUCT |
|---|---|
| 22-channel gamma correction buffer | BUF22821 |
| 16-channel gamma correction buffer | BUF16821 |
| 12-channel gamma correction buffer | BUF12800 |
| 18-/20-channel programmable buffer, 10-Bit, $V_{COM}$ | BUF20800 |
| 18-/20-Channel programmable buffer with memory | BUF20820 |
| Programmable $V_{COM}$ driver | BUF01900 |
| 22-V supply, traditional gamma buffers | BUF11705 |
| High-resolution, fully-programmable LCD bias IC for TV | TPS65168 |

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---|---|---|---|
| BUF08630 | VQFN-20 | RGW | BUF08630 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | BUF08630 | UNIT |
|---|---|---|---|
| Supply voltage | $V_S$ | +22 | V |
| | $V_{SH}$ | GND + 4.0 < $V_{SH}$ < $V_S$ – 4.0 | V |
| | $V_{SD}$ | +6 | V |
| Digital input pins, SCL, SDA, AO, BKSEL: voltage | | –0.5 to +6 | V |
| Digital input pins, SCL, SDA, AO, BKSEL: current | | ±10 | mA |
| Output pins, OUT1 through OUT4(2) | | (V–) – 0.5 to ($V_{SH}$) + 0.5 | V |
| Output pins, OUT5 through OUT8(2) | | ($V_{SH}$) – 0.5 to (V+) + 0.5 | V |
| $V_{COM}$(2) | | (V–) – 0.5 to (V+) + 0.5 | V |
| Output short-circuit(3) | | Continuous | |
| Ambient operating temperature | | –40 to +95 | °C |
| Ambient storage temperature | | –65 to +150 | °C |
| Junction temperature, $T_J$ | | +125 | °C |
| ESD ratings | Human body model (HBM) | 4 | kV |
| | Charged device model (CDM) | 1 | kV |
| | Machine model (MM) | 200 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) See the *Output Protection* section.
(3) Short-circuit to ground, one amplifier per package. Exposed thermal die is soldered to the printed circuit board (PCB) using thermal vias. Refer to Texas Instruments' application report SLAU271, *QFN/SON PCB Attachment*.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | BUF08630 RGW 20 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 42.4 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 34.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 10.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.4 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | 2.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +95°C.**
At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = 9.0 V, $V_{SD}$ = +2 V, and $C_L$ = 200 pF, unless otherwise noted.

| PARAMETER | | CONDITIONS | BUF08630 MIN | BUF08630 TYP | BUF08630 MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG GAMMA BUFFER CHANNELS** | | | | | | |
| Reset value | | Code = 512 | | 9 | | V |
| **OUT1, 4 output swing: high** | | **Code = 1023, sourcing 10 mA** | **17.7** | **17.85** | | **V** |
| **OUT1, 4 output swing: low** | | **Code = 512, sinking 10 mA** | | **$V_{SH}$ + 0.07** | **$V_{SH}$ + 0.3** | **V** |
| **OUT2, 3 output swing: high** | | **Code = 1023, sourcing 10 mA** | **17.5** | **17.85** | | **V** |
| **OUT2, 3 output swing: low** | | **Code = 512, sinking 10 mA** | | **$V_{SH}$ + 0.07** | **$V_{SH}$ + 0.5** | **V** |
| **OUT5, 8 output swing: high** | | **Code = 511, sourcing 10 mA** | **$V_{SH}$ – 0.3** | **$V_{SH}$ – 0.15** | | **V** |
| **OUT5, 8 output swing: low** | | **Code = 0, sinking 10 mA** | | **0.05** | **0.3** | **V** |
| **OUT6, 7 output swing: high** | | **Code = 511, sourcing 10 mA** | **$V_{SH}$ – 0.5** | **$V_{SH}$ – 0.15** | | **V** |
| **OUT6, 7 output swing: low** | | **Code = 0, sinking 10 mA** | | **0.05** | **0.5** | **V** |
| **$V_{COM}$ output swing: high**(1) | | **Code = 960, sourcing 400 mA** | **13** | **15.3** | | **V** |
| $V_{COM}$ output swing: low(1) | | Code = 0, sinking 400 mA | | 3.8 | 5 | V |
| **vs Temperature** | | **Code = 0, sinking 400 mA** | | | **6** | **V** |
| $V_{COM}$ slew rate(2) | | $R_{LOAD}$ = 60 Ω, $C_{LOAD}$ = 100 pF | | 45 | | V/µs |
| Continuous output current | | Note (3) | | 30 | | mA |
| Output accuracy, $V_{COM}$(4) | | Code = 512 | | ±20 | ±50 | mV |
| **vs Temperature** | | **Code = 512** | | **±25** | | **µV/°C** |
| Output accuracy, OUT1 to OUT4 | | Code = 768, $V_{SH}$ = 9 V, $V_S$ = 18 V | | ±20 | ±50 | mV |
| **vs Temperature** | | **Code = 768** | | **±25** | | **µV/°C** |
| Output accuracy, OUT5 to OUT8 | | Code = 256, $V_{SH}$ = 9 V, $V_S$ = 18 V | | ±20 | ±50 | mV |
| **vs Temperature** | | **Code = 256** | | **±25** | | **µV/°C** |
| Integral nonlinearity(4) | INL | | | 0.3 | | LSB |
| Differential nonlinearity(4) | DNL | | | 0.3 | | LSB |
| Load regulation | REG | OUT1 to OUT4 code = 768, $I_{OUT}$ = +5-mA to –5-mA step | | 0.5 | 1.5 | mV/mA |
| | | OUT5 to OUT8 code = 256, $I_{OUT}$ = +5-mA to –5-mA step | | 0.5 | 1.5 | mV/mA |
| **OTP MEMORY** | | | | | | |
| Number of OTP write cycles | | | | | 16 | Cycles |
| Memory retention | | | | 100 | | Years |
| **ANALOG POWER SUPPLY** | | | | | | |
| Operating range | | | 9 | | 20 | V |
| Total analog supply current | $I_S$ | OUT1 to OUT4 set code = 768, OUT5 to OUT8 set code = 256, no load | | 6.9 | 11 | mA |
| **Over temperature** | | | | | **11** | **mA** |
| **DIGITAL** | | | | | | |
| Logic 1 input voltage | $V_{IH}$ | | 0.7 × $V_{SD}$ | | | V |
| Logic 0 input voltage | $V_{IL}$ | | | | 0.3 × $V_{SD}$ | V |
| Logic 0 output voltage | $V_{OL}$ | $I_{SINK}$ = 3-mA | | 0.15 | 0.4 | V |
| Input leakage | | | | ±0.01 | ±10 | µA |
| **Clock frequency** | **$f_{CLK}$** | **Standard/Fast mode** | | | **400** | **kHz** |
| | | **High-Speed mode** | | | **3.4** | **MHz** |
| **DIGITAL POWER SUPPLY** | | | | | | |
| Specified range | $DV_{DD}$ | | 2.0 | | 5.5 | V |
| Digital supply current(3) | $DI_{DD}$ | Outputs at reset values, no load, two-wire bus inactive | | 115 | 180 | µA |
| **Over temperature** | | | | **115** | **180** | **µA** |

(1) The BUF08630 $V_{COM}$ DAC limits can be programmed. These default limits apply if the device is not programmed. See the *Programmable Vcom Limits* section.
(2) See Figure 19, *Large-Signal Step Response, $V_{COM}$*.
(3) Observe maximum power dissipation.
(4) The $V_{COM}$ output voltage is limited to codes 0 to 960 because of the common-mode input range of the $V_{COM}$ amplifier. This limitation is for $V_{COM}$ only; it does not affect DAC OUT1 to 8.

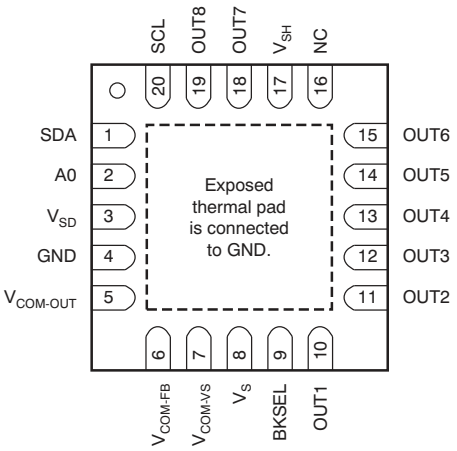
## ELECTRICAL CHARACTERISTICS (continued)

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +95°C.**
At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = 9.0 V, $V_{SD}$ = +2 V, and $C_L$ = 200 pF, unless otherwise noted.

| PARAMETER | CONDITIONS | BUF08630 MIN | BUF08630 TYP | BUF08630 MAX | UNIT |
|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | |
| Specified range | | –40 | | +95 | °C |
| Storage range | | –65 | | +150 | °C |

## PIN CONFIGURATION

**RGW PACKAGE**
**VQFN-20**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| PIN NAME | PIN NO. | DESCRIPTION |
|---|---|---|
| A0 | 2 | A0 address pin for two-wire address; connect to either logic 1 or logic 0. See Table 1. |
| BKSEL | 9 | Selects memory bank 0 or 1; connect to either logic 1 to select bank 1 or logic 0 to select bank 0. |
| GND | 4 | Ground |
| NC | 16 | No Connect |
| OUT1 | 10 | DAC output 1 |
| OUT2 | 11 | DAC output 2 |
| OUT3 | 12 | DAC output 3 |
| OUT4 | 13 | DAC output 4 |
| OUT5 | 14 | DAC output 5 |
| OUT6 | 15 | DAC output 6 |
| OUT7 | 18 | DAC output 7 |
| OUT8 | 19 | DAC output 8 |
| SCL | 20 | Serial clock input; connect to pull-up resistor. |
| SDA | 1 | Serial data I/O; open-drain, connect to pull-up resistor. |
| $V_{COM-AVDD}$ | 7 | $V_{COM}$ supply |
| $V_{COM-FB}$ | 6 | $V_{COM}$ feedback |
| $V_{COM-OUT}$ | 5 | $V_{COM}$ output |
| $V_S$ | 8 | $V_S$ connected to analog supply. |
| $V_{SD}$ | 3 | Digital supply; connect to logic supply. |
| $V_{SH}$ | 17 | $V_{SH}$ connected to 1/2 analog supply. |

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = +9 V, and $V_{SD}$ = +2 V, unless otherwise noted.

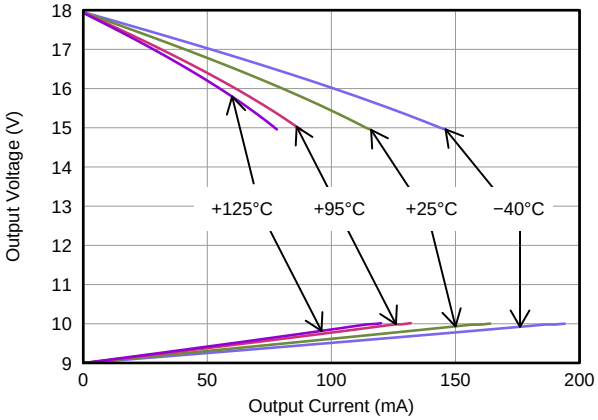



**Figure 1.**

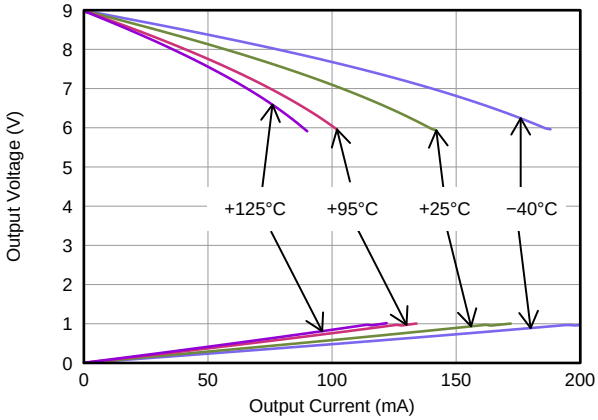



**Figure 2.**

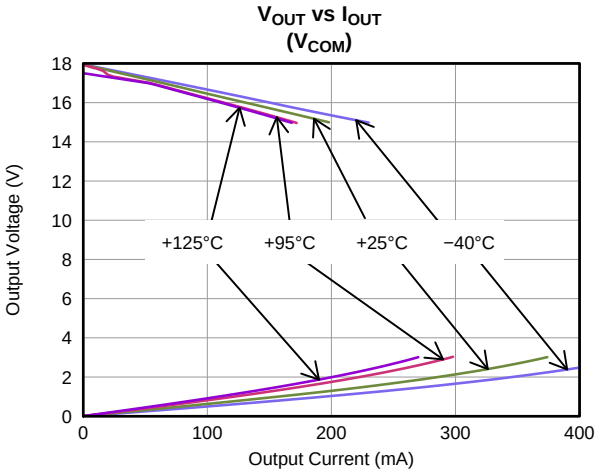



**Figure 3.**

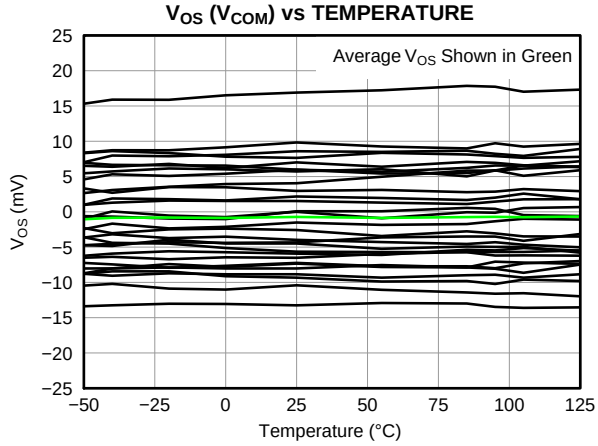



**Figure 4.**

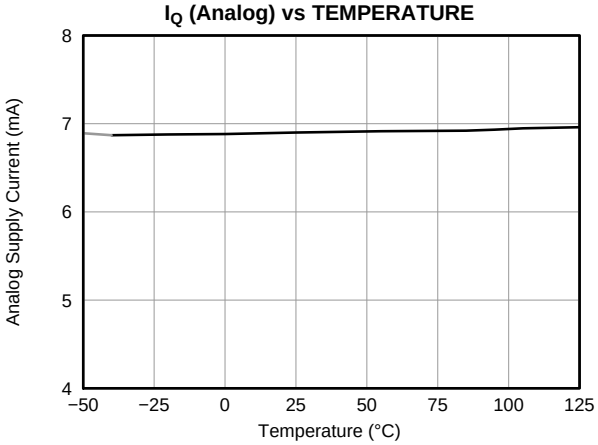



**Figure 5.**

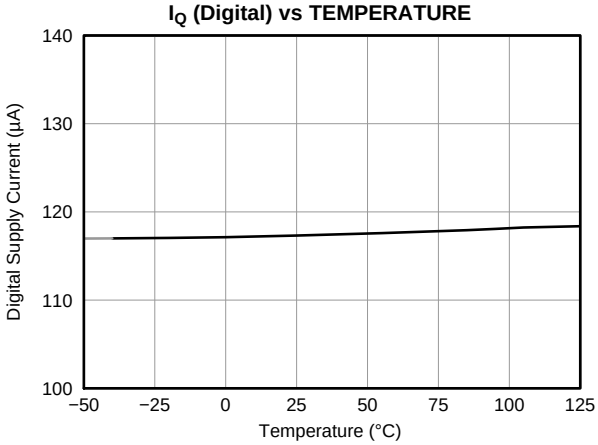



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = +9 V, and $V_{SD}$ = +2 V, unless otherwise noted.

**INTEGRAL LINEARITY ERROR ($V_{COM}$)**

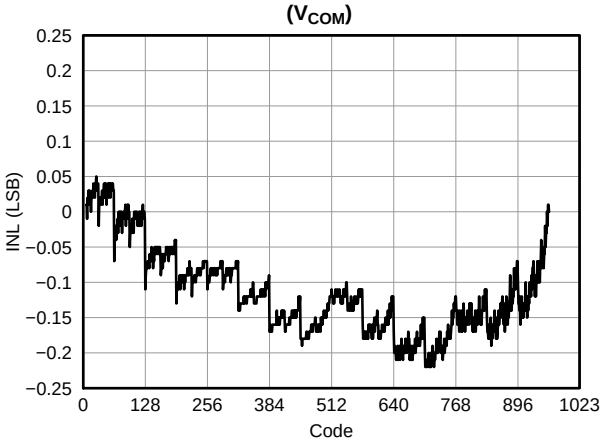



**Figure 7.**

**DIFFERENTIAL LINEARITY ERROR ($V_{COM}$)**

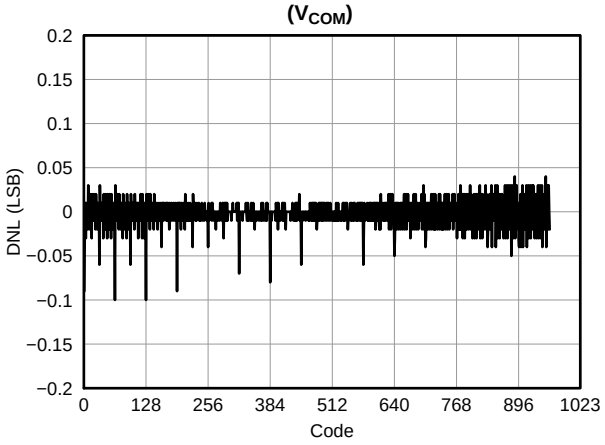



**Figure 8.**

**INTEGRAL LINEARITY ERROR (OUT1 to OUT4)**

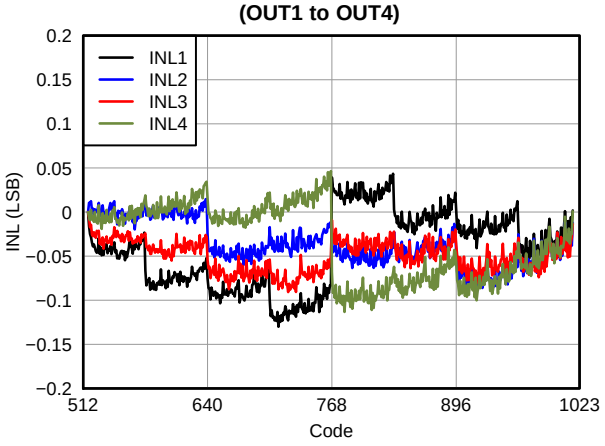



**Figure 9.**

**DIFFERENTIAL LINEARITY ERROR (OUT1 to OUT4)**

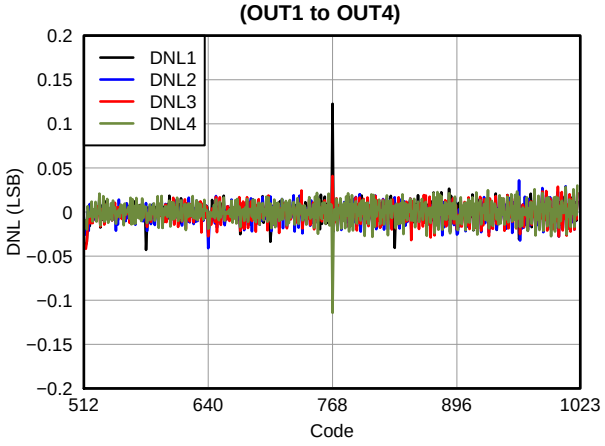



**Figure 10.**

**INTEGRAL LINEARITY ERROR (OUT5 to OUT8)**

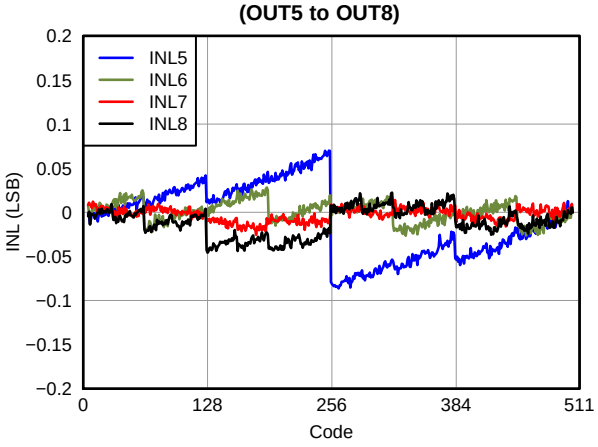



**Figure 11.**

**DIFFERENTIAL LINEARITY ERROR (OUT5 to OUT8)**

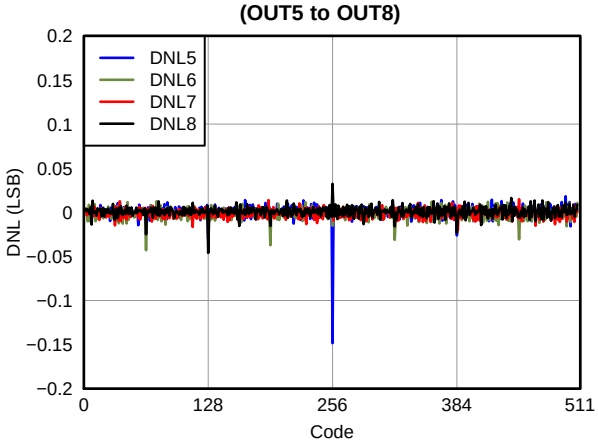



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = +9 V, and $V_{SD}$ = +2 V, unless otherwise noted.

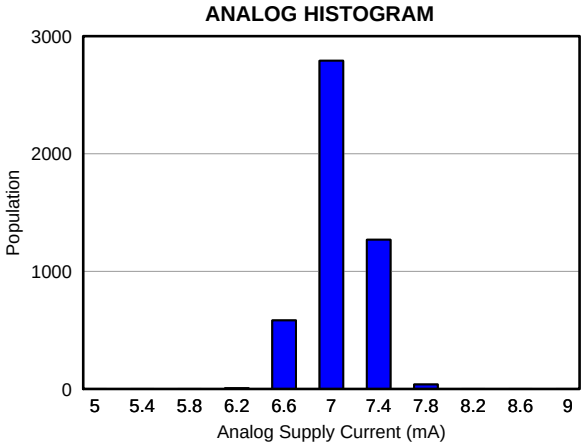



**Figure 13.**

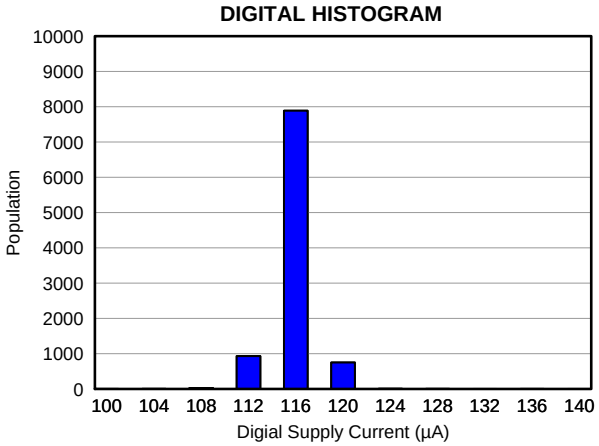



**Figure 14.**

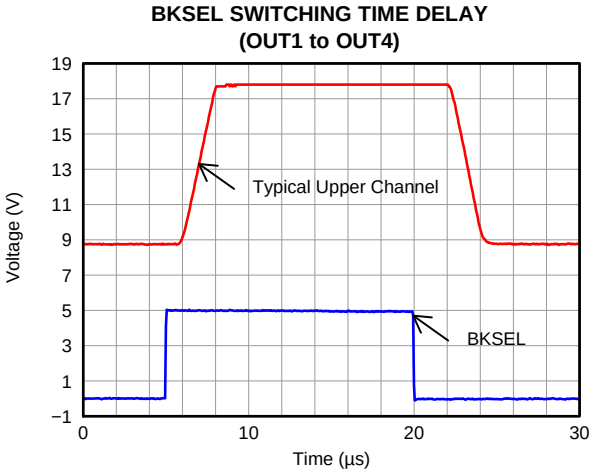



**Figure 15.**

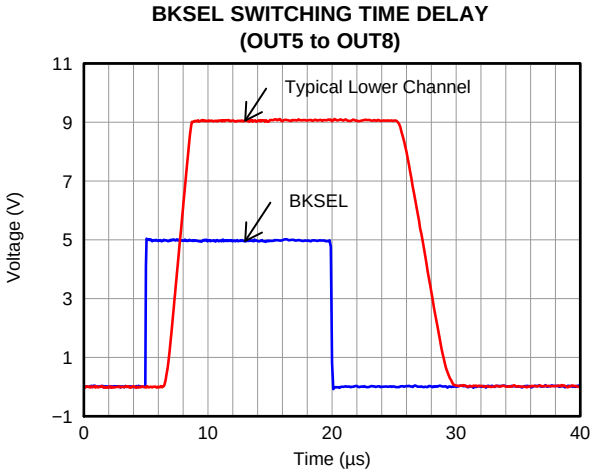



**Figure 16.**

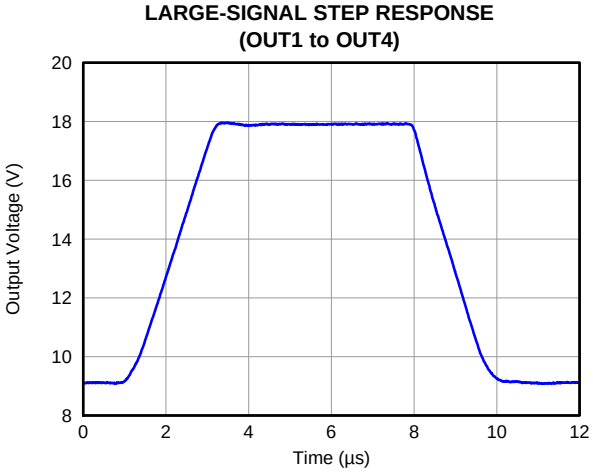



**Figure 17.**

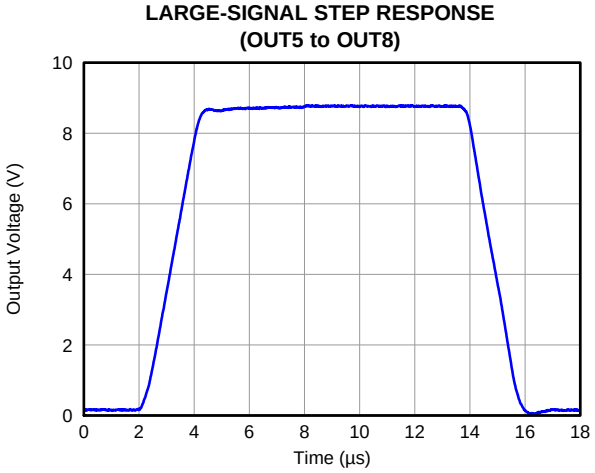



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = +18 V, $V_{SH}$ = +9 V, and $V_{SD}$ = +2 V, unless otherwise noted.

**LARGE-SIGNAL STEP RESPONSE ($V_{COM}$)**

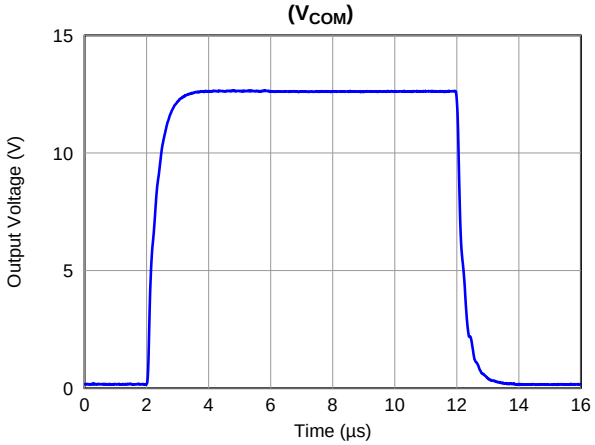



**Figure 19.**

# APPLICATION INFORMATION

## GENERAL DESCRIPTION

The BUF08630 programmable voltage reference allows fast and easy adjustment of eight programmable gamma reference outputs and a $V_{COM}$ output, each with 10-bit resolution. The BUF08630 is programmed through a high-speed, two-wire interface. The final gamma and $V_{COM}$ values can be stored in the onboard, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08630 supports up to 16 write operations to the onboard memory. The BUF08630 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves.

The BUF08630 can be powered using an analog supply voltage from 9 V to 20 V, and a digital supply from 2 V to 5.5 V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. In addtion, analog supply voltage $V_S$ should be turned on before $V_{SH}$.

### Power-Up Sequence

When applying power to the BUF08630, the digital supply must be powered up first. The analog supply for the $V_{COM}$ amplifier ($V_{COM-VS}$), and the analog supply ($V_S$) should be brought up at least 1.2 ms later so that the programmed values in the nonvolatile memory can be written to the DAC registers. The analog supply voltage ($V_{COM-VS}$) must always preceed $V_S$, or the two supply pins should be tied together so that they turn on and off simultaneously. The supply voltage $V_{SH}$ must always follow $V_S$.

**CAUTION**

If $V_{COM-VS}$ is brought up after $V_S$, damage will occur to the analog switches for $V_{COM}$.

It is recommended that the TPS65168 be used together with the BUF08630 for best performance, as shown in Figure 24. Note that the TPS65168 provides the power sequence previously described and required by the BUF08630.

Figure 20 shows the proper power-up sequence when two supplies are used (that is, $V_S$ and $V_{COM-VS}$ are connected together).Figure 21 shows the proper power-up sequence when three supplies are used (that is, $V_{SH}$, $V_S$, and $V_{COM-VS}$ are separate supplies).

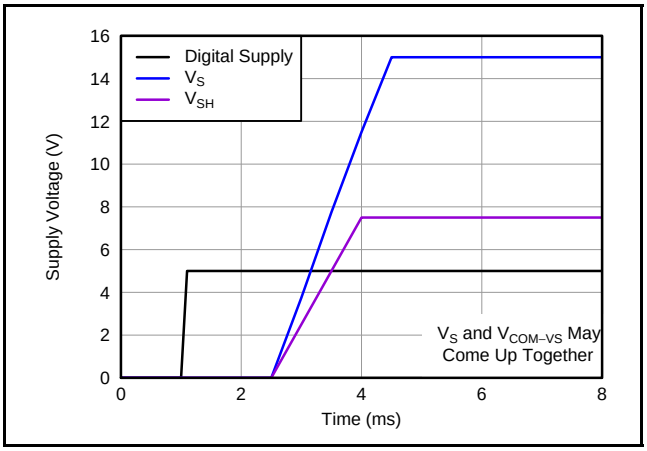



**Figure 20. Startup Requirement with Two Supplies**

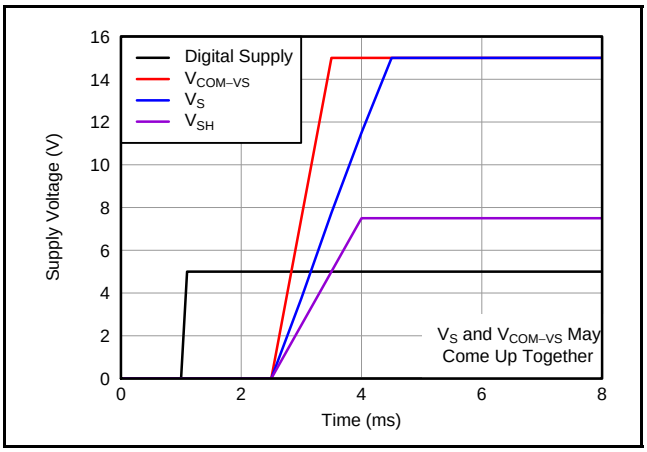



**Figure 21. Startup Requirement with Three Supplies**

### Power-Down Sequence

When removing power from the BUF08630, the reverse sequence from that described in the *Power-Up Sequence* must be used. Figure 22 shows the sequence that must be followed when $V_{COM-VS}$ is connected to $V_S$. Figure 23 shows the sequence that must be followed when $V_{COM-VS}$ is not connected to $V_S$.

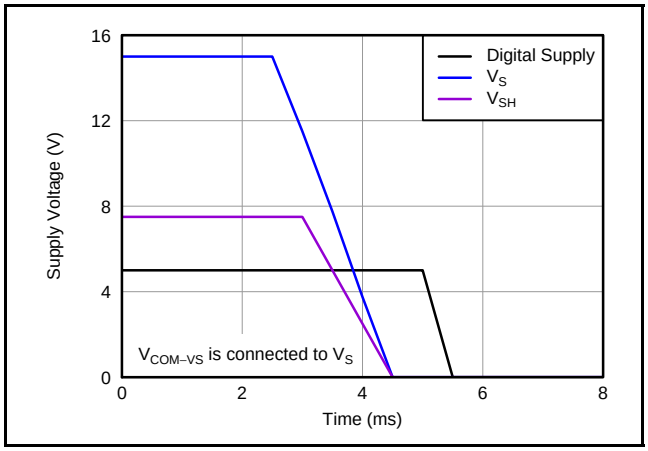



**Figure 22. Shutdown Requirement with Two Supplies**

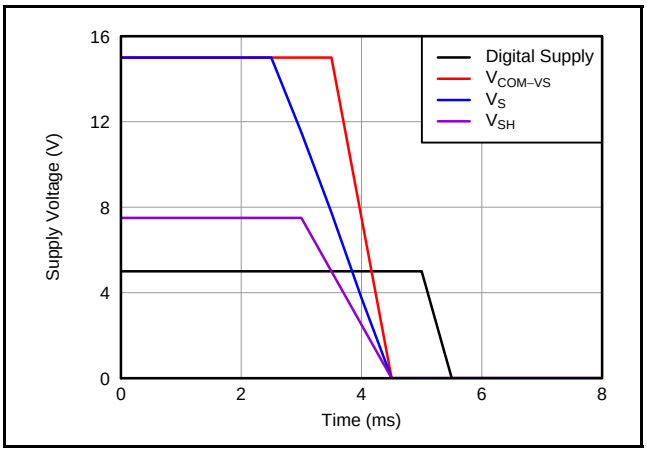



**Figure 23. Shutdown Requirement with Three Supplies**

A separate supply pin is provided for $V_{COM-VS}$ so that separate supplies can be used for the gamma buffers and $V_{COM}$. The gamma buffers could be powered with a *clean* supply to prevent noise coupling into the gamma channels. The $V_{COM}$ amplifier can then be supplied by a power source with more current capability, but with higher noise.

It is highly recommended that a Schottky diode be placed between $V_S$ and $V_{SH}$, as shown in Figure 37.

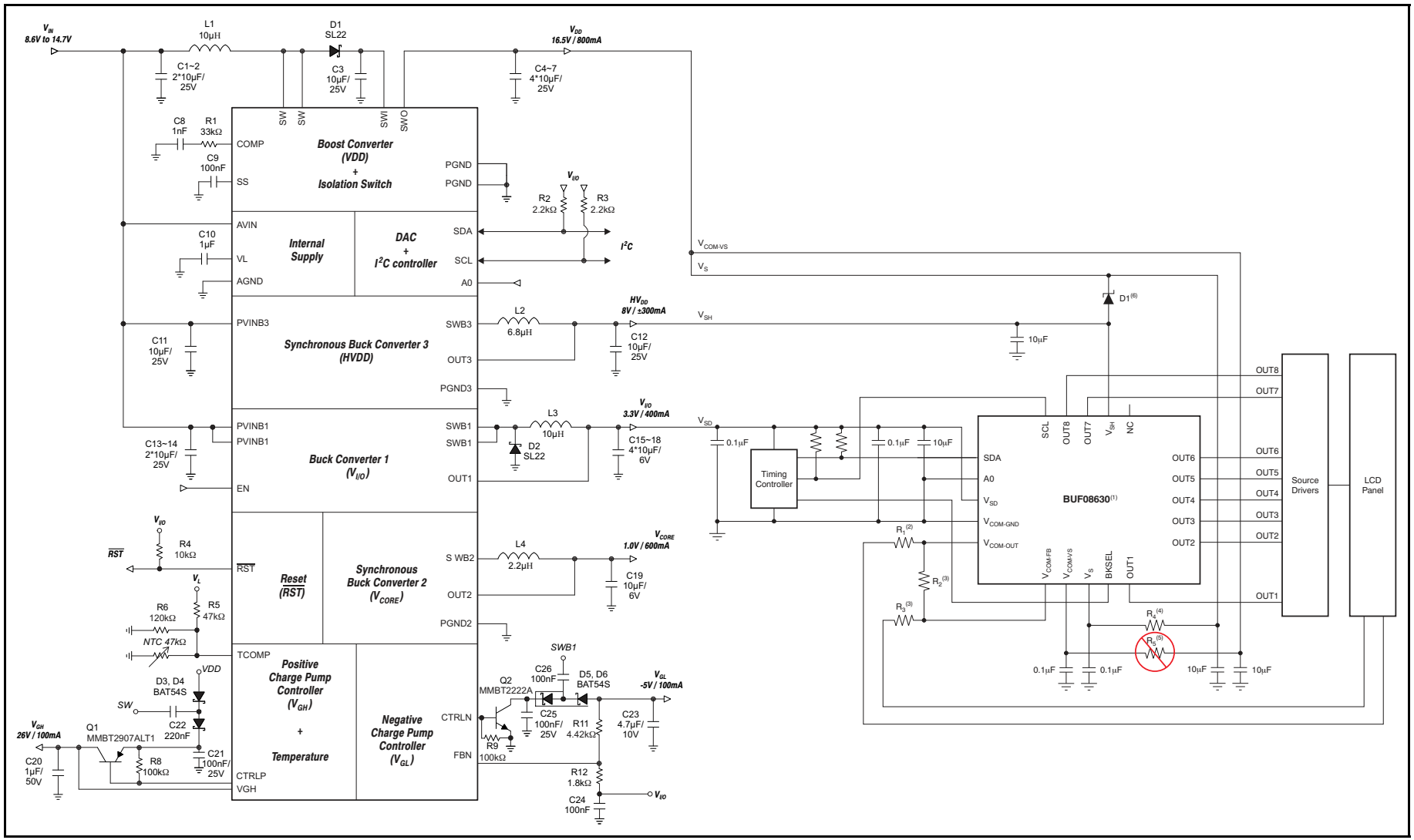



**Figure 24. Typical Application Circuit using the TPS65168**

## TWO-WIRE BUS OVERVIEW

The BUF08630 communicates over an industry-standard, two-wire interface to receive data in slave mode. This model uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from low to high while SCL is high. The BUF08630 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF08630.

## ADDRESSING THE BUF08630

The address of the BUF08630 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is low, the device acknowledges on address 74h (*1110100*). If the A0 pin is high, the device acknowledges on address 75h (*1110101*). Table 1 shows the A0 pin settings and BUF08630 address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

**Table 1. Quick Reference of BUF08630 Addresses**

| DEVICE/COMPONENT<br>BUF08630 ADDRESS | ADDRESS |
|---|---|
| A0 pin is low<br>(device acknowledges on address 74h) | 1110100 |
| A0 pin is high<br>(device acknowledges on address 75h) | 1110101 |

## DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows clock frequency up to 100 kHz;
- Fast: allows clock frequency up to 400 kHz; and
- High-speed mode (also called Hs mode): allows clock frequency up to 3.4 MHz.

The BUF08630 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with SCL ≤ 400 kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Table 2 provides a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read/write status.) The BUF08630 responds to the High-speed command regardless of the value of these last three bits. The BUF08630 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF08630 switches on its Hs mode filters, and communicates at up to 3.4 MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF08630 switches out of Hs mode with the next STOP condition.

**Table 2. Quick Reference of Command Codes**

| COMMAND | CODE |
|---|---|
| General-Call Reset | Address byte of 00h followed by a data byte of 06h. |
| High-Speed Mode | 00001xxx, with SCL ≤ 400 kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code. |

## GENERAL-CALL RESET AND POWER-UP

The BUF08630 responds to a General-Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (*0000 0110*). The BUF08630 acknowledges both bytes. Table 2 provides a reference for the General-Call Reset command code. Upon receiving a General-Call Reset, the BUF08630 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General-Call address byte of 00h (*0000 0000*), but does not acknowledge any General-Call data bytes other than 06h (*0000 0110*).

When the BUF08630 powers up, it automatically performs a reset. As part of the reset, the BUF08630 is configured for all outputs to change to the last programmed nonvolatile memory values, or *1000000000* if the nonvolatile memory values have not been programmed.

Upon power-up or general-call reset, the DAC registers for channels 1 though 8 are set to 200 (default) that corresponds to mid-scale output for a 10-bit DAC. The high and low limit registers are set to 3FF and 000 respectively. Therefore, the limits are transparent if not programmed. Reset typically requires approximately 1ms.

## OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage ($V_S$) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left( \frac{\text{Code}}{1024} \right) \quad (1)$$

Where Code = 0 to 1023.

The BUF08630 outputs are capable of a full-scale voltage output change in typically 5 µs; no intermediate steps are required.

## UPDATING THE DAC OUTPUT VOLTAGES

Because the BUF08630 features a double-buffered register structure, updating the digital-to-analog converter (DAC) and/or the $V_{COM}$ *register* is not the same as updating the DAC and/or $V_{COM}$ *output voltage*. There are two methods for updating the DAC/$V_{COM}$ output voltages.

**Method 1:** Method 1 is used when it is desirable to have the DAC/$V_{COM}$ output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC/$V_{COM}$ output voltage update occurs after receiving the 16th data bit for the currently-written register.

**Method 2:** Method 2 is used when it is desirable to have all DAC/$V_{COM}$ output voltages change at the same time. First, the master writes to the desired DAC/$V_{COM}$ channels with data bit 15 a '0'. Then, when writing the last desired DAC/$V_{COM}$ channel, the master sets data bit 15 to a '1'. All DAC/$V_{COM}$ channels are updated at the same time after receiving the 16th data bit.

## NONVOLATILE MEMORY

### BKSEL Pin

The BUF08630 has 16x rewrite capability of the nonvolatile memory. Additionally, the BUF08630 has the ability to store two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, BANK0 is selected; when this pin is high, BANK1 is selected.

When the BKSEL pin changes state, the BUF08630 loads values from the DAC registers to the DAC outputs for the newly chosen bank. At power-up, the state of the BKSEL pin determines which memory bank is selected.

The two-wire master also has the ability to update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

### General Acquire Command

A general acquire command is used to update all registers and DAC/$V_{COM}$ outputs to the last programmed values stored in nonvolatile memory. A single-channel acquire command updates only the register and DAC/$V_{COM}$ output of the DAC/$V_{COM}$ corresponding to the DAC/$V_{COM}$ address used in the single-channel acquire command.

These are the steps of the sequence to initiate a general channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the appropriate device address (based on A0) and the read/write bit = low. The BUF08630 acknowledges this byte.
4. Send a DAC/$V_{COM}$ pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5-D0 are any valid DAC/$V_{COM}$ address. Although the BUF08630 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/$V_{COM}$ addresses.
5. Send a STOP condition on the bus.

Approximately 750µs (±80 µs) after issuing this command, all DAC/$V_{COM}$ registers and DAC/$V_{COM}$ output voltages change to the respective, appropriate nonvolatile memory values.

### Single-Channel Acquire Command

These are the steps to initiate a single-channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the device address (based on A0) and read/write bit = low. The BUF08630 acknowledges this byte.
4. Send a DAC/$V_{COM}$ pointer address byte using the DAC/$V_{COM}$ address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5-D0 are the DAC/$V_{COM}$ address. Although the BUF08630 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   It returns *0000* reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/$V_{COM}$ addresses.
5. Send a STOP condition on the bus.

Approximately 36µs (±4 µs) after issuing this command, the specified DAC/$V_{COM}$ register and DAC/$V_{COM}$ output voltage change to the appropriate memory value.

### MaxBank

The BUF08630 can provide the user with the number of times the nonvolatile memory of a particular DAC/$V_{COM}$ channel nonvolatile memory has been written to for the current memory bank. This information is provided by reading the register at pointer address 111111.

There are two ways to update the MaxBank register:

1. After initiating a single acquire command, the BUF08630 updates the MaxBank register with a code corresponding to how many times that particular channel memory has been written to.
2. Following a general acquire command, the BUF08630 updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1-8 and $V_{COM}$s) has been written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory has been programmed and the corresponding state of the MaxBank Register.

**Table 3. MaxBank Details**

| NUMBER OF TIMES WRITTEN TO | RETURNS CODE |
|---|---|
| 0 | 0000 |
| 1 | 0000 |
| 2 | 0001 |
| 3 | 0010 |
| 4 | 0011 |
| 5 | 0100 |
| 6 | 0101 |
| 7 | 0110 |
| 8 | 0111 |
| 9 | 1000 |
| 10 | 1001 |
| 11 | 1010 |
| 12 | 1011 |
| 13 | 1100 |
| 14 | 1101 |
| 15 | 1110 |
| 16 | 1111 |

### Parity Error Correction

The BUF08630 provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. If a single bit of nonvolatile memory for a channel fails, the BUF08630 corrects for it and updates the appropriate DAC with the intended value when its memory is acquired.

If more than one bit of nonvolatile memory for a channel fails, the BUF08630 does not correct for it, and updates the appropriate DAC/$V_{COM}$ with the default value of 1000000000.

## DIE_ID AND DIE_REV REGISTERS

The user can verify the presence of the BUF08630 in the system by reading from address 111101. The BUF08630 returns *0010000110110110* when read at this address.

The user can also determine the die revision of the BUF08630 by reading from register 111100. BUF08630 returns *0000000000000000* when a RevA die is present. RevB would be designated by *0000000000000001* and so on.

## READ/WRITE OPERATIONS

Read and write operations can be done for a single DAC/$V_{COM}$ or for multiple DAC/$V_{COM}$s. Writing to a DAC/$V_{COM}$ register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determines if data are written to the DAC/$V_{COM}$ register or the nonvolatile memory.

### Read/Write: DAC/$V_{COM}$ Register (volatile memory)

The BUF08630 is able to read from a single DAC/$V_{COM}$, or multiple DAC/$V_{COM}$s, or write to the register of a single DAC/$V_{COM}$ or multiple DAC/$V_{COM}$s in a single communication transaction. DAC pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). The $V_{COM}$ address is 010010.

Write commands are performed by setting the read/write bit low. Setting the read/write bit high performs a read transaction.

### Writing: DAC/$V_{COM}$ Register (Volatile Memory)

To write to a single DAC/$V_{COM}$ register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = low. The BUF08630 acknowledges this byte.
3. Send a DAC/$V_{COM}$ pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/$V_{COM}$ address. Although the BUF08630 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   - 000000 through 000111
   - 010010

   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/$V_{COM}$ addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF08630 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/$V_{COM}$ register is not the same as updating the DAC/$V_{COM}$ output voltage; see the *Updating the DAC Output Voltages* section.

The process of updating multiple DAC/$V_{COM}$ registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF08630 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/$V_{COM}$ registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = low. The BUF08630 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/$V_{COM}$ is the first in the sequence of DAC/$V_{COM}$s to be updated. The BUF08630 begins with this DAC/$V_{COM}$ and steps through subsequent DAC/$V_{COM}$s in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC/$V_{COM}$ addressed in the previous step. The DAC/$V_{COM}$ register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/$V_{COM}$. That DAC/$V_{COM}$ register is updated after receiving the fourth byte. This process continues until the registers of all following DAC/$V_{COM}$s have been updated. The BUF08630 accepts data for eight DACS, $V_{COM}$ voltage, gain set, $V_{COM}$ high limit, and $V_{COM}$ low limit. Note that between these addresses, there are some unused addresses that must be skipped. For more details, see Table 4. The write disable bit cannot be accessed using this method. It must be written to using *the write to a single DAC register* procedure.
5. Send a STOP or START condition on the bus.

The BUF08630 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

### Reading: DAC/$V_{COM}$/OTHER Register (Volatile Memory)

Reading a register returns the data stored in that DAC/$V_{COM}$/OTHER register.

To read a single DAC/$V_{COM}$/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = low. The BUF08630 acknowledges this byte.
3. Send the DAC/$V_{COM}$/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC/$V_{COM}$/OTHER address. NOTE: The BUF08630 stores and returns data only from these addresses:
   - 000000 through 000111
   - 010010
   - 111100 through 111111

   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for valid DAC/$V_{COM}$/OTHER addresses.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = high. The BUF08630 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC/$V_{COM}$ channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = low. The BUF08630 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DAC/$V_{COM}$s to be read. The BUF08630 begins with this DAC/$V_{COM}$ and steps through subsequent DAC/$V_{COM}$s in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = high. The BUF08630 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/$V_{COM}$. The first received byte is the most significant byte (bits D15–D8; only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers DieID, DieRev, and MaxBank is not supported in this mode of operation (these values must be read using the single register read method).

### Write: Nonvolatile Memory for the DAC Register

The BUF08630 is able to write to the nonvolatile memory of a single DAC/$V_{COM}$ in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC/$V_{COM}$ pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). The $V_{COM}$ address is 010010.

When programming the nonvolatile memory, the analog supply voltage must be between 9 V and 20 V. Write commands are performed by setting the read/write bit low.

To write to a single nonvolatile register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = low. The BUF08630 acknowledges this byte. Although the BUF08630 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   It returns *0000* for reads from 001000 through 010001, and 010011 through 010111. See Table 4 for DAC/$V_{COM}$ addresses.
3. Send a DAC/$V_{COM}$ pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/$V_{COM}$ address.
4. Send two bytes of data for the nonvolatile register of the specified DAC/$V_{COM}$. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF08630 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC/$V_{COM}$ register and output voltage.

The DAC/$V_{COM}$ register and DAC/$V_{COM}$ output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250µs. Once a nonvolatile register write command has been issued, no communication with the BUF08630 should take place for at least 250 µs. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

### Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC/$V_{COM}$ channel, the master must first issue a general acquire command, or a single acquire command with the appropriate DAC/$V_{COM}$ channel chosen. This action updates both the DAC/$V_{COM}$ register(s) and DAC/$V_{COM}$ output voltage(s). The master may then read from the appropriate DAC/$V_{COM}$ register as described earlier.

## PROGRAMMABLE $V_{COM}$ LIMITS

The BUF08630 $V_{COM}$ output has a programmable high limit and low limit. The implementation and interface of these limits are the same as with the DAC registers. These registers are written to and read back through the two-wire bus. Addresses for limiters are 1E and 1F for the high limit and low limit, respectively. See Table 4 for register pointer addresses.

Upon power-up or general-call reset, the DAC registers for $V_{COM}$ are set to 200 (default) that corresponds to mid-scale output for a 10-bit DAC. The high and low limit registers are set to 3FF and 000 respectively. Therefore, the limits are transparent if not programmed. Reset typically requires approximately 1ms.

The BUF08630 uses double-buffered registers. The input of data is stored in the first layer. The input may be latched to the DAC output, depending upon application. The DACs update only when the second layer of latches are enabled.

The high and low limits can be programmed to any desired value to limit the $V_{COM}$ output. The limit can be programmed before or after programming the $V_{COM}$ channel. Because the input of data is stored in the first layer of latches, the $V_{COM}$ output is limited according to the following rule in either sequence:

1. If the $V_{COM}$ OTP write is enabled, then the $V_{COM}$ input is always stored in the OTP. Limit comparison happens only before the DAC output.
2. If the $V_{COM}$ input is higher than the high limit, then the high limit is latched to the DAC output. Reading of the DAC register returns the high limit.
3. If the $V_{COM}$ input is lower than the low limit, then the low limit is latched to the DAC output. Reading of the DAC register returns the low limit.
4. If the $V_{COM}$ input is in between the high and low limit, then the programmed value is latched to DAC output. Reading of the DAC register returns the programmed value.
5. If the high limit is lower than the low limit, then the BUF08630 ignores the limits and latches the programmed value to the DAC output. Reading of the DAC register returns the programmed value.

There are two banks of OTP associated with each of the two limit registers. OTP operations on these two addresses are valid, just like OTP for DAC registers.

## Table 4. Register Pointer Addresses

| COMMENT | POINTER ADDRESS | REGISTER FUNCTION | READ/WRITE PERMISSION |
|---|---|---|---|
| Add control MSBs M1 and M0 (see Table 5) | 000000 | Channel 1 address | R/W |
| | 000001 | Channel 2 address | R/W |
| | 000010 | Channel 3 address | R/W |
| | 000011 | Channel 4 address | R/W |
| | 000100 | Channel 5 address | R/W |
| | 000101 | Channel 6 address | R/W |
| | 000110 | Channel 7 address | R/W |
| | 000111 | Channel 8 address | R/W |
| | 001000 | Reserved | R/W |
| | 001001 | Reserved | R/W |
| | 001010 | Reserved | R/W |
| | 001011 | Reserved | R/W |
| | 001100 | Reserved | R/W |
| | 001101 | Reserved | R/W |
| | 001110 | Reserved | R/W |
| | 001111 | Reserved | R/W |
| | 010000 | Reserved | R/W |
| | 010001 | Reserved | R/W |
| | 010010 | $V_{COM}$ address | R/W |
| | 010011 | Reserved | R/W |
| | 010100 | Reserved | R/W |
| | 010101 | Reserved | R/W |
| | 010110 | Reserved | R/W |
| | 010111 | Reserved | R/W |
| | 011000 | Reserved | R/W |
| | 011001 | Reserved | R/W |
| | 011010 | Reserved | R/W |
| | 011011 | Reserved | R/W |
| | 011100 | Gain set | R/W |
| | 011101 | Reserved | R/W |
| | 011110 | $V_{COM}$ high limit | R/W |
| | 011111 | $V_{COM}$ low limit | R/W |
| | 100000 | Reserved | R/W |
| These special addresses are only valid in this exact format | 00111100 | Die revision | Read only |
| | 00111101 | Die ID | Read only |
| | 00111111 | MaxBank | Read only |
| | 00111110 | Memory raw data | Read only |

## Table 5. Control Bits M1 and M0

| M0 | M1 | OPERATION |
|---|---|---|
| 0 | 0 | Write to DAC register if Write command is received. Read DAC Register if Read command is received. |
| 0 | 1 | Single acquire nonvolatile memory pointed to by the current register address. |
| 1 | 0 | General acquire nonvolatile memory for all DAC registers. |
| 1 | 1 | Not allowed. |

## ADJUSTABLE GAIN $V_{COM}$

The VCOM channel has eight internal, adjustable gain configurations that are selectable through the $I^2C$ bus, as shown in Table 6. The selectable gains include buffer gains of 1, 2, 3, 4, 5, and 6; a buffer configuration; and an external user-defined, gain-select configuration, as shown in Table 7. The internal configuration uses the topology depicted in Figure 25 to achieve the different gain selections that are selected by setting internal switches 1 through 8.

**Table 6. $V_{COM}$ Gain Set Register Description**

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | NUMBER OF BITS | VOLATILE MEMORY WRITE TIMES | POWER-ON RESET VALUE | NONVOLATILE MEMORY WRITE TIMES |
|---|---|---|---|---|---|---|
| 1Ch | VcomGain | Set $V_{COM}$ gain | 8 | Unlimited | 1 (1) | 16 |

(1) Power-on reset requires 1.2ms.

**Table 7. $V_{COM}$ Gain Set Register (Address = 1Ch)**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | GAIN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | –1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | –2 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | –3 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | –4 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | –5 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | –6 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Set by external resistor |

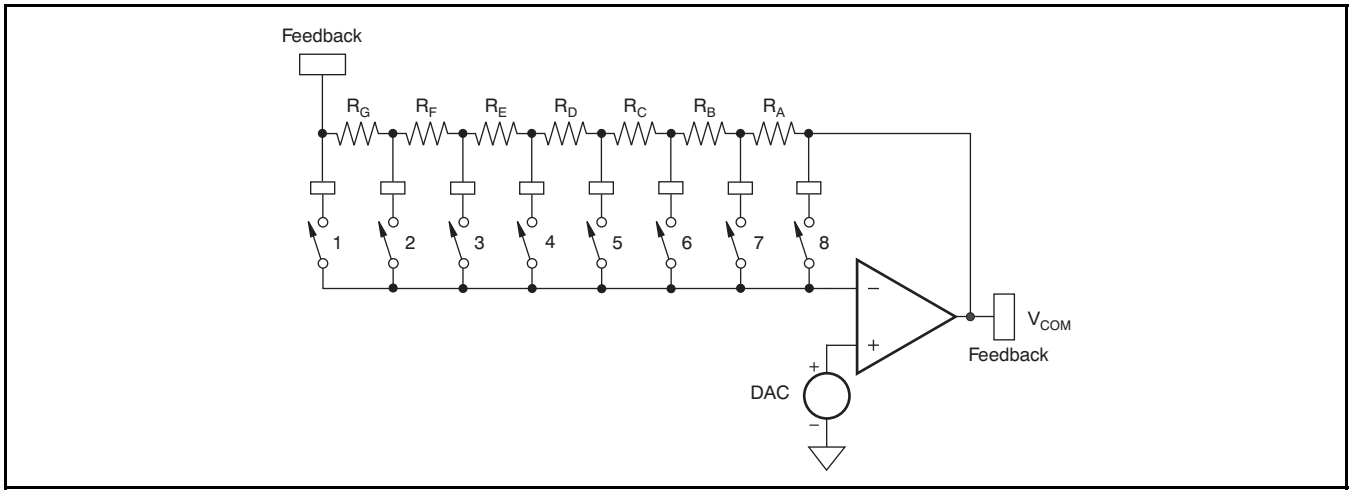



**Figure 25. Feedback Configuration Topology**

Table 8 lists the approximate values (±15%) of the internal resistors in the feedback configuration depicted in Figure 25, for a total resistive value of approximately 13 kΩ (±15%).

**Table 8. Feedback Resistor Values**

| RESISTOR | TYPICAL VALUE(1) (Ω) |
|---|---|
| $R_A$ | 6502.5 |
| $R_B$ | 2165 |
| $R_C$ | 1083 |
| $R_D$ | 651.25 |
| $R_E$ | 432.5 |
| $R_F$ | 310.625 |
| $R_G$ | 1858.75 |

(1) All values are ±15%.

For switch positions 2, 3, 4, 5, 6, and 7, the buffer is configured in an internal inverting gain, as shown in Figure 26.

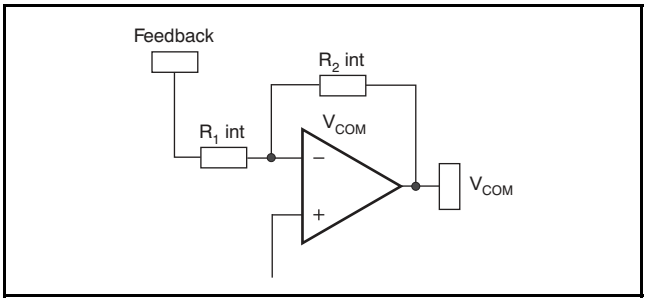



**Figure 26. Configuration for Switch Positions 2, 3, 4, 5, 6, 7**

**Table 9. Gain Select Resistor Ratio (±15%)**

| GAIN | VALUE OF $R_2$ BASED ON SWITCH POSITIONS | VALUE OF $R_1$ BASED ON SWITCH POSITIONS |
|---|---|---|
| G = 1 | 6502 Ω | 6501 Ω |
| G = 2 | 8667 Ω | 4336 Ω |
| G = 3 | 9750 Ω | 3253 Ω |
| G = 4 | 10401 Ω | 2601 Ω |
| G = 5 | 10834 Ω | 2169 Ω |
| G = 6 | 11144 Ω | 1858 Ω |

Table 10 shows the theoretical gain values of the inverting configuration using the internal resistors, ±15%.

**Table 10. Gain Equation**

| GAIN | RATIO | TYPICAL VALUE |
|---|---|---|
| G = 1 | $-R_2/R_1$ | –1.00021 |
| G = 2 | $-R_2/R_1$ | –1.9989 |
| G = 3 | $-R_2/R_1$ | –2.99727 |
| G = 4 | $-R_2/R_1$ | –3.99779 |
| G = 5 | $-R_2/R_1$ | –4.99418 |
| G = 6 | $-R_2/R_1$ | –5.9959 |

A buffer configuration is achieved using switch position 8 as indicated in Figure 27

An external user-selectable gain configuration is achieved using switch position 1, as indicated in Figure 28. By using a single external gain resistor value and the internal values of the resistor string, a wide range of selectable gains can be achieved using the internal switch configuration.

Table 11 shows the possible gains that can be achieved with a single 1-kΩ external resistor for each of the internal switch selections.

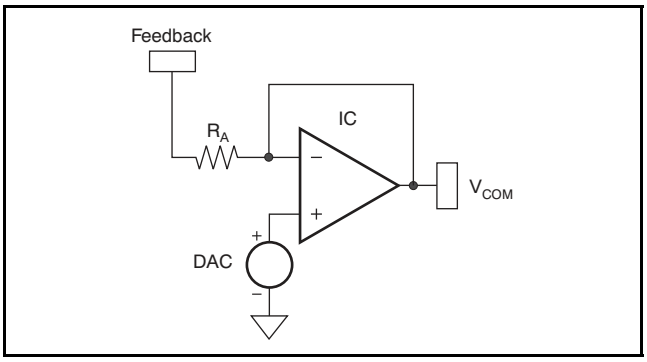



**Figure 27. Configuration for Switch Position 8**

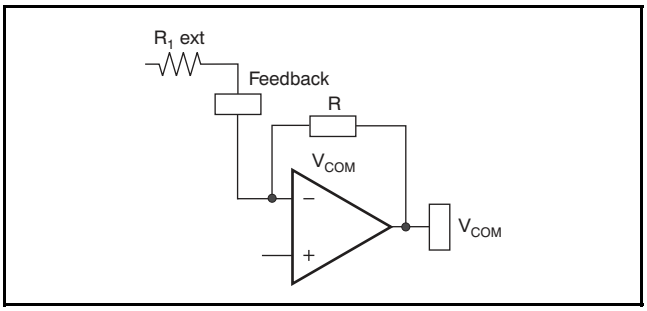



**Figure 28. Configuration for Switch Position 1**

**Table 11. Possible Gains Using a 1-kΩ External Resistor**

| EXTERNAL RESISTANCE | INTERNAL RESISTANCE | GAIN | SWITCH POSITION |
|---|---|---|---|
| $R_1$ ext = 1000 Ω | R = 13003.63 Ω | –13.0036 | 1 |
| $R_1$ ext + $R_{INT}$ = 2858.75 Ω | R = 11144.88 Ω | –3.89851 | 2 |
| $R_1$ ext + $R_{INT}$ = 3169.375 Ω | R = 10834.25 Ω | –3.41842 | 3 |
| $R_1$ ext + $R_{INT}$ = 3601.875 Ω | R = 10401.75 Ω | –2.88787 | 4 |
| $R_1$ ext + $R_{INT}$ = 4253.125 Ω | R = 9750.5 Ω | –2.29255 | 5 |
| $R_1$ ext + $R_{INT}$ = 5336.125 Ω | R = 8667.5 Ω | –1.62431 | 6 |
| $R_1$ ext + $R_{INT}$ = 7501.125 Ω | R = 6502.5 Ω | –0.86687 | 7 |

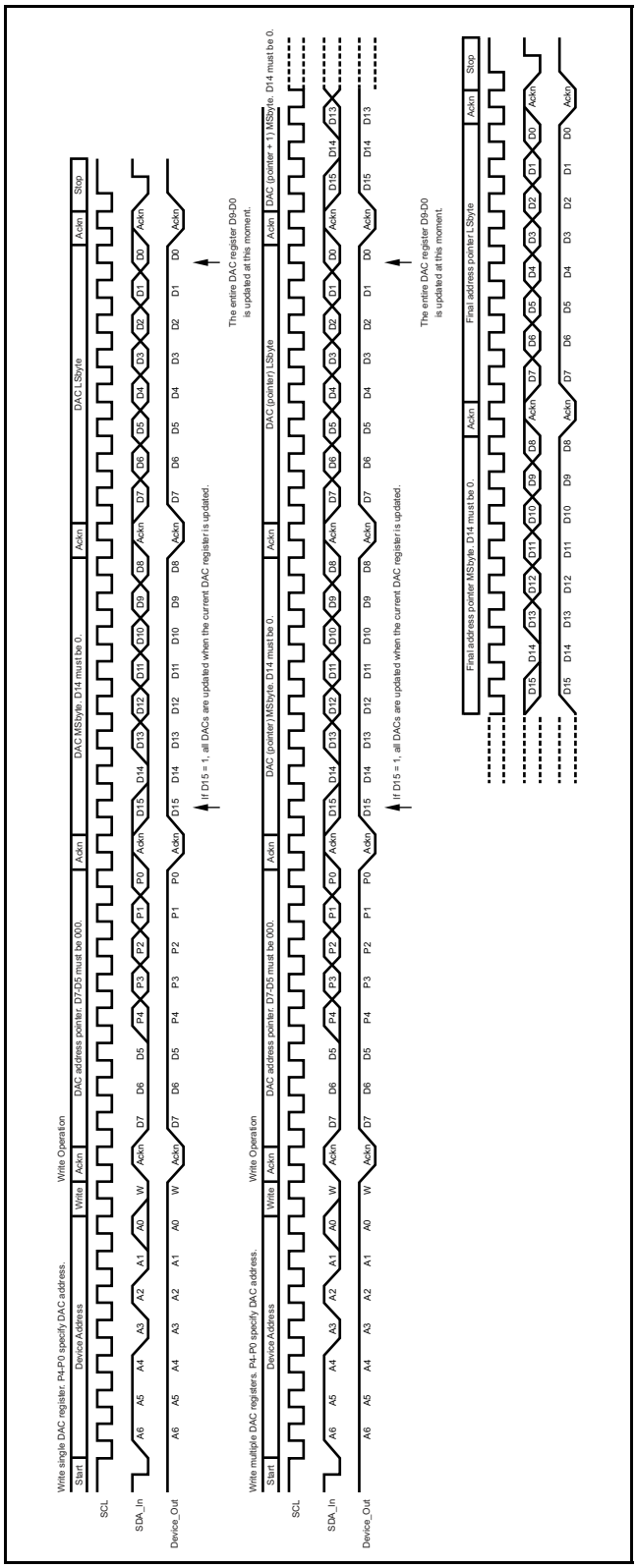



**Figure 29. Write DAC Register Timing**

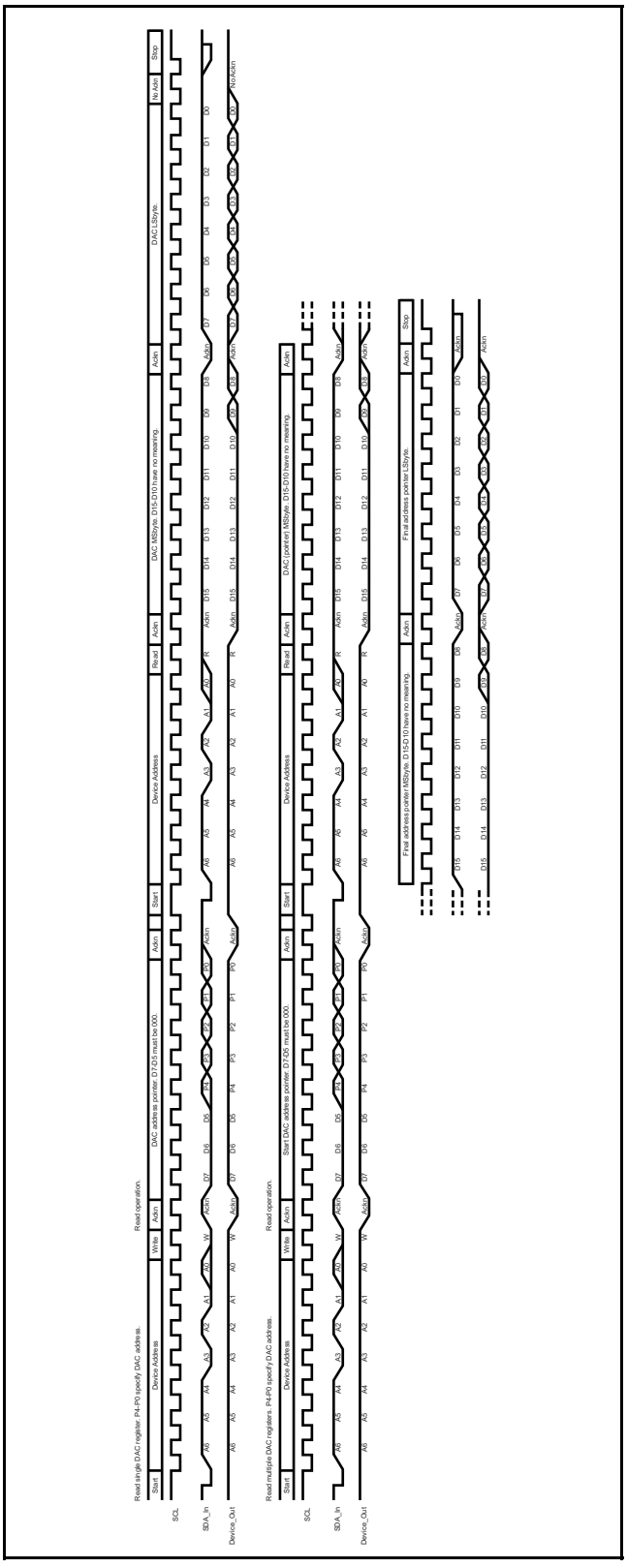



**Figure 30. Read Register Timing**

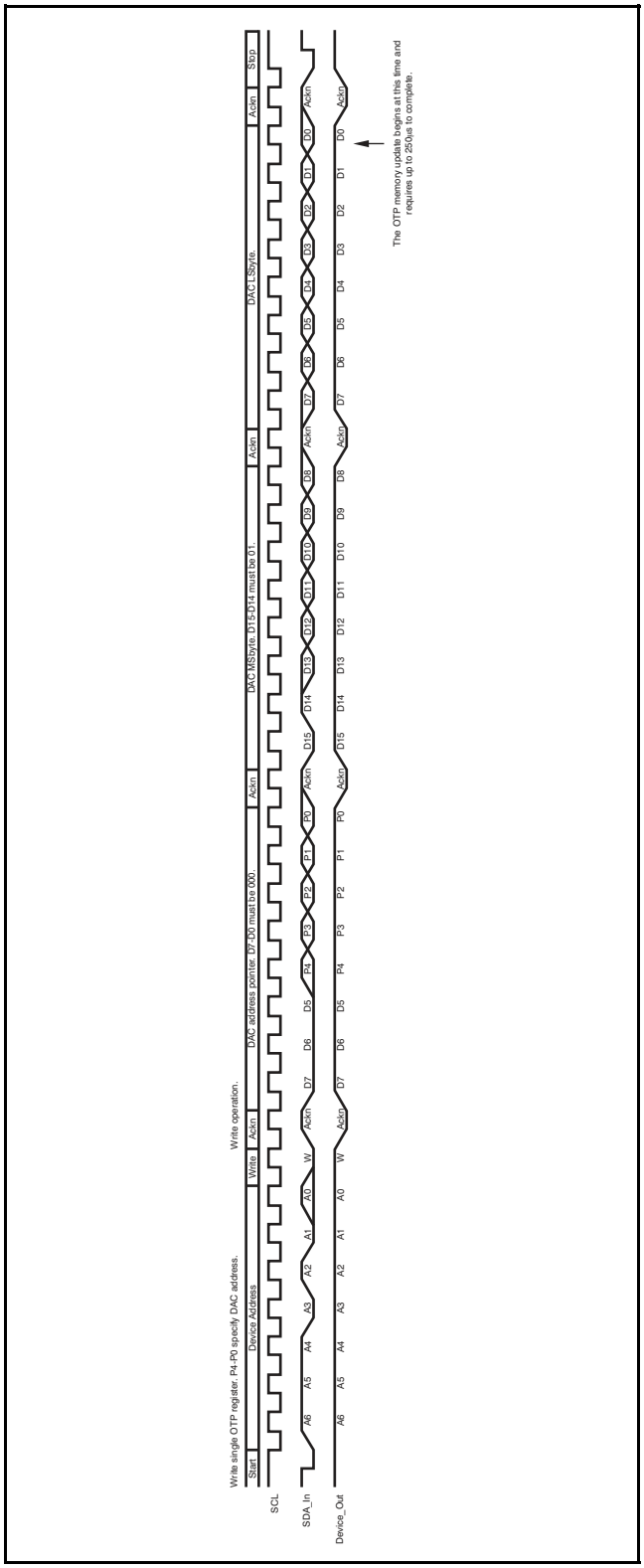



**Figure 31. Write Nonvolatile Register Timing**

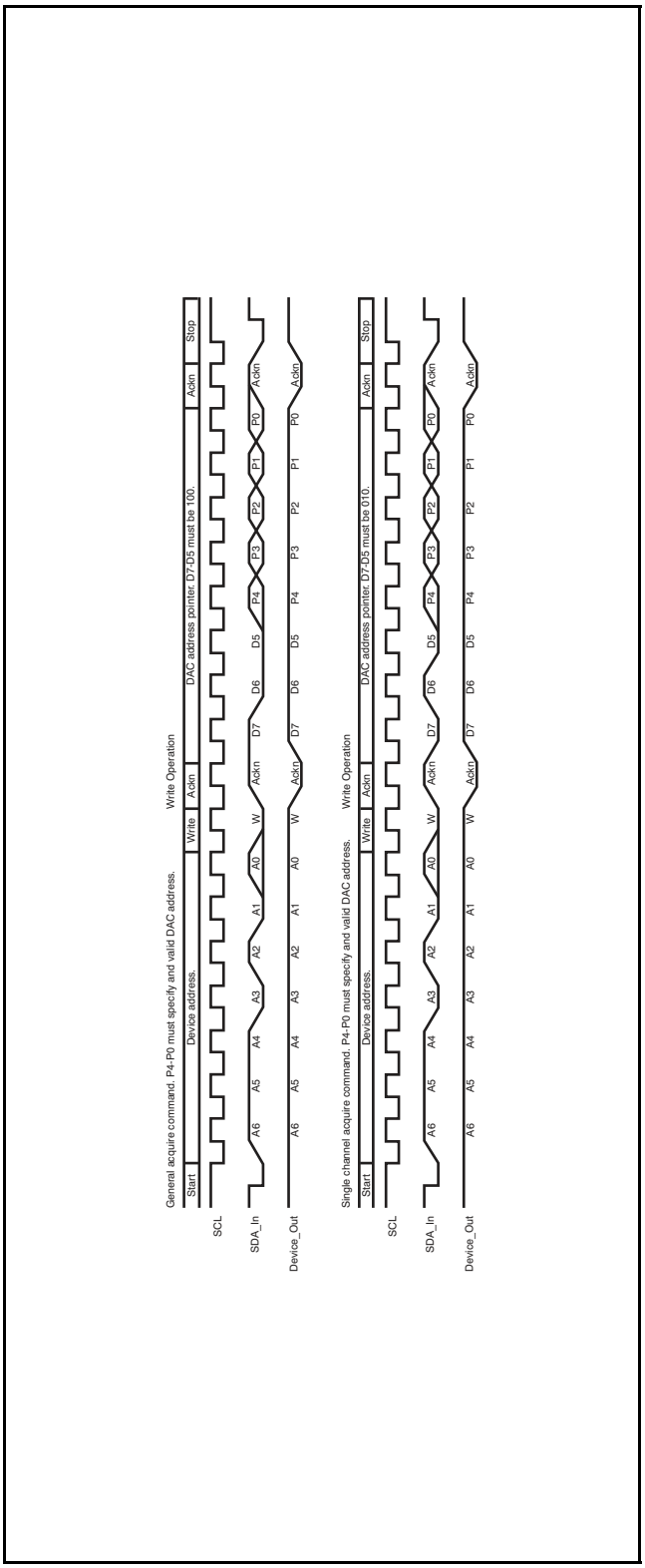



**Figure 32. Acquire Operation Timing**

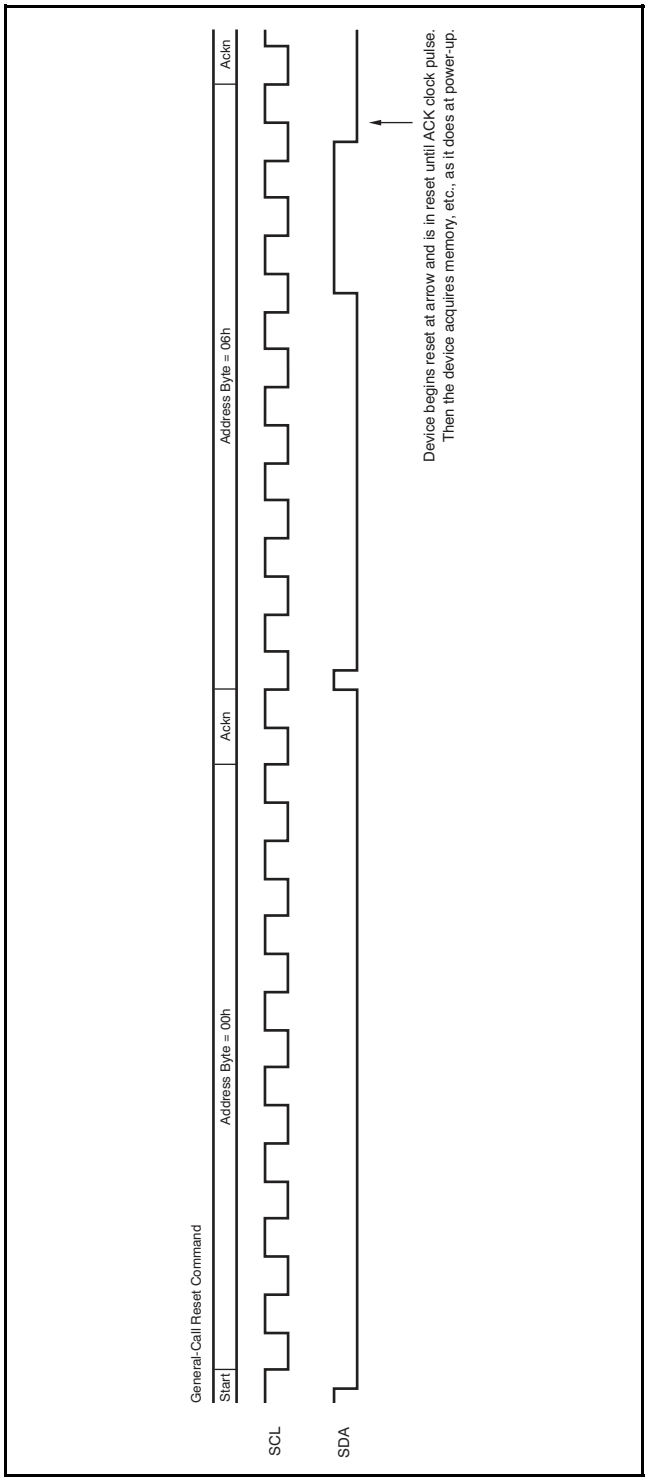



**Figure 33. General-Call Reset Timing**

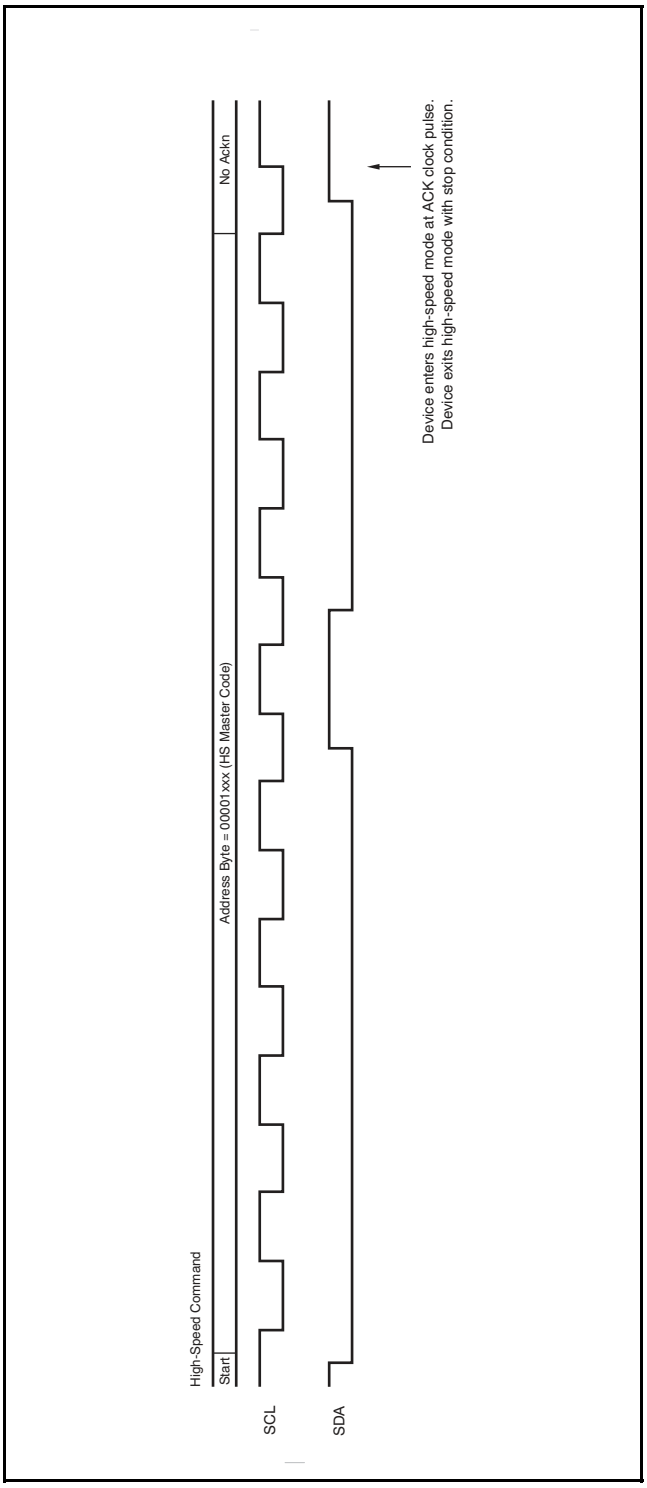



**Figure 34. High-Speed Mode Timing**

## END-USER SELECTED GAMMA CONTROL

Because the BUF08630 has two banks of nonvolatile memory, it is well-suited for providing two levels of gamma control by using the BKSEL pin, as shown in Figure 35. When the state of the BKSEL pin changes, the BUF08630 updates all nine programmable buffer outputs simultaneously after 10 µs, typical.

To update all nine programmable output voltages simultaneously via hardware, toggle the BKSEL pin to switch between Gamma Curve 0 (stored in Bank0) and Gamma Curve 1 (stored in Bank1).

All DAC/$V_{COM}$ registers and output voltages are updated simultaneously after approximately 10 µs, typical.

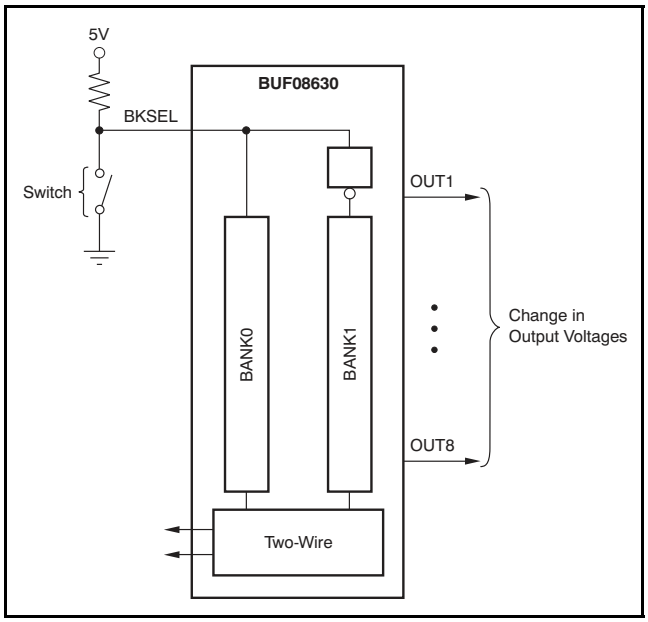



**Figure 35. Gamma Control**

## DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. Using the BKSEL pin to switch between two gamma curves does not often provide good results because of the 750 µs required to transfer the data from the nonvolatile memory to the DAC register. However, dynamic gamma control can still be accomplished by storing two gamma curves in an external EEPROM and writing directly to the DAC register (volatile).

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC/$V_{COM}$ output values remain unchanged—the display is unaffected. At the beginning or the end of a picture frame, the DAC/$V_{COM}$ outputs (and therefore, the gamma voltages) can be quickly updated by writing a '1' in bit 15 of any DAC/$V_{COM}$ register. For details on the operation of the double register input structure, see the *Updating the DAC Output Voltages* section.

To update all nine programmable output voltages simultaneously via software, perform the following actions:

**STEP 1:** Write to registers 1–9 with bit 15 always '0'.

**STEP 2:** Write any DAC/$V_{COM}$ register a second time with identical data. Make sure that bit 15 is set to '1'. All DAC/$V_{COM}$ channels are updated simultaneously after receiving the last bit of data.

## OUTPUT PROTECTION

The BUF08630 output stages can safely source and sink the current levels indicated in Figure 1 and Figure 2. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT8, and $V_{COM}$) include ESD protection diodes, as shown in Figure 36. Normally, these diodes do not conduct and are passive during typical device operation. However, unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds ($V_S$) + 0.5 V, or drops below GND – 0.5 V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF08630 power-supply source ($V_S$) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing a Schottky diode as shown in Figure 36. This diode must be capable of discharging the capacitor without allowing more than 0.5V to develop across the internal ESD current sterring diodes.

**CAUTION**

Do not connect large capacitors to the output of the gamma buffers without connecting a Schottky diode. Otherwise, the device will be damaged.

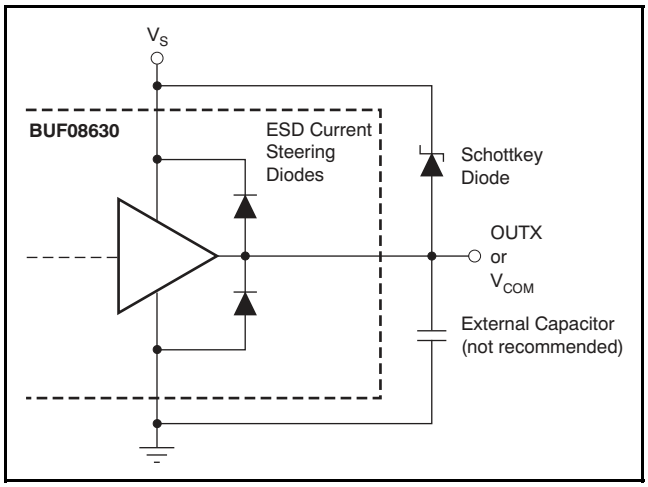


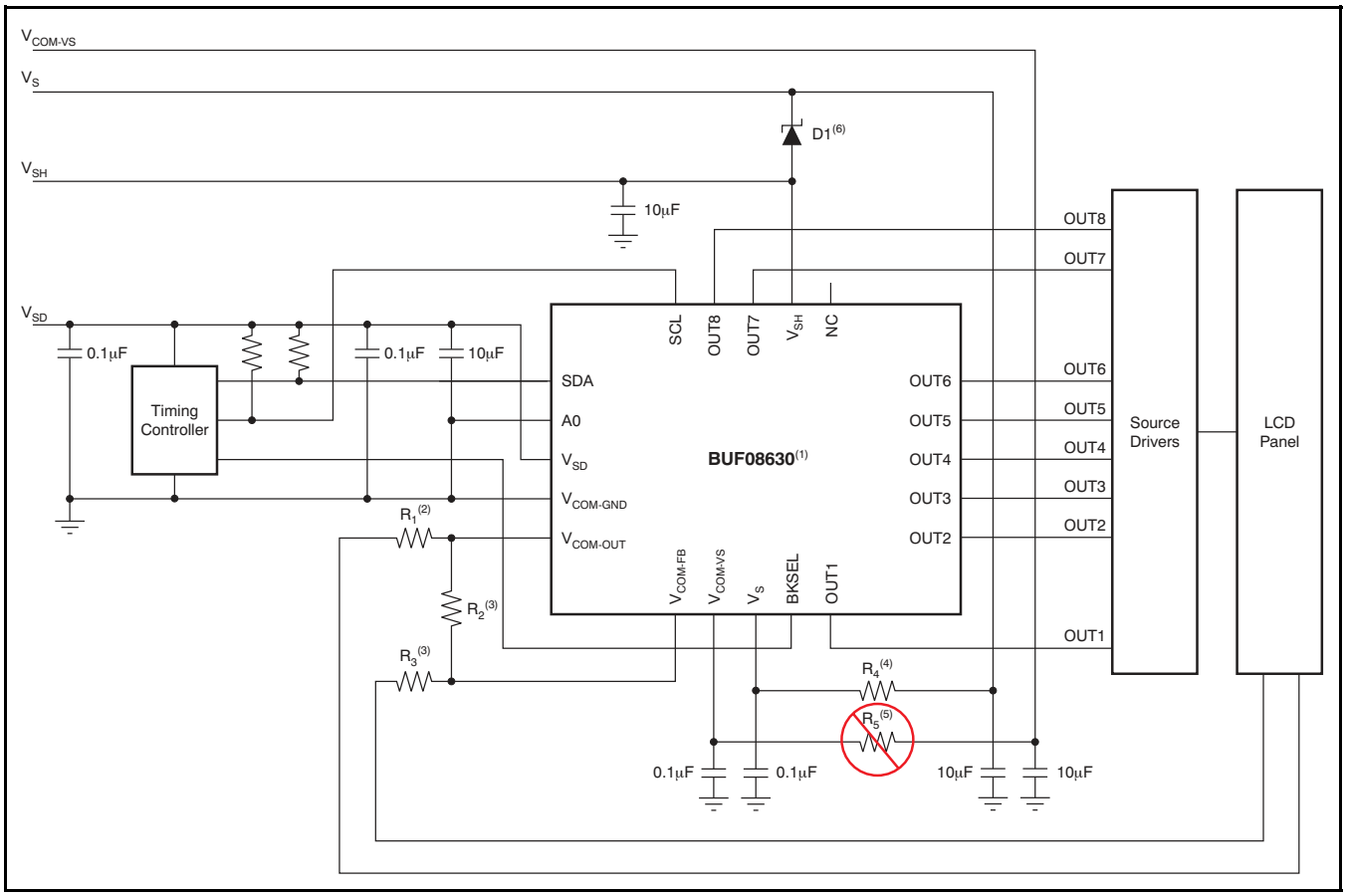

**Figure 36. Output Pins ESD Protection Current-Steering Diodes**

## APPLICATION INFORMATION

Figure 37 shows a typical application circuit.

## GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF08630 is available in a thermally-enhanced PowerPAD package. The exposed thermal die must be soldered to the PCB using thermal vias. Refer to Texas Instruments' application report SLAU271, *QFN/SON PCB Attachment*.




(1) Exposed thermal pad must be connected to GND.

(2) $R_1$ should be chosen for best stability.

(3) $R_2$ and $R_3$ are not needed if internal gain is used.

(4) $R_4$ must not exceed 10 Ω.

(5) $R_5$ must never be used. $V_{COM}$ can provide up to 400mA. A 10-Ω resistor would cause a 4V drop to the device.

(6) D1 should be used if there is any possibility of $V_{SH}$ exceeding $V_S$.

**Figure 37. Typical Application Circuit**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (October 2010) to Revision A | Page |
|---|---|
| • Changed data sheet associated to BUF08630 device from 1-page (SBOS535) to this full PDF | 1 |
| • Updated step 4 in the *To write to multiple DAC/$V_{COM}$ registers* subsection | 16 |
| • Updated Table 4 | 19 |
| • Changed Figure 29 | 23 |
| • Changed Figure 30 | 23 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BUF08630RGWR | ACTIVE | VQFN | RGW | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 95 | BUF 08630 | Samples |
| BUF08630RGWT | ACTIVE | VQFN | RGW | 20 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 95 | BUF 08630 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

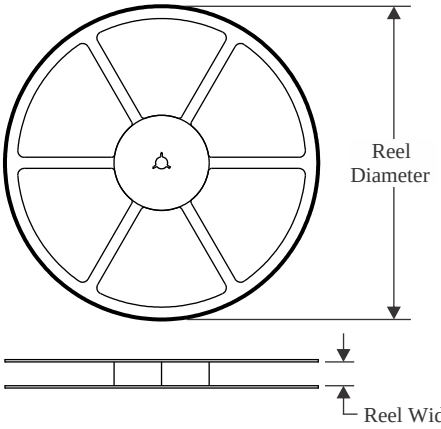
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

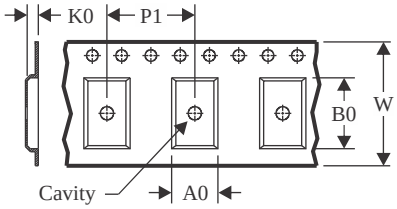
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

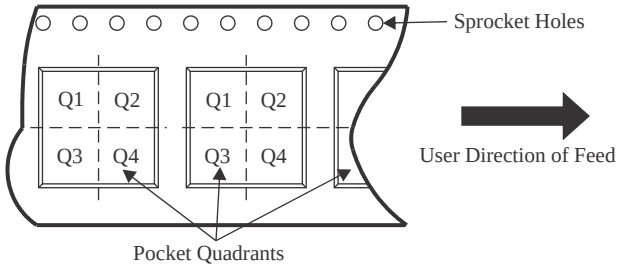



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

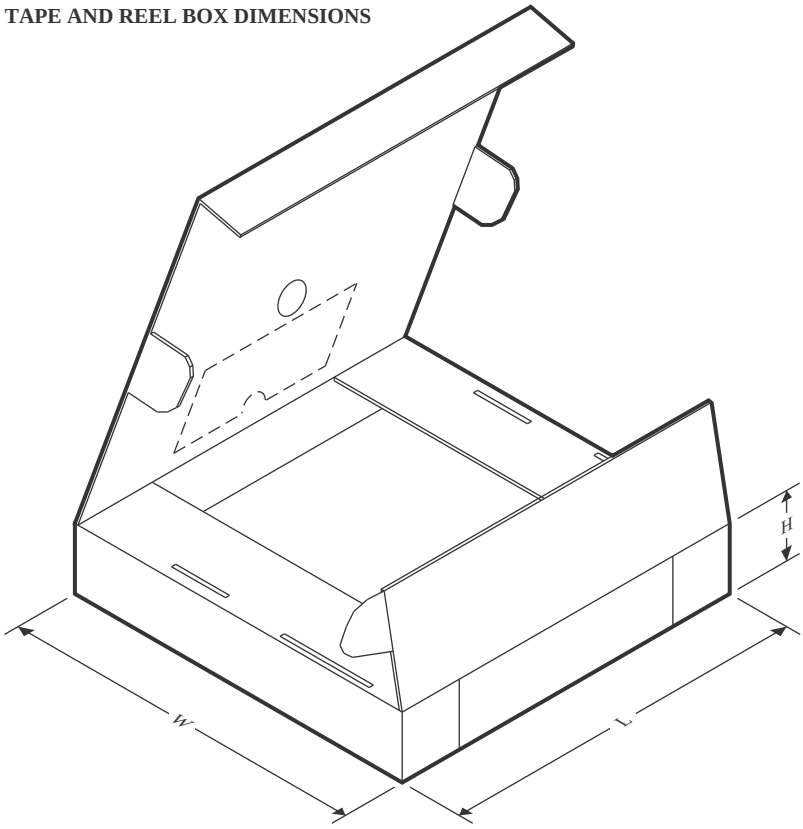
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BUF08630RGWR | VQFN | RGW | 20 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BUF08630RGWT | VQFN | RGW | 20 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BUF08630RGWR | VQFN | RGW | 20 | 3000 | 346.0 | 346.0 | 33.0 |
| BUF08630RGWT | VQFN | RGW | 20 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

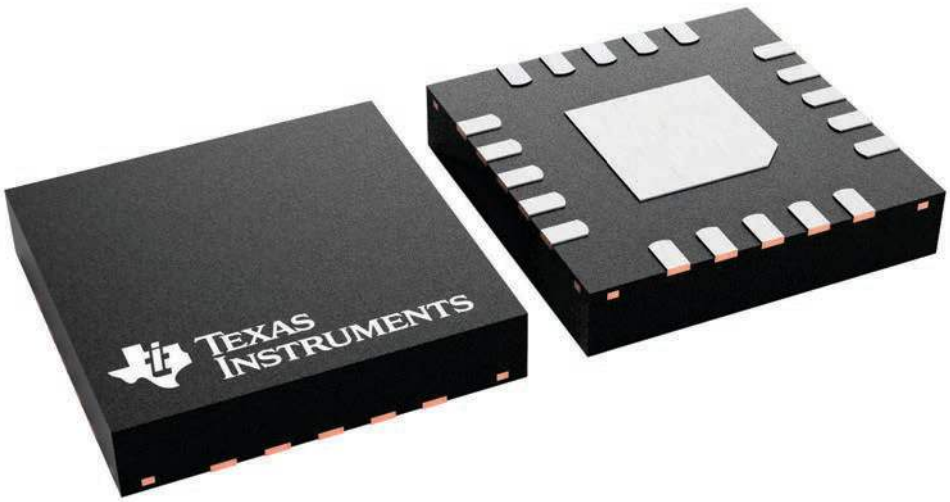
## RGW 20

## VQFN - 1 mm max height

**5 x 5, 0.65 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



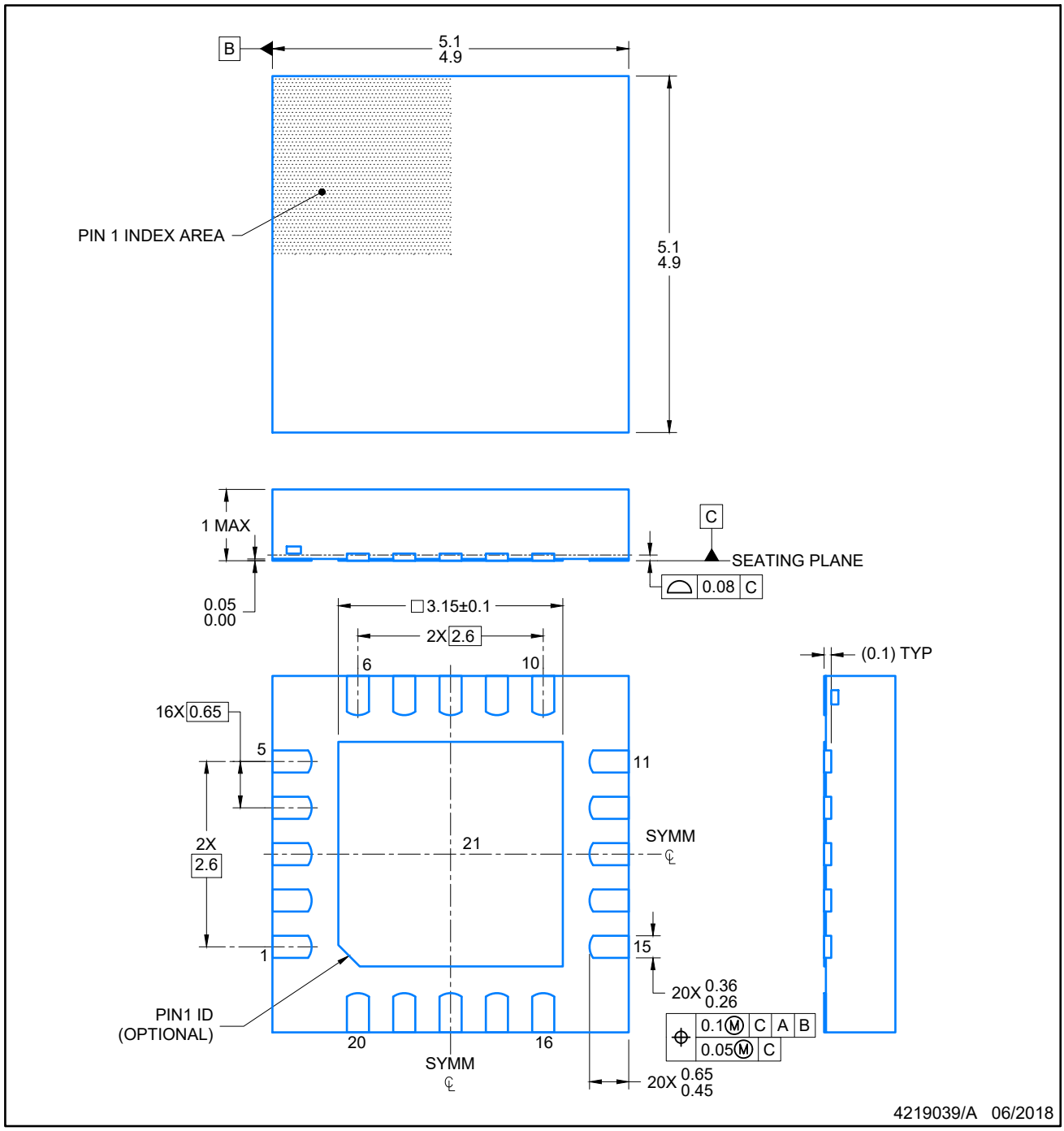

4227157/A

# PACKAGE OUTLINE

## RGW0020A

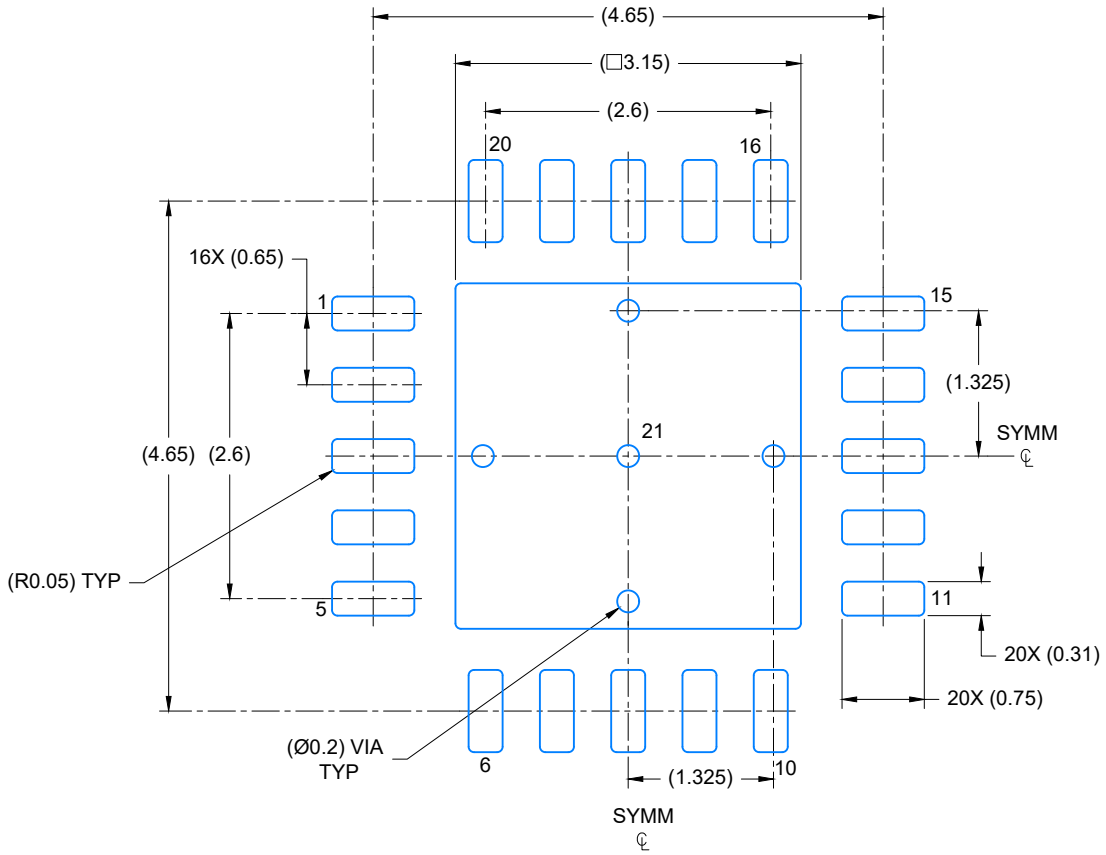
### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



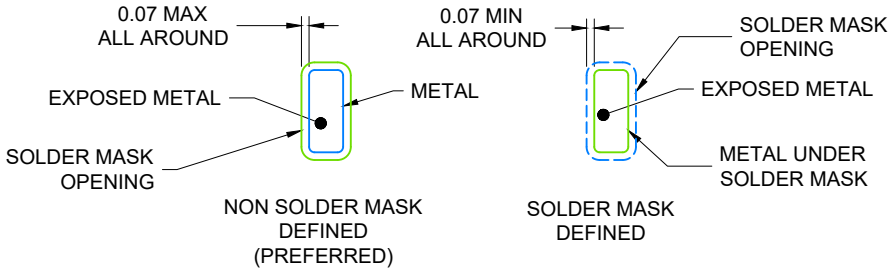

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE

SCALE: 15X

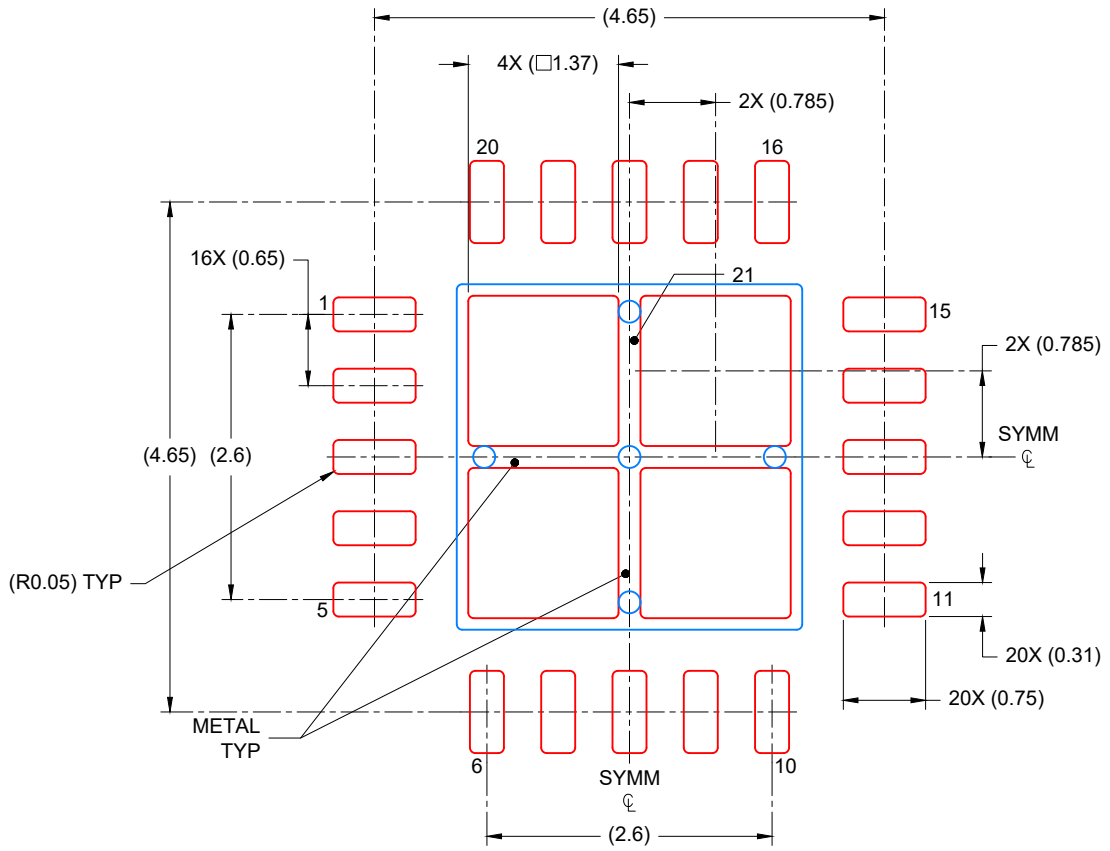



SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265