MOSFET

StrongIRFET™

Features

- Very low $R_{DS(on)}$
- High current carrying capability
- 175°C operating temperature
- Optimized for broadest availability from distribution partners

Benefits

- Reduced conduction losses
- Increased power density
- Increased reliability versus 150°C rated parts
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

D^2-PAK 7pin

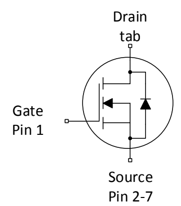


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),typ}$	0.95	mΩ
$R_{DS(on),max}$	1.3	mΩ
$I_{D(Silicon\ Limited)}$	363	A
$I_{D(Package\ Limited)}$	360	A
Q_G(0V..10V)	311	nC

Type / Ordering Code	Package	Marking	Related Links
IRF60SC241	PG-TO263-7	IRF60SC241	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	360 363 256	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=25 °C (silicon limited) V_{GS}=10 V, T_C=100 °C[1]
Pulsed drain current[1]	$I_{D,pulse}$	-	-	1440	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	799	mJ	I_D=100 A, R_{GS}=50 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	417 2.4	W	T_C=25 °C T_A=25 °C, R_{THJA}=62 °C/W[3]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, 0[4]	R_{thJC}	-	-	0.36	°C/W	-
Thermal resistance, junction -Ambient, 0	R_{thJA}	-	-	62	°C/W	-
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.5	-	°C/W	-

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] When mounted on 1″ square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994:
[4] R_{thJC} is measured at T_J approximately 90°C.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=250 uA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	43	-	mV/°C	I_D=5 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	2.2	-	3.7	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 150	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.945 1.2	1.30 -	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=50 A
Gate resistance[1]	R_G	-	2.3	-	Ω	-
Transconductance	g_{fs}	-	340	-	S	$\|V_{DS}\| \geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	16000	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	1600	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	1000	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Rise time	t_r	-	59	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Turn-off delay time	$t_{d(off)}$	-	227	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Fall time	t_f	-	88	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=2.7 Ω

[1] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	79	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	48	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge[2]	Q_{gd}	-	95	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	126	-	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[2]	Q_g	-	311	388	nC	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	216	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	77	-	nC	V_{DD}=30 V, V_{GS}=0 V

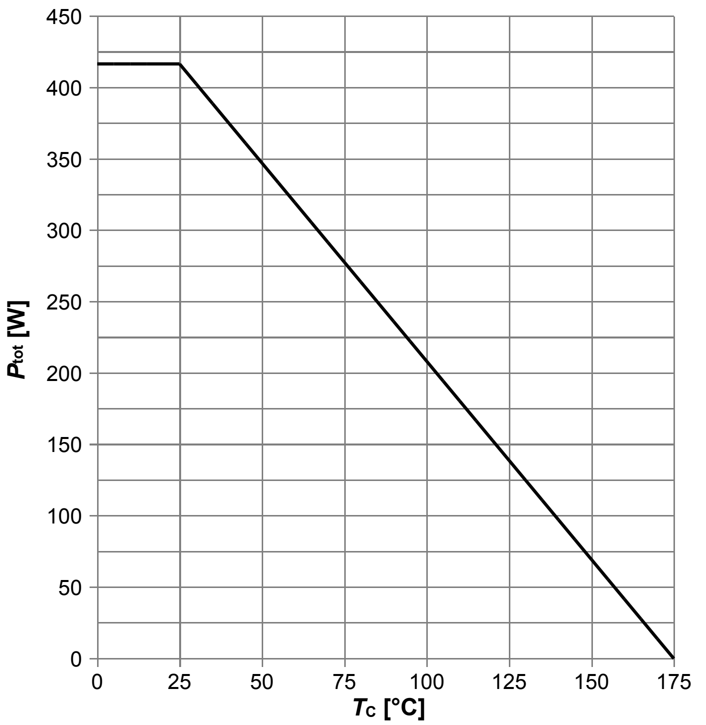
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	347	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1440	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.86	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[2]	t_{rr}	-	43	-	ns	V_R=51 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge[2]	Q_{rr}	-	58	-	nC	V_R=51 V, I_F=100 A, di_F/dt=100 A/µs

[1] See "Gate charge waveforms" for parameter definition
[2] Defined by design. Not subject to production test.

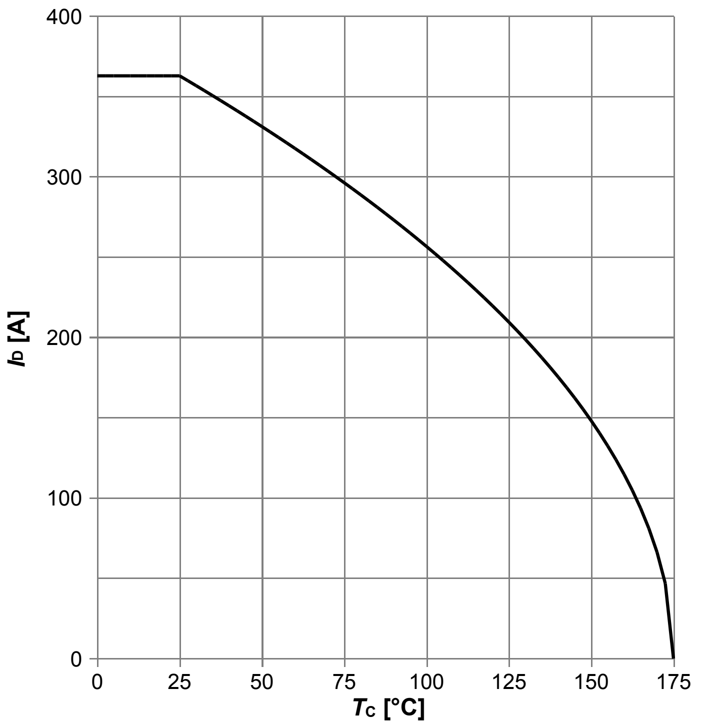
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



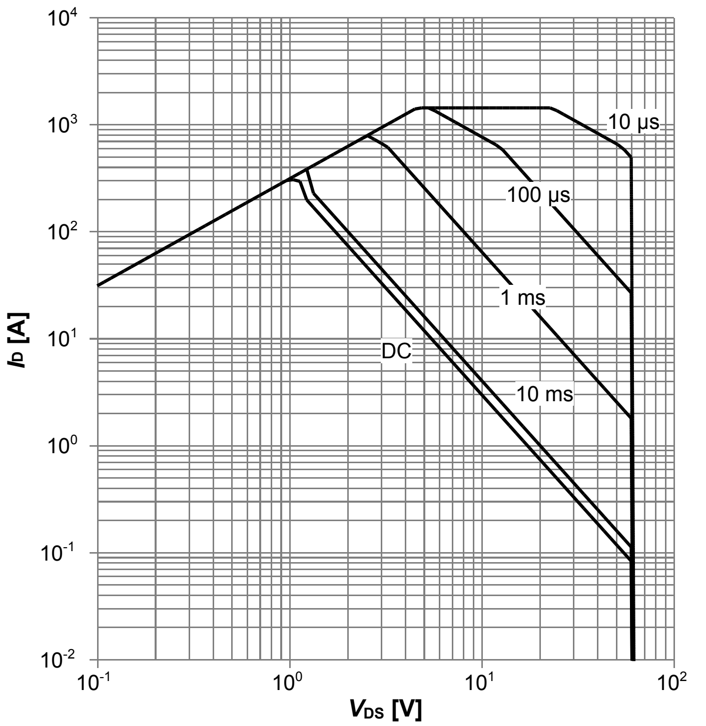
P_{tot}=f(T_C)

Diagram 2: Drain current



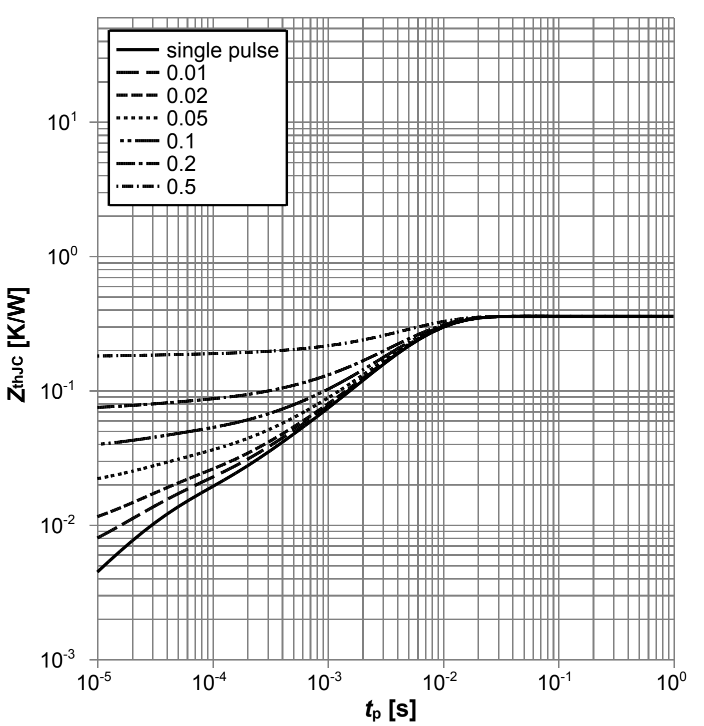
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

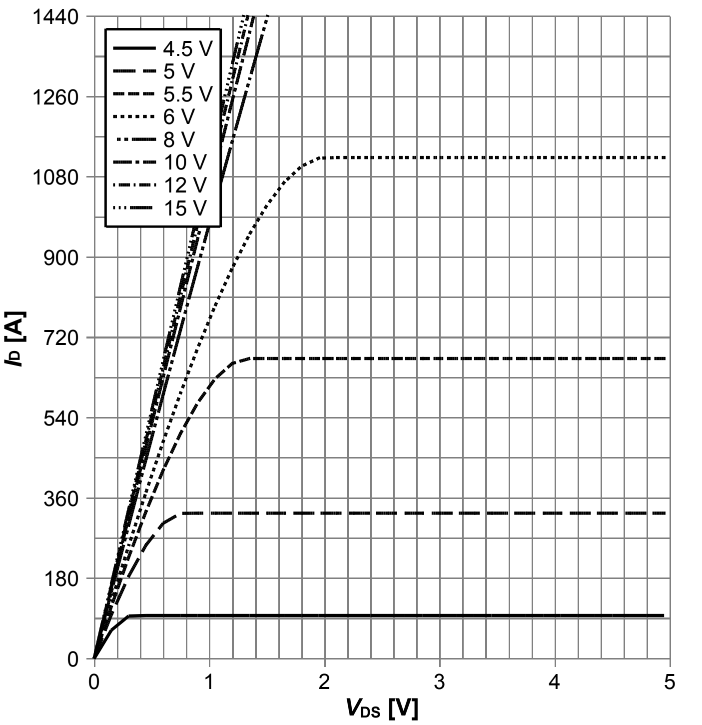
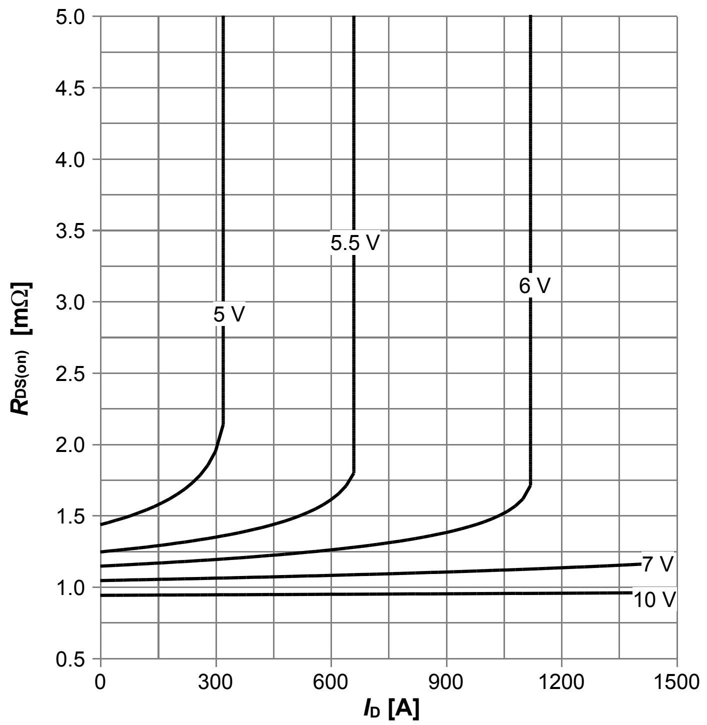
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

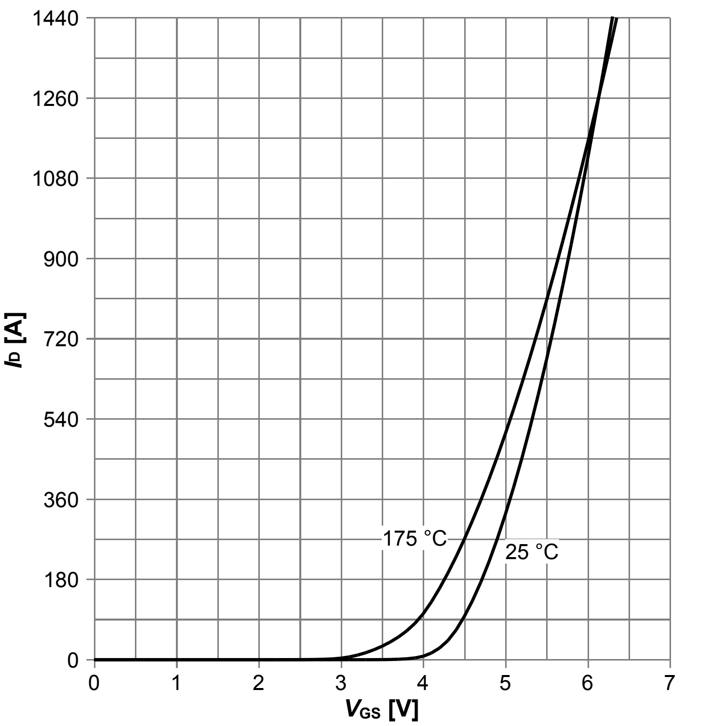
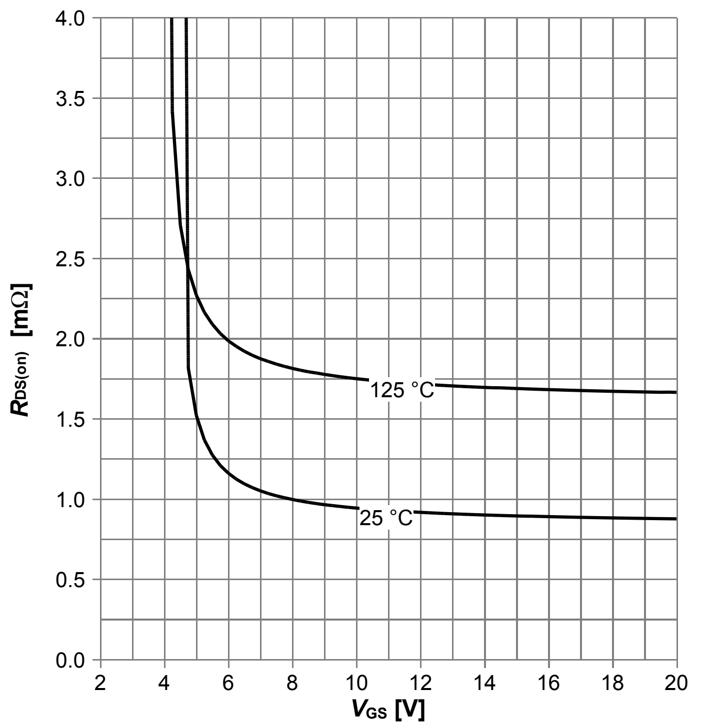
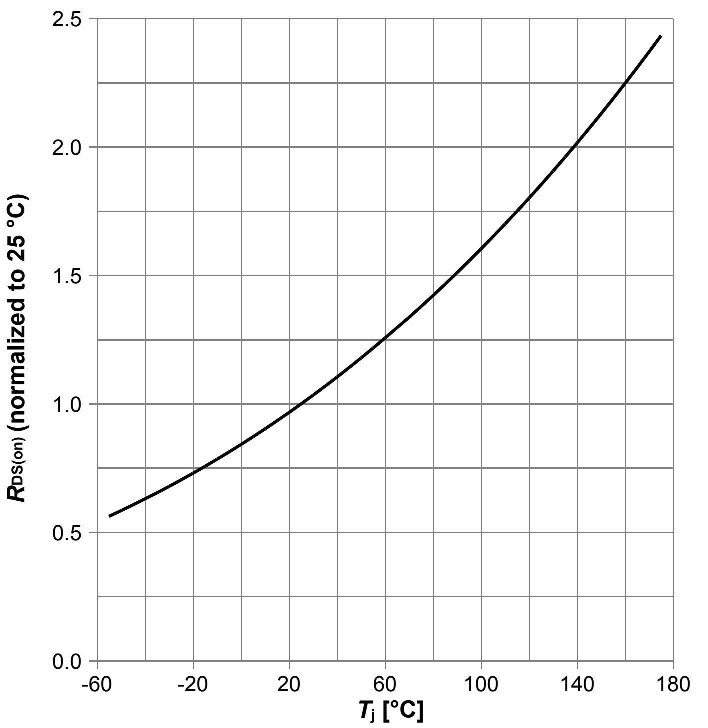
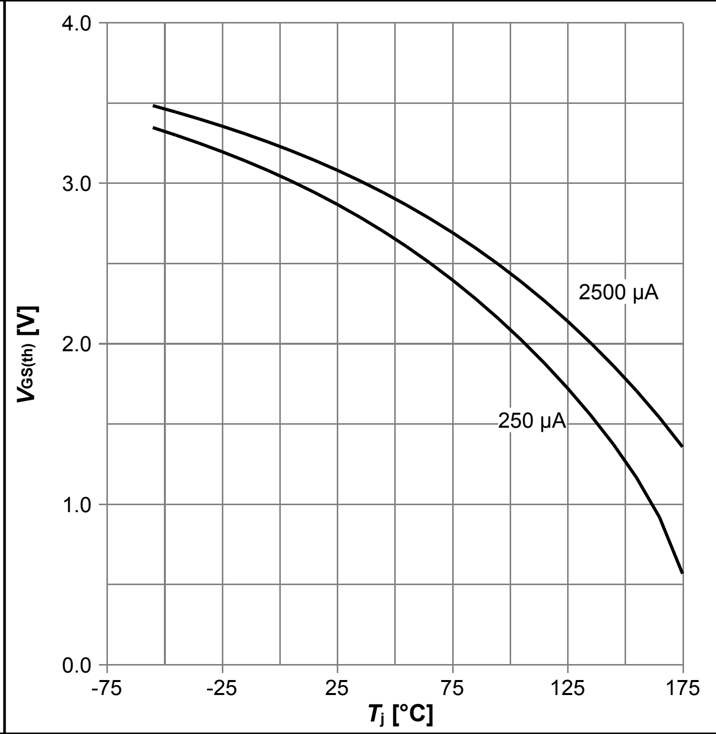
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on resistance
	
I_D=f(V_{GS}), $\|V_{DS}\|$>2$\|I_D\|R_{DS(on)max}$; parameter: T_j	$R_{DS(on)}$=f(V_{GS}), I_D=100 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



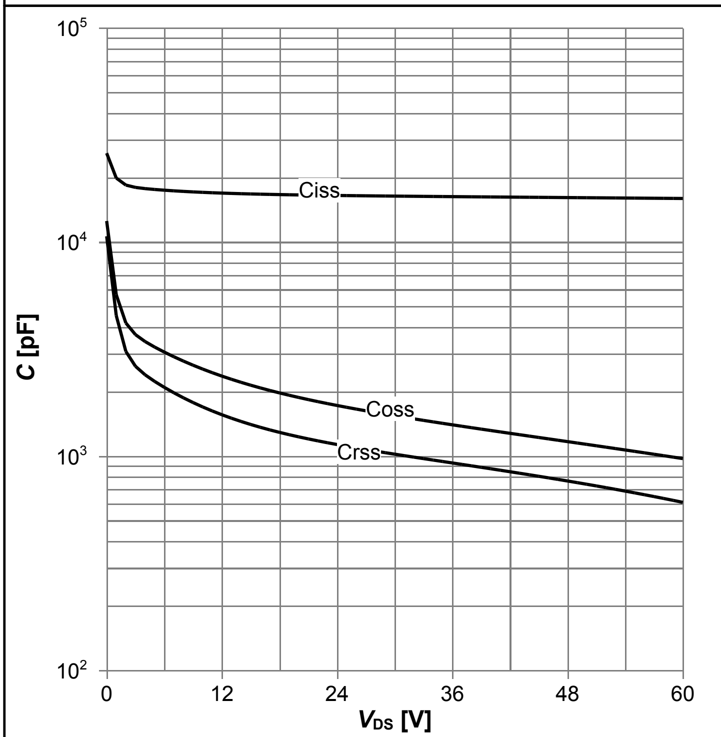
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



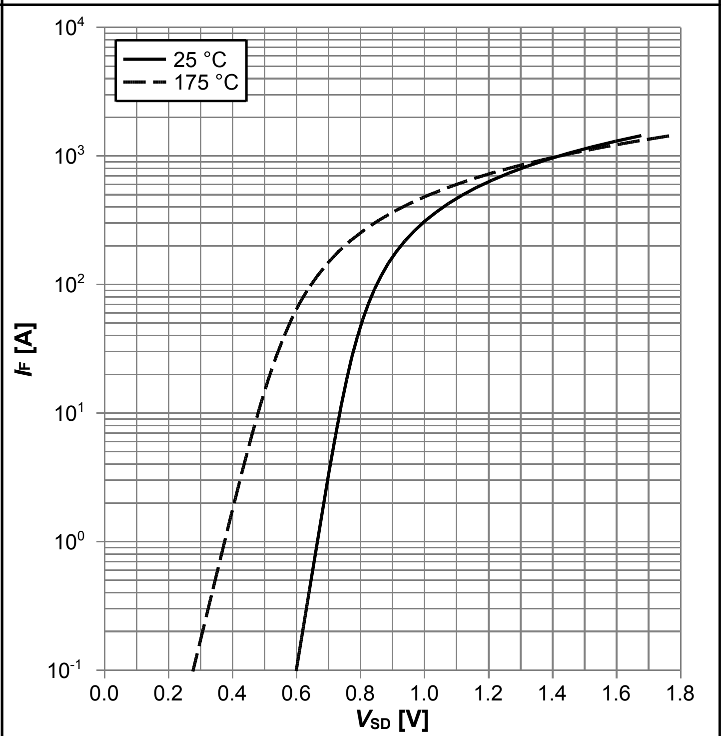
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



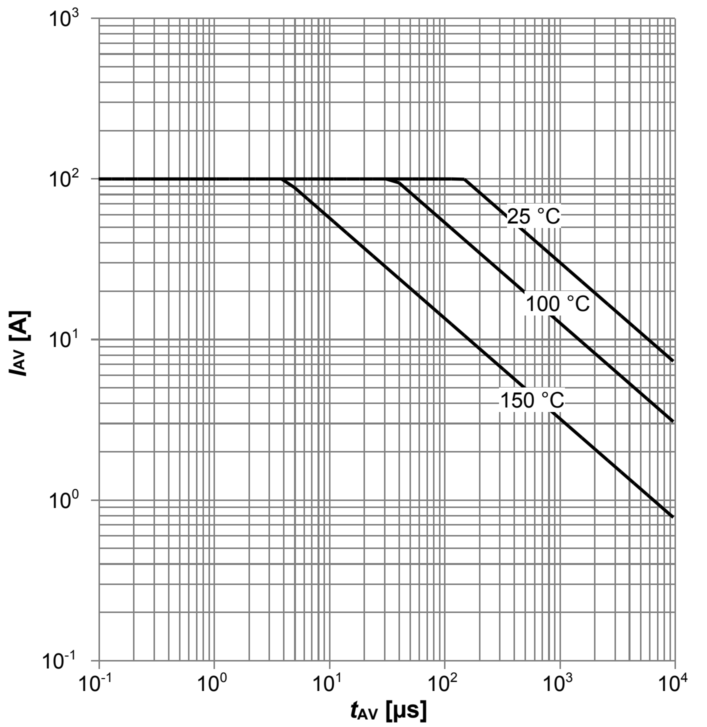
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



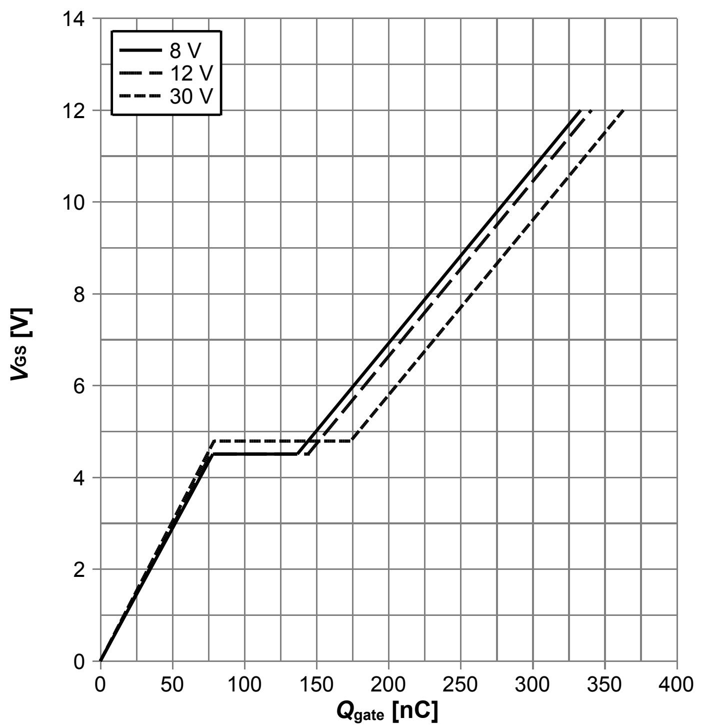
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



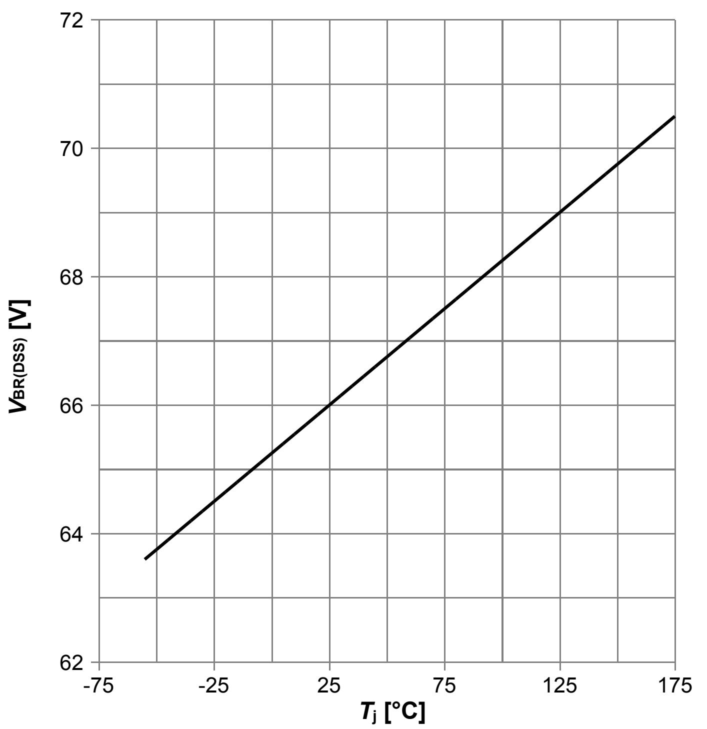
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



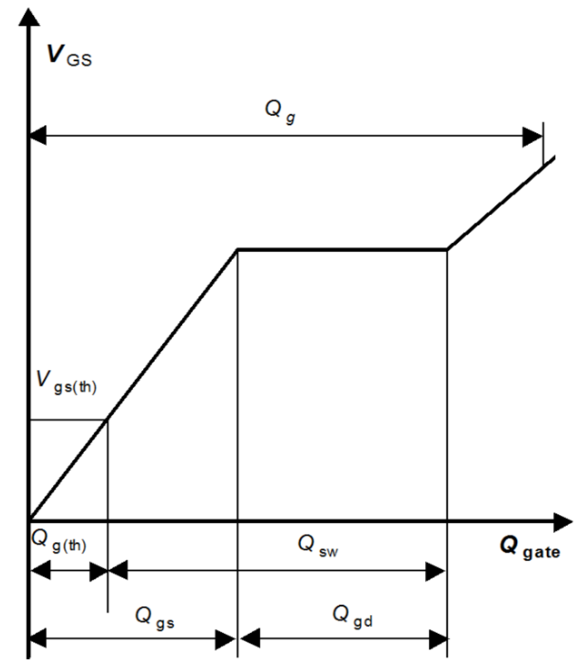
V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines

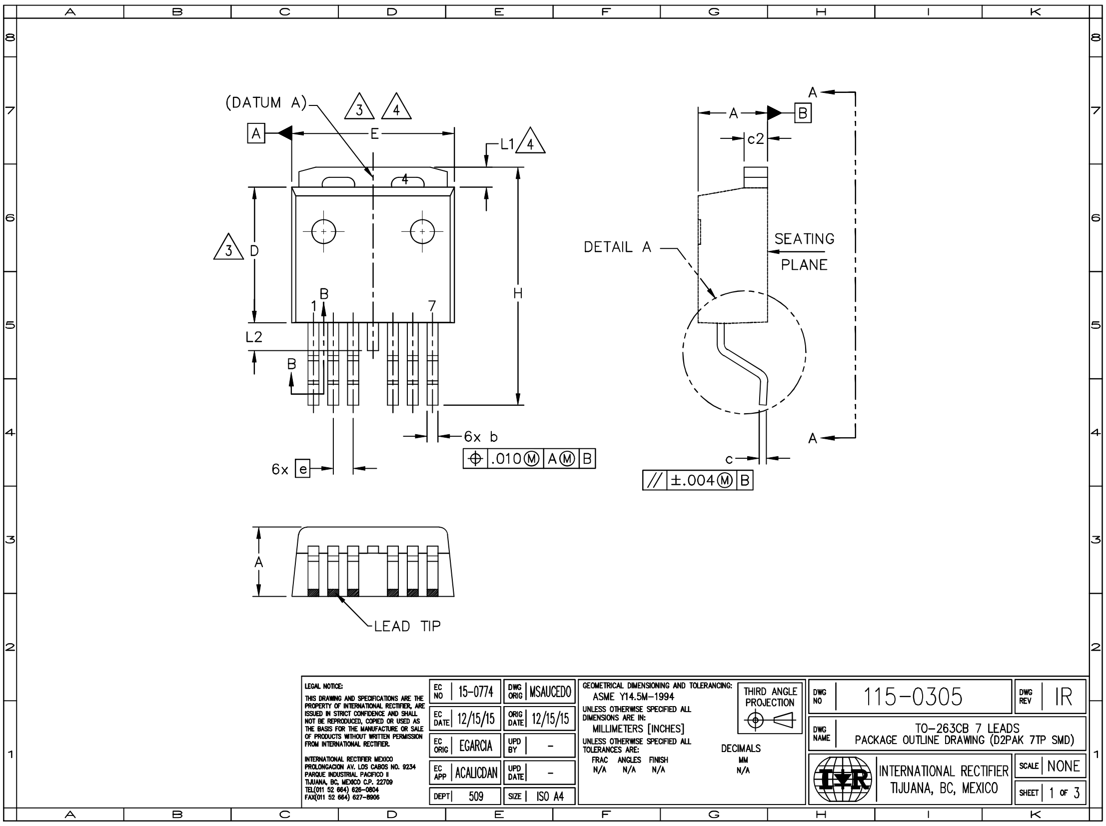


Figure 1 Outline PG-TO263-7, dimensions in mm/inches

Revision History

IRF60SC241

Revision: 2020-08-10, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-11-28	Release of preliminary version
2.0	2018-12-04	Release of final version
2.1	2019-05-08	Removed “Qualified according to JEDEC standard” from the features section since it’s redundant-page1
2.2	2020-08-10	Removed IR MOSFET, should only be StrongIRFET in the header. Update the package picture to the picture with StrongIRFET TM

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