

### Features

- Throughput Rate ..... 160MHz
- Resolution (HI20201)..... 10-Bit
- Differential Linearity Error .....0.5 LSB
- Low Glitch Noise
- Analog Multiplying Function
- Low Power Consumption .....420mW
- Evaluation Board Available
- Direct Replacement for Sony CX20201-1, CX20202-1

### Applications

- Wireless Communications
- Signal Reconstruction
- Direct Digital Synthesis
- High Definition Video Systems
- Digital Measurement Systems
- Radar

### Description

The HI20201 is a 160MHz ultra high speed D/A converter. The converter is based on an R/2R switched current source architecture that includes an input data register with a complement feature and is Emitter Coupled Logic (ECL) compatible.

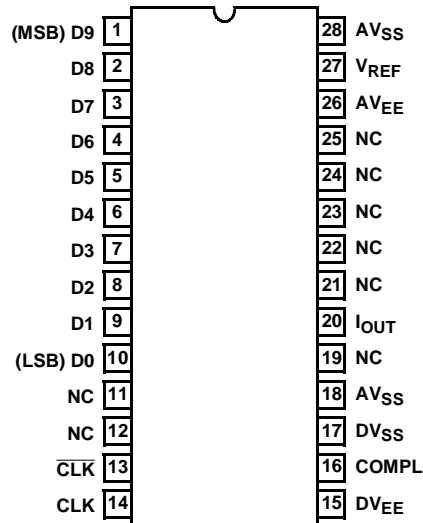
The HI20201 is available in a commercial temperature range and offered in a 28 lead plastic SOIC (300 mil) and a 28 lead plastic DIP package.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI20201JCB	-20 to 75	28 Ld SOIC	M28.3A-S
HI20201JCP	-20 to 75	28 Ld PDIP	E28.6A-S
HI20201-EV	25	Evaluation Kit	

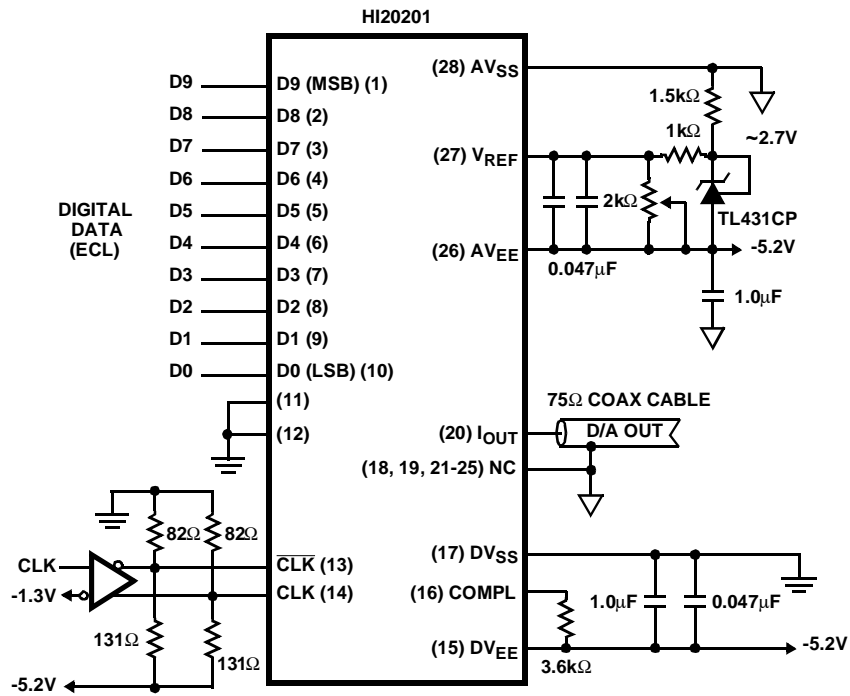
### Pinout

HI20201  
(PDIP, SOIC)  
TOP VIEW

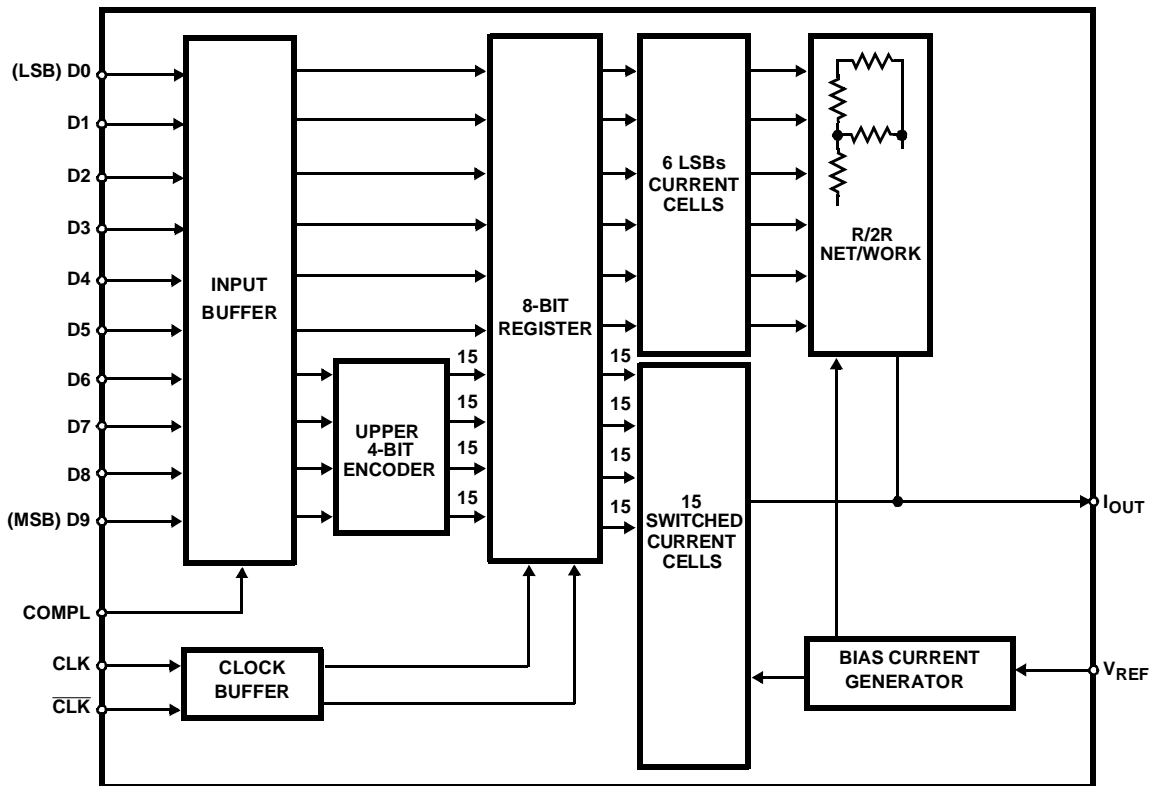


# HI20201

## Typical Application Circuit



## Functional Block Diagram



# HI20201

## Absolute Maximum Ratings

Digital Supply Voltage $DV_{EE}$ to $DV_{SS}$ .....	-7.0V
Analog Supply Voltage $AV_{DD}$ to $AV_{SS}$ .....	-7.0V
Digital Input Voltage .....	+0.3 to $DV_{EE}$ V
Reference Input Voltage .....	+0.3 to $AV_{EE}$ V
Output Current .....	20mA

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package .....	67
PDIP Package .....	58
Maximum Junction Temperature (Plastic Package) .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)

## Recommended Operating Conditions

Supply Voltage	
$AV_{EE}$ , $DV_{EE}$ .....	-4.75V to -5.45V
$AV_{EE}$ - $DV_{EE}$ .....	-0.05V to +0.05V
Digital Input Voltage	
$V_{IH}$ .....	-1.0V to -0.7V
$V_{IL}$ .....	-1.9V to -1.6V

Reference Input Voltage, $V_{REF}$ .....	$V_{EE} + 0.5V$ to $V_{EE} + 1.4V$
Load Resistance, $R_L$ .....	$\geq 75\Omega$
Output Voltage, $V_{OUT}$ .....	0.8V to 1.2V
Temperature Range .....	-20°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$T_A = 25^\circ\text{C}$ ,  $AV_{EE} = DV_{EE} = -5.2V$ ,  $AGND = DGND = 0V$ ,  $R_L = \infty$ ,  $V_{OUT} = -1V$

PARAMETER	TEST CONDITIONS	HI20201JCB/JCP			UNITS
		MIN	TYP	MAX	
<b>SYSTEM PERFORMANCE</b>					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	$f_S = 160\text{MHz}$ (End Point)	-	-	$\pm 1.0$	LSB
Differential Linearity Error, DNL	$f_S = 160\text{MHz}$	-	-	$\pm 0.50$	LSB
Offset Error, $V_{OS}$ (Adjustable to Zero)	(Note 3)	-	7	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 3)	-	-	$\pm 102$	LSB
Full Scale Output Current, $I_{FS}$		-	-	20	mA
<b>DYNAMIC CHARACTERISTICS</b>					
Throughput Rate	See Figure 11	160	-	-	MHz
Glitch Energy, GE	$R_{OUT} = 75\Omega$	-	15	-	pV/s
<b>REFERENCE INPUT</b>					
Voltage Reference Input Range	With Respect to $AV_{EE}$	+0.5	-	+1.4	V
Reference Input Current	$V_{REF} = -4.58V$	-0.1	-0.4	-3.0	$\mu\text{A}$
Voltage Reference to Output Small Signal Bandwidth	-3dB point 1V <sub>p-p</sub> Input	-	14.0	-	MHz
Output Rise Time, $t_r$	$R_{LOAD} = 75\Omega$	-	1.5	-	ns
Output Fall Time, $t_f$	$R_{LOAD} = 75\Omega$	-	1.5	-	ns
<b>DIGITAL INPUTS</b>					
Input Logic High Voltage, $V_{IH}$	(Note 2)	-1.0	-0.89		V
Input Logic Low Voltage, $V_{IL}$	(Note 2)		-1.75	-1.6	V
Input Logic Current, $I_{IL}$ , $I_{IH}$ (For D9 thru D6, COMPL)	$V_{IH} = -0.89V$ , $V_{IL} = -1.75V$ (Note 2)	0.1	1.5	6.0	$\mu\text{A}$
Input Logic Current, $I_{IL}$ , $I_{IH}$ (For D5 thru D0)	$V_{IH} = -0.89V$ , $V_{IL} = -1.75V$ (Note 2)	0.1	0.75	3.0	$\mu\text{A}$
<b>TIMING CHARACTERISTICS</b>					
Data Setup Time, $t_{SU}$	See Figure 11	5	-	-	ns
Data Hold Time, $t_{HLD}$	See Figure 11	1	-	-	ns
Propagation Delay Time, $t_{PD}$	See Figure 11	-	3.8	-	ns
Settling Time, $t_{SET}$ (to $1/2$ LSB)	See Figure 11	-	5.2	-	ns

# HI20201

## Electrical Specifications $T_A = 25^\circ\text{C}$ , $AV_{EE} = DV_{EE} = -5.2\text{V}$ , $AGND = DGND = 0\text{V}$ , $R_L = \infty$ , $V_{OUT} = -1\text{V}$ (Continued)

PARAMETER	TEST CONDITIONS	HI20201JCB/JCP			UNITS
		MIN	TYP	MAX	
<b>POWER SUPPLY CHARACTERISTICS</b>					
$I_{EE}$		-60	-75	-90	mA
Power Dissipation	75 $\Omega$ load	-	420	470	mW

### NOTES:

- Parameter guaranteed by design or characterization and not production tested.
- Excludes error due to reference drift.
- Electrical specifications guaranteed only under the stated operating conditions.

## Timing Diagram

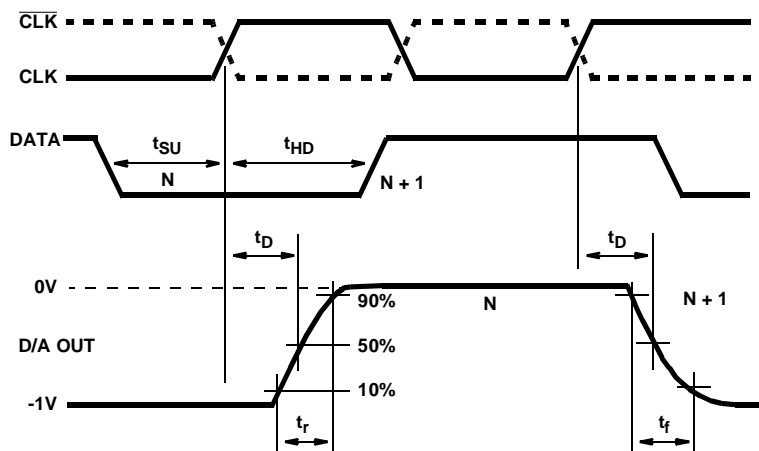


FIGURE 1. LADDER SETTLING TIME FULL POWER BANDWIDTH (LS)

## Pin Descriptions

28 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB)-D9 (MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 9, the Most Significant Bit.
11, 12, 19, 21- 25	NC	No Connect, not used.
13	$\overline{\text{CLK}}$	Negative Differential Clock Input.
14	CLK	Positive Differential Clock Input
15	$DV_{EE}$	Digital (ECL) Power Supply -4.75V to -7V.
16	COMPL	Data Complement Pin. When set to a (ECL) logic High the input data is complemented in the input buffer. When cleared to a (ECL) logic Low the input data is not complemented.
17	$DV_{SS}$	Digital Ground.
18	$AV_{SS}$	Analog Ground.
20	$I_{OUT}$	Current Output Pin.
26	$AV_{EE}$	Analog Supply -4.75V to -7V.
27	$V_{REF}$	Input Reference Voltage used to set the output full scale range.
28	$AV_{SS}$	Analog Ground.

Typical Performance Curves

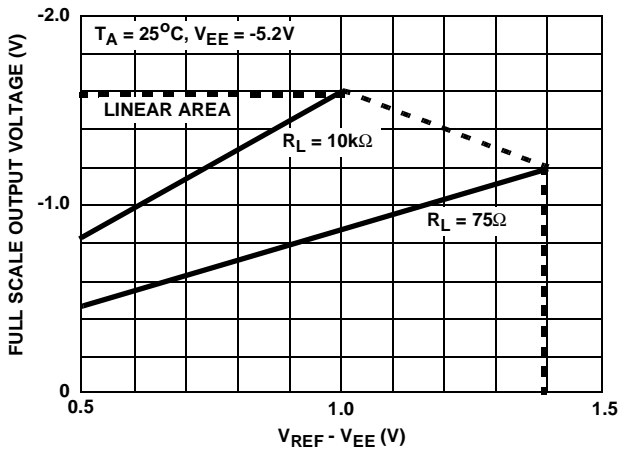


FIGURE 2.  $V_{O(FS)}$  RATIO vs  $(V_{REF} - V_{EE})$

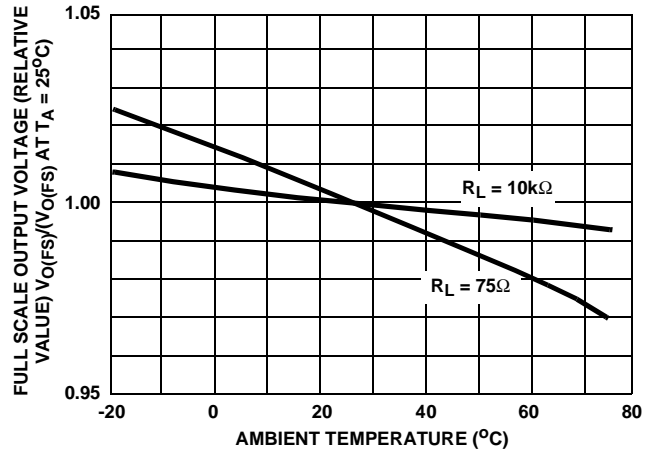


FIGURE 3. FULL SCALE OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

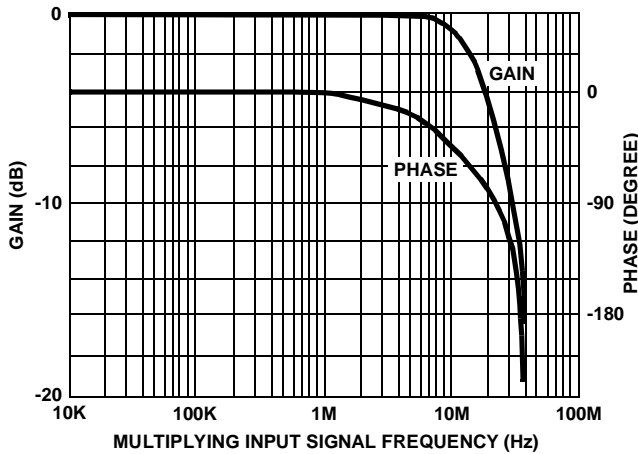


FIGURE 4. OUTPUT CHARACTERISTICS vs MULTIPLYING INPUT SIGNAL FREQUENCY

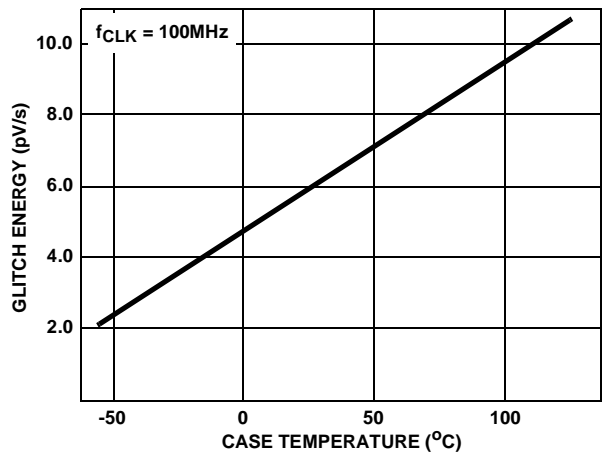


FIGURE 5. GLITCH ENERGY vs CASE TEMPERATURE (FULL SCALE - 1023mV)

### Detailed Description

The HI20201 is a 10-bit, current output D/A converter. The DAC can run at 160MHz and is ECL compatible. The architecture is segmented/R2R combination to reduce glitch and improve linearity.

#### Architecture

The HI20201 is a combined R2R/segmented current source design. The 6 least significant bits of the converter are derived by a traditional R2R network to binary weight the 1mA current sources. The upper 4 most significant bits are implemented as segmented or thermometer encoded current sources. The encoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources. The thermometer encoder will convert binary to individual control lines. See Table 1.

TABLE 1. THERMOMETER ENCODER

MSB	BIT 8	BIT 7	BIT 6	THERMOMETER CODE 1 = ON, 0 = OFF, I <sub>15</sub> - I <sub>0</sub>
0	0	0	0	000 0000 0000 0000
0	0	0	1	000 0000 0000 0001
0	0	1	0	000 0000 0000 0011
0	0	1	1	000 0000 0000 0111
0	1	0	0	000 0000 0000 1111
0	1	0	1	000 0000 0001 1111
0	1	1	0	000 0000 0011 1111
0	1	1	1	000 0000 0111 1111
1	0	0	0	000 0000 1111 1111
1	0	0	1	000 0001 1111 1111
1	0	1	0	000 0011 1111 1111
1	0	1	1	000 0111 1111 1111
1	1	0	0	000 1111 1111 1111
1	1	0	1	001 1111 1111 1111
1	1	1	0	011 1111 1111 1111
1	1	1	1	111 1111 1111 1111

The architecture of the HI20201 is designed to minimize glitch while providing a manufacturable 10-bit design that does not require laser trimming to achieve good linearity.

#### Glitch

Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). In an ECL system where the logic levels switch from one non-saturated level to another, the switching times can be considered close to symmetrical. This helps to reduce glitch in the D/A. Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Inter-sil HI20201 employs an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e.,

01 1111 1111 to 10 0000 0000. But in the HI20201 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R2R/segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI20201 the output is terminated into a 75Ω load. The glitch is measured at the major carry's throughout the DAC's output range.

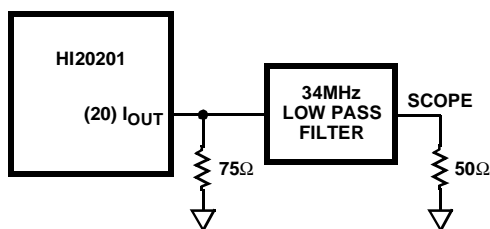


FIGURE 6. HI20201 GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 7 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).

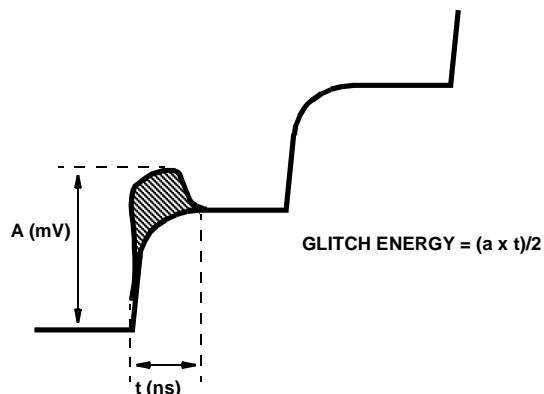


FIGURE 7. GLITCH ENERGY

#### Setting Full Scale

The full scale output voltage is set by the Voltage Reference pin (27). The output voltage performance will vary as shown in Figure 2.

The output structure of the HI20201 can handle down to a 75Ω load effectively. To drive a 50Ω load Figure 8 is suggested. Note the equivalent output load is ~75Ω.

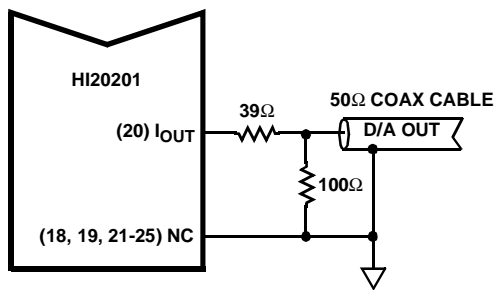


FIGURE 8. HI20201 DRIVING A 50Ω LOAD

**Variable Attenuator Capability**

The HI20201 can be used in a multiplying mode with a variable frequency input on the  $V_{REF}$  pin. In order for the part to operate correctly a DC bias must be applied and the incoming AC signal should be coupled to the  $V_{REF}$  pin. See Figure 13 for the application circuit. The user must first adjust the DC reference voltage. The incoming signal must be attenuated so as not to exceed the maximum (+1.4V) and minimum (+0.5V) reference input. The typical output Small Signal Bandwidth is 14MHz.

**Integral Linearity**

The Integral Linearity is measured using the End Point method. In the End Point method the gain is adjusted. A line is then established from the zero point to the end point or Full Scale of the converter. All codes along the transfer curve must fall within an error band of 1 LSB of the line. Figure 10 shows the linearity test circuit.

**Differential Linearity**

The Differential Linearity is the difference from the ideal step. To guarantee monotonicity a maximum of 1 LSB differential error is allowed. When more than 1 LSB is specified the converter is considered to be missing codes. Figure 10 shows the linearity test circuit.

**Clock Phase Relationship**

The HI20201 is designed to be operated at very high speed (i.e., 160MHz). The clock lines should be driven with ECL100K logic for full performance. Any external data drivers and clock drivers ringing should be terminated with 50Ω to minimize reflections and ringing.

**Internal Data Register**

The HI20201 incorporates a data register as shown in the Functional Block Diagram. This register is updated on the rising edge of the CLK line. The state of the Complement bit (COMPL) will determine the data coding. See Table 2.

TABLE 2. INPUT CODING TABLE

INPUT CODE	OUTPUT CODE	
	COMPL = 1	COMPL = 0
00 0000 0000	0	-1
10 0000 0000	-0.5	-0.5
11 1111 1111	-1	0

**Thermal Considerations**

The temperature coefficient of the full scale output voltage and zero offset voltage depend on the load resistance connected to  $I_{OUT}$ . The larger the load resistor, the better (i.e., smaller) the temperature coefficient of the D/A. See Figure 3 in the performance curves section.

**Noise Reduction**

Digital switching noise must be minimized to guarantee system specifications. Since 1 LSB corresponds to 1mV for 10-bit resolution, care must be taken in the layout of a circuit board.

Separate ground planes should be used for  $DV_{SS}$  and  $AV_{SS}$ . They should be connected back at the power supply.

Separate power planes should be used for  $DV_{EE}$  and  $AV_{EE}$ . They should be decoupled with a 1μF tantalum capacitor and a ceramic 0.047μF capacitor positioned as close to the body of the IC as possible.

Test Circuits

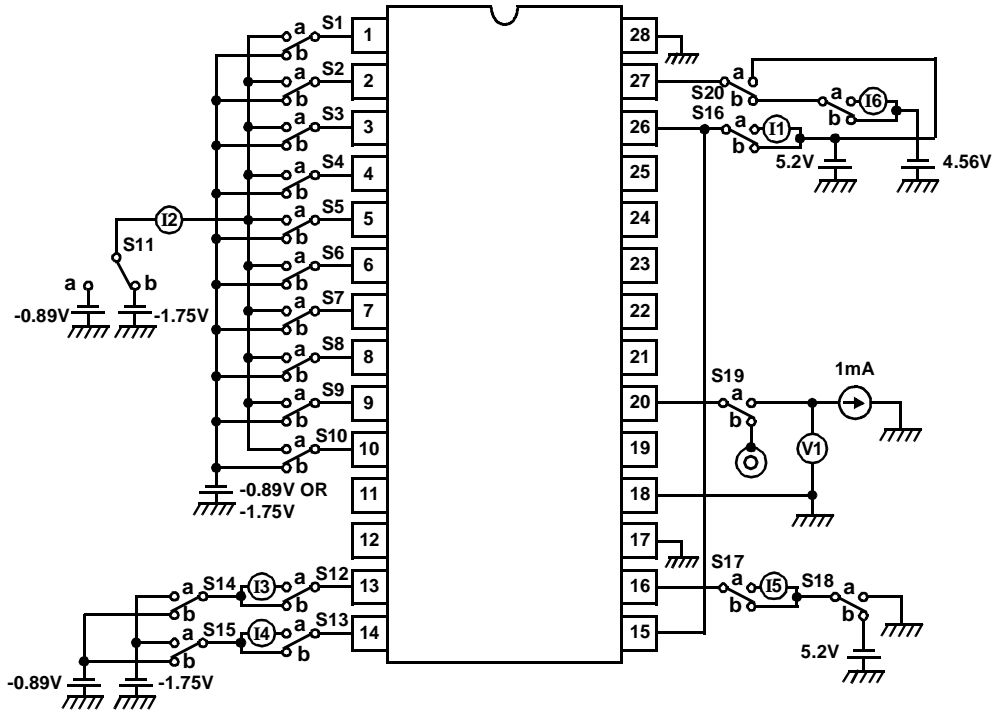
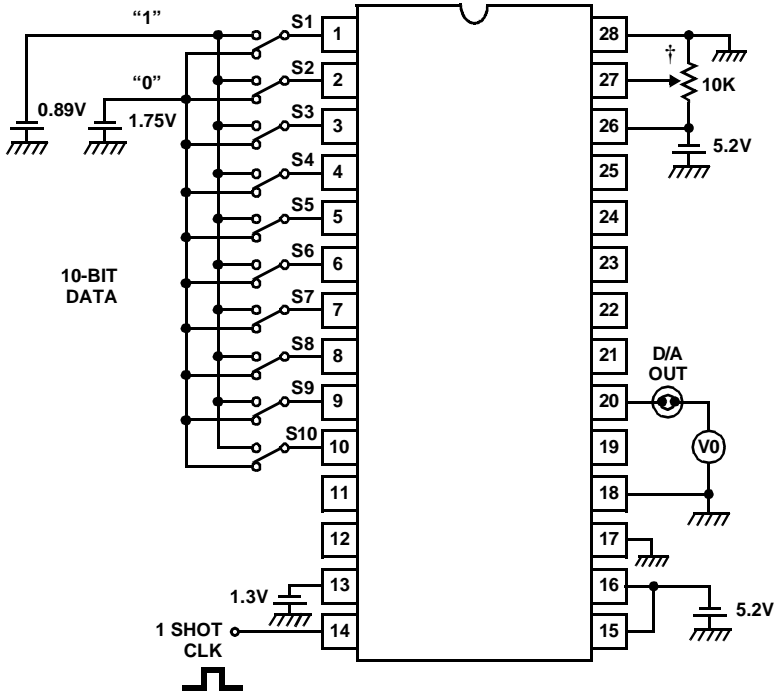


FIGURE 9. CURRENT CONSUMPTION, INPUT CURRENT AND OUTPUT RESISTANCE



Test Circuits (Continued)



† Adjust so that the full scale of DC voltage at pin 20 becomes 1.023V, that is, to satisfy  $V_0 - V_{1023} = 1.023V$ .

LINEARITY ERRORS ARE MEASURED AS FOLLOWS

S1	S2	S3	...	S9	S10	D/A OUT
0	0	0	...	0	0	$V_0$
0	0	0	...	0	1	$V_1$
0	0	0	...	1	0	$V_2$
			...			...
1	1	1	...	1	1	$V_{1023}$

INTEGRAL LINEARITY ERROR	DIFFERENTIAL LINEARITY ERROR
$V_0$	
$V_1$	$V_1 - V_0$
$V_2$	$V_2 - V_1$
$V_4$	$V_4 - V_3$
$V_8$	$V_8 - V_7$
$V_{16}$	$V_{16} - V_{15}$
$V_{32}$	$V_{32} - V_{31}$
$V_{64}$	$V_{64} - V_{63}$
$V_{128}$	$V_{128} - V_{127}$
$V_{192}$	$V_{192} - V_{191}$
...	...
$V_{960}$	$V_{960} - V_{959}$
$V_{1023}$	

Error at individual measurement points are calculated according to the following definition.

$$(V_{1023} - V_0)/1023 = V_{0(FS)}/1023 \approx 1 \text{ LSB.}$$

FIGURE 10. DIFFERENTIAL LINEARITY ERROR AND LINEARITY ERROR

Test Circuits (Continued)

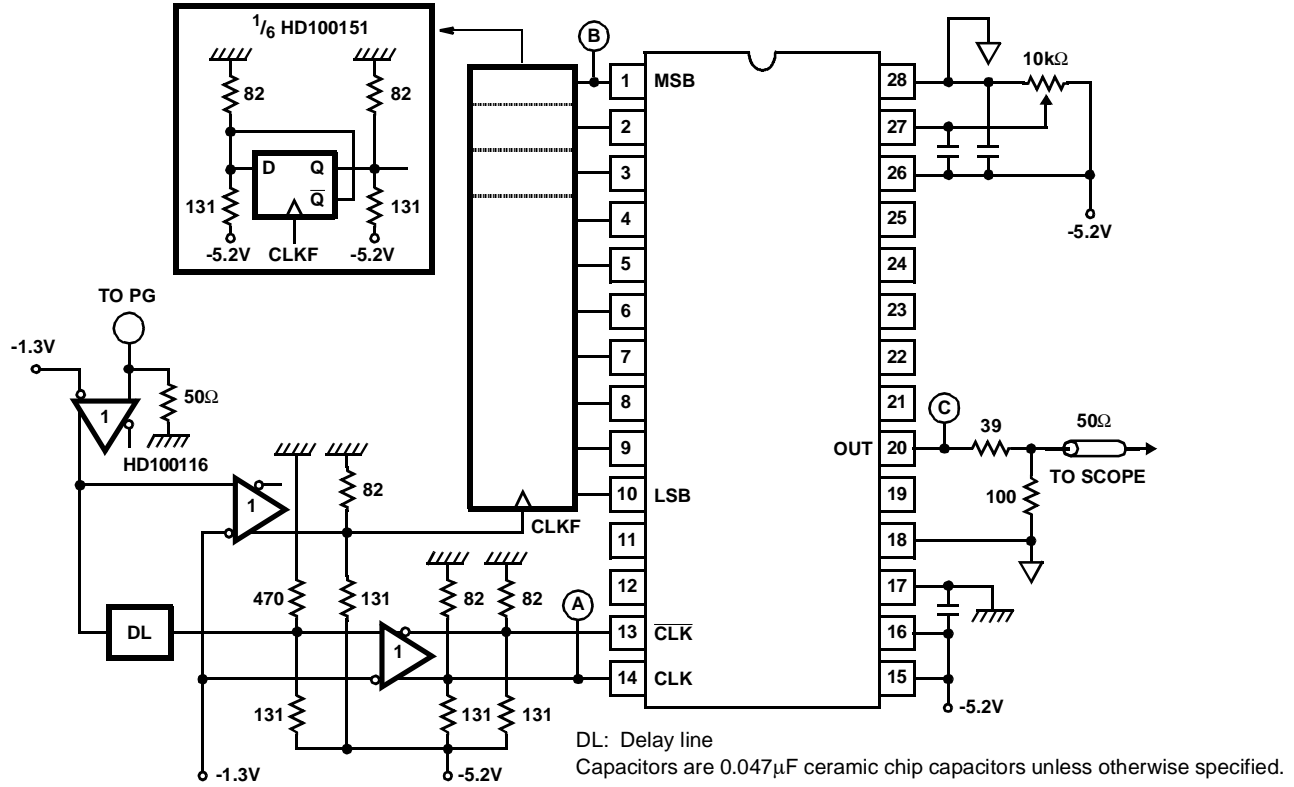


FIGURE 11. MAXIMUM CONVERSION RATE, RISE TIME, FALL TIME, PROPAGATION DELAY, SETUP TIME, HOLD TIME AND SETTLING TIME CIRCUIT

**Test Circuits (Continued)**  
**Measuring Settling Time**

Settling time is measured as follows. The relationship between  $V$  and  $V_{0(FS)}$  as shown in the D/A output waveform in Figure 12 is expressed as

$$V = V_{0(FS)} (1 - e^{-t/\tau}).$$

The settling time for respective accuracy of 10, 9 and 8-bit is specified as

$$V = 0.9995 V_{0(FS)}$$

$$V = 0.999 V_{0(FS)}$$

$$V = 0.999 V_{0(FS)}$$

which results in the following:

$$t_S = 7.60\tau \text{ for 10-bit,}$$

$$t_S = 6.93\tau \text{ for 9-bit, and}$$

$$t_S = 6.24\tau \text{ for 8-bit,}$$

Rise time ( $t_r$ ) and fall time ( $t_f$ ) are defined as the time interval to slew from 10% to 90% of full scale voltage ( $V_{0(FS)}$ ):

$$V = 0.1 V_{0(FS)}$$

$$V = 0.9 V_{0(FS)}$$

and calculated as  $t_r = t_f = 2.20\tau$ .

The settling time is obtained by combining these expressions:

$$t_S = 3.45t_r \text{ for 10-bit,}$$

$$t_S = 3.15t_r \text{ for 9-bit, and}$$

$$t_S = 6.24t_r \text{ for 8-bit}$$

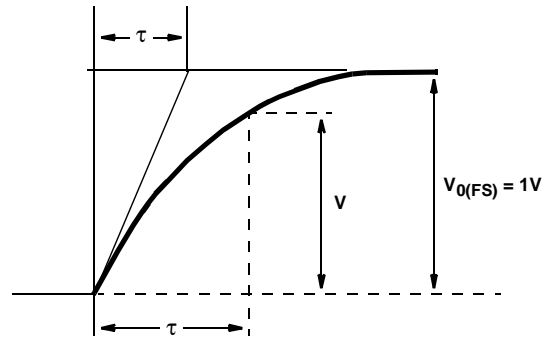


FIGURE 12. D/A OUTPUT WAVEFORM

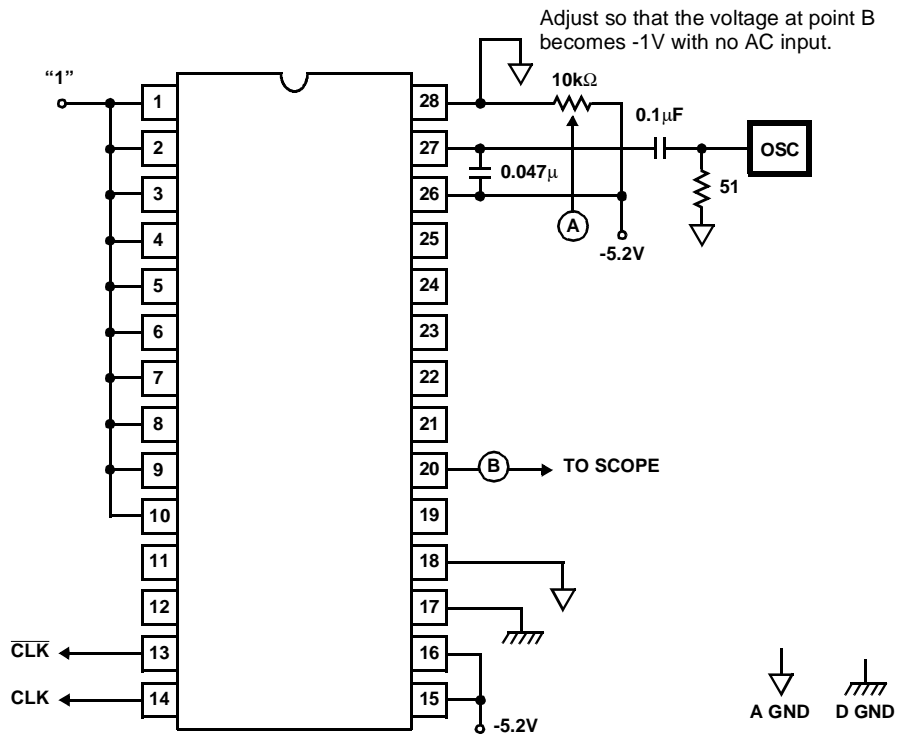


FIGURE 13A.

**Test Circuits** (Continued)

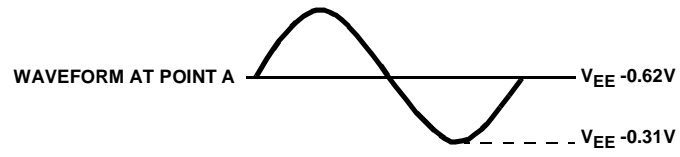


FIGURE 13B.

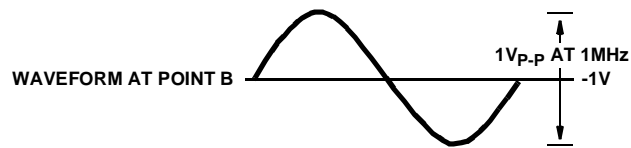


FIGURE 13C.

FIGURE 13. MULTIPLYING BANDWIDTH

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