REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	55	56	57	58	59															
REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																
REV																
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
99-12-01

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, DIGITAL, QUAD,
(4 X 32-BIT) MICROCONTROLLER, +5 VOLT SUPPLY

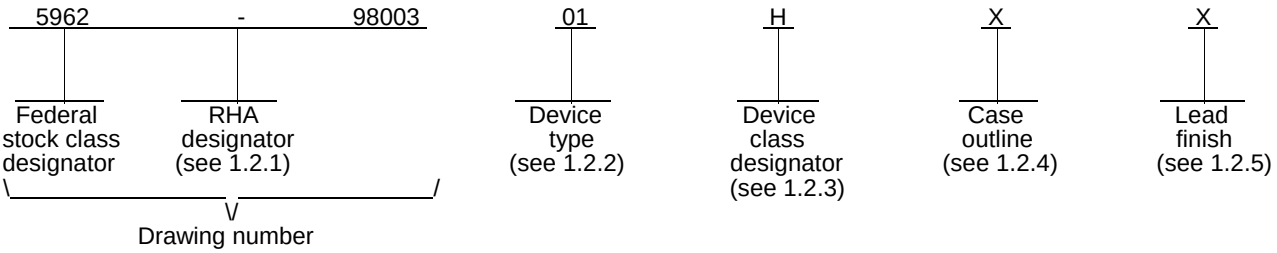
SIZE	CAGE CODE	
A	**67268**	**5962-98003**

SHEET 1 OF 59

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	AD14160BB/QML-4	Quad digital signal processor, +5 V supply, 40 MHz, sixteen 40 megabyte/s link ports (4 from each processor), eight 40 megabit/s serial ports (2 from each procesor).
02	AD14160TB/QML-4	Quad digital signal processor, +5 V supply, 40 MHz, sixteen 40 megabyte/s link ports (4 from each processor), eight 40 megabit/s serial ports (2 from each procesor).

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	1284 2/	Ceramic ball grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 3/

Supply voltage (V_{DD})	-0.3 V dc to +7.0 V dc
Input voltage (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage swing (V_{OUT})	-0.3 V dc to V_{DD} + 0.5 V dc
Load capacitance	200 pF
Junction temperature under bias (T_J)	+130°C
Junction to case temperature (θ_{JC})	0.36°C/W
Solder reflow temperature 4/	+240°C
Storage temperature range	-65°C to +150°C

1/ Inactive for new design. Not available from a QML-38534 manufacturer.
2/ The total number of solder balls is 1284, but only 452 require electrical attachment.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ See recommended solder reflow profile in figure 2.

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.75 V dc to +5.25 V dc
Case operating temperature range (T_C):	
Device type 01	-40°C to +100°C
Device type 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Assembly recommendations for maximum reliability. The assembly recommendations for maximum reliability shall be as specified on figure 2.

3.2.3 Lid deflection. The lid deflection shall be as specified on figure 3.

3.2.4 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.5 Block diagram(s). The block diagram(s) shall be as specified on figure 5.

3.2.6 Timing waveform(s). The timing waveform(s) shall be as specified on figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in MIL-HDBK-103 and QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

(1) Static supply current ($I_{DD}q$).
Checks that current draw is not grossly excessive. Current exceeding 1.3 amperes on the module indicates failure. Normal measured current is about 0.5 amperes.

(2) Interconnects.
Checks for electrical continuity through the package leads and wirebonds, along with continuity of internal wiring within the module.

(3) Single processor functional.
A collection of test routines perform a rudimentary check of the basic functionally of each individual processor. The following individual processor units are tested: DAGs 1 and 2, timer, program sequencer, PX register, multiplier, data register file, shifter, ALU, link ports, serial ports, DMA, IOP registers, and memory.

(a) Serial port test.
This routine uses internal loopback to test basic operation of serial port 0 and serial port 1, by transmitting and receiving 16-bit words. In addition, the COMPare operation of the ALU and BitSET operation of the shifter are tested. Serial ports are tested at a clock rate of 10 MHz.

(b) Computation routine.
The routine tests basic operation of the ALU through ADD, SUBTRACT, and COMPare functions. In addition, the multiplier and DAGs are tested usings floating point multiply and load/write functions, while the shifter is tested with a BitSET function. All operations use 32-bit words.

(c) Link routine.
Using 32-bit data and internal memory to memory receive, basic operation of Link buffers 0 - 5 is tested. In addition, the ALU, COMPare, and shifter BitSET functions are tested.

(d) PX routine.
This routine tests basic operation of the PX register and short word addressing. The PX register is loaded with a 48-bit word, then the PX is read into memory. Short word addressing is used to read back, in 16-bit word segments, the 48-bit word from memory. In addition, the ALU, COMPare, and shifter BitSET functions are tested.

(e) Timer routine.
This routine will count down the timer until $t_{count} = 0$, at which time an interrupt will occur, followed by a return to the code. This test will verify operation of the program sequencer, timer, ALU, COMPare function, and shifter BitSET function.

(4) Multiprocessor functional.

(a) Interprocessor links: all tested using 2 times the clock rate (80 MHz).

(b) Multiprocessor memory space: each processor accesses and checks memory of the other three processors.

c. Final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level input voltage 2/	V_{IH1}	V_{DD} = +5.25 V dc	1, 2, 3	01,02	2.0		V
High level input voltage 3/	V_{IH2}	V_{DD} = +5.25 V dc	1, 2, 3	01,02	2.2		V
Low level input voltage 2/ 3/	V_{IL}	V_{DD} = +4.75 V dc	1, 2, 3	01,02		0.8	V
High level output voltage 4/	V_{OH}	V_{DD} = +4.75 V dc, 5/ I_{OH} = -2.0 mA	1, 2, 3	01,02	4.1		V
Low level output voltage 4/	V_{OL}	V_{DD} = +4.75 V dc, 5/ I_{OL} = 4.0 mA	1, 2, 3	01,02		0.4	V
High level input current 6/ 7/ 8/	I_{IH}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1, 2, 3	01,02		10	µA
High level input current 8/ 9/ 10/	I_{IHx4}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1, 2, 3	01,02		40	µA
Low level input current 6/	I_{IL}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		10	µA
Low level input current 9/	I_{ILx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		40	µA
Low level input current 7/	I_{ILP}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		150	µA
Low level input current 8/ 10/	I_{ILPx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		600	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Three state 11/ 12/ 13/ 14/ leakage current	I_{OZH}	V_{DD} = +5.25 V dc, $V_{IN} = V_{DD}MAX$	1, 2, 3	01,02		10	µA
Three state 15/ leakage current	I_{OZHx4}	V_{DD} = +5.25 V dc, $V_{IN} = V_{DD}MAX$	1, 2, 3	01,02		40	µA
Three state leakage 11/ 16/ current	I_{OZL}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		10	µA
Three state leakage 15/ current	I_{OZLx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		40	µA
Three state leakage 16/ current	I_{OZHP}	V_{DD} = +5.25 V dc, $V_{IN} = V_{DD}MAX$	1, 2, 3	01,02		350	µA
Three state leakage 14/ current	I_{OZLC}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		1.5	mA
Three state leakage 17/ current	I_{OZLA}	V_{DD} = +5.25 V dc, V_{IN} = 2 V	1, 2, 3	01,02		350	µA
Three state leakage 13/ current	I_{OZLAR}	V_{DD} = +5.25 V dc, V_{IN} = 0 V dc	1, 2, 3	01,02		4.2	mA
Three state leakage 12/ current	I_{OZLS}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1, 2, 3	01,02		150	µA
Supply current (internal) 18/	I_{DDIN}	t_{CK} = 25 ns, V_{DD} = MAX	1, 2, 3	01,02		2.92	A

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current (idle) 19/	I_{DDIDLE}	V_{DD} = MAX	1, 2, 3	01		800	mA
				02		1200	
Input capacitance	C_{IN}	f = 1 MHz, T_C = +25°C, V_{IN} = 2.5 V dc	----	01,02	20/		
Functional tests		See 4.3.1.c	7, 8	01,02			
Clock Input Timing Requirements							
CLKIN period	t_{CK}	See figure 6.	9, 10, 11	01,02	25	100	ns
CLKIN width low	t_{CKL}				7		
CLKIN width high	t_{CKH}				5		
CLKIN rise/fall (0.4 V - 2.0 V)	t_{CKRF}					3	
Reset Timing Requirements							
$\overline{\text{RESET}}$ pulse width low 22/	t_{WRST}	See figure 6. 21/	9, 10, 11	01,02	$4t_{CK}$		ns
$\overline{\text{RESET}}$ setup before 23/ CLKIN high	t_{SRST}				14.5+DT/2	t_{CK}	
Interrupts Timing Requirements							
$\overline{\text{IRQ2-0}}$ setup before 24/ CLKIN high	t_{SIR}	See figure 6. 21/	9, 10 ,11	01,02	18+3DT / 4		ns
$\overline{\text{IRQ2-0}}$ hold before 24/ CLKIN high	t_{HIR}					12+3DT / 4	
$\overline{\text{IRQ2-0}}$ width pulse 25/	t_{IPW}				$2+t_{CK}$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Timer Switching Characteristic							
CLKIN high to TIMEXP	t_{DTEX}	See figure 6. 21/	9, 10, 11	01,02		15.5	ns
FLAGS Timing and Switching Requirements							
FLAG2-0$_{IN}$ setup 26/ before CLKIN high	t_{SFI}	See figure 6. 21/	9, 10, 11	01,02	8+5DT/16		ns
FLAG2-0$_{IN}$ hold after 26/ CLKIN high	t_{HFI}				0 - 5DT / 16		
FLAG2-0$_{IN}$ delay after 26/ RD/ WR low	t_{DWRFI}					5+7DT/16	
FLAG2-0$_{IN}$ hold after 26/ RD/ WR deasserted	t_{HFIWR}				0.5		
FLAG2-0$_{OUT}$ delay after CLKIN high	t_{DFO}					16.5	
FLAG2-0$_{OUT}$ hold after CLKIN high	t_{HFO}				4		
CLKIN high to FLAG2-0$_{OUT}$ enable	t_{DFOE}				3		
CLKIN high to FLAG2-0$_{OUT}$ disable	t_{DFOD}					14.5	
Memory Read - Bus Master Timing and Switching Requirements							
Address delay to 28/ 29/ data valid	t_{DAD}	See figure 6. 21/ 27/	9, 10, 11	01,02		17+DT+W	ns
$\overline{RD}$ low to data valid 28/	t_{DRLD}					11+5DT/D +W	
Data hold from address 30/	t_{HDA}				1.5		
Data hold from $\overline{RD}$ high 30/	t_{HDRH}				3		
ACK delay from 29/ 31/ address	t_{DAAK}					13+7DT/8 +W	
ACK delay from $\overline{RD}$ low 30/	t_{DSAK}					7+DT/2 +W	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Memory Read - Bus Master Timing and Switching Requirements - Continued.							
Address hold after $\overline{RD}$ high	t_{DRHA}	See figure 6. 21/ 27/	9, 10, 11	01,02	-1 + H		ns
Address to $\overline{RD}$ low 29/	t_{DARL}				1+3DT/8		
$\overline{RD}$ pulse width	t_{RW}				12.5+5DT/8 +W		
$\overline{RD}$ high to $\overline{WR}$, $\overline{RD}$, DMAGx low	t_{RWR}				7.5+3DT/8 +HI		
Address setup before 29/ ADRCLK high	t_{SADADC}				-0.5 + DT/4		
Memory Write - Bus Master Timing and Switching Requirements							
ACK delay from 29/ 31/ address selects	t_{DAAK}	See figure 6. 21/ 27/	9, 10, 11	01,02		13+7DT/8 +W	ns
ACK delay from $\overline{WR}$ 31/ low	t_{DSAK}					7+DT/2 +W	
Address, selects to 29/ $\overline{WR}$ deasserted	t_{DAWH}				16+15DT/16 +W		
Address, selects to 29/ $\overline{WR}$ low	t_{DAWL}				2+3DT/8		
$\overline{WR}$ pulse width	t_{WW}				12+9DT/16 +W		
Data setup before $\overline{WR}$ high	t_{DDWH}				6+DT/2 +W		
Address hold after $\overline{WR}$ deasserted	t_{DWHA}				0+DT/16 +H		
Data disabled after 32/ $\overline{WR}$ deasserted	t_{DATRWH}				0.5+DT/16 +H	7+DT/16 +H	
$\overline{WR}$ high to $\overline{WR}$, $\overline{RD}$, DMAGx low	t_{WWR}				7.5+7DT/16 +H		
Data disable before $\overline{WR}$ or $\overline{RD}$ low	t_{DDWR}				4+3DT/8+1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Memory Write - Bus Master Timing and Switching Requirements - Continued.							
$\overline{WR}$ low to data enabled	t_{WDE}	See figure 6. 21/ 27/	9, 10, 11	01,02	-1.5+DT/16		ns
Address, selects to ADRCLK high 29/	t_{SADADC}				-0.5+DT/4		
Synchronous Read/Write - Bus Master Timing and Switching Requirements							
Data setup before CLKIN	t_{SSDATI}	See figure 6. 21/ 27/	9, 10, 11	01,02	3.5 + DT/8		ns
Data hold after CLKIN	t_{HSDATI}				3.5 - DT/8		
ACK delay after address, MSx, SW, BMS 29/ 31/	t_{DAAK}					13+7DT/8 +W	
ACK setup before CLKIN 31/	t_{SACKC}				7 + DT/4		
ACK hold after CLKIN	t_{HACKC}				-1 - DT/4		
Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$, delay after CLKIN 29/	t_{DADRO}					8 - DT/8	
Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$, hold after CLKIN 29/	t_{HADRO}				-1 - DT/8		
PAGE delay after CLKIN	t_{DPGC}				9 + DT/8	16.5+DT/8	
$\overline{RD}$ high delay after CLKIN	t_{DRDO}				-2 - DT/8	5 - DT/8	
$\overline{WR}$ high delay after CLKIN	t_{DWRO}				-3 - 3DT/16	5 - 3DT/16	
$\overline{RD}$ / $\overline{WR}$ low delay after CLKIN	t_{DRWL}				8 + DT/4	13.5+DT/4	
Data delay after CLKIN	t_{SDDATO}			01		20 + 5DT/16	
				02		20.5 + 5DT /16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Synchronous Read/Write - Bus Master Timing and Switching Requirements - Continued.							
Data disable after CLKIN 32/	t_{DATTR}	See figure 6. 21/ 27/	9, 10, 11	01,02	0 - DT/8	8 - DT/8	ns
ADRCLK delay after CLKIN	t_{DADCCK}				4 + DT/8	10.5 + DT/8	
ADRCLK period	t_{ADRCK}				t_{CK}		
ADRCLK width high	t_{ADRCKH}				(t_{CK}/2 - 2)		
ADRCLK width low	t_{ADRCKL}				(t_{CK}/2 - 2)		
Synchronous Read/Write - Bus Slave Timing and Switching Requirements							
Address, $\overline{SW}$ setup before CLKIN	t_{SADRI}	See figure 6. 21/ 27/	9, 10, 11	01,02	15.5+DT/2		ns
Address, $\overline{SW}$ hold before CLKIN	t_{HADRI}					5 + DT/2	
$\overline{RD}$ / $\overline{WR}$ low setup before CLKIN 33/	t_{SRWLI}				10+5DT/16		
$\overline{RD}$ / $\overline{WR}$ low hold after CLKIN	t_{HRWLI}			01	-4 - 5DT/16	7.5+7DT/16	
				02	-3.5 - 5DT / 16	8 + 7DT/16	
$\overline{RD}$ / $\overline{WR}$ pulse high	t_{RWHPI}			01,02	3		
Data setup before $\overline{WR}$ high	t_{SDATWH}				6		
Data hold after WR high	t_{HDATWH}				1.5		
Data delay after CLKIN	t_{SDDATO}			01		20+5DT/16	
				02		20.5 + 5DT /16	
Data disable after CLKIN 32/	t_{DATTR}			01,02	0 - DT/8	8 - DT/8	
ACK delay after address 34/ $\overline{SW}$	t_{DACKAD}					10	
ACK disable after CLKIN 34/	t_{ACKTR}				-1 - DT/8	7 - DT/8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Multiprocessor Bus Request and Host Request Timing and Switching Requirements							
$\overline{HBG}$ low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$, valid	$t_{HBGRCSV}$	See figure 6. 21/ 27/	9, 10, 11	01,02		19.5+5DT/4	ns
$\overline{HBR}$ setup before 36/ CLKIN	t_{SHBRI}				20+3DT/4		
$\overline{HBR}$ hold before 36/ CLKIN	t_{HHBRI}					14+3DT/4	
$\overline{HBG}$ setup before CLKIN	t_{SHBGI}				13+DT/2		
$\overline{HBG}$ hold before CLKIN high	t_{HHBGI}			01		6 + DT/2	
				02		5.75+DT/2	
$\overline{BRx}$, $\overline{CPA}$ setup before 37/ CLKIN high	t_{SBRI}			01,02	13.5+DT/2		
$\overline{BRx}$, CPA hold before CLKIN high	t_{HBRI}					6 + DT/2	
RPBA setup before CLKIN	t_{SRPBAI}				21.5+3DT/4		
RPBA hold before CLKIN	t_{HRPBAI}					12 + 3DT/4	
$\overline{HBG}$ delay after CLKIN	t_{DHBGO}					7.5 - DT/8	
$\overline{HBG}$ hold after CLKIN	t_{HHBGO}				-2 - DT/8		
$\overline{BRx}$ delay after CLKIN	t_{DBRO}					8 - DT/8	
$\overline{BRx}$ hold after CLKIN	t_{HBRO}				-2 - DT/8		
$\overline{CPA}$ low delay after CLKIN	t_{DCPAO}					8.5 - DT/8	
$\overline{CPA}$ disable after CLKIN	t_{TRCPA}				-2 - DT/8	5 - DT/8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Multiprocessor Bus Request and Host Request Timing and Switching Requirements - Continued.							
REDY (O/D) or (A/D) 38/ low from CS and HBR low	t_{DRDYCS}	See figure 6. 21/ 27/	9, 10, 11	01,02		9.5	ns
REDY (O/D) disable or 38/ REDY (A/D) high from HBG	t_{TRDYHG}				39.5+27DT /16		
REDY (A/D) disable from 38/ CS or HBR high	t_{ARDYTR}					11	
Asynchronous Read Cycle Timing and Switching Requirements							
Address setup/$\overline{CS}$ low 39/ before RD low	t_{SADRDL}	See figure 6. 21/ 27/	9, 10, 11	01,02	1		ns
Address hold/$\overline{CS}$ hold low after RD	t_{HADRDH}				1		
$\overline{RD}$/$\overline{WR}$ high width	t_{WRWH}				6		
$\overline{RD}$ high delay after REDY (O/D) disable	$t_{DRDHRDY}$				0.5		
$\overline{RD}$ high delay after REDY (A/D) disable	$t_{DRDHRDY}$				0.5		
Data valid before REDY disable from low	$t_{SDATRDY}$				1		
REDY (O/D) or (A/D) low delay after RD low	$t_{DRDYRDL}$					11	
REDY (O/D) or (A/D) low pulse width for read	t_{RDYPRD}				45 + DT		
Data disable after $\overline{RD}$ high	t_{HDARWH}				2	9.5	
Asynchronous Write Cycle Timing and Switching Requirements							
$\overline{CS}$ low setup before $\overline{WR}$ low	t_{SCSWRL}	See figure 6. 21/ 27/	9, 10, 11	01,02	0		ns
$\overline{CS}$ low hold after $\overline{WR}$ high	t_{HCSWRH}				0.5		
Address setup before $\overline{WR}$ high	t_{SADWRH}				6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Asynchronous Write Cycle Timing and Switching Requirements - Continued.							
Address hold after $\overline{WR}$ high	t_{HADWRH}	See figure 6. 21/ 27/	9, 10, 11	01,02	2.5		ns
$\overline{WR}$ low width	t_{WWRL}				7		
$\overline{RD}$/$\overline{WR}$ high width	t_{WRWH}				6		
$\overline{WR}$ high delay after REDY (O/D) or (A/D) disable	$t_{DWRHRDY}$				0.5		
Data setup before $\overline{WR}$ high	t_{SDATWH}				6		
Data hold after $\overline{WR}$ high	t_{HDATWH}				1.5		
REDY (O/D) or (A/D) low delay after WR/CS low	$t_{DRDYWRL}$					11	
REDY (O/D) or (A/D) low pulse width for write	t_{RDYPWR}				15		
REDY (O/D) or (A/D) disable to CLKIN	t_{SRDYCK}				0.5+7DT/16	8+7DT/16	
Three State Timing - (Bus Master, Bus Slave, HBR, SBTS) Timing and Switching Requirements							
$\overline{SBTS}$ setup before CLKIN	t_{STSCK}	See figure 6. 21/ 27/	9, 10, 11	01,02	12 + DT/2		ns
$\overline{SBTS}$ hold before CLKIN	t_{HTSCK}					6 + DT/2	
Address/select enable after CLKIN	t_{MIENA}				-1.5 - DT/8		
Strobes enable after 40/ CLKIN	t_{MIENS}				-1.5 - DT/8		
$\overline{HBG}$ enable after CLKIN	t_{MIENHG}				-1.5 - DT/8		
Address select/disable after CLKIN	t_{MITRA}			01		1 - DT/4	
				02		1.15 - DT/4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Three State Timing - (Bus Master, Bus Slave, HBR, SBTS) Timing and Switching Requirements - Continued.							
Strobes disable after 40/ CLKIN	t_{MITRS}	See figure 6. 21/ 27/	9, 10, 11	01,02		2.5 - DT/4	ns
$\overline{HBG}$ disable after CLKIN	t_{MITRHG}					2.5 - DT/4	
Data enable after CLKIN 41/	t_{DATEN}				9 + 5DT/16		
Data disable after CLKIN 41/	t_{DATTR}				0 - DT/8	8 - DT/8	
ACK enable after CLKIN 41/	t_{ACKEN}				7.5 + DT/4		
ACK disable after CLKIN 41/	t_{ACKTR}				-1 - DT/8	7 - DT/8	
ADRCLK enable after 41/ CLKIN	t_{ADCEN}				-2 - DT/8		
ADRCLK disable after 41/ CLKIN	t_{ADCTR}					8.5 - DT/4	
Memory interface 42/ disable before HBG low	t_{MTRHBG}				-0.5 + DT/8		
Memory interface 42/ enable after HBG low	t_{MENHBG}				18.5 + DT		
DMA Handshake Timing and Switching Requirements							
$\overline{DMARx}$ low setup 43/ before CLKIN	t_{SDRLC}	See figure 6. 21/ 27/	9, 10, 11	01,02	5.5		ns
$\overline{DMARx}$ high setup 43/ before CLKIN	t_{SDRHC}				5.5		
$\overline{DMARx}$ width low (nonsynchronous)	t_{WDR}				6		
Data setup after 44/ DMAGx low	$t_{SDATDGL}$					9 + 5DT/8	
Data hold after $\overline{DMAGx}$ high	$t_{HDATIDG}$				2.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DMA Handshake Timing and Switching Requirements - Continued.							
Data valid after DMARx high 44/	t_{DATDRH}	See figure 6. 21/ 27/	9, 10, 11	01,02		15+7DT/8	ns
$\overline{DMAGx}$ low edge to low edge	t_{DMARLL}				23+7DT/8		
$\overline{DMAGx}$ width high	t_{DMARH}				6		
$\overline{DMAGx}$ low delay after CLKIN	t_{DDGL}				9 + DT/4	16 + DT/4	
$\overline{DMAGx}$ high width	t_{WDGH}				6 + 3DT/8		
$\overline{DMAGx}$ low width	t_{WDGL}				12 + 5DT/8		
$\overline{DMAGx}$ high delay after CLKIN	t_{HDGC}				-2 - DT/8	7 - DT/8	
Data valid before $\overline{DMAGx}$ high 45/	$t_{VDATDGH}$				7+9DT/16		
Data disable after $\overline{DMAGx}$ high 32/	$t_{DATRDGH}$				-0.5	8	
$\overline{WR}$ low before $\overline{DMAGx}$ low	t_{DGWRL}				-0.5	2.5	
$\overline{DMAGx}$ low before $\overline{WR}$ high	t_{DGWRH}				9.5+5DT/8 +W		
$\overline{WR}$ high before $\overline{DMAGx}$ high	t_{DGWRR}				0.5 + DT/16	3.5 + DT/16	
$\overline{RD}$ low before $\overline{DMAGx}$ low	t_{DGRDL}			01	-0.75	2.5	
				02	-1	2.5	
$\overline{RD}$ low before $\overline{DMAGx}$ high	t_{DRDGH}			01,02	10.5+9DT /16+W		
$\overline{RD}$ high before $\overline{DMAGx}$ high	t_{DGRDR}				-0.5	3.5	
$\overline{DMAGx}$ high to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$ low	t_{DGWR}				5+3DT/8 +HI		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DMA Handshake Timing and Switching Requirements - Continued.							
Address/select valid to DMAGx high	t_{DADGH}	See figure 6. 21/ 27/	9, 10, 11	01,02	16 + DT		ns
Address/select hold after DMAGx high	t_{DDGHA}				-1.5		
Link Ports: 1 times Clock Speed Operation, Receive Timing and Switching Requirements							
Data setup before LCLK low	t_{SLDCL}	See figure 6. 21/ 27/	9, 10, 11	01,02	3.5		ns
Data hold after LCLK low	t_{HLDCL}				3		
LCLK period (1 x operation)	t_{LCLKIW}				t_{CK}		
LCLK width low	$t_{LCLKRWL}$				6		
LCLK width high	$t_{LCLKRWH}$				5		
LACK high delay after CLKIN high	t_{DLAHC}				18 + DT/2	29 + DT/2	
LACK low delay after 46/ CLKIN high	t_{DLALC}				-3	13.5	
LACK enable from CLKIN	t_{ENDLK}				5 + DT/2		
LACK disable from CLKIN	t_{TDLK}					20.5 + DT/2	
Link Ports: 1 times Clock Speed Operation, Transmit Timing and Switching Requirements							
LACK setup before LCLK high	t_{SLACH}	See figure 6. 21/ 27/	9, 10, 11	01	18		ns
				02	19.25		
LACK hold after LCLK high	t_{HLACH}			01,02	-7		
LCLK delay after CLKIN (1 x operation)	t_{DLCLK}			01		16	
				02		16.5	
Data delay after LCLK high	t_{DLDCH}			01,02		3.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Link Ports: 1 times Clock Speed Operation, Transmit Timing and Switching Requirements - Continued.							
Data hold after LCLK high	t_{HLDCH}	See figure 6. 21/ 27/	9, 10, 11	01,02	-3		ns
LCLK width low	$t_{LCLKTWL}$			01	$(t_{Ck}/2) - 2$	$(t_{Ck}/2) + 2$	
				02	$(t_{Ck}/2) - 2$	$(t_{Ck}/2) + 2.25$	
LCLK width high	$t_{LCLKTWH}$			01	$(t_{Ck}/2) - 2$	$(t_{Ck}/2) + 2$	
				02	$(t_{Ck}/2) - 2.25$	$(t_{Ck}/2) + 2$	
LCLK low delay after LACK high	t_{DLACLK}			01	$(t_{Ck}/2) + 8.5$	$(3*t_{Ck}/2) + 17.5$	
				02	$(t_{Ck}/2) + 8.5$	$(3*t_{Ck}/2) + 18.5$	
LDAT, LCLK enable after CLKIN	t_{ENDLK}			01,02	5 + DT/2		
LDAT, LCLK disable after CLKIN	t_{TDLK}					20.5 + DT/2	
Link Port Service Request Interrupts: 1 times and 2 times Speed Operation Timing Requirements							
LACK/LCLK setup before CLKIN low 47/	t_{SLCK}	See figure 6. 21/ 27/	9, 10, 11	01,02	10		ns
LACK/LCLK hold after CLKIN low 47/	t_{HLCK}				2		
Link Ports: 2 times Speed Operation, Receive Timing and Switching Requirements							
Data setup before LCLK low	t_{SLDCL}	See figure 6. 21/ 27/	9, 10, 11	01,02	2.75		ns
Data hold after LCLK low	t_{HLDCL}				2.25		
LCLK period (2 x operation)	t_{LCLKIW}				$t_{CK}/2$		
LCLK width low	$t_{LCLKRWL}$			01	4.6		
				02	4.7		
LCLK width high	$t_{LCLKRWH}$			01,02	4.25		
LACK high delay after CLKIN high	t_{DLAHC}				18 + DT/2	31 + DT/2	
LACK low delay after CLKIN high 46/	t_{DLALC}				6	17.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Link Ports: 2 times Speed Operation, Transmit Timing and Switching Requirements							
LACK setup before LCLK high	t_{SLACH}	See figure 6. 21/ 27/	9, 10, 11	01	20.25		ns
				02	19.25		
LACK hold after LCLK high	t_{HLACH}			01,02	-6.5		
LCLK delay after CLKIN (2 x operation)	t_{DLCLK}					8.5	
Data delay after LCLK high	t_{DLDCH}			01		3.25	
				02		3.35	
Data hold after LCLK high	t_{HLDCH}			01,02	-2		
LCLK width low	$t_{LCLKTWL}$				$(t_{Ck}/4) - 1$	$(t_{Ck}/4) + 1.5$	
LCLK width high	$t_{LCLKTWH}$				$(t_{Ck}/4) - 1.5$	$(t_{Ck}/4) + 1$	
LCLK low delay after LACK high	t_{DLACLK}				$(t_{Ck}/4) + 9$	$(3* t_{Ck}/4) + 17$	
Link data set-up skew 48/	t_{SLSK}					0.4 49/	
Link data hold skew 50/	t_{HLSK}					3.3	
Serial Ports: External Clock Timing Requirements							
TFS/RFS setup before 51/ TCLK/RCLK	t_{SFSE}	See figure 6. 21/ 27/	9, 10, 11	01,02	3.5		ns
TFS/RFS hold after 51/ 52/ TCLK/RCLK	t_{HFSE}				4		
Receive data setup 51/ before RCLK	t_{SDRE}				1.5		
Receive data hold 51/ after RCLK	t_{HDRE}				4		
TCLK/RCLK width	t_{SCLKW}				9		
TCLK/RCLK period	t_{SCLK}				t_{CK}		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Serial Ports: Internal Clock Timing Requirements							
TFS setup before TCLK; 51/ RFS setup before RCLK	t_{SFSI}	See figure 6. 21/ 27/	9, 10, 11	01,02	8		ns
TFS/RFS hold after 51/ 52/ TCLK/RCLK	t_{HFSI}				1		
Receive data setup 51/ before RCLK	t_{SDRI}				3		
Receive data hold 51/ after RCLK	t_{HDRI}				3		
Serial Ports: External or Internal Clock Switching Requirements							
RFS delay after RCLK 53/ (internally generated RFS)	t_{DFSE}	See figure 6. 21/ 27/	9, 10, 11	01,02		13.5	ns
RFS hold after RCLK 53/ (internally generated RFS)	t_{HOFSE}				3		
Serial Ports: External Clock Switching Requirements							
TFS delay after TCLK 53/ (internally generated TFS)	t_{DFSE}	See figure 6. 21/ 27/	9, 10, 11	01,02		13.5	ns
TFS hold after TCLK 53/ (internally generated TFS)	t_{HOFSE}				3		
Transmit data delay 53/ after TCLK	t_{DDTE}					16.5	
Transmit data hold 53/ after TCLK	t_{HDTE}				5		
Serial Ports: Internal Clock Switching Requirements							
TFS delay after TCLK 53/ (internally generated TFS)	t_{DFSI}	See figure 6. 21/ 27/	9, 10, 11	01,02		4.5	ns
TFS hold after TCLK 53/ (internally generated TFS)	t_{HOFSI}				-1.5		
Transmit data delay 53/ after TCLK	t_{DDTI}					7.5	
Transmit data hold 53/ after TCLK	t_{HDTI}				0		
TCLK/RCLK width	t_{SCLKIW}				(SCLK/2)-2	(SCLK/2)+2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Serial Ports: Enable and Three State Switching Requirements							
Data enable from external TCLK 53/	t_{DDTEN}	See figure 6. 21/ 27/	9, 10, 11	01,02	3.5		ns
Data disable from external TCLK 53/	t_{DDTTE}					11	
Data enable from internal TCLK 53/	t_{DDTIN}				0		
Data disable from internal TCLK 53/	t_{DDTTI}					3	
TCLK/RCLK delay from CLKIN	t_{DCLK}					22.5+3DT/8	
SPORT disable after CLKIN	t_{DPTR}					17.5	
Serial Ports: Gated SCLK with External TFS (Mesh Multiprocessing)							
TFS setup before CLKIN 54/	t_{STFSCK}	See figure 6. 21/	9, 10, 11	01	5		ns
				02	5.1		
TFS hold afterCLKIN 54/	t_{HTFSCK}			01,02	$t_{CK}/2$		
Serial Ports: External Late Frame Sync Switching Requirements							
Data delay from late external TFS or RFS with MCE = 1, MFD = 0 55/	$t_{DDTLFSE}$	See figure 6. 21/ 27/	9, 10, 11	01,02		13.1	ns
Data enable from late FS or MCE = 1, MFD = 0 55/	$t_{DDTENFS}$				3		
JTAG Test Access Port Emulatiom Timing and Switching Requirements							
TCK period	t_{TCK}	See figure 6. 21/	9, 10, 11	01,02	t_{CK}		ns
TDI, TMS, setup before TCK high	t_{STAP}				5.5		
TDI, TMS, hold after TCK high	t_{HTAP}				6.5		
Systems inputs setup before TCK low 56/	t_{SSYS}			01	7		
				02	8		
Systems inputs hold after TCK low 56/	t_{HSYS}			01,02	18.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
JTAG Test Access Port Emulatiom Timing and Switching Requirements - Continued.							
$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	See figure 6. 21/	9, 10, 11	01,02	$4t_{CK}$		ns
TD0 delay from TCK low before TCK low	t_{DTDO}					13.5	
Systems outputs delay 57/ after TCK low	t_{DSYS}					20	

1/ Device type 01, -40°C ≤ T_C ≤ +100°C and +4.75 V dc ≤ V_{DD} ≤ +5.25 V dc, unless otherwise specified.
Device type 02, -55°C ≤ T_C ≤ +125°C and +4.75 V dc < V_{DD} ≤ +5.25 V dc, unless otherwise specified.

2/ Applies to input and bidirectional pins: DATA47-0, ADDR31-0, RD, WR, SW, ACK, SBTS, IRQy2-0, FLAGy3-0, HBG, CSy, DMAR1, DMAR2, BR6-1, IDy2-0, RPBA, CPAy, TFSy0, TFSy1, RFSy0, RFSy1, LyxDAT3-0, LyxCLK, LyxACK, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, BMSA, BMSBCD, TMS, TDI, TCK, HBR, DRy0, DRy1, TCLKy0, TCLKy1, RCLKy0, RCLKy1. For the group of signals LyxDAT3-0, LyxCLK, and LyxACK, only Link Port 4 signals (Ly4DT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

3/ Applies to input pins: CLKIN, RESET,TRST.

4/ Applies to output and bidirectional pins: DATA47-0, ADDR31-0, $\overline{\text{MS}}$3-0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, ADRCLK, $\overline{\text{SW}}$, ACK, FLAGy3-0, TIMEXPy, HBG, REDY, DMAG1, DMAG2, BR6-1, CPAy, DTyO, DTy1, TCLKy0, TCLKy1, RCLKy0, RCLKy1, TFSy0, TFSy1, RFSy0, RFSy1, LyxDAT3-0, LyxCLK, LyxACK, BMSA, BMSBCD, TDO, EMU. For the group of signals LyxDAT3-0, LyxCLK, and LyxACK, only Link Port 4 signals (Ly4DAT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

5/ See "output drive currents" for typical drive current capabilities.

6/ Applies to input pins: IRQy2-0, CSy, IDy2-0, EBOOTA, LBOOTA.

7/ Applies to input pins with internal pull-ups: DRy0, DRy1, TDI.

8/ Individual signals tested to limits of I_{IH} = 10 µA and I_{ILP} = 150 µA at die level prior to assembly. At the module level, all eight DR0 and DRy1 inputs connected together are tested to limits of I_{IH} = 80 µA and I_{ILP} = 1200 µA.

9/ Applies to bussed input pins: SBTS, HBR, DMAR1, DMAR2, RPBA, EBOOTBCD, LBOOTBCD, CLKIN, RESET, TCK.

10/ Applies to bussed input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS.

11/ Applies to three statable pins and bidirectional pins; FLAGy3-0, BMSA, TD0, TFSy0, TFSy1, RFSy0, RFSy1. TFSy0, TFSy1, RFSy0, and RFSy1 are tested individually to the limits of I_{OZH} = 10 µA and I_{OZL} = 10 µA at die level. At the module level, eight pins connected together are tested to limits of I_{OZH} = 80 µA and I_{OZL} = 80 µA.

12/ Applies to three statable pins with internal pull-ups: DTy0, DTy1, TCLKy0, TCLKy1, RCLKy0, RCLKy1. Individual signals tested to limit of I_{OZH} = 10 µA and I_{OZLS} = 150 µA at die level. At the module level, eight serial port pins connected together are tested to limits of I_{OZH} = 80 µA and I_{OZLS} = 1200 µA.

13/ Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with a 2 kΩ resistor during reset in a multiprocessor system, when ID2-0 = 001 and another single processor is not requesting bus mastership.)

14/ Applies to CPAy pin.

TABLE 1. Electrical performance characteristics - Continued.

15/ Applies to bussed three statable pins and bidirectional pins: DATA47-0, ADDR31-0, MS3-0, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, SW, ACK, HBG, REDY, DMAG1, DMAG2, BMSBCD, BR6-1, EMU. (Note that ACK is pulled up internally with a 2 kΩ resistor during reset in a multiprocessor system, when ID2-0 = 001 and another single processor is not requesting bus mastership.) HBG and EMU are not tested for leakage current.

16/ Applies to three statable pins with internal pull-downs: LyxDAT3-0, LyxCLK, LyxACK. Only Link Port 4 signals (Ly4DAT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

17/ Applies to ACK pin when keeper latch enabled.

18/ Applies to V_{DD} pins. Conditions of operation: each processor executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from cache each internal memory block, and one DMA transfer occurring form/to internal memory at t_{CK} = 25 ns. Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers: $P_{TOTAL} = P_{INT} + P_{EXT}$. Internal power dissipation is $P_{INT} = I_{DDIN} \times V_{DD}$. The external component of total power dissipation is caused by the switching of output pins, and depends on: the number of pins that switch each cycle (O), the maximum frequency at which they can switch (f), the load capacitance per pin (C), the output voltage swing (V_{DD}): $P_{EXT} = O \times C \times V_{DD}^2 \times f$. Address and data pins can switch at f = 1/ ($2t_{CK}$). WR can switch at 1/ t_{CK}. MSx pins switch at 1/ ($2t_{CK}$).

19/ Applies to V_{DD} pins. Idle denotes like device type state during execution of IDLE instruction.

20/ Not tested. Nominal value of 15 pF derived through RC measurement at design characterization.

21/ Timing test limits are target limits for the module, based on calculated predictions only. The module is 100% production tested, and the test limits are guaranteed by design/analysis, and characterization testing (at $T_A = 25^\circ C$) of the individual discrete mircocontrollers. The limits shown are based on a CLKIN frequency of 40 MHz. DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns: DT = t_{CK} - 25 ns. Link and serial ports: all are 100% tested at die level, serial ports are 100% AC tested at module level, only Link Port 4 from each processor is AC tested at module level, then link and serial ports are DC tested at module level.

22/ Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while RESET is low, assuming stable V_{DD} and CLKIN (not including start-up time of external oscillator).

23/ Only required if multiple microcontrollers must come out of reset synchronous to CLKIN with program counters (PC) equal (i. e. for a SIMD system). Not required for multiple microcontrollers communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes it self automatically after reset.

24/ Only required for IRQx recognition in the following cycle.

25/ Applies only if t_{SIR} and t_{HIR} requirements are not met.

26/ Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

27/ W = (number of wait states specified in WAIT register) times t_{CK}. HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0). H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0). I = t_{CK} (if bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

28/ Data delay/setup: User must meet t_{DAD} or t_{DRLD} or synchronous specification t_{SSDATI}.

29/ For MSx, SW, and BMS, the falling edge is referenced.

30/ Data hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. To determine system hold time, the data output hold time in a particular system, first calculate $t_{DECAY} = C_L \Delta V / I_L$. Choose ΔV to be the difference between the microcontroller's output voltage and the input threshold for the device requiring the hold. Typical ΔV is 0.4 volt. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i. e. t_{HDWD} for the write cycle).

31/ ACK delay/setup: User must meet t_{DSAK} or t_{DAAK} or synchronous specification t_{SACKC}.

32/ To determine system hold time, the data output hold time in a particular system, first calculate $t_{DECAY} = C_L \Delta V / I_L$. Choose ΔV to be the difference between the microcontroller's output voltage and the input threshold for the device requiring the hold. Typical ΔV is 0.4 volt. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i. e. t_{HDWD} for the write cycle).

TABLE 1. Electrical performance characteristics - Continued.

33/ t_{SRWLI}(min) = 10 + 5DT/16, when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI}(min) = 4.5 + DT/8.

34/ t_{DACKAD} is true only if the address and SW inputs have setup times (before CLKIN) greater than 10.5 + DT/8 and less than 19 + 3DT/4. If the address and SW inputs have setup times greater than 19 + 3DT/4, then ACK is valid 15 + DT/4 (max) after CLKIN. A slave that sees an address with a M field match will respond with ACK reguardless of the state of MMSWS or strobes. A slave will three state ACK every cycle with t_{ACKTR}.

35/ For first asynchronous access after HBR and CS asserted, ADDR 31-0 must be a non-MMS value 1/2t_{CK} before $\overline{RD}$ or WR goes low or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when HBG is asserted.

36/ Only required for recognition in the current cycle.

37/ CPA assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

38/ (O/D) = open drain, (A/D) = active drain.

39/ Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR 31-0 must be a non-MMS value 1/2t_{CK} before $\overline{RD}$ or WR goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when HBG is asserted. For address bits to be driven during asynchronous host accesses, see QML manufacturer.

40/ Strobes = $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, PAGE, and DMAG.

41/ In addition to bus master transition cycles, these specifications also apply to bus master and bus slave synchronous read/write.

42/ Memory interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{SW}$, $\overline{HBG}$, PAGE, $\overline{DMAGx}$, and $\overline{BMS}$ (in EPROM boot mode).

43/ Only required for recognition in the current cycle.

44/ $t_{SDATDGL}$ is the data setup requirement if DMARx is not being used to hold off completion of a write. Otherwise, if $\overline{DMARx}$ low holds off completion of the write , the data can be driven t_{DATDRH} after DMARx is brought high.

45/ $t_{VDATDGH}$ is valid if DMARx is not being used to hold off completion of a read. If DMARx is used to prolong the read, then $t_{VDATDGH} = 7 + 9DT/16 + (n * t_{CK})$ where "n" equals the number of extra cycles that the access is prolonged.

46/ LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receivers link buffer is not about to fill.

47/ Only required for interrupt recognition in the current cycle.

48/ t_{SLSK} is the maximum delay that can be introduced in the transmission path of LDATA relative LCLK:
$t_{SLSK} = (t_{LCLKTWH} - t_{DLDCH})^{min} - t_{SLDCL}^{max}$.

49/ If link port 2 is transmitter, t_{SLSK} = 0.23 ns. Because of this small margin, extreme care must be taken in system design. If adequate setup time cannot be assured, link port operation should be limited to 1X, or system CLKIN frequency should be reduced to increase the setup margin at 2X.

50/ t_{HLSK} is the maximum delay that can be introduced in the transmission path of LCLK relative to LDATA:
$t_{HLSK} = (t_{LCLKTWL} - t_{HLDCH})^{min} - t_{HLDCL}^{max}$.

51/ Reference to sample edge.

52/ RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

53/ Reference to drive edge.

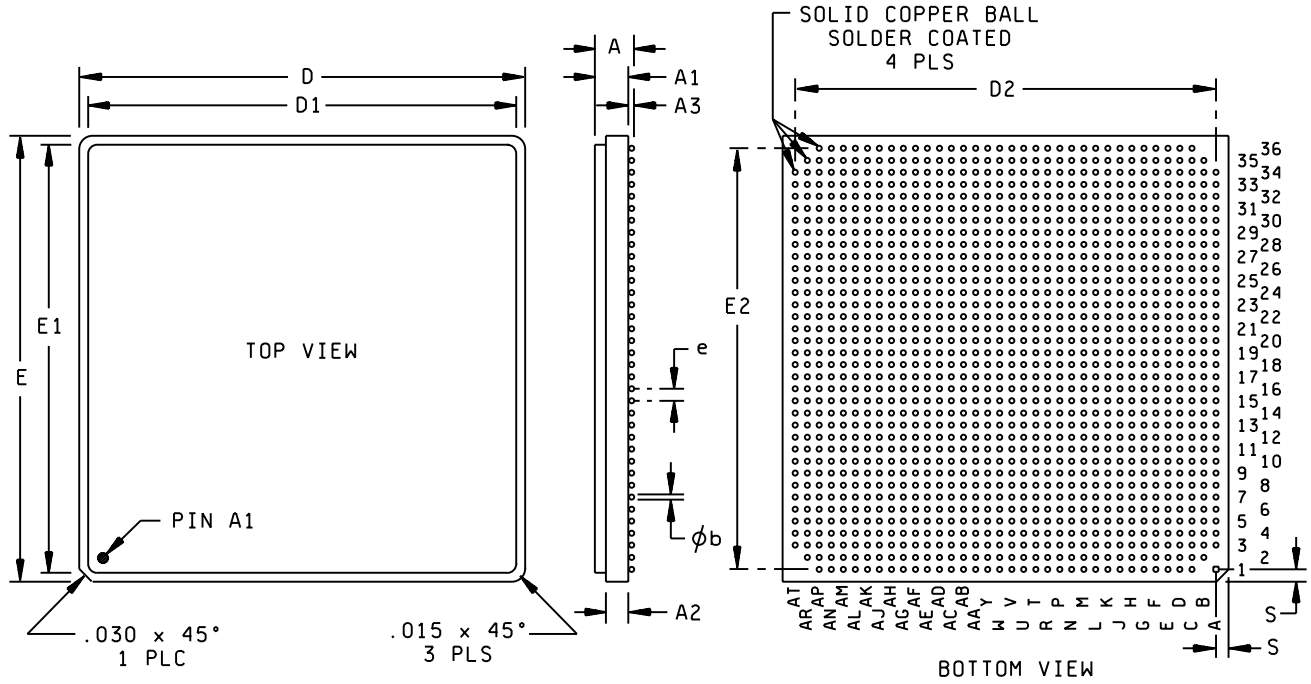
54/ Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.

55/ MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

56/ System inputs = DATA47-0, ADDR31-0, RD, $\overline{WR}$, ACK, SBTS, $\overline{SW}$, $\overline{HBR}$, HBG, CS, $\overline{DMAR1}$, $\overline{DMAR2}$, BR6-1, IDy2-0, RPBA, IRQ2-0, FLAG3-0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCLK, LxACK, EBOOT, LBOOT, BMS, CLKIN, RESET.

57/ System outputs = DATA47-0, ADDR31-0, MS3-0, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, BR6-1, CPA, FLAG3-0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCLK, LxACK, BMS.

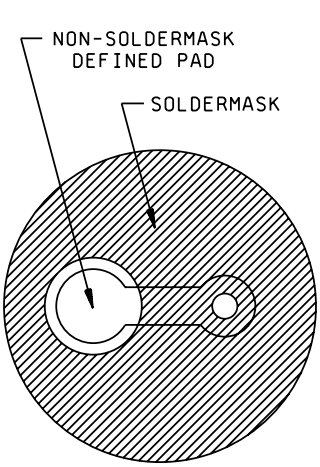
Case outline X.



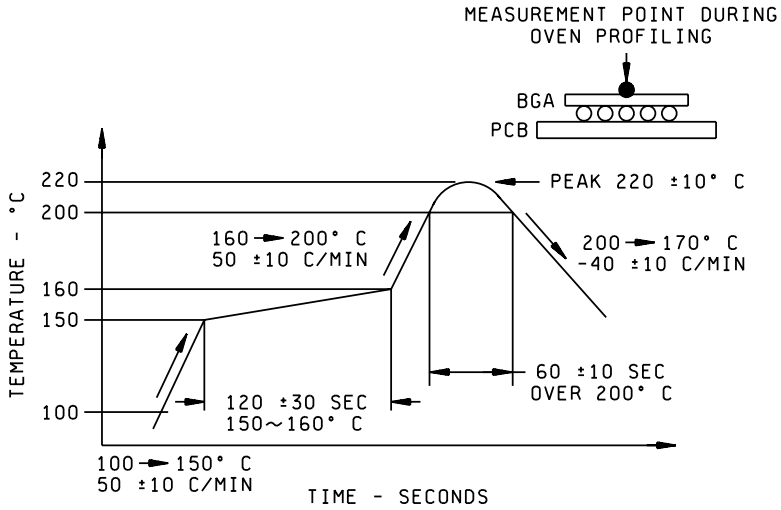
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A 1/		5.08		0.200
A1 1/		4.32		0.170
A2	2.29	2.79	0.090	0.110
A3	0.61 TYP		0.024 TYP	
øb	0.84 TYP		0.033 TYP	
e	1.14	1.40	0.045	0.055
D/E	46.69	47.30	1.838	1.862
D1/E1	45.34	45.59	1.785	1.795
D2/E2	44.16	44.76	1.738	1.762
S	1.02	1.52	0.040	0.060

NOTES:
1. Package height is measured at the sidewall. At reduced ambient pressure, the center of the lid will extend beyond the height measured (dimensions A and A1) at the sidewall. See figure 3.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. Pin numbers and letters are for reference only.

FIGURE 1. Case outline(s).



PRINTED CIRCUIT
BOARD PAD LAYOUT
SEE NOTE 1

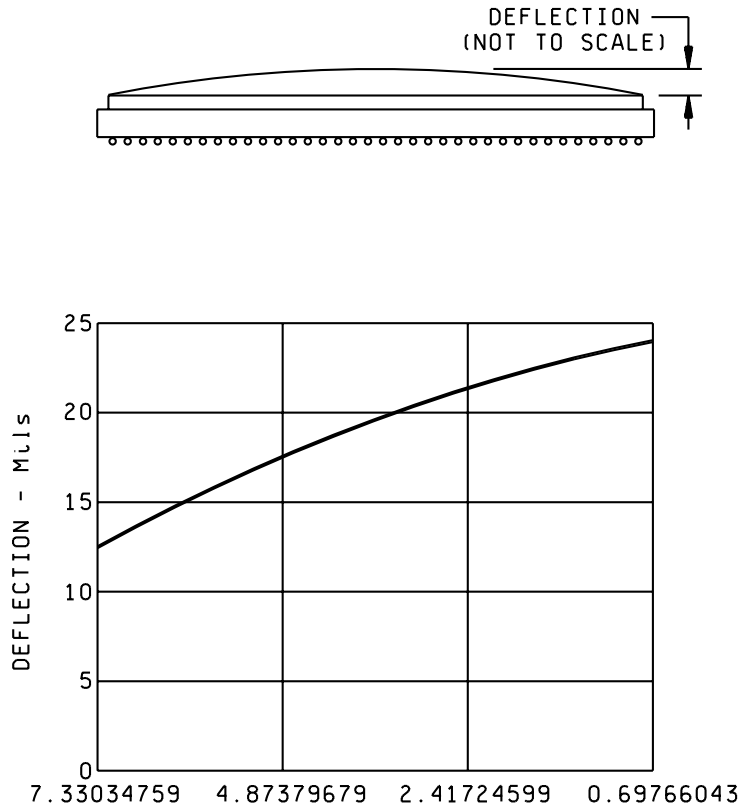


REFLOW PROFILE

NOTES:

1. A classical dog bone style pad or a pad with microvia should be used. A solder pad diameter of 0.65 mm is recommended. The pad should be non-soldermask defined. A solder paste print of 0.7 mm diameter with a thickness of 0.15 to 0.2 mm is recommended. Normal solder paste alloy can be used, example, 60/40, 63/37, and so on.
2. Card level reliability should be determined by the customer, based upon the specific application. TCE mismatch of the ceramic module and printed circuit board can result in stress failures based upon the extremes of the temperature cycles and the magnitude of the TCE mismatch. Recent studies of the temperature cycle effects using semi-continuous monitoring of the resistance has shown the assemblies capable of surviving 400 temperature cycles of -40°C to +125°C ambient, when assembled to standard FR4 board. Based on these results and the Coffin/Manson acceleration factor equation, a life in excess of 10 years is predicted when the device is operated at room temperature and cycled once a day from +25°C to +75°C ambient, again when considering the worst case condition of a standard FR4 board. Other life predictions can be calculated based upon specific thermal cycling extremes and frequency.
3. Literature indicates extended life can be obtained by using printed circuit board material which matches the TCE of the ceramic within ±2 PPM, such as Arlon 85NT. Quoted material in no way should be construed as a recommendation of that material, but is only provided to give customers additional information and alternatives. Thermal cycle life is affected by the specific board and application: therefore the customer should conduct their own tests for their specific application.
4. There are a series of daisy chain contacts (TEST1, TEST2, through TEST16) available on the package which, if wired up in the final assembly could be used to monitor the relability of the package interconnect on the actual board, in real time and warn of any impending failure. Refer to the Approved Source data sheet for additional design features of the package.

FIGURE 2. Assembly recommendations for maximum reliability.



TYPICAL LID DEFLECTION
(mils) vs EXTERNAL PRESSURE

FIGURE 3. Lid deflection.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A3	(GND)	B10	(unused)	C15	(unused)	D19	(VDD)
A4	(GND)	B11	(unused)	C16	(unused)	D20	(unused)
A5	(GND)	B12	(unused)	C17	(unused)	D21	(GND)
A6	(GND)	B13	(unused)	C18	(GND)	D22	(unused)
A7	(GND)	B14	(unused)	C19	(VDD)	D23	(GND)
A8	(GND)	B15	(unused)	C20	(unused)	D24	(unused)
A9	(GND)	B16	(unused)	C21	(unused)	D25	(GND)
A10	(GND)	B17	(unused)	C22	(unused)	D26	(unused)
A11	(GND)	B18	(unused)	C23	(unused)	D27	(GND)
A12	(GND)	B19	(unused)	C24	(unused)	D28	(unused)
A13	(GND)	B20	(unused)	C25	(unused)	D29	(GND)
A14	(GND)	B21	(unused)	C26	(unused)	D30	(unused)
A15	(GND)	B22	(unused)	C27	(unused)	D31	(GND)
A16	(GND)	B23	(unused)	C28	(unused)	D32	(unused)
A17	(GND)	B24	(unused)	C29	(unused)	D33	(GND)
A18	(GND)	B25	(unused)	C30	(unused)	D34	(unused)
A19	(GND)	B26	(unused)	C31	(unused)	D35	(unused)
A20	(GND)	B27	(unused)	C32	(unused)	D36	(GND)
A21	(GND)	B28	(unused)	C33	(GND)	E1	(GND)
A22	(GND)	B29	(unused)	C34	(unused)	E2	(unused)
A23	(GND)	B30	(unused)	C35	(VDD)	E3	(unused)
A24	(GND)	B31	(unused)	C36	(GND)	E4	(unused)
A25	(GND)	B32	(unused)	D1	(GND)	E5	(GND)
A26	(GND)	B33	(unused)	D2	(unused)	E6	(unused)
A27	(GND)	B34	(unused)	D3	(unused)	E7	(GND)
A28	(GND)	B35	(GND)	D4	(GND)	E8	(unused)
A29	(GND)	C1	(GND)	D5	(unused)	E9	(GND)
A30	(GND)	C2	(GND)	D6	(GND)	E10	(unused)
A31	(GND)	C3	(unused)	D7	(unused)	E11	(GND)
A32	(GND)	C4	(VDD)	D8	(GND)	E12	(unused)
A33	(GND)	C5	(unused)	D9	(unused)	E13	(GND)
A34	(GND)	C6	(unused)	D10	(GND)	E14	(unused)
B2	(GND)	C7	(unused)	D11	(unused)	E15	(GND)
B3	(unused)	C8	(unused)	D12	(GND)	E16	(unused)
B4	(unused)	C9	(unused)	D13	(unused)	E17	(unused)
B5	(unused)	C10	(unused)	D14	(GND)	E18	(VDD)
B6	(unused)	C11	(unused)	D15	(unused)	E19	(VDD)
B7	(unused)	C12	(unused)	D16	(GND)	E20	(unused)
B8	(unused)	C13	(unused)	D17	(unused)	E21	(unused)
B9	(unused)	C14	(unused)	D18	(VDD)	E22	(GND)

See note at end of table.

FIGURE 4. Terminal connections.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
E23	(unused)	F27	(GND)	G31	(unused)	H35	(unused)
E24	(GND)	F28	(unused)	G32	(GND)	H36	(GND)
E25	(unused)	F29	(GND)	G33	(unused)	J1	(GND)
E26	(GND)	F30	(unused)	G34	(unused)	J2	(unused)
E27	(unused)	F31	(GND)	G35	(unused)	J3	(unused)
E28	(GND)	F32	(unused)	G36	(GND)	J4	(unused)
E29	(unused)	F33	(GND)	H1	(GND)	J5	(GND)
E30	(GND)	F34	(unused)	H2	(unused)	J6	(unused)
E31	(unused)	F35	(unused)	H3	(unused)	J7	(GND)
E32	(GND)	F36	(GND)	H4	(GND)	J8	(unused)
E33	(unused)	G1	(GND)	H5	(unused)	J9	(GND)
E34	(unused)	G2	(unused)	H6	(GND)	J10	(unused)
E35	(unused)	G3	(unused)	H7	(unused)	J11	(TEST11)
E36	(GND)	G4	(unused)	H8	(GND)	J12	DATA10
F1	(GND)	G5	(GND)	H9	(unused)	J13	LB2ACK
F2	(unused)	G6	(unused)	H10	(GND)	J14	LB2CLK
F3	(unused)	G7	(GND)	H11	(unused)	J15	LB2DAT0
F4	(GND)	G8	(unused)	H12	(TEST11)	J16	LB2DAT1
F5	(unused)	G9	(GND)	H13	LB1ACK	J17	GND
F6	(GND)	G10	(unused)	H14	LB1CLK	J18	VDD
F7	(unused)	G11	(GND)	H15	LB1DAT0	J19	DRA1
F8	(GND)	G12	(unused)	H16	LB1DAT1	J20	DRA0
F9	(unused)	G13	(GND)	H17	LB2DAT2	J21	ACK
F10	(GND)	G14	(unused)	H18	LB2DAT3	J22	PAGE
F11	(unused)	G15	(GND)	H19	RCLKA1	J23	GND
F12	(GND)	G16	GND	H20	RCLKA0	J24	VDD
F13	(unused)	G17	LB1DAT2	H21	REDY	J25	GND
F14	(GND)	G18	LB1DAT3	H22	VDD	J26	(TEST14)
F15	(unused)	G19	RFSA1	H23	GND	J27	(unused)
F16	(GND)	G20	RFSA0	H24	VDD	J28	(GND)
F17	(TEST12)	G21	VDD	H25	(TEST14)	J29	(unused)
F18	(TEST12)	G22	(GND)	H26	(unused)	J30	(GND)
F19	(TEST13)	G23	(unused)	H27	(GND)	J31	(unused)
F20	(TEST13)	G24	(GND)	H28	(unused)	J32	(GND)
F21	(GND)	G25	(unused)	H29	(GND)	J33	(unused)
F22	(unused)	G26	(GND)	H30	(unused)	J34	(unused)
F23	(GND)	G27	(unused)	H31	(GND)	J35	(unused)
F24	(unused)	G28	(GND)	H32	(unused)	J36	(GND)
F25	(GND)	G29	(unused)	H33	(GND)	K1	(GND)
F26	(unused)	G30	(GND)	H34	(unused)	K2	(unused)

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
K3	(unused)	L7	(GND)	M11	DATA23	N15	$\overline{\text{DMAG2}}$
K4	(GND)	L8	(unused)	M12	DATA13	N16	SBTS
K5	(unused)	L9	(TEST10)	M13	DATA2	N17	(unused)
K6	(GND)	L10	DATA30	M14	$\overline{\text{DATA0}}$	N18	(unused)
K7	(unused)	L11	DATA22	M15	$\overline{\text{DMAG1}}$	N19	(unused)
K8	(GND)	L12	DATA12	M16	$\overline{\text{DMAR1}}$	N20	(unused)
K9	(unused)	L13	LB4ACK	M17	DMAR2	N21	(unused)
K10	GND	L14	LB4CLK	M18	VDD	N22	LA4ACK
K11	DATA21	L15	LB4DAT0	M19	DTA1	N23	LA4CLK
K12	DATA11	L16	LB4DAT1	M20	$\overline{\text{DTA0}}$	N24	LA4DAT0
K13	LB3ACK	L17	LB4DAT2	M21	CPAA	N25	LA4DAT1
K14	LB3CLK	L18	LB4DAT3	M22	LA3ACK	N26	LA4DAT2
K15	LB3DAT0	L19	TCLKA1	M23	LA3CLK	N27	LA4DAT3
K16	LB3DAT1	L20	$\overline{\text{TCLKA}}$0	M24	LA3DAT0	N28	GND
K17	LB3DAT2	L21	RESET	M25	LA3DAT1	N29	VDD
K18	LB3DAT3	L22	LA2ACK	M26	LA3DAT2	N30	(GND)
K19	TFSA1	L23	LA2CLK	M27	LA3DAT3	N31	(unused)
K20	$\overline{\text{TFSA}}$0	L24	LA2DAT0	M28	VDD	N32	(GND)
K21	CSA	L25	LA2DAT1	M29	(TEST15)	N33	(unused)
K22	LA1ACK	L26	LA2DAT2	M30	(unused)	N34	(unused)
K23	LA1CLK	L27	LA2DAT3	M31	(GND)	N35	(unused)
K24	LA1DAT0	L28	(TEST15)	M32	(unused)	N36	(GND)
K25	LA1DAT1	L29	(unused)	M33	(GND)	P1	(GND)
K26	LA1DAT2	L30	(GND)	M34	(unused)	P2	(unused)
K27	LA1DAT3	L31	(unused)	M35	(unused)	P3	(unused)
K28	(unused)	L32	(GND)	M36	(GND)	P4	(GND)
K29	(GND)	L33	(unused)	N1	(GND)	P5	(unused)
K30	(unused)	L34	(unused)	N2	(unused)	P6	(GND)
K31	(GND)	L35	(unused)	N3	(unused)	P7	(unused)
K32	(unused)	L36	(GND)	N4	(unused)	P8	RFSB1
K33	(GND)	M1	(GND)	N5	(GND)	P9	DRB0
K34	(unused)	M2	(unused)	N6	(unused)	P10	DATA33
K35	(unused)	M3	(unused)	N7	(GND)	P11	DATA25
K36	(GND)	M4	(GND)	N8	VDD	P12	DATA15
L1	(GND)	M5	(unused)	N9	RCLKB0	P13	DATA4
L2	(unused)	M6	(GND)	N10	DATA33	P14	GND
L3	(unused)	M7	(unused)	N11	DATA24	P15	GND
L4	(unused)	M8	(TEST10)	N12	DATA14	P16	IDB0
L5	(GND)	M9	RFSB0	N13	DATA3	P17	IDB1
L6	(unused)	M10	DATA31	N14	DATA1	P18	IDB2

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P19	(unused)	R23	RPBA	T27	ADDR31	U31	(TEST16)
P20	(unused)	R24	MS0	T28	IRQA0	U32	(unused)
P21	(unused)	R25	MS1	T29	EBOOTA	U33	(unused)
P22	GND	R26	MS2	T30	GND	U34	(unused)
P23	GND	R27	MS3	T31	(GND)	U35	(unused)
P24	GND	R28	IDA0	T32	(unused)	U36	(GND)
P25	GND	R29	LBOOTA	T33	(GND)	V1	(GND)
P26	GND	R30	(GND)	T34	(unused)	V2	(GND)
P27	GND	R31	(unused)	T35	(unused)	V3	(VDD)
P28	IDA1	R32	(GND)	T36	(GND)	V4	(VDD)
P29	IDA2	R33	(unused)	U1	(GND)	V5	(VDD)
P30	(unused)	R34	(unused)	U2	(unused)	V6	(TEST9)
P31	(GND)	R35	(unused)	U3	(unused)	V7	CSB
P32	(unused)	R36	(GND)	U4	(unused)	V8	TCLKB1
P33	(GND)	T1	(GND)	U5	(unused)	V9	DATA45
P34	(unused)	T2	(unused)	U6	(TEST9)	V10	DATA37
P35	(unused)	T3	(unused)	U7	GND	V11	DATA28
P36	(GND)	T4	(GND)	U8	TFSB1	V12	DATA19
R1	(GND)	T5	(unused)	U9	DTB0	V13	DATA8
R2	(unused)	T6	(GND)	U10	DATA36	V14	FLAGB0
R3	(unused)	T7	VDD	U11	CLKIN	V15	FLAGB1
R4	(unused)	T8	DRB1	U12	DATA18	V16	FLAGB2
R5	(GND)	T9	TCLKB0	U13	DATA7	V17	FLAGB3
R6	(unused)	T10	DATA35	U14	VDD	V18	VDD
R7	(GND)	T11	DATA27	U15	GND	V19	VDD
R8	RCLKB1	T12	DATA17	U16	TIMEXPB	V20	GND
R9	TFSB0	T13	DATA6	U17	VDD	V21	VDD
R10	DATA34	T14	VDD	U18	VDD	V22	BMSA
R11	DATA26	T15	GND	U19	VDD	V23	GND
R12	DATA16	T16	GND	U20	VDD	V24	ADDR20
R13	DATA5	T17	GND	U21	VDD	V25	ADDR21
R14	GND	T18	GND	U22	GND	V26	ADDR22
R15	GND	T19	GND	U23	GND	V27	ADDR23
R16	GND	T20	(unused)	U24	ADDR24	V28	FLAGA0
R17	IRQB0	T21	(unused)	U25	ADDR25	V29	FLAGA1
R18	IRQB1	T22	(unused)	U26	ADDR26	V30	TIMEXPA
R19	IRQB2	T23	(unused)	U27	ADDR27	V31	(TEST16)
R20	GND	T24	ADDR28	U28	IRQA1	V32	(VDD)
R21	GND	T25	ADDR29	U29	IRQA2	V33	(VDD)
R22	GND	T26	ADDR30	U30	TDOA	V34	(GND)

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
V35	(VDD)	Y3	(unused)	AA7	GND	AB11	RSFC1
V36	(GND)	Y4	(unused)	AA8	HBR	AB12	RFSC0
W1	(GND)	Y5	(unused)	AA9	BR2	AB13	TDOB
W2	(GND)	Y6	(TEST8)	AA10	CPAB	AB14	(unused)
W3	(VDD)	Y7	VDD	AA11	DATA44	AB15	(unused)
W4	(VDD)	Y8	SW	AA12	DATA42	AB16	(GND)
W5	(VDD)	Y9	BR1	AA13	DATA40	AB17	(GND)
W6	(TEST8)	Y10	DATA<47>	AA14	(unused)	AB18	(GND)
W7	(GND)	Y11	DATA<43>	AA15	(unused)	AB19	(GND)
W8	DTB1	Y12	DATA<41>	AA16	GND	AB20	VDD
W9	DATA46	Y13	DATA<39>	AA17	GND	AB21	VDD
W10	DATA38	Y14	(unused)	AA18	GND	AB22	VDD
W11	DATA29	Y15	(unused)	AA19	GND	AB23	VDD
W12	DATA20	Y16	GND	AA20	GND	AB24	ADDR4
W13	DATA9	Y17	GND	AA21	VDD	AB25	ADDR5
W14	(unused)	Y18	VDD	AA22	VDD	AB26	ADDR6
W15	(unused)	Y19	VDD	AA23	GND	AB27	ADDR7
W16	GND	Y20	VDD	AA24	ADDR8	AB28	FLAGD2
W17	VDD	Y21	VDD	AA25	ADDR9	AB29	IRQD2
W18	VDD	Y22	GND	AA26	ADDR10	AB30	(GND)
W19	VDD	Y23	GND	AA27	ADDR11	AB31	(unused)
W20	GND	Y24	ADDR12	AA28	FLAG01	AB32	(GND)
W21	VDD	Y25	ADDR13	AA29	IRQD1	AB33	(unused)
W22	VDD	Y26	ADDR14	AA30	VDD	AB34	(unused)
W23	GND	Y27	ADDR15	AA31	(GND)	AB35	(unused)
W24	ADDR16	Y28	FLAGD0	AA32	(unused)	AB36	(GND)
W25	ADDR17	Y29	IRQD0	AA33	(GND)	AC1	(GND)
W26	ADDR18	Y30	(GND)	AA34	(unused)	AC2	(unused)
W27	ADDR19	Y31	(TEST1)	AA35	(unused)	AC3	(unused)
W28	FLAGA3	Y32	(unused)	AA36	(GND)	AC4	(GND)
W29	FLAGA2	Y33	(unused)	AB1	(GND)	AC5	(unused)
W30	TDI	Y34	(unused)	AB2	(unused)	AC6	(GND)
W31	(TEST1)	Y35	(unused)	AB3	(unused)	AC7	(unused)
W32	(VDD)	Y36	(GND)	AB4	(unused)	AC8	GND
W33	(VDD)	AA1	(GND)	AB5	(GND)	AC9	BR4
W34	(GND)	AA2	(unused)	AB6	(unused)	AC10	FLAGC0
W35	VDD	AA3	(unused)	AB7	(GND)	AC11	RCLKC1
W36	(GND)	AA4	(GND)	AB8	HBG	AC12	RCLKC0
Y1	(GND)	AA5	(unused)	AB9	BR3	AC13	ADRCLK
Y2	(unused)	AA6	(GND)	AB10	(GND)	AC14	VDD

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AC15	VDD	AD19	RFSD1	AE23	LD2CLK	AF27	LD3DAT3
AC16	VDD	AD20	RFSD0	AE24	LD2DAT0	AF28	(TEST2)
AC17	VDD	AD21	BMSBCD	AE25	LD2DAT1	AF29	(unused)
AC18	GND	AD22	LD1ACK	AE26	LD2DAT2	AF30	(GND)
AC19	GND	AD23	LD1CLK	AE27	LD2DAT3	AF31	(unused)
AC20	GND	AD24	LD1DAT0	AE28	VDD	AF32	(GND)
AC21	VDD	AD25	LD1DAT1	AE29	(TEST2)	AF33	(unused)
AC22	VDD	AD26	LD1DAT2	AE30	(unused)	AF34	(unused)
AC23	TIMEXPC	AD27	LD1DAT3	AE31	(GND)	AF35	(unused)
AC24	ADDR0	AD28	TIMEXPD	AE32	(unused)	AF36	(GND)
AC25	ADDR1	AD29	GND	AE33	(GND)	AG1	(GND)
AC26	ADDR2	AD30	(GND)	AE34	(unused)	AG2	(unused)
AC27	ADDR3	AD31	(unused)	AE35	(unused)	AG3	(unused)
AC28	FLAGD3	AD32	(GND)	AE36	(GND)	AG4	(GND)
AC29	VDD	AD33	(unused)	AF1	(GND)	AG5	(unused)
AC30	(unused)	AD34	(unused)	AF2	(unused)	AG6	(GND)
AC31	(GND)	AD35	(unused)	AF3	(unused)	AG7	(unused)
AC32	(unused)	AD36	(GND)	AF4	(unused)	AG8	(GND)
AC33	(GND)	AE1	(GND)	AF5	(GND)	AG9	(unused)
AC34	(unused)	AE2	(unused)	AF6	(unused)	AG10	GND
AC35	(unused)	AE3	(unused)	AF7	(GND)	AG11	DTC1
AC36	(GND)	AE4	(GND)	AF8	(unused)	AG12	DTC0
AD1	(GND)	AE5	(unused)	AF9	(TEST7)	AG13	IRQC0
AD2	(unused)	AE6	(GND)	AF10	FLAGC3	AG14	IRQC1
AD3	(unused)	AE7	(unused)	AF11	TCLKC1	AG15	IRQC2
AD4	(unused)	AE8	(TEST7)	AF12	TCLKC0	AG16	IDC0
AD5	(GND)	AE9	BR6	AF13	LC2ACK	AG17	IDC1
AD6	(unused)	AE10	FLAGC2	AF14	LC2CLK	AG18	IDC2
AD7	(GND)	AE11	TFSC1	AF15	LC2DAT0	AG19	TFSD1
AD8	VDD	AE12	TFSC0	AF16	LC2DAT1	AG20	TFSD0
AD9	BR5	AE13	LC1ACK	AF17	LC2DAT2	AG21	CSD
AD10	FLAGC1	AE14	LC1CLK	AF18	LC2DAT3	AG22	LD4ACK
AD11	DRC1	AE15	LC1DAT0	AF19	DRD1	AG23	LD4CLK
AD12	DRC0	AE16	LC1DAT1	AF20	DRD0	AG24	LD4DAT0
AD13	CPAC	AE17	LC1DAT2	AF21	RD	AG25	LD4DAT1
AD14	CSC	AE18	LC1DAT3	AF22	LD3ACK	AG26	LD4DAT2
AD15	EMU	AE19	RCLKD1	AF23	LD3CLK	AG27	LD4DAT3
AD16	(GND)	AE20	RCLKD0	AF24	LD3DAT0	AG28	(unused)
AD17	TMS	AE21	WR	AF25	LD3DAT1	AG29	(GND)
AD18	TRST	AE22	LD2ACK	AF26	LD3DAT2	AG30	(unused)

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AG31	(GND)	AH35	(unused)	AK3	(unused)	AL7	(unused)
AG32	(unused)	AH36	(GND)	AK4	(unused)	AL8	(GND)
AG33	(GND)	AJ1	(GND)	AK5	(GND)	AL9	(unused)
AG34	(unused)	AJ2	(unused)	AK6	(unused)	AL10	(GND)
AG35	(unused)	AJ3	(unused)	AK7	(GND)	AL11	(unused)
AG36	(GND)	AJ4	(GND)	AK8	(unused)	AL12	(GND)
AH1	(GND)	AJ5	(unused)	AK9	(GND)	AL13	(unused)
AH2	(unused)	AJ6	(GND)	AK10	(unused)	AL14	(GND)
AH3	(unused)	AJ7	(unused)	AK11	(GND)	AL15	(unused)
AH4	(unused)	AJ8	(GND)	AK12	(unused)	AL16	(GND)
AH5	(GND)	AJ9	(unused)	AK13	(GND)	AL17	(TEST5)
AH6	(unused)	AJ10	(GND)	AK14	(unused)	AL18	(TEST5)
AH7	(GND)	AJ11	(unused)	AK15	(GND)	AL19	(TEST4)
AH8	(unused)	AJ12	(TEST6)	AK16	GND	AL20	(TEST4)
AH9	(GND)	AJ13	LC4ACK	AK17	VDD	AL21	(GND)
AH10	(unused)	AJ14	LC4CLK	AK18	GND	AL22	(unused)
AH11	(TEST6)	AJ15	LC4DAT0	AK19	VDD	AL23	(GND)
AH12	VDD	AJ16	LC4DAT1	AK20	VDD	AL24	(unused)
AH13	LC3ACK	AJ17	LC4DAT2	AK21	GND	AL25	(GND)
AH14	LC3CLK	AJ18	LC4DAT3	AK22	(GND)	AL26	(unused)
AH15	LC3DAT0	AJ19	DTD1	AK23	(unused)	AL27	(GND)
AH16	LC3DAT1	AJ20	$\overline{\text{DTD0}}$	AK24	(GND)	AL28	(unused)
AH17	LC3DAT2	AJ21	CPAD	AK25	(unused)	AL29	(GND)
AH18	LC3DAT3	AJ22	TDO	AK26	(GND)	AL30	(unused)
AH19	TCLKD1	AJ23	LBOOTBCD	AK27	(unused)	AL31	(GND)
AH20	TCLKD0	AJ24	TCK	AK28	(GND)	AL32	(unused)
AH21	IDD0	AJ25	(TEST3)	AK29	(unused)	AL33	(GND)
AH22	IDD1	AJ26	(unused)	AK30	(GND)	AL34	(unused)
AH23	IDD2	AJ27	(GND)	AK31	(unused)	AL35	(unused)
AH24	EBOOTBCD	AJ28	(unused)	AK32	(GND)	AL36	(GND)
AH25	TDOC	AJ29	(GND)	AK33	(unused)	AM1	(GND)
AH26	(TEST3)	AJ30	(unused)	AK34	(unused)	AM2	(unused)
AH27	(unused)	AJ31	(GND)	AK35	(unused)	AM3	(unused)
AH28	(GND)	AJ32	(unused)	AK36	(GND)	AM4	(unused)
AH29	(unused)	AJ33	(GND)	AL1	(GND)	AM5	(GND)
AH30	(GND)	AJ34	(unused)	AL2	(unused)	AM6	(unused)
AH31	(unused)	AJ35	(unused)	AL3	(unused)	AM7	(GND)
AH32	(GND)	AJ36	(GND)	AL4	(GND)	AM8	(unused)
AH33	(unused)	AK1	(GND)	AL5	(unused)	AM9	(GND)
AH34	(unused)	AK2	(unused)	AL6	(GND)	AM10	(unused)

See note at end of table.

FIGURE 4. Terminal connections - Continued.

Device type		01 and 02					
Case outline		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AM11	(GND)	AN16	(GND)	AP21	(unused)	AR27	(unused)
AM12	(unused)	AN17	(unused)	AP22	(unused)	AR28	(unused)
AM13	(GND)	AN18	(VDD)	AP23	(unused)	AR29	(unused)
AM14	(unused)	AN19	(VDD)	AP24	(unused)	AR30	(unused)
AM15	(GND)	AN20	(unused)	AP25	(unused)	AR31	(unused)
AM16	(unused)	AN21	(GND)	AP26	(unused)	AR32	(unused)
AM17	(unused)	AN22	(unused)	AP27	(unused)	AR33	(unused)
AM18	(VDD)	AN23	(GND)	AP28	(unused)	AR34	(unused)
AM19	(VDD)	AN24	(unused)	AP29	(unused)	AR35	(GND)
AM20	(unused)	AN25	(GND)	AP30	(unused)	AT3	(GND)
AM21	(unused)	AN26	(unused)	AP31	(unused)	AT4	(GND)
AM22	(GND)	AN27	(GND)	AP32	(unused)	AT5	(GND)
AM23	(unused)	AN28	(unused)	AP33	(GND)	AT6	(GND)
AM24	(GND)	AN29	(GND)	AP34	(unused)	AT7	(GND)
AM25	(unused)	AN30	(unused)	AP35	(VDD)	AT8	(GND)
AM26	(GND)	AN31	(GND)	AP36	(GND)	AT9	(GND)
AM27	(unused)	AN32	(unused)	AR2	(GND)	AT10	(GND)
AM28	(GND)	AN33	(GND)	AR3	(unused)	AT11	(GND)
AM29	(unused)	AN34	(unused)	AR4	(unused)	AT12	(GND)
AM30	(GND)	AN35	(unused)	AR5	(unused)	AT13	(GND)
AM31	(unused)	AN36	(GND)	AR6	(unused)	AT14	(GND)
AM32	(GND)	AP1	(GND)	AR7	(unused)	AT15	(GND)
AM33	(unused)	AP2	(GND)	AR8	(unused)	AT16	(GND)
AM34	(unused)	AP3	(unused)	AR9	(unused)	AT17	(GND)
AM35	(unused)	AP4	(VDD)	AR10	(unused)	AT18	(GND)
AM36	(GND)	AP5	(unused)	AR11	(unused)	AT19	(GND)
AN1	(GND)	AP6	(unused)	AR12	(unused)	AT20	(GND)
AN2	(unused)	AP7	(unused)	AR13	(unused)	AT21	(GND)
AN3	(unused)	AP8	(unused)	AR14	(unused)	AT22	(GND)
AN4	(GND)	AP9	(unused)	AR15	(unused)	AT23	(GND)
AN5	(unused)	AP10	(unused)	AR16	(unused)	AT24	(GND)
AN6	(GND)	AP11	(unused)	AR17	(unused)	AT25	(GND)
AN7	(unused)	AP12	(unused)	AR18	(unused)	AT26	(GND)
AN8	(GND)	AP13	(unused)	AR19	(unused)	AT27	(GND)
AN9	(unused)	AP14	(unused)	AR20	(unused)	AT28	(GND)
AN10	(GND)	AP15	(unused)	AR21	(unused)	AT29	(GND)
AN11	(unused)	AP16	(unused)	AR22	(unused)	AT30	(GND)
AN12	(GND)	AP17	(unused)	AR23	(unused)	AT31	(GND)
AN13	(unused)	AP18	(GND)	AR24	(unused)	AT32	(GND)
AN14	(GND)	AP19	(VDD)	AR25	(unused)	AT33	(GND)
AN15	(unused)	AP20	(unused)	AR26	(unused)	AT34	(GND)

NOTE:
1. Terminal symbols encolsed within parentheses are redundant pins beyond the standard package 452 leads. These are not required to be connected. Pins labeled "(unused)" are not electrically connected. Pins labeled (VDD) and (GND) are redundant power and ground connections. Pins labeled (TESTn), n = 1 through 16, are daisy chain test pin pairs.

FIGURE 4. Terminal connections - Continued.

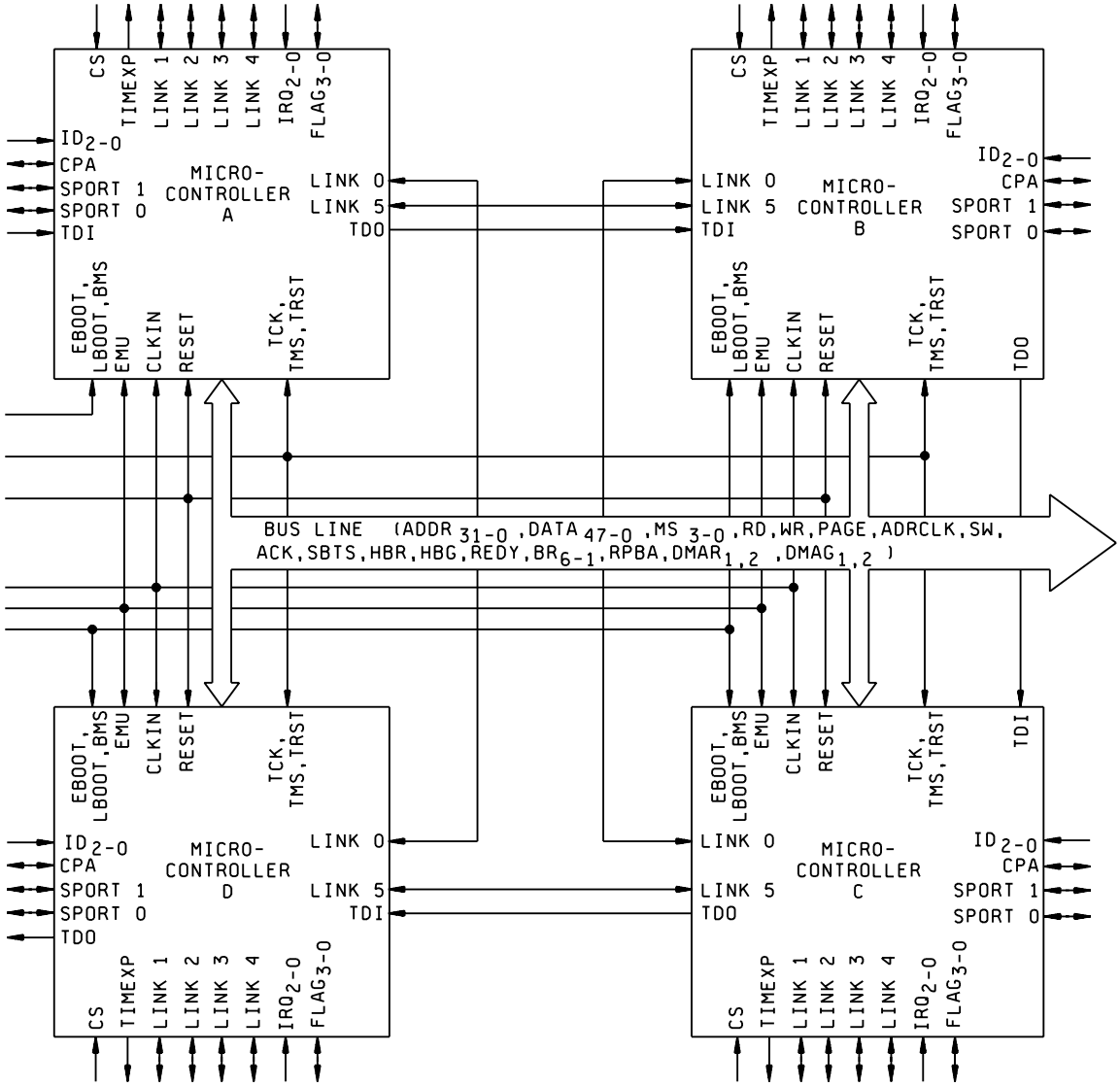
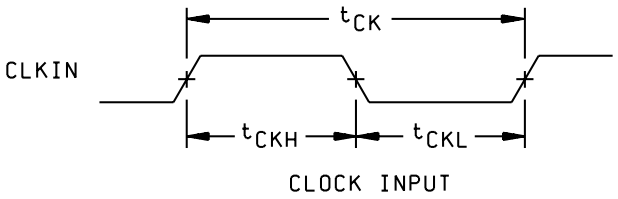
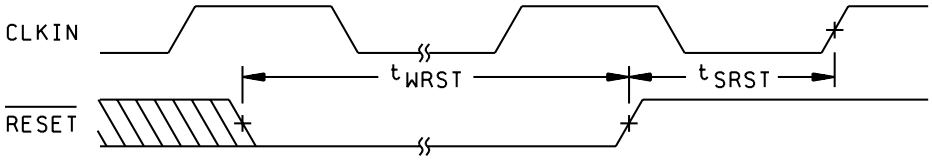


FIGURE 5. Block diagram.

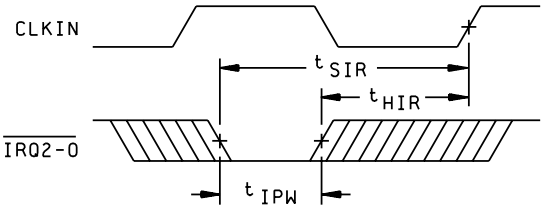
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-98003
		REVISION LEVEL	SHEET 37



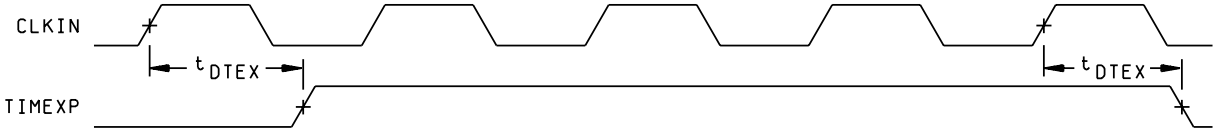
CLOCK INPUT



RESET

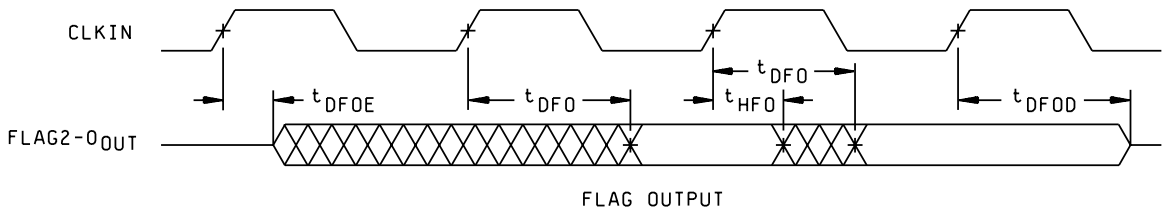


INTERRUPTS

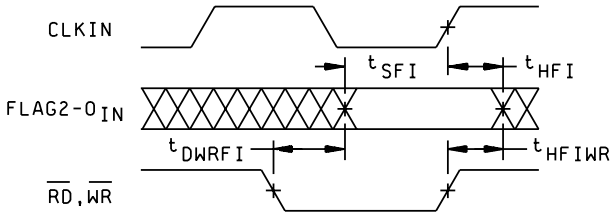


TIMER

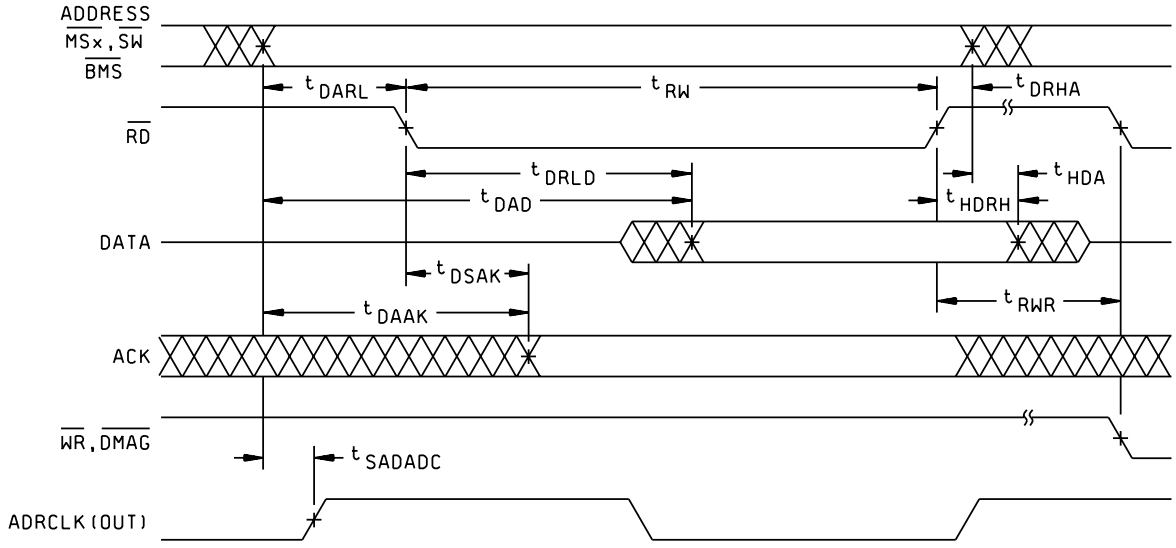
FIGURE 6. Timing waveforms.



FLAG OUTPUT

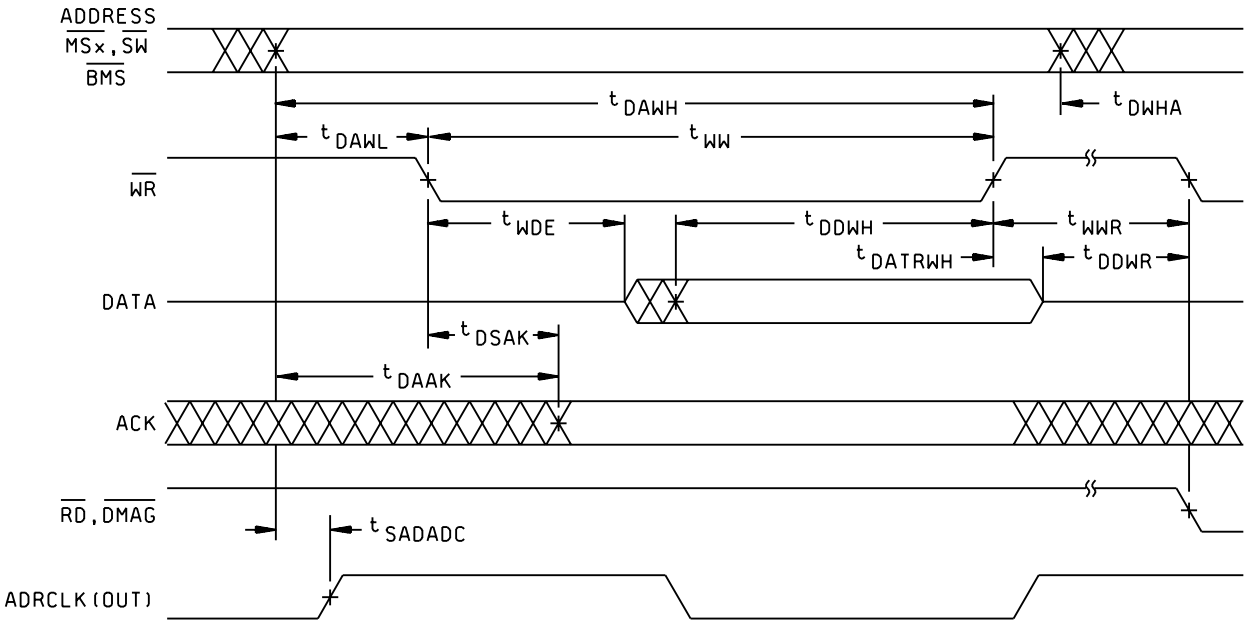


FLAG INPUT



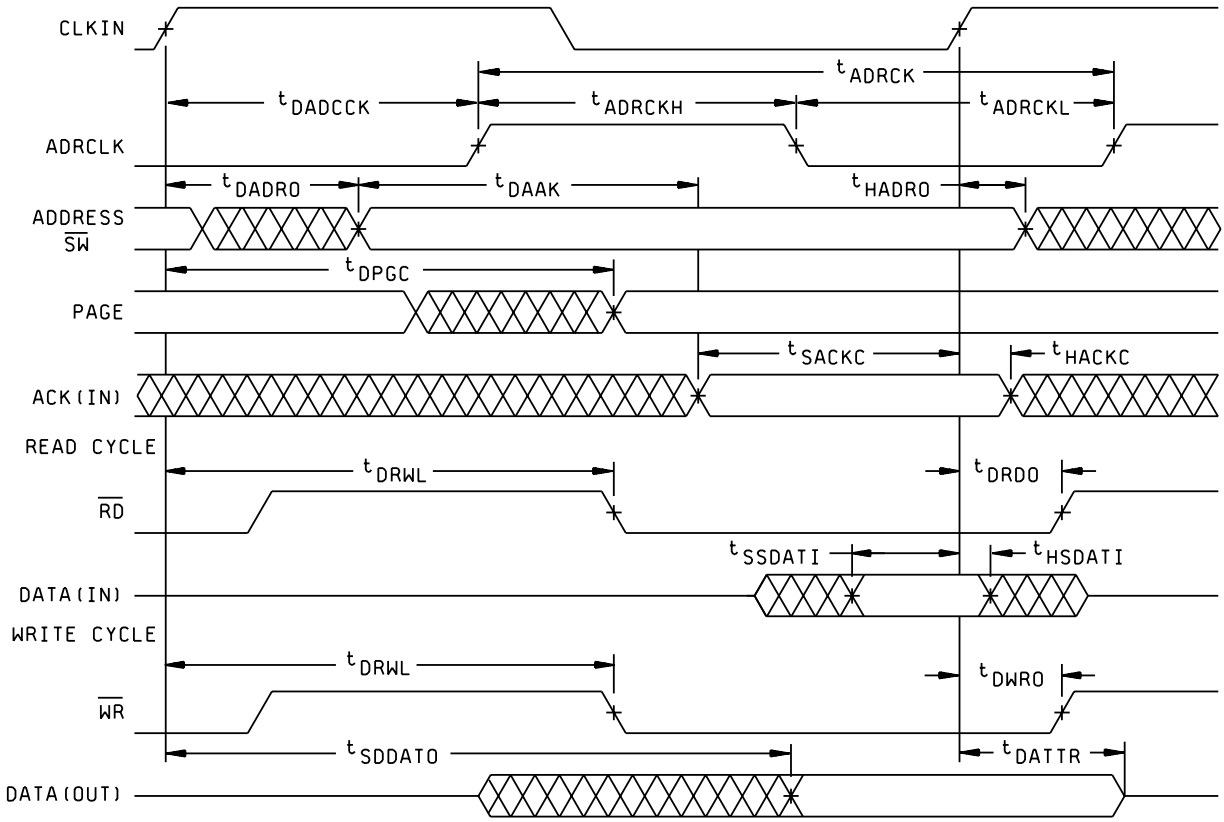
MEMORY READ - BUS MASTER

FIGURE 6. Timing waveforms - Continued.



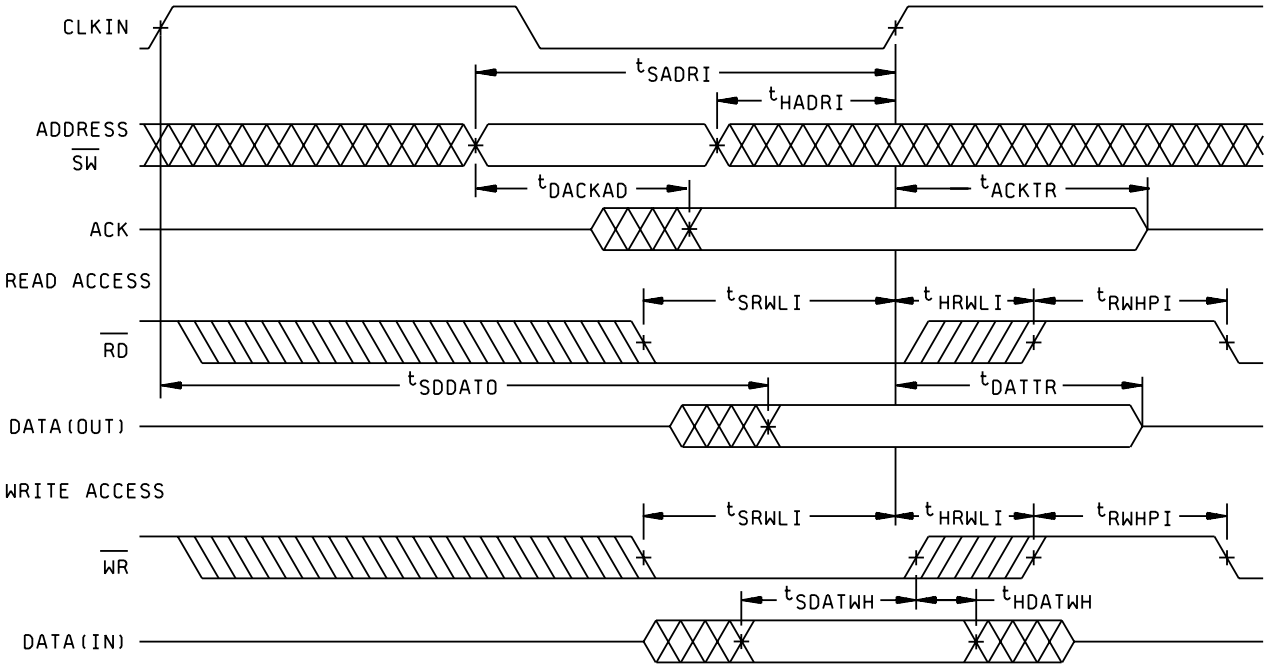
MEMORY WRITE - BUS MASTER

FIGURE 6. Timing waveforms - Continued.



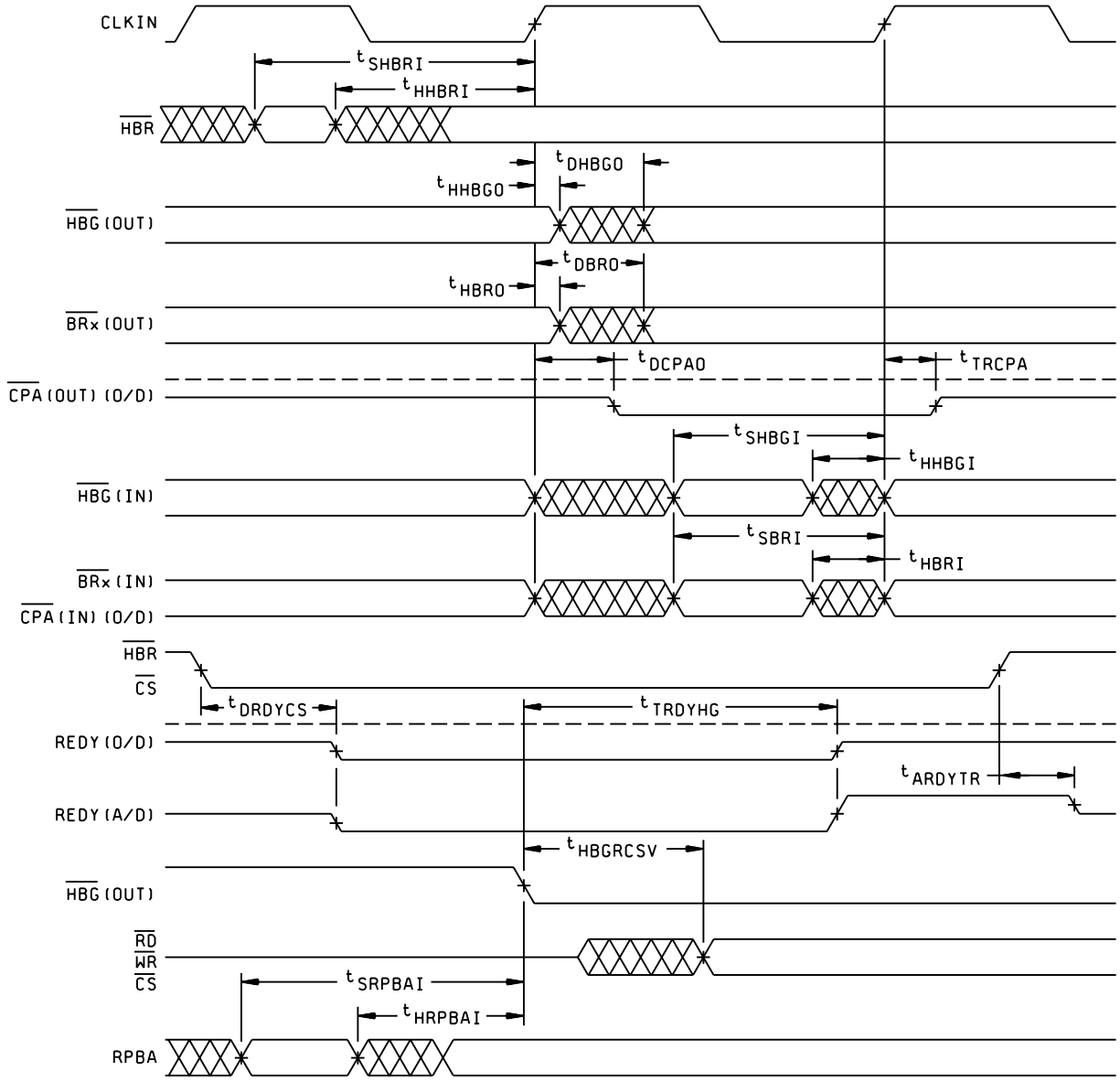
SYNCHRONOUS READ/WRITE - BUS MASTER

FIGURE 6. Timing waveforms - Continued.



SYNCHRONOUS READ/WRITE - BUS SLAVE

FIGURE 6. Timing waveforms - Continued.



MULTIPROCESSOR BUS REQUEST AND HOST BUS REQUEST

FIGURE 6. Timing waveforms - Continued.

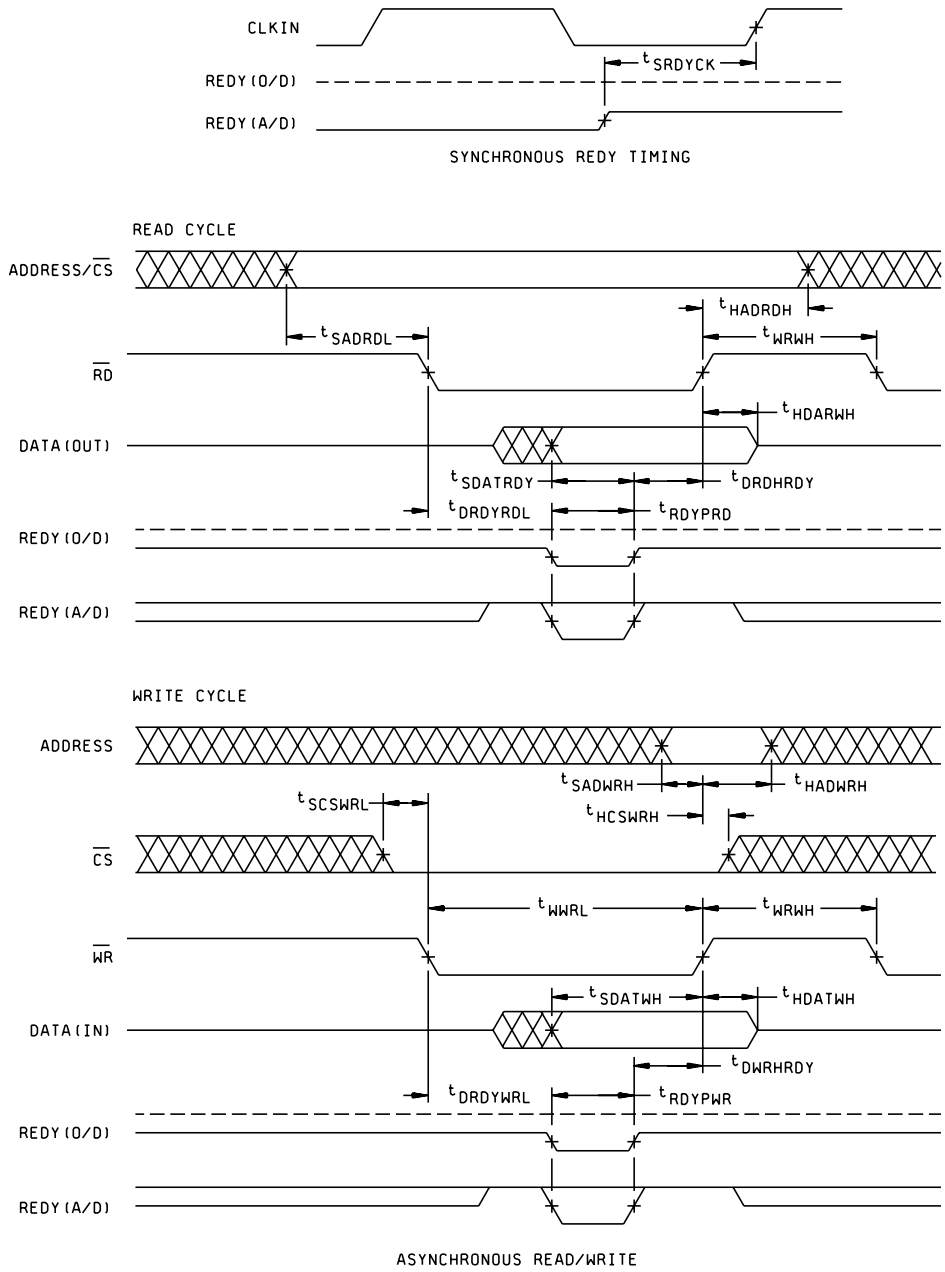


FIGURE 6. Timing waveforms - Continued.

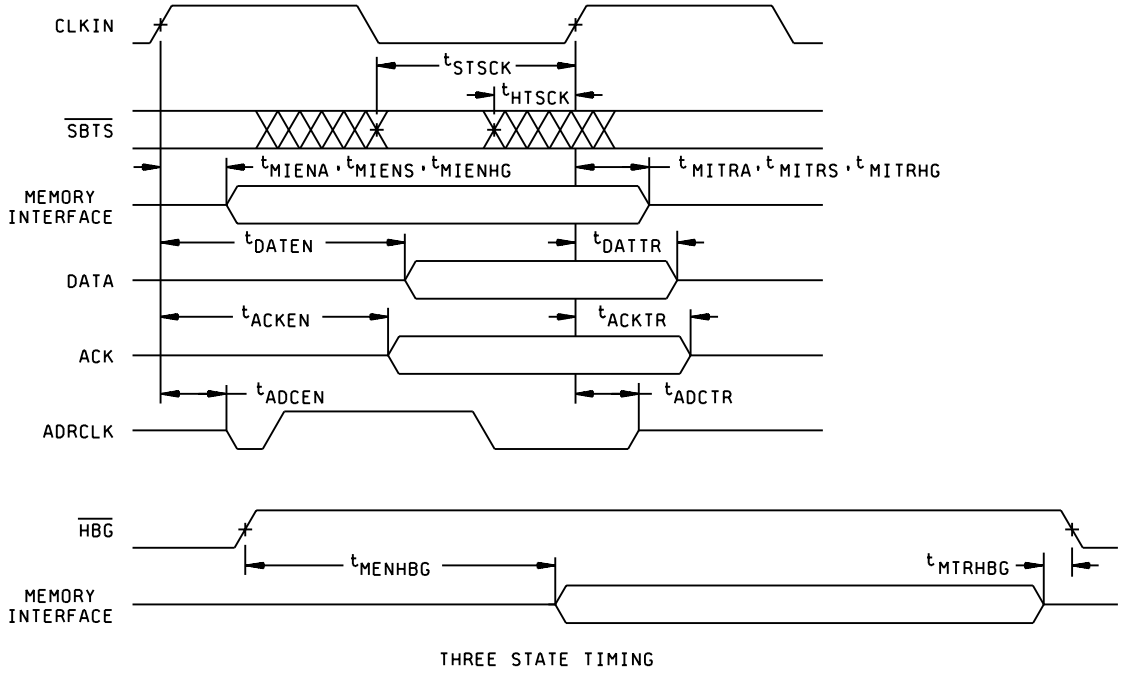
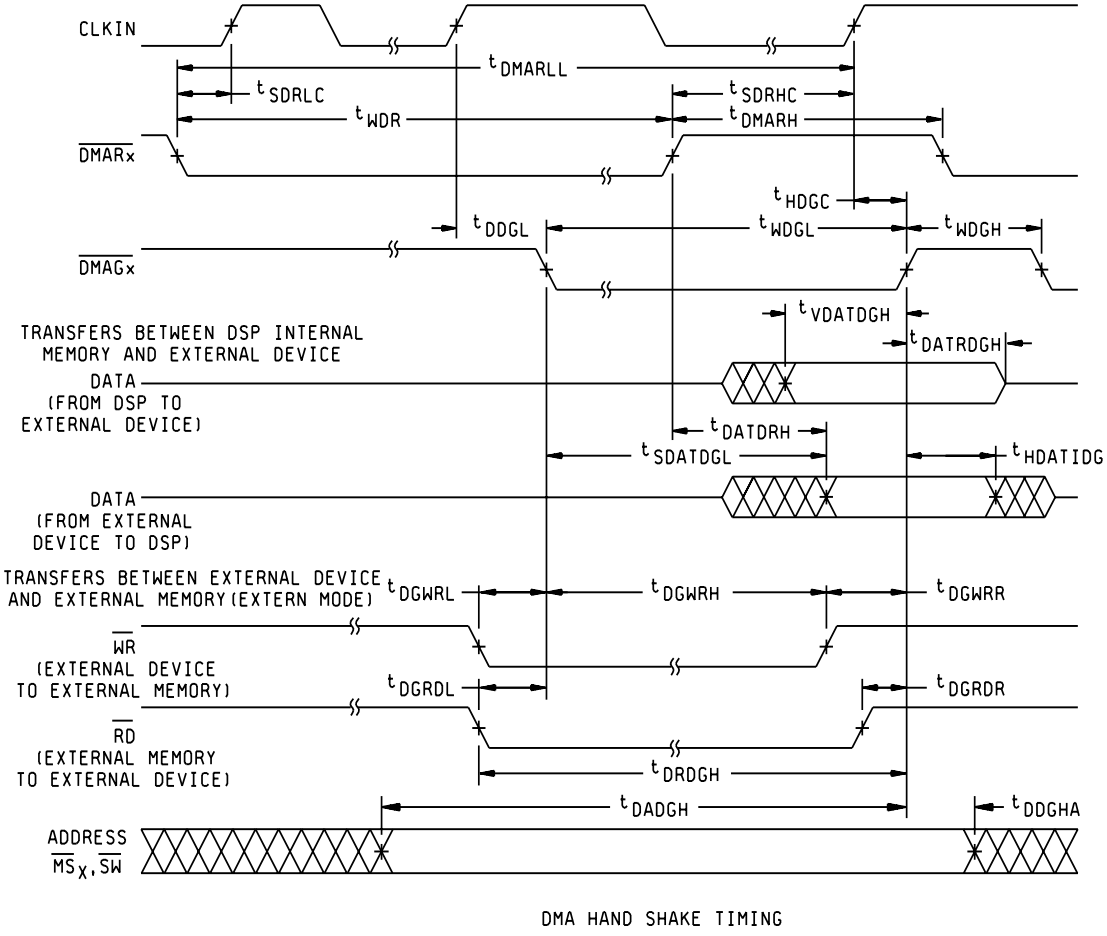
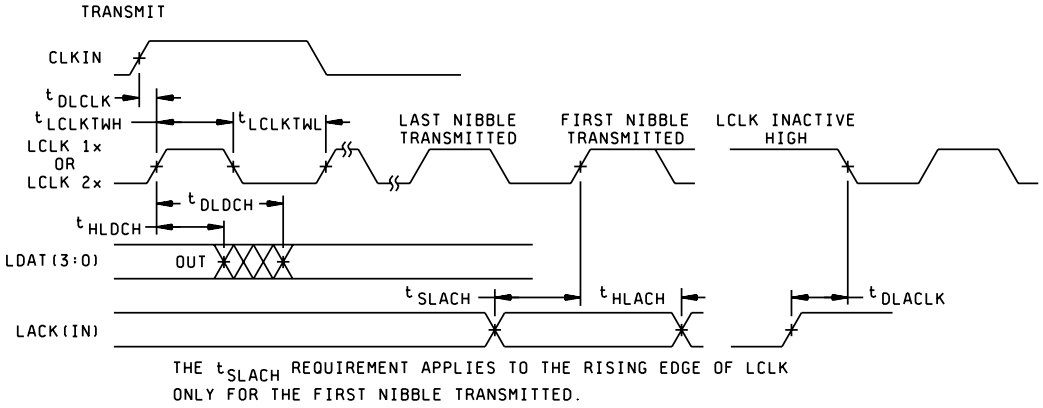


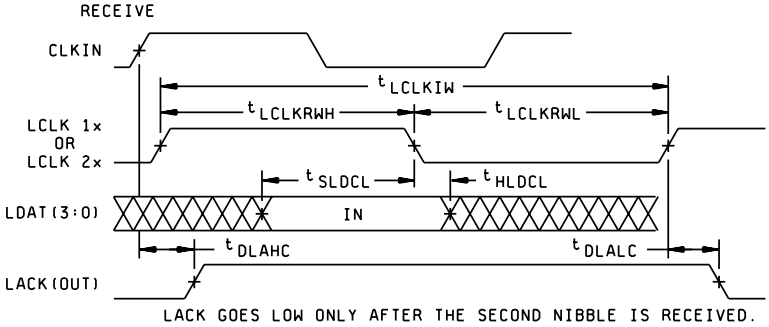
FIGURE 6. Timing waveforms - Continued.

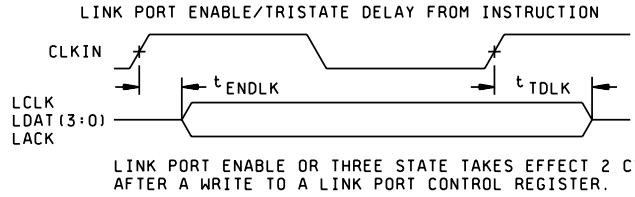


DMA HAND SHAKE TIMING

FIGURE 6. Timing waveforms - Continued.







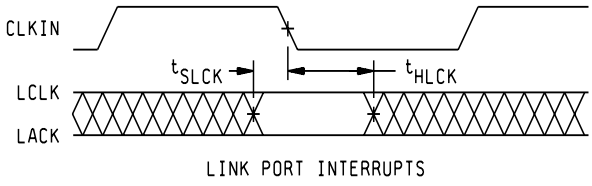
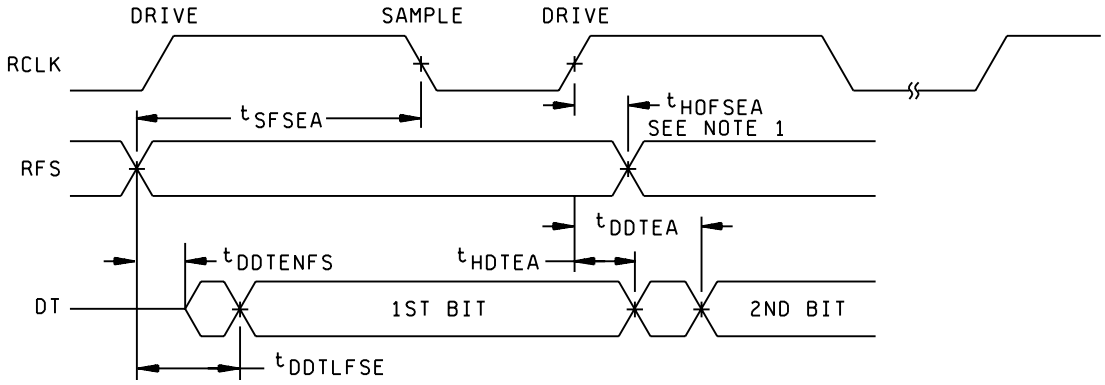
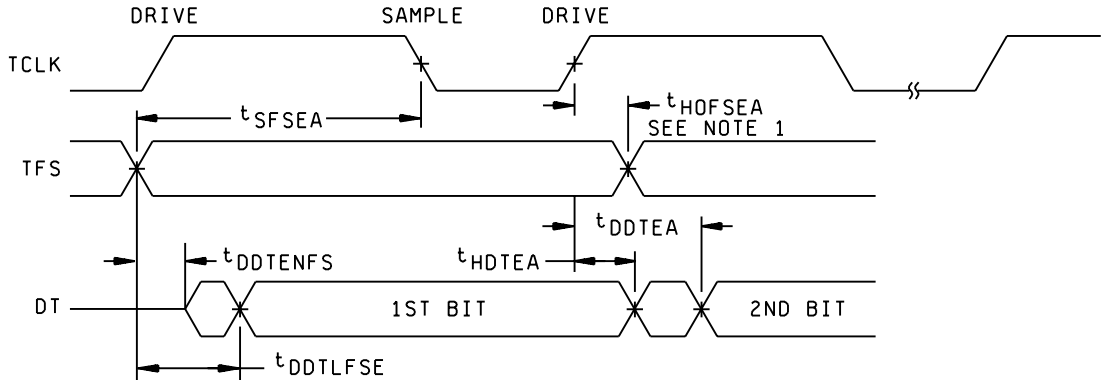


FIGURE 6. Timing waveforms - Continued.

EXTERNAL RFS WITH MCE = 1, MFD = 0



LATE EXTERNAL TFS



EXTERNAL LATE FRAME SYNC

NOTE:
1. RFS hold after RCLK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCLK for late external TFS is 0 ns minimum form drive edge.

FIGURE 6. Timing waveforms - Continued.

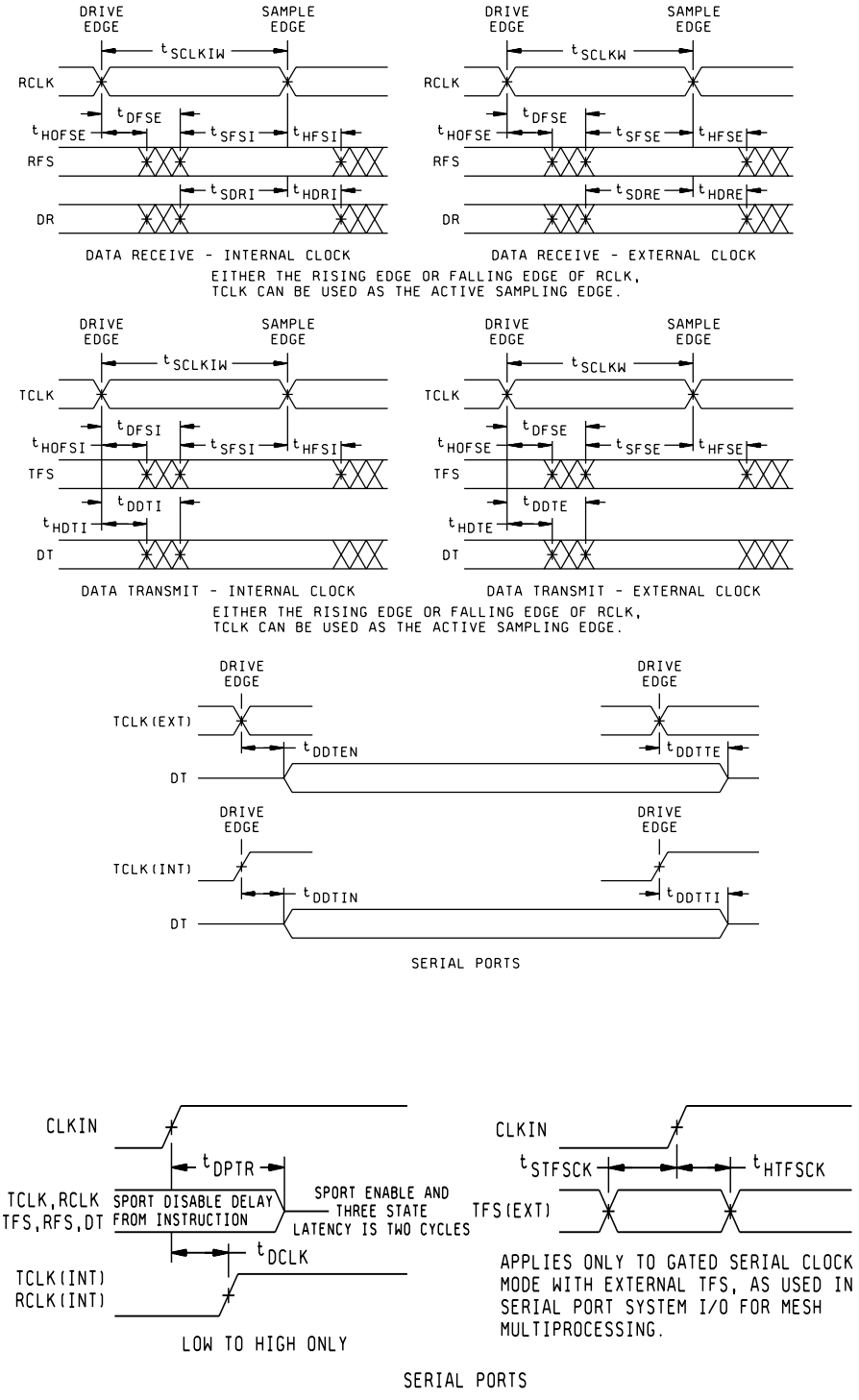


FIGURE 6. Timing waveforms - Continued.

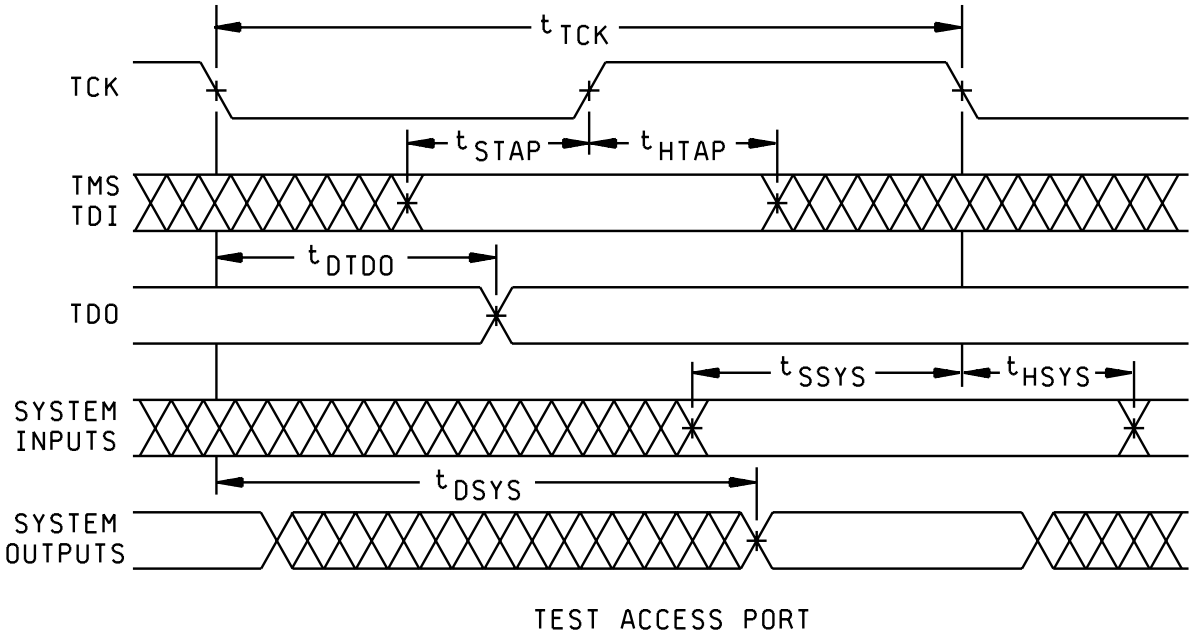
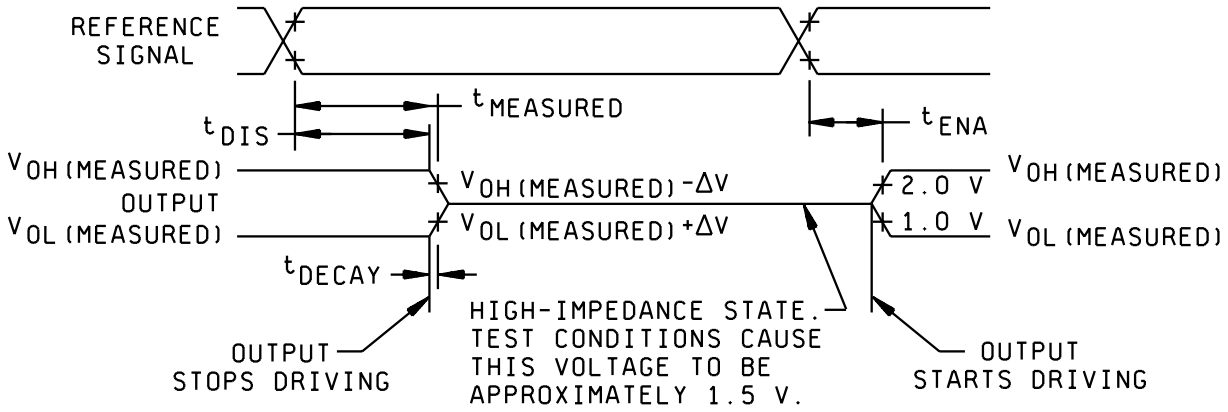
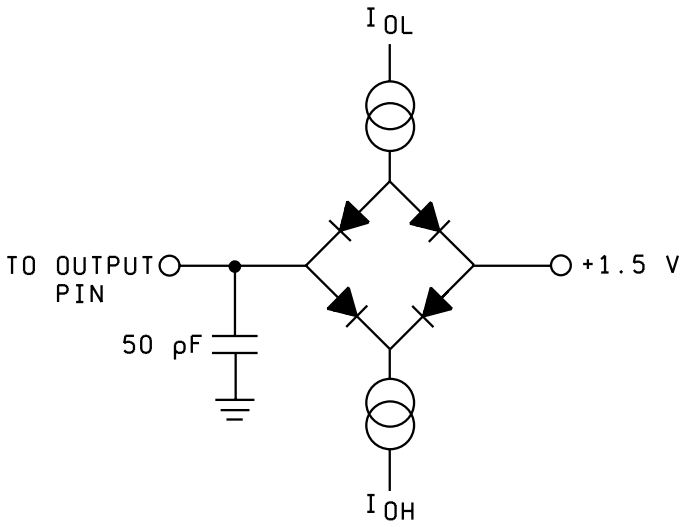


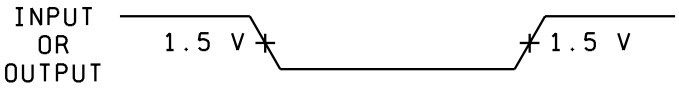
FIGURE 6. Timing waveforms - Continued.



OUTPUT ENABLE/DISABLE



EQUIVALENT DEVICE LOADING
FOR AC MEASUREMENTS
(INCLUDES ALL FIXTURES)



VOLTAGE REFERENCE LEVELS
FOR AC MEASUREMENTS
(EXCEPT OUTPUT ENABLE/DISABLE)

FIGURE 6. Timing waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	Paragraph 4.2.b
Final electrical parameters	Paragraph 4.2.b*, 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 7, 9
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to paragraph 4.2.b, functional testing.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the functionality of the device.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation hardness assurance (RHA) insepction. RHA inspection is currently not applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	Type 1/	Function
ADDR31-0	I/O/T	External Bus Address. (Common to all processors). The module outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes on the internal memory or IOP registers of slave processors. The module inputs addresses when a host processor or multiprocessing bus master is reading or writing the internal memory or IOP registers of internal processors.
DATA47-0	I/O/T	External Bus DATA. (Common to all processors). The module inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47 - 16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47 - 8 of the bus. 16-bit short word data is transferred over bits 31 - 16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23 - 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS3-0}}$	O/T	Memory Select Lines. (Common to all processors). These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the individual processors system control registers (SYSCON). The MS3-0 lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the MS3-0 lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. MS0 can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In multiprocessing system, the MS3-0 lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	Memory Read Strobe. (Common to all processors). This pin is asserted (low) when the processor reads from external devices or when the internal memory of internal processors is being accessed. External devices (including other processors) must assert RD to read from the processors internal memory. In a multiprocessing system, RD is output by the bus master and is input by all other processors.
$\overline{\text{WR}}$	I/O/T	Memory Write Strobe. (Common to all processors). This pin is asserted (low) when the processor writes from external devices or when the internal memory of internal processors is being accessed. External devices (including other processors) must assert WR to write from the processors internal memory. In a multiprocessing system, WR is output by the bus master and is input by all other processors.
PAGE	O/T	DRAM Page Boundary. (Common to all processors). The module asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the individual processor's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master.
ADRCLK	O/T	Clock Output Reference. (Common to all processors). In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	Synchronous Write Select. (Common to all processors). This signal is used to interface the processor to synchronous memory devices (including other processors). The module asserts SW (low) to provide an early indication of an impending write cycle, which can be aborted if WR is not later asserted (e.g. in a conditional write instruction). In a multiprocessing system, SW is output by the bus master and is input by all other processors to detemine if the multiprocessor memory access is a read or write. SW is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to module.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
ACK	I/O/S	Memory Acknowledge. (Common to all processors). External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The module deasserts ACK, as an output, to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave processor deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.
$\overline{\text{SBTS}}$	I/S	Suspend Bus Three State. (Common to all processors). External devices can assert SBTS (low) to place the external bus address, data, selects, and strobes in a high impedence state for the following cycle. If the module attempts to access external memory while SBTS is asserted, the processor will halt and the memory access will not be completed until SBTS is deasserted. SBTS should only be used to recover from the host processor/ the module deadlock, or used with a DRAM controller.
$\overline{\text{HBR}}$	I/A	Host Bus Request. (Common to all processors). Must be asserted by a host processor to request control of the module's external bus. When HBR is asserted in a multiprocessor system, the processor that is bus master will relinquish the bus and assert HBG. To relinquish the bus, the processor places the address, data, select, and strobe lines in a high impedance state. HBR has priority over all processor bus requests (BR 6-1) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	Host Bus Grant. (Common to all processors). Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. HBG is asserted (held low) by the module until HBR is released. In a multiprocessing system, HBG is output by the processor bus master and is monitored by all others.
$\overline{\text{CSA}}$	I/A	Chip Select. Asserted by host processor to select processor-A.
$\overline{\text{CSB}}$	I/A	Chip Select. Asserted by host processor to select processor-B.
$\overline{\text{CSC}}$	I/A	Chip Select. Asserted by host processor to select processor-C.
$\overline{\text{CSD}}$	I/A	Chip Select. Asserted by host processor to select processor-D.
REDY (O/D)	O	Host Bus Acknowledge. (Common to all processors). The module deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register of indiviual processors to be active drive (A/D). REDY will only be output if the CS and HBR inputs are asserted.
$\overline{\text{BR6-1}}$	I/O/S	Multiprocessing Bus Requests. (Common to all processor). Used by multiprocessing processors to arbitrate for bus mastership. A processor only drives its own BRx line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessing system with less than six processors the unused BRx pins should be pulled high; BR4-1 must not be pulled high or low because they are outputs.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
IDy2-0	I	Multiprocessing ID. (Individual ID2-0 from y = processor-A, -B, -C, -D). Determines which multiprocessing bus request (BR1 - BR6) is used by the individual processors. ID = 001 corresponds to BR1, ID = 010 corresponds to BR2 and so on. ID = 000 is reserved for single processor systems. These lines are a system configuration selection, which should be hardwired or only changed at reset.
RPBA	I/S	Rotating Priority Bus Arbitration Select. (Common to all processors). When RPBA is high, rotating priority fot multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every processor. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{\text{CPA}}$y (O/D)	I/O	Core Priority Access (y = processor-A, -B, -C, -D). Asserting its $\overline{\text{CPA}}$ pin allows the core processor of a bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open drain output that is connected to all processors in the system, if this function is required. The $\overline{\text{CPA}}$ pin of each internal processor is brought out individually. The $\overline{\text{CPA}}$ pin has an internal 5 kohm pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTy0	O/T	Data Transmit (y = processor -A, -B, -C, -D). DT pin has four parallel 50 kohm internal pull-up resistors.
DRy0	I	Data Receive (y = processor -A, -B, -C, -D). DR pin has four parallel 50 kohm internal pull-up resistors.
TCLKy0	I/O	Transmit Clock (y = processor -A, -B, -C, -D). TCLK pin has four parallel 50 kohm internal pull-up resistors.
RCLKy0	I/O	Receiver Clock (y = processor -A, -B, -C, -D). RCLK pin has four parallel 50 kohm internal pull-up resistors.
TFSy0	I/O	Transmit Frame Sync (y = processor -A, -B, -C, -D).
RFSy0	I/O	Receiver Frame Sync (y = processor -A, -B, -C, -D).
DTy1	O/T	Data Transmit (Serial port 1 individual from processor-A, -B, -C, -D). Each DT pin has a 50 kohm internal pull-up resistor.
DRy1	I	Data Receive (Serial port 1 individual from processor-A, -B, -C, -D). Each DR pin has a 50 kohm internal pull-up resistor.
TCLKy1	I/O	Transmit Clock (Serial port 1 individual from processor-A, -B, -C, -D). Each TCLK pin has a 50 kohm internal pull-up resistor.
RCLKy1	I/O	Receive Clock (Serial port 1 individual from processor-A, -B, -C, -D). Each RCLK pin has a 50 kohm internal pull-up resistor.
TFSy1	I/O	Transmit Frame Sync (Serial port 1 individual from processor-A, -B, -C, -D).
RFSy1	I/O	Receive Frame Sync (Serial port 1 individual from processor-A, -B, -C, -D).

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
FLAGy3-0	I/O/A	FLAG Pins. (FLAG3-0 individual from processor-A, -B, -C, and -D). Each is configured by control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{IRQy2-0}}$	I/A	Interrupt Request Lines. (Individual IRQ2-0 from y = processor-A, -B, -C, -D). May be either edge-triggered or level-sensitive.
$\overline{\text{DMAR1}}$	I/A	DMA Request 1 (DMA Channel 7). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAR2}}$	I/A	DMA Request 1 (DMA Channel 8). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAG1}}$	O/T	DMA Grant 1 (DMA Channel 7). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAG2}}$	O/T	DMA Grant 2 (DMA Channel 8). Common to processor-A, -B, -C, -D.
LyxCLK	I/O	Link Port Clock (y = processor-A, -B, -C, -D; x = Link Ports 1, 2, 3, 4), 2/. Each LyxCLK pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
LyxDAT3-0	I/O	Link Port Data (y = processor-A, -B, -C, -D; x = Link Ports 1, 2, 3, 4), 2/. Each LyxDAT pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
LyxACK	I/O	Link Port Acknowledge (y = processor-A, -B, -C, -D; x = Link Ports 1, 2, 3, 4), 2/. Each LyxACK pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
$\overline{\text{BMSA}}$	I/O/T 3/	Boot Memory Select. Output: Used as chip select for boot EPROM devices (when EBOOTA = 1, LBOOTA = 0). In a multiprocessor system, BMS is output by the bus master. Input: When low, indicates that no booting will occur and that processor-A will begin executing instructions from external memory. See table in note 3. This input is a system configuration selection which should be hardwired.
EBOOTA	I	EPROM Boot Select. (processor-A) When EBOOTA is high, processor-A is configured for booting from an 8-bit EPROM. When EBOOTA is low, the LBOOTA and BMSA inputs determine booting mode for processor-A. See table in note 3. This signal is a configuration selection which should be hardwired.
LBOOTA	I	Link Boot. When LBOOTA is high, processor-A is configured for link port booting. When LBOOTA is low, processor-A is configured for host processor booting or no booting. See table in note 3. This signal is a system configuration selection which should be hardwired.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
EBOOTBCD	I	EPROM Boot Select. (Common to processor-B, -C, -D). When EBOOTBCD is high, processor-B, -C, -D are configured for booting from an 8-bit EPROM. When EBOOTBCD is low, the LBOOTBCD and BMSBCD inputs determine booting mode for processor-B, -C, and -D. See table in note 3. This signal is a system configuration selection which should be hardwired.
LBOOTBCD	I	LINK Boot. (Common to processor-B, -C, -D). When LBOOTBCD is high, processor-B, -C, -D are configured for link port booting. When LBOOTBCD is low, multiprocessor-B, -C, -D are configured for host processor booting or no booting. See table in note 3. This signal is a system configuration selection which should be hardwired.
$\overline{\text{BMSBCD}}$	I/O/T 3/	Boot Memory Select. Output: Used as chip select for boot EPROM devices (when EBOOTBCD = 1, LBOOTBCD = 0). In a multiprocessor system, BMS is output by the bus master. Input: When low, indicates that no booting will occur and that processor-B, -C, -D will begin executing instructions from external memory. See table in note 3. This input is a system configuration selection which should be hardwired.
TIMEXPy	O	Timer Expired. (Individual TIMEXP from y = processor-A, -B, -C, -D). Asserted for four cycles when the timer is enabled and t_{count} decrements to zero.
CLKIN	I	Clock In. (Common to all processors). External clock input to the module. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	Module Reset. (Common to all processors). Resets the module to a known state. This input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). (Common to all processors). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). (Common to all processors). Used to control the test state machine. TMS has four parallel 20 kohm internal pull-up resistors.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic chain starting at processor-A. TDI has a 20 kohm pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan chain path, from processor-D.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Common to all processors). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the module. TRST has four parallel 20 kohm internal pull-up resistors.
$\overline{\text{EMU}}$(O/D)	O	Emulation Status. (Common to all processors). Pin AD15 must be connected to the module's target board test connector only.
VDD	P	Power Supply. Nominally +5.0 V dc.
GND	G	Power supply returns. The lid to the module is electrically connected to GND.

See footnotes on the following page.

TABLE III. Pin functions - Continued.

NOTES:

1/ Type: A = asynchronous, A/D = active drive, G = ground, I = input, O = output, O/D= open drain, P = power supply, S = synchronous, T = three state (when SBTS is asserted, or when the module is a bus slave).

Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN(or to TCK forTRST).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{SW}$, and inputs that have internal pull-up or pull-down resistors (CPA, ACK, DTx, DRx, TCLKx, RCLKx, LxDAT3-0, LxCLK, LxACK, TMS, and TDI) - these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

ID pins are hardwired internally.

2/ LINK PORTS 0 and 5 are connected internally between processors -A, -B, -C, and -D.

3/ Three statable only in EPROM boot mode (when $\overline{BMS}$ is an output).

EBOOT	LBOOT	$\overline{BMS}$	Booting Mode
1	0	output	EPROM (connect $\overline{BMS}$ to EPROM chip select)
0	0	1 (input)	Host processor
0	1	1 (input)	Link port
0	0	0 (input)	No booting. Processor executes from external memory.
0	1	0 (input)	Reserved
1	1	x (input)	Reserved

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-12-01

Approved sources of supply for SMD 5962-98003 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38534 during the next revision. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9800301HXA 3/	24355	AD14160BB/QML-4
5962-9800302HXA	24355	AD14160TB/QML-4

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Inactive for new design. Not available from a QML-38534 manufacturer.

Vendor CAGE number	Vendor name and address
24355	Analog Devices RT 1 Industrial Park P. O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605