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Single 2-Input Exclusive OR Gate

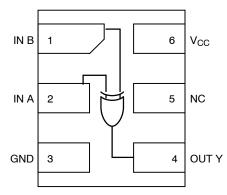
NLU1G86

The NLU1G86 MiniGate[™] is an advanced high-speed CMOS 2-input Exclusive OR gate in ultra-small footprint.

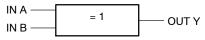
The NLU1G86 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns} (Typ) @ V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices









PIN ASSIGNMENT

1	IN B
2	IN A
3	GND
4	OUT Y
5	NC
6	V _{CC}

FUNCTION TABLE

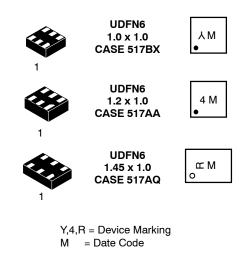
Inp	out	Output
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L



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MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	±20	mA
Ι _Ο	DC Output Source/Sink Current	±12.5	mA
I _{CC}	DC Supply Current Per Supply Pin	±25	mA
I _{GND}	DC Ground Current per Ground Pin	±25	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
TJ	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
ILATCHUP	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

2. Tested to EIA / JESD22-A114-A.

3. Tested to EIA / JESD22-A115-A.

4. Tested to JESD22-C101-A.

5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	Digital Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage	0	5.5	V	
T _A	Operating Free-Air Temperature	-55	+125	°C	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Vo	_{CC} = 3.3 V ± 0.3 V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

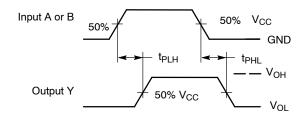
DC ELECTRICAL CHARACTERISTICS

			V_{CC} $T_A = 25 °C$		T _A = +85°C		T _A = −55°C to +125°C				
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Low-Level Input Voltage		1.65	0.75 x V _{CC}			0.75 x V _{CC}				V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}				
V _{IL}	Low–Level Input Voltage		1.65			0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \ \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
ICC	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		10		40	μA

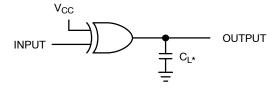
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ nS}$)

		V _{cc}		т	= 25 °	с	T _A = +	-85°C	T _A = -5 +12		
Symbol	Parameter	(V)	Test Condition	Min	Тур	Мах	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation	3.0 to 3.6	C _L = 15 pF		4.4	11		13		15.5	ns
^I PHL	t _{PHL} Delay, Input A or B to		C _L = 50 pF		5.7	14.5		16.5		19.5	
	Output Y	4.5 to	C _L = 15 pF		3.5	6.8		8.0		10	
		5.5	C _L = 50 pF		4.2	8.8		10		12	
C _{IN}	Input Capacitance				5.5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	5.0			10						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.







*Includes all probe and jig capacitance. A 1–MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

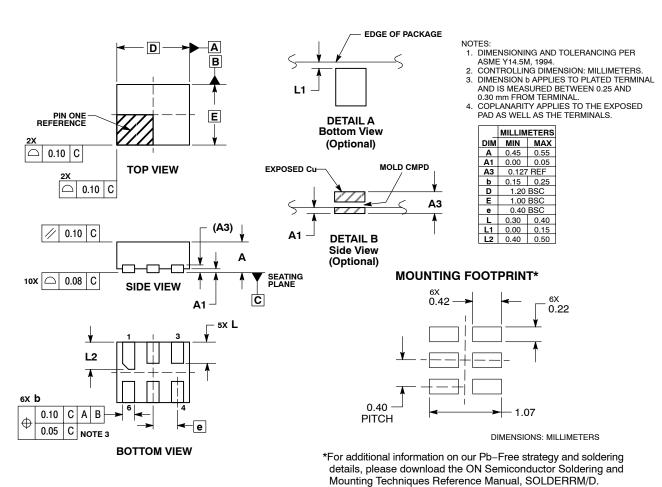
ORDERING INFORMATION

Device	Specific Device Code	Package	Shipping [†]
NLU1G86AMUTCG	R (Rotated 270 degrees)	UDFN6, 1.45 x 1.0, 0.5P (Pb–Free)	3000 / Tape & Reel
NLU1G86MUTCG	4	UDFN6, 1.2 x 1.0, 0.4P (Pb–Free)	3000 / Tape & Reel
NLU1G86CMUTCG	Y (Rotated 180 degrees)	UDFN6, 1.0 x 1.0, 0.35P (Pb–Free)	3000 / Tape & Reel

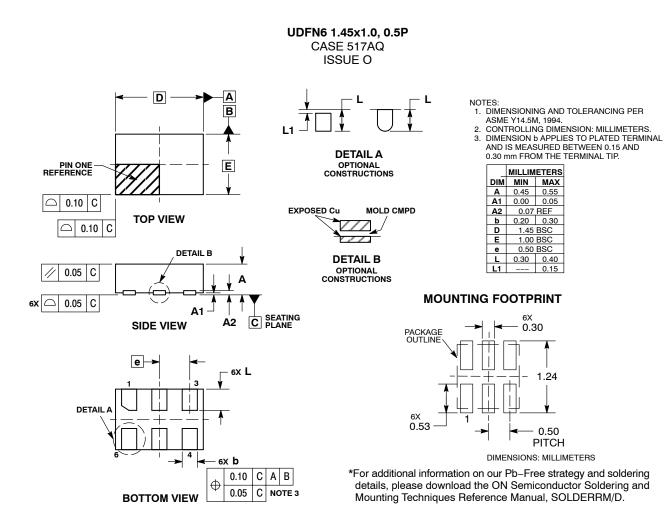
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UDFN6, 1.2x1.0, 0.4P CASE 517AA ISSUE D

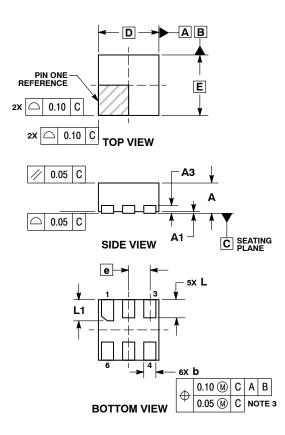


PACKAGE DIMENSIONS



PACKAGE DIMENSIONS

UDFN6 1.0x1.0, 0.35P CASE 517BX ISSUE O

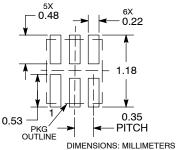


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN
- TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP. 4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

BURF	BURRS AND MOLD FL					
	MILLIMETERS					
DIM	MIN MAX					
Α	0.45	0.55				
A1	0.00	0.05				
A3	0.13 REF					
b	0.12	0.22				
D	1.00	BSC				
E	1.00 BSC 0.35 BSC					
е						
L	0.25	0.35				
L1	0.30	0.40				

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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