HC-55536

Continuous Variable Slope Delta Demodulator (CVSD)

Features

- ALL DIGITAL
- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 1.5mW FROM SINGLE 3.0-7.0V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION

Applications

- VOICE DECODER FOR DIGITAL SYSTEMS AND SPEECH SYNTHESES
- VOICE MAIN
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.
- PAGERS/SATELLITES

Description

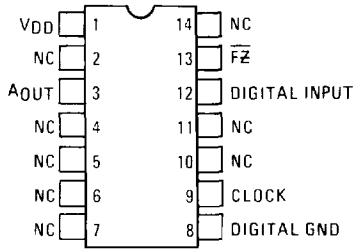
The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the Continuously Variable Slope (CVSD) method of demodulation.

While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to inplement. The device is usable from 9K bits/sec. to above 64K bits/sec.,and may be easily configured with the HC-55564 CVSD for a complete transmit/receive voice channel.

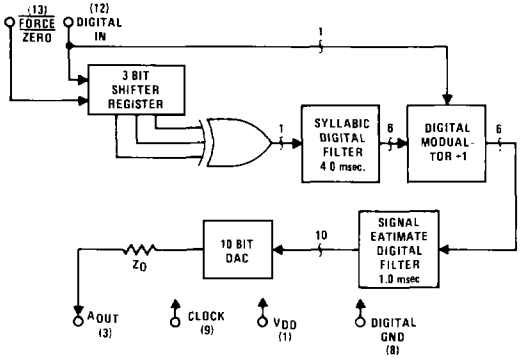
The HC-55536 is available in a 14 pin ceramic DIP package.

Pinout

HC-55536 (CERAMIC DIP)
TOP VIEW



Functional Diagram



8 TELECOMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Minimum V_{DD} Voltage ..... +3.0V
Operating V_{DD} Range ..... +3.0V to +7.0V
Junction Temperature ..... 175°C

Operating Temperature Ranges
HC-55536-5 ..... 0°C to +75°C
HC-55536-9 ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Unless Otherwise Specified: V_{DD} = +5.0V; Bit Range = 16K Bits/sec; typical parameters are at +25°C. Min-Max parameters are over operating temperature.

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Clock Sampling Rate	9	16	64	Kbps	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+3.0		+7.0	V	
Supply Current		0.3	1.5	mA	
Logic "1" Input, V_{IH}	3.5	4.5		V	(2)
Logic "0" Input, V_{IL}			1.5	V	(2)
Audio Output Voltage		0.5	1.2	V_{rms}	(3)
Audio Output Impedance		150		kΩ	(4)
Syllabic Filter Time Constant		4.0		ms	(5)
L.P. Signal estimate Filter Time Conatant		1.0		ms	(5)
Step Size Ratio		24		dB	(6)
Resolution		0.1		%	(7)
Minimum Step Size		0.2		%	(8)
Signal/Noise Ratio	25			dB	
Quieting Pattern Amplitude		10		mV_{p-p}	(9)
Clamping Threshold		0.75		F.S.	(11)

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit. Clock may be run at greater than 64Kbps or less than 9Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. This output includes a DC bias of $V_{DD}/2$; therefore, an AC coupling capacitor is required unless the output filter also includes this bias.
4. Presents approximately 150KΩ in series with recovered audio voltage. Zero-signal reference is $V_{DD}/2$.
5. Note that filter time cinstants are inversely proportional to clock rate. Both filters approximate single pole responses.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. The "quieting" pattern or idle-channel audio output steps at ½ the bit rate, changing state on negative clock transitions.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered singal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

FIG. 1. Illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

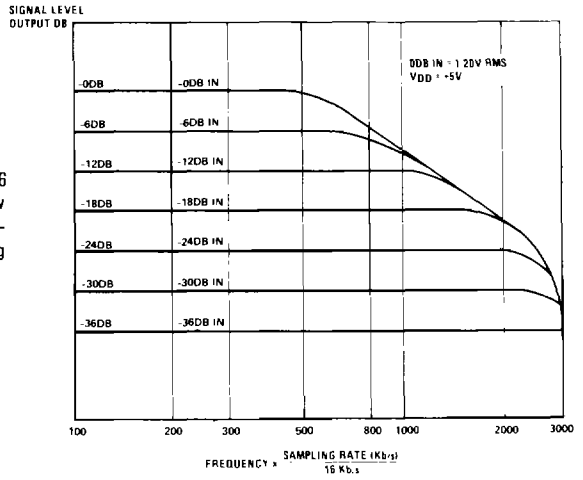


FIGURE 1 - TRANSFER FUNCTION FOR CVSD AT 16Kbps

Die Characteristics

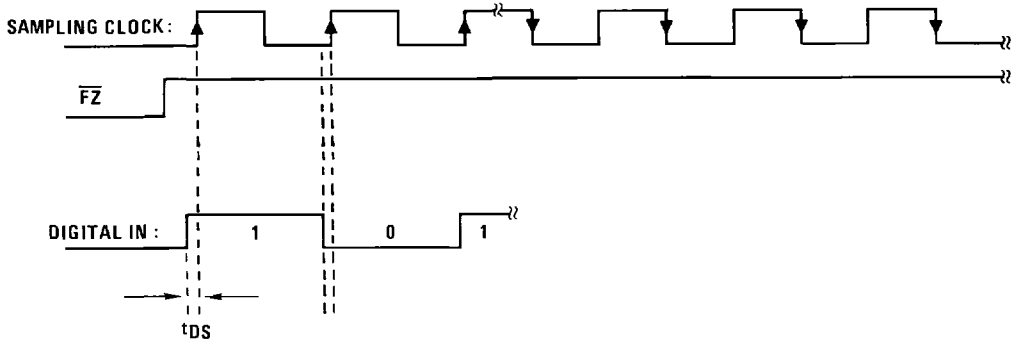
Transistor Count	1790	
Die Dimensions	154 x 93	
Substrate Potential	+V	
Process	SAJI CMOS	
Thermal Constants (^{o}C/W)	θ_{ja}	θ_{jc}
Ceramic DIP, HC-55536	75	15

Pin Description

PIN NO. 14-LEAD DIP	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage.
2	N.C.	No internal connection is made to this pin.
3	Audio Out	Recovered audio out. Presents approximately 150KΩ source with DC offset of $V_{DD}/2$ should be externally AC couples.
4	N.C.	No internal connection is made to this pin.
5	N.C.	No internal connection is made to this pin.
6, 7	N.C.	No internal connection is made to these pins.
8	Digital GND.	Logic Ground.
9	Clock	Sampling rote clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10	N.C.	No internal connection is made to this pin.
11	N.C.	No internal connection is made to this pin.
12	Digital In	Input for the received serial NRZ digital data.
13	$\overline{FZ}$	Active low logic input. Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	N.C.	No internal connection is made to this pin.

NOTE: No active input should be left in a "floating condition".

Timing Waveforms



tDS : DATA SET UP TIME 100ns TYPICAL

FIGURE 2 – CVSD TIMING DIAGRAM