REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, page 7; correct $\overline{SCLR}$ minimum limit. Change code ident. no. to 67268. Page 4, V_{OH} and V_{OL}, Editorial corrections for V_{IN}. Page 11, Fig. 3; Correct CCO output. Editorial Changes.	87-10-15	R. P. Evans
B	Table I, change Min. Limits on t_{s1}, t_{s5}, and t_{s6}. Editorial changes throughout. -les	00-02-28	Raymond Monnin

Current CAGE Code 67268

REV																				
SHEET																				
REV	B	B																		
SHEET	15	16																		

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Monica Grosel

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
87-04-01

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL, BIPOLAR SYNCHRONOUS FOUR-BIT BINARY UP-DOWN COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-87544**

SHEET 1 OF 16

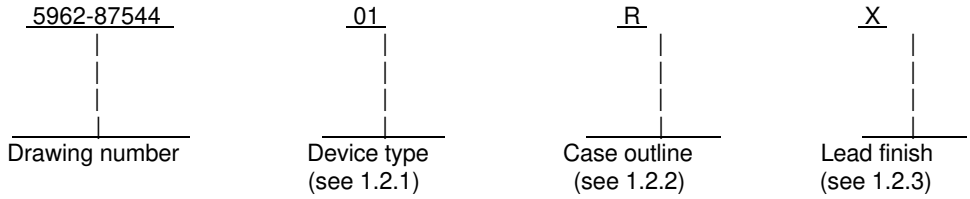
DSCC FORM 2233
APR 97

5962-E526-00

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	25LS2569	Synchronous four-bit binary up-down counter with three state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage	-1.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	0.7W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C
DC input current	-30 mA to +5.0 mA
DC output current into output	30 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high-level input voltage (V_{IH})	+2.0 V dc
Maximum low-level input voltage (V_{IL})	+0.7 V dc

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = +4.5 V, V_{IN} = 0.7 V or 2.0 V	Y outputs I_{OH} = -1.0 mA	1, 2, 3	2.4		V
			I_{OH} = -440 µA CCO, $\overline{RCO}$ outputs	1, 2, 3	2.5		V
Low level output voltage	V_{OL}	V_{CC} = +4.5 V, V_{IN} = 0.7 V or 2.0 V	I_{OL} = 4.0 mA	1, 2, 3		0.4	V
			I_{OL} = 8.0 mA	1, 2, 3		0.45	V
Input clamp voltage	V_{IC}	I_{IN} = -18 mA, V_{CC} = 4.5 V		1, 2, 3		-1.5	V
High level input current	I_{IH1}	V_{CC} = +5.5 V, V_{IN} = 2.7 V		1, 2, 3		20	µA
	I_{IH2}	V_{CC} = +5.5 V, V_{IN} = 7.0 V		1, 2, 3		100	µA
Low level input current	I_{IL}	V_{CC} = +5.5 V, V_{IN} = 0.4 V	$\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{LOAD}$	1, 2, 3		-300	µA
			A, B, C, D, CP, $\overline{CEP}$	1, 2, 3		-400	µA
			$\overline{CET}$, $\overline{SCLR}$	1, 2, 3		-650	µA
Low level input current	I_{OZ}	V_{CC} = +5.5 V	V_{OUT} = 0.4 V	1, 2, 3		-20	µA
			V_{OUT} = 2.4 V	1, 2, 3		20	µA
Output short circuit current	I_{OS}	V_{CC} = +5.5 V, 1/ V_{OUT} = 0.0 V		1, 2, 3	-15	-85	mA
Power supply current	I_{CC}	V_{CC} = +5.5 V, $\overline{OE}$ = High All inputs = GND		1, 2, 3		43	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Functional testing		See 4.3.1c		7			
Propagation delay time clock to any Q $\overline{LOAD}$ = low	t_{PLH1}	R_{L1} = 5 kΩ R_{L2} = 2 kΩ (figure 4)	C_L = 50 pF 2/	9, 10, 11		24	ns
			C_L = 15 pF 3/	9		18	
	t_{PHL1}		C_L = 50 pF 2/	9, 10, 11		35	ns
			C_L = 15 pF 3/	9		21	
Propagation delay time clock to any Q $\overline{LOAD}$ = high	t_{PLH2}		C_L = 50 pF 2/	9, 10, 11		24	ns
			C_L = 15 pF 3/	9		18	
	t_{PHL2}		C_L = 50 pF 2/	9, 10, 11		35	ns
			C_L = 15 pF 3/	9		21	
Propagation delay time $\overline{CET}$ to $\overline{RCO}$	t_{PLH3}	R_L = 2 kΩ (figure 4)	C_L = 50 pF 2/	9, 10, 11		19	ns
			C_L = 15 pF 3/	9		16	
	t_{PHL3}		C_L = 50 pF 2/	9, 10, 11		21	ns
			C_L = 15 pF 3/	9		14	
Propagation delay time U/$\overline{D}$ to $\overline{RCO}$	t_{PLH4}		C_L = 50 pF 2/	9, 10, 11		28	ns
			C_L = 15 pF 3/	9		23	
	t_{PHL4}		C_L = 50 pF 2/	9, 10, 11		30	ns
			C_L = 15 pF 3/	9		20	
Propagation delay time clock to $\overline{RCO}$	t_{PLH5}		C_L = 50 pF 2/	9, 10, 11		40	ns
			C_L = 15 pF 3/	9		35	
	t_{PHL5}		C_L = 50 pF 2/	9, 10, 11		39	ns
			C_L = 15 pF 3/	9		26	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time clock to CCO	t_{PLH6}	$R_{L2} = 2\ k\Omega$ (figure 4)	$C_L = 50\ pF$ 2/	9, 10, 11		18	ns
			$C_L = 15\ pF$ 3/	9		15	
	t_{PHL6}		$C_L = 50\ pF$ 2/	9, 10, 11		27	ns
			$C_L = 15\ pF$ 3/	9		15	
Propagation delay time $\overline{CET}$ or $\overline{CEP}$ to CCO	t_{PLH7}		$C_L = 50\ pF$ 2/	9, 10, 11		17	ns
			$C_L = 15\ pF$ 3/	9		15	
	t_{PHL7}		$C_L = 50\ pF$ 2/	9, 10, 11		45	ns
			$C_L = 15\ pF$ 3/	9		25	
Propagation delay time $\overline{ACLR}$ to any Q	t_{PLH8}	$R_{L1} = 5\ k\Omega$ $R_{L2} = 2\ k\Omega$ (figure 4)	$C_L = 50\ pF$ 2/	9, 10, 11		N/A	ns
			$C_L = 15\ pF$ 3/	9		N/A	
	t_{PHL8}		$C_L = 50\ pF$ 2/	9, 10, 11		45	ns
			$C_L = 15\ pF$ 3/	9		26	
Setup time A, B, C, D	t_{S1}	2/		9, 10, 11	35		ns
		3/		9	22		
Setup time $\overline{SCLR}$	t_{S2}	2/		9, 10, 11	35		ns
		3/		9	20		
Setup time $\overline{LOAD}$	t_{S3}	2/		9, 10, 11	45		ns
		3/		9	30		
Setup time U/$\overline{D}$	t_{S4}	2/		9, 10, 11	45		ns
		3/		9	30		
Setup time $\overline{CET}$, $\overline{CEP}$	t_{S5}	2/		9, 10, 11	65		ns
		3/		9	32		
Setup time $\overline{SCLR}$ recovery time (inactive to clock)	t_{S6}	2/		9, 10, 11	60		ns
		3/		9	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Data hold	t_H	2/		9, 10, 11	5		ns
		3/		9	0		
Clock pulse width	t_{PW}	2/		9, 10, 11	37		ns
		3/		9	25		
Enable time $\overline{OE}$ to any Q	t_{PZH}	$R_{L1} = 5\ k\Omega$ $R_{L2} = 2\ k\Omega$ (figure 4)	$C_L = 50$ pF 2/	9, 10, 11		20	ns
			$C_L = 15$ pF 3/	9		11	
Enable time $\overline{OE}$ to any clock	t_{PZL}		$C_L = 50$ pF 2/	9, 10, 11		34	ns
			$C_L = 15$ pF 3/	9		19	
Disable time $\overline{OE}$ to any Q	t_{PHZ}	$C_L = 5$ pF $R_{L1} = 5\ k\Omega$ $R_{L2} = 2\ k\Omega$	2/	9, 10, 11		22	ns
			3/	9		18	
	t_{PLZ}		2/	9, 10, 11		36	ns
			3/	9		24	

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed one second.

2/ Supply voltage = +4.5 V to +5.5 V, operating temperature = -55°C to +125°.

3/ Supply voltage = +5.0 V, operating temperature = +25°C.

Device type	01	
Case Outline	R and S	2
Terminal Number	Terminal Symbol	Terminal Symbol
1	U/$\overline{D}$	U/$\overline{D}$
2	CP	CP
3	A	A
4	B	B
5	C	C
6	D	D
7	$\overline{CEP}$	$\overline{CEP}$
8	$\overline{ACLR}$	$\overline{ACLR}$
9	$\overline{SCLR}$	$\overline{SCLR}$
10	GND	GND
11	$\overline{LOAD}$	$\overline{LOAD}$
12	$\overline{CET}$	$\overline{CET}$
13	Y_D	Y_D
14	Y_C	Y_C
15	Y_B	Y_B
16	Y_A	Y_A
17	$\overline{OE}$	$\overline{OE}$
18	CCO	CCO
19	$\overline{RCO}$	$\overline{RCO}$
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Mode	Load	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Async clear	Sync clear	$\overline{OE}$ 1/	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	Clock carry
Clear (async)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1 2/
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	⊓
Clear (sync)	X	X	X	1	1	0	0	X	X	X	X	.	0	0	0	0	1	1 2/
	X	X	X	0	1	0	0	X	X	X	X	.	0	0	0	0	0	⊓
Load	0	X	1	X	1	1	0	X	X	X	X	.	$Q_n = D_n$				1	1 2/
	0	X	0	0	1	1	0	0	0	0	0	.	0	0	0	0	0	⊓
	0	X	0	1	1	1	0	1	1	1	1	.	1	1	1	1	0	2/ ⊓
Count up	1	0	0	1	1	1	0	X	X	X	X	.	Q_n +1				3/	4/
Count down	1	0	0	1	1	1	0	X	X	X	X	.	Q_n -1				5/	4/
Inhibit	1	0	1	X	1	1	0	X	X	X	X	↑	NC				NC	1
	1	1	0	X	1	1	0	X	X	X	X	↑	NC				NC	1
	1	1	1	X	1	1	0	X	X	X	X	.	NC				NC	1
Output disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	NC	NC

↑ = Clock low-to-high transition.
X = Don't care.
D_n = D_0 through D_3 input level prior to clock transition.
Q_n +1 = Next higher count in binary sequence.
Q_n -1 = Next lower count in binary sequence.
NC = No change.

NOTES:
1. Register performs at correct logic for any state of $\overline{OE}$, but $\overline{OE}$ = 0 to view outputs.
2. Follows clock if $\overline{CET}$ = $\overline{CEP}$ = 0, otherwise remains high.
3. Low for one full clock cycle when maximum count is reached otherwise remains high.
4. Follows clock when RC = 0.
5. Low for one full clock cycle when minimum count is reached otherwise remains high.

FIGURE 2. Truth table.

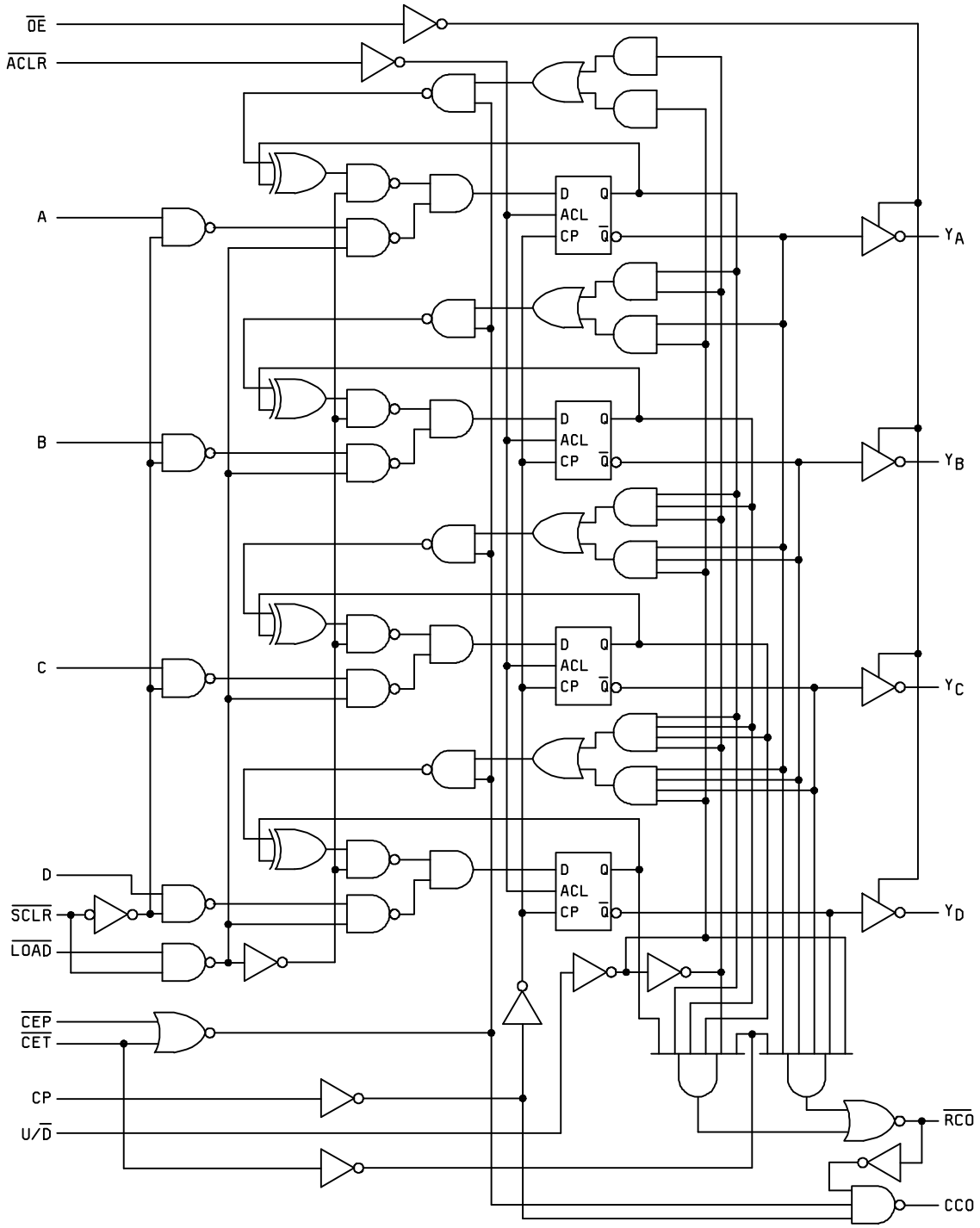
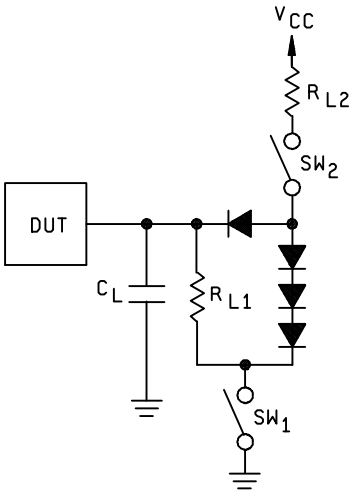
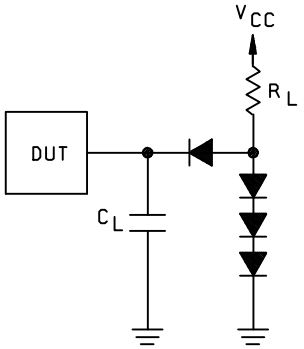


FIGURE 3. Logic diagram.

AC BENCH LOAD TEST CIRCUIT
FOR THREE-STATE OUTPUTS



AC BENCH LOAD TEST CIRCUIT
FOR NON THREE-STATE OUTPUTS

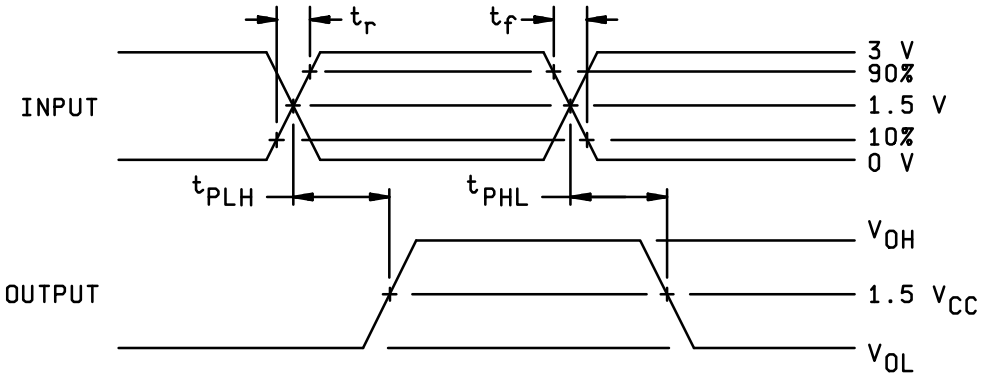


Switch Matrix

Parameter	SW_1	SW_2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{ZL}	Open	Closed
t_{ZH}	Closed	Open
t_{LZ}	Closed	Closed
t_{HZ}	Closed	Closed

FIGURE 4. Switching waveforms and test circuits.

PROPAGATION DELAY TIME



ENABLE TIME

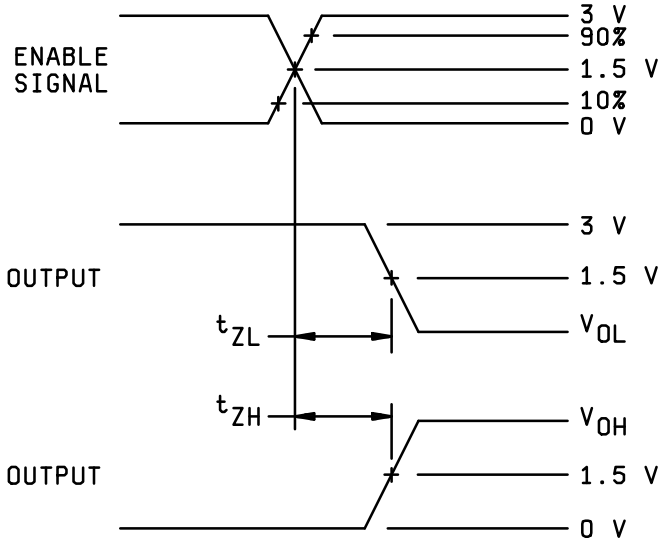
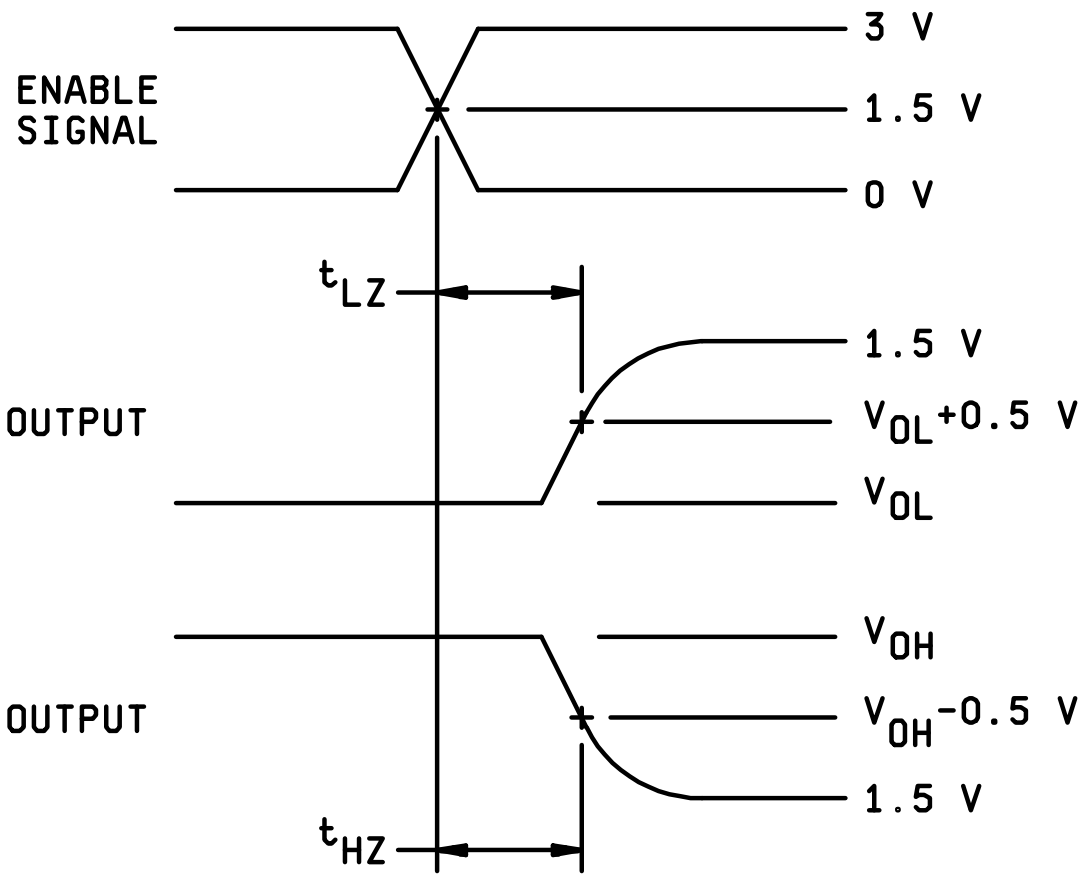


FIGURE 4. Switching waveforms and test circuits - Continued.

DISABLE TIME



NOTES:
1. Pulse generator for all pulses.
2. Rate < 1.0 MHz; $Z_0 = 50\Omega$; $t_r \leq 14$ ns; tf < 6.0 ns.
3. C_L includes probe and jig capacitance.
4. All diodes ar 1N916 or `1N3064.

FIGURE 4. Switching waveforms and test circuits - Continued.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-02-28

Approved sources of supply for SMD 5962-87544 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8754401RA	3V146	25LS2569/BRA
5962-8754401SA	3V146	25LS2569/BSA
5962-87544012A	3V146	25LS2569/B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950