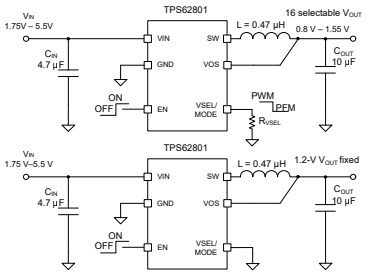
# TPS6280x 1.75-V to 5.5-V, 0.6-A/1-A, 2.3-µA $I_Q$ Step Down Converter 6-Pin, 0.35-mm Pitch WCSP Package

## 1 Features

- 1.75-V to 5.5-V input voltage range
- 2.3-µA operating quiescent current
- Up to 4-MHz switching frequency
- 0.6-A or 1-A output current
- 1% output voltage accuracy
- Selectable power save and forced PWM mode
- R2D converter for flexible $V_{OUT}$ setting
- 16 selectable and one fixed output voltages
  - TPS62800 (4 MHz): 0.4 V to 0.775 V
  - TPS62801 (4 MHz): 0.8 V to 1.55 V
  - TPS62802 (4 MHz): 1.8 V to 3.3 V
  - TPS62806 (1.5 MHz): 0.4 V to 0.775 V
  - TPS62807 (1.5 MHz): 0.8 V to 1.55 V
  - TPS62808 (1.5 MHz): 1.8 V to 3.3 V
- Smart enable pin
- Optimized pinout to support 0201 components
- DCS-Control topology
- Output discharge
- 100% duty cycle operation
- Tiny 6-pin, 0.35-mm pitch WCSP package
- Supports < 0.6-mm solution height
- Supports < 5-mm$^2$ solution size
- Create a custom design using the:
  - TPS62800 WEBENCH® Power Designer
  - TPS62801 WEBENCH® Power Designer
  - TPS62802 WEBENCH® Power Designer
  - TPS62806 WEBENCH® Power Designer
  - TPS62807 WEBENCH® Power Designer
  - TPS62808 WEBENCH® Power Designer

## 2 Applications

- Wearable electronics, IoT applications
- 2× AA battery-powered applications
- Smartphones




**Typical Application**

## 3 Description

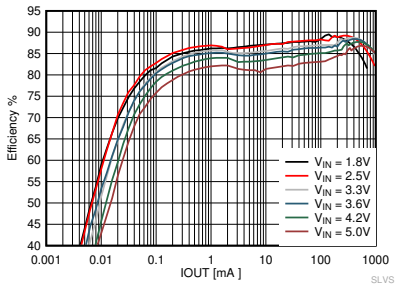
The TPS6280x device family is a step-down converter with 2.3-µA typical quiescent current featuring the highest efficiency and smallest solution size. TI's DCS-Control™ topology enables the device to operate with tiny inductors and capacitors with a switching frequency up to 4 MHz. At light load conditions, the device seamlessly enters power save mode to reduce switching cycles and maintain high efficiency.

Connecting the VSEL/MODE pin to GND selects a fixed output voltage. With only one external resistor connected to VSEL/MODE pin, 16 internally set output voltages can be selected. An integrated R2D (resistor-to-digital) converter reads out the external resistor and sets the output voltage. The same device part number can be used for different applications and voltage rails just by changing a single resistor. Furthermore, the internally set output voltage provides better accuracy compared to a traditional external resistor divider network. Once the device has started up, the DC/DC converter enters forced PWM mode by applying a high level at the VSEL/MODE pin. In this operating mode, the device runs at a typical 4-MHz or 1.5-MHz switching frequency, enabling lowest output voltage ripple and highest efficiency. The TPS6280x device series comes in a tiny 6-pin WCSP package with 0.35-mm pitch.

**Device Information**

| Part Number | Package(1) | Body Size (NOM) |
|---|---|---|
| TPS62800 | DSBGA (6) | 1.05 mm × 0.70 mm × 0.4 mm |
| TPS62801 | | |
| TPS62802 | | |
| TPS62806 | | |
| TPS62807 | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Efficiency Versus $I_{OUT}$ at 1.2 $V_{OUT}$**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (July 2018) to Revision F (June 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 1 |
| • Updated the minimum input voltage to 1.75 V | 1 |
| • Updated max rising UVLO spec | 6 |

| Changes from Revision D (July 2018) to Revision E (January 2019) | Page |
|---|---|
| • Added devices TPS62807 and TPS62808 throughout data sheet | 1 |

## 5 Device Comparison Table

| Device | Function VSEL/MODE | Fixed VOUT | Selectable Output Voltages with $R_{VSEL}$ | $f_{SW}$ [MHz] | $I_{OUT}$ [A] | Soft Start, $t_{SS}$ | Output Discharge |
|---|---|---|---|---|---|---|---|
| TPS62800 | VSEL + MODE | 0.7 V (VSEL / MODE = GND) | 0.4 V–0.775 V in 25-mV steps | 4 | 1 | 125 µs | Yes |
| TPS62801 | VSEL + MODE | 1.20 V (VSEL / MODE = GND) | 0.8 V–1.55 V in 50-mV steps | 4 | 1 | 125 µs | Yes |
| TPS62802 | VSEL + MODE | 1.8 V (VSEL / MODE = GND) | 1.8 V–3.3 V in 100-mV steps | 4 | 1 | 400 µs | Yes |
| TPS62806 | VSEL + MODE | 0.7 V (VSEL / MODE = GND) | 0.4 V–0.775 V in 25-mV steps | 1.5 | 0.6 | 125 µs | Yes |
| TPS62807 | VSEL + MODE | 1.20 V (VSEL / MODE = GND) | 0.8 V–1.55 V in 50-mV steps | 1.5 | 0.6 | 125 µs | Yes |
| TPS62808 | VSEL + MODE | 1.8 V (VSEL / MODE = GND) | 1.8 V–3.3 V in 100-mV steps | 1.5 | 0.6 | 125 µs | Yes |

## 6 Pin Configuration and Functions

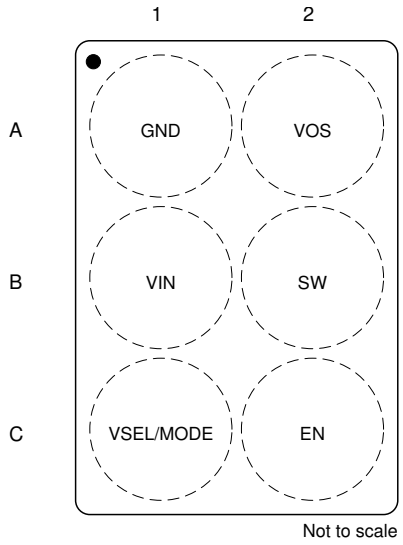



**Figure 6-1. 6-Pin DSBGA YKA Package (Top View)**

**Table 6-1. Pin Functions**

| Pin | | I/O | Description |
|---|---|---|---|
| Name | NO. | | |
| GND | A1 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| VIN | B1 | PWR | $V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required. |
| VSEL/MODE | C1 | IN | Connecting a resistor to GND selects a pre-defined output voltage. Once the device has started up, the R2D converter is disabled and the pin operates as an input. Applying a high level selects forced PWM mode operation and a low level power save mode operation. |
| VOS | A2 | IN | Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges $V_{OUT}$ by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| SW | B2 | OUT | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| EN | C2 | IN | A high level enables the devices, and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up. |

**Table 6-2. Output Voltage Setting (VSEL/MODE Pin)**

| VSEL | Output Voltage Setting $V_{OUT}$ [V] | | | $R_{VSEL}$ Resistance [kΩ], E96 Resistor Series, 1% Accuracy, Temperature Coefficient Better or Equal than ±200 ppm/°C |
|---|---|---|---|---|
| | TPS62800 TPS62806 | TPS62801 TPS62807 | TPS62802 TPS62808 | |
| 0 | 0.700 | 1.2 | 1.8 | Connected to GND (no resistor needed) |
| 1 | 0.400 | 0.8 | 1.8 | 10.0 |
| 2 | 0.425 | 0.85 | 1.9 | 12.1 |
| 3 | 0.450 | 0.9 | 2.0 | 15.4 |
| 4 | 0.475 | 0.95 | 2.1 | 18.7 |
| 5 | 0.500 | 1.0 | 2.2 | 23.7 |
| 6 | 0.525 | 1.05 | 2.3 | 28.7 |
| 7 | 0.550 | 1.1 | 2.4 | 36.5 |
| 8 | 0.575 | 1.15 | 2.5 | 44.2 |
| 9 | 0.600 | 1.2 | 2.6 | 56.2 |
| 10 | 0.625 | 1.25 | 2.7 | 68.1 |
| 11 | 0.650 | 1.3 | 2.8 | 86.6 |
| 12 | 0.675 | 1.35 | 2.9 | 105.0 |
| 13 | 0.700 | 1.4 | 3.0 | 133.0 |
| 14 | 0.725 | 1.45 | 3.1 | 162.0 |
| 15 | 0.750 | 1.5 | 3.2 | 205.0 |
| 16 | 0.775 | 1.55 | 3.3 | 249.0 or larger |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

| | | MIN(1) | MAX(1) | UNIT |
|---|---|---|---|---|
| Pin voltage(2) | VIN | –0.3 | 6 | V |
| | SW | –0.3 | $V_{IN}$ + 0.3 V | V |
| | SW (AC), less than 10 ns while switching | –2.5 | 9 | V |
| | EN, VSEL/MODE | –0.3 | 6 | V |
| | VOS | –0.3 | 5 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage, $V_{IN}$ | 1.75 | | 5.5 | V |
| $I_{OUT}$ | Output current, $V_{IN}$ ≥ 2.3 V, TPS62800, TPS62801, TPS62802 | | | 1 | A |
| $I_{OUT}$ | Output current, $V_{IN}$ < 2.3 V, TPS62800, TPS62801, TPS62802 | | | 0.7 | A |
| $I_{OUT}$ | Output current, TPS62806, TPS62807, TPS62808 | | | 0.6 | A |
| L | Effective inductance, TPS62800, TPS62801, TPS62802 | 0.33 | 0.47 | 0.82 | µH |
| $C_{OUT}$ | Effective output capacitance, TPS62800, TPS62801, TPS62802 | 2 | | 26 | µF |
| L | Effective inductance, TPS62806, TPS62807, TPS62808 | 0.7 | 1.0 | 1.2 | µH |
| $C_{OUT}$ | Effective output capacitance, TPS62806, TPS62807, TPS62808 | 3 | | 26 | µF |
| $C_{IN}$ | Effective input capacitance | 0.5 | 4.7 | | µF |
| $C_{VSEL/MODE}$ | External parasitic capacitance at the VSEL/MODE pin | | | 30 | pF |
| $R_{VSEL}$ | Resistance range for external resistor at VSEL/MODE pin (E96 1% resistor values) | 10 | | 249 | kΩ |
| | External resistor tolerance E96 series at VSEL/MODE pin | | | 1% | |
| | E96 resistor series temperature coefficient (TCR) | –200 | | +200 | ppm/°C |
| $T_J$ | Operating junction temperature range | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | YKA (DSBGA) | UNIT |
|---|---|---|---|
| | | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 147.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 47.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

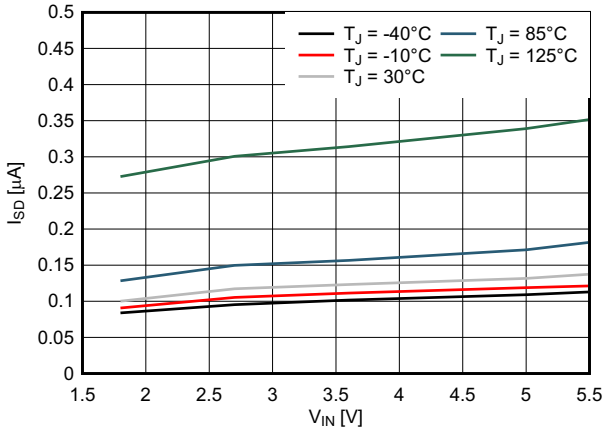
$V_{IN}$ = 3.6 V, $T_J$ = –40°C to 125°C typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Operating quiescent current (power save mode) | EN = $V_{IN}$, $I_{OUT}$ = 0 µA, $V_{OUT}$ = 1.2 V, device not switching, $T_J$ = –40°C to +85°C | | 2.3 | 4 | µA |
| | | EN = $V_{IN}$, $I_{OUT}$ = 0 µA, $V_{OUT}$ = 1.2 V, device switching | | 2.5 | | µA |
| | Operating quiescent current (PWM mode) | EN = $V_{IN}$, VSEL/MODE = $V_{IN}$ (after power up), device switching, $I_{OUT}$ = 0 mA, $V_{OUT}$ = 1.2 V | | 8 | | mA |
| $I_{SD}$ | Shutdown current | EN = GND, shutdown current into $V_{IN}$, VSEL/MODE = GND, $T_J$ = –40°C to +85°C | | 120 | 250 | nA |
| $V_{TH\_UVLO+}$ | Undervoltage lockout threshold | Rising $V_{IN}$ | | 1.65 | 1.75 | V |
| $V_{TH\_UVLO-}$ | | Falling $V_{IN}$ | | 1.56 | 1.7 | V |
| **INPUT EN** | | | | | | |
| $V_{IH\ TH}$ | High level input voltage | | 0.8 | | | V |
| $V_{IL\ TH}$ | Low level input voltage | | | | 0.4 | V |
| $I_{IN}$ | Input bias current | $T_J$ = –40°C to +85°C, EN = high | | 10 | 25 | nA |
| $R_{PD}$ | Internal pulldown resistance | EN = low | | 500 | | kΩ |
| **INPUT VSEL/MODE** | | | | | | |
| $V_{IH\ TH}$ | High level input voltage (digital input) | | 0.8 | | | V |
| $V_{IL\ TH}$ | Low level input voltage (digital input) | | | | 0.4 | V |
| $I_{IN}$ | Input bias current | EN = high | | 10 | 25 | nA |
| **POWER SWITCHES** | | | | | | |
| $I_{LKG\_SW}$ | Leakage current into the SW pin | $V_{SW}$ = 1.2 V, $T_J$ = –40°C to +85°C | | 10 | 25 | nA |
| $R_{DS(ON)}$ | High side MOSFET on-resistance | $I_{OUT}$ = 500 mA | | 120 | 170 | mΩ |
| | Low side MOSFET on-resistance | $I_{OUT}$ = 500 mA | | 80 | 115 | mΩ |
| $I_{LIMF}$ | High-side MOSFET switch current limit | TPS62806, TPS62807, TPS62808 | 0.95 | 1.1 | 1.2 | A |
| $I_{LIMF}$ | Low-side MOSFET switch current limit | TPS62806, TPS62807, TPS62808 | 0.85 | 1 | 1.1 | A |
| $I_{LIMF}$ | High-side MOSFET switch current limit | TPS62800, TPS62801 | 1.3 | 1.45 | 1.55 | A |
| | | TPS62802 | 1.4 | 1.55 | 1.65 | A |
| $I_{LIMF}$ | Low-side MOSFET switch current limit | TPS62800, TPS62801 | 1.2 | 1.35 | 1.45 | A |
| | | TPS62802 | 1.3 | 1.45 | 1.55 | A |
| **OUTPUT VOLTAGE DISCHARGE** | | | | | | |

$V_{IN}$ = 3.6 V, $T_J$ = –40°C to 125°C typical values are at $T_J$ = 25°C (unless otherwise noted)

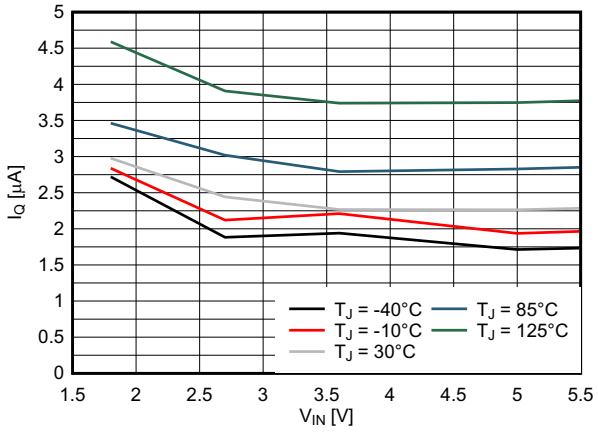
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DSCH\_VOS}$ | MOSFET on-resistance | EN = GND, $I_{VOS}$ = –10 mA into the VOS pin<br>$T_J$ = –40°C to +85°C | | 7 | 11 | Ω |
| $I_{IN\_VOS}$ | Bias current into the VOS pin | EN = $V_{IN}$, $V_{OUT}$ = 1.2 V (internal 12-MΩ resistor divider), $T_J$ = –40°C to +85°C | | 100 | 400 | nA |
| **THERMAL PROTECTION** | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | Rising junction temperature, PWM mode | | 160 | | °C |
| | Thermal shutdown hysteresis | | | 20 | | °C |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage range | TPS62800, TPS62806, 25-mV steps | 0.4 | | 0.775 | V |
| $V_{OUT}$ | Output voltage range | TPS62801, TPS62807, 50-mV steps | 0.8 | | 1.55 | V |
| $V_{OUT}$ | Output voltage range | TPS62802, TPS62808, 100-mV steps | 1.8 | | 3.3 | V |
| $V_{OUT}$ | Output voltage accuracy | Power save mode | | 0% | | |
| $V_{OUT}$ | Output voltage accuracy | PWM mode, $I_{OUT}$ = 0 mA, $T_J$ = 25°C to +85°C | –1% | 0% | 1% | |
| $V_{OUT}$ | Output voltage accuracy | PWM mode, $I_{OUT}$ = 0 mA, $T_J$ = –40°C to +125°C | –2% | 0% | 1.7% | |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V, PWM operation | | 4 | | MHz |
| $f_{SW}$ | Switching frequency | TPS62806<br>$V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.7 V, PWM operation | | 1.5 | | MHz |
| $f_{SW}$ | Switching frequency | TPS62807<br>$V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V, PWM operation | | 1.5 | | MHz |
| $f_{SW}$ | Switching frequency | TPS62808<br>$V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.8 V, PWM operation | | 1.5 | | MHz |
| $t_{Startup\_delay}$ | Regulator start-up delay time | From transition EN = low to high until device starts switching, VSEL = 16 | | 500 | 1100 | µs |
| $t_{SS}$ | Soft-start time | TPS62801, from $V_{OUT}$ = 0 V to 0.95% of $V_{OUT}$ nominal | | 125 | 170 | µs |
| $t_{SS}$ | Soft-start time | TPS62800, TPS62806, TPS62807, TPS62808 from $V_{OUT}$ = 0 V to 0.95% of $V_{OUT}$ nominal | | 125 | 210 | µs |
| $t_{SS}$ | Soft-start time | TPS62802, from $V_{OUT}$ = 0 V to 0.95% of $V_{OUT}$ nominal | | 400 | 500 | µs |

## 7.6 Typical Characteristics



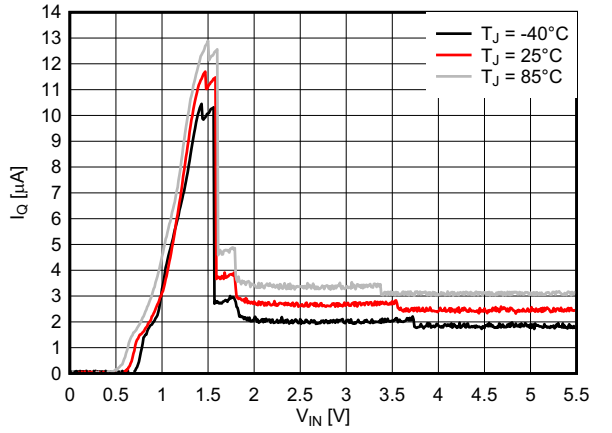

EN = GND

**Figure 7-1. Shutdown Current, $I_{SD}$**




Device not switching

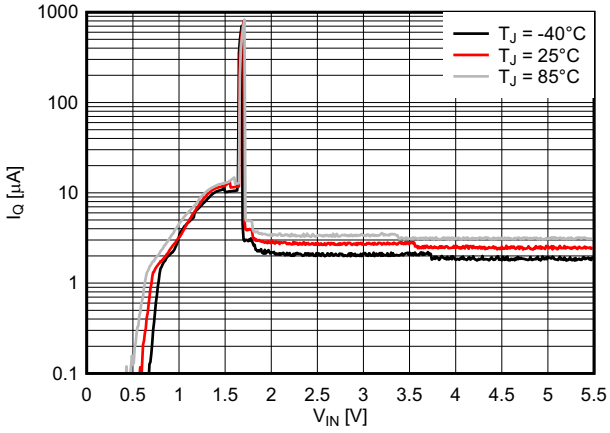
**Figure 7-2. Quiescent Current, $I_Q$**




$V_{IN}$ falling
$EN = V_{IN}$

Device switching, no load, $V_{OUT}$ = 1.2 V
VSEL/MODE = GND

**Figure 7-3. Operating Quiescent Current, $I_Q$**




$V_{IN}$ rising
$EN = V_{IN}$

Device switching, no load, $V_{OUT}$ = 1.2 V
VSEL/MODE = GND

**Figure 7-4. Operating Quiescent Current, $I_Q$**

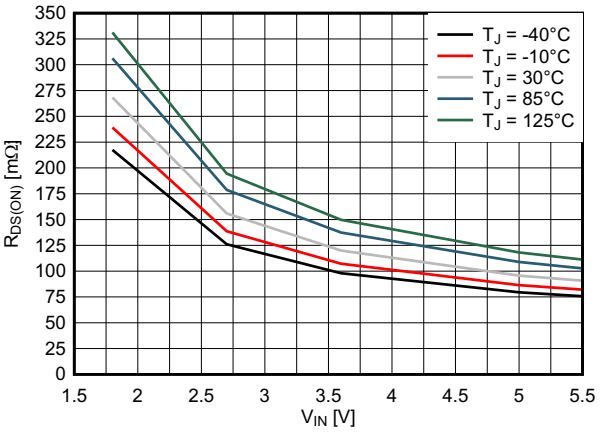



**Figure 7-5. High-Side Switch Drain Source Resistance, $R_{DS(ON)}$**

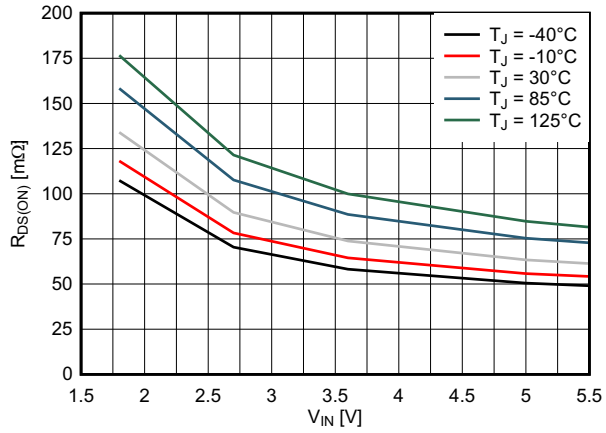



**Figure 7-6. Low-Side Switch Drain Source Resistance, $R_{DS(ON)}$**

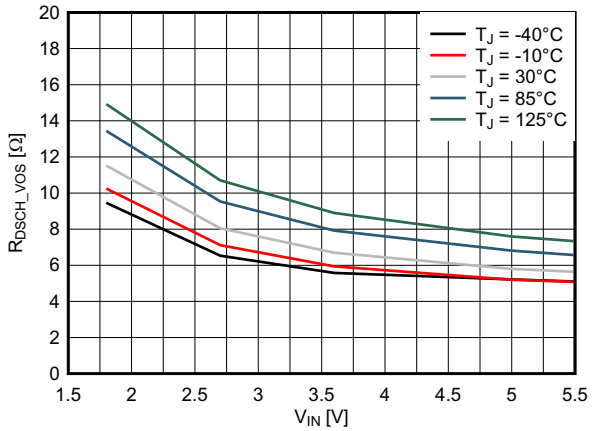



**Figure 7-7. VOS Discharge Switch Drain Source Resistance, $R_{DSCH\_VOS}$**

# 8 Detailed Description

## 8.1 Overview

The TPS6280x is a high frequency synchronous step-down converter with ultra-low quiescent current consumption. Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power save mode operation. TI's DCS-Control (Direct Control with Seamless Transition into power save mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop, which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

## 8.2 Functional Block Diagram

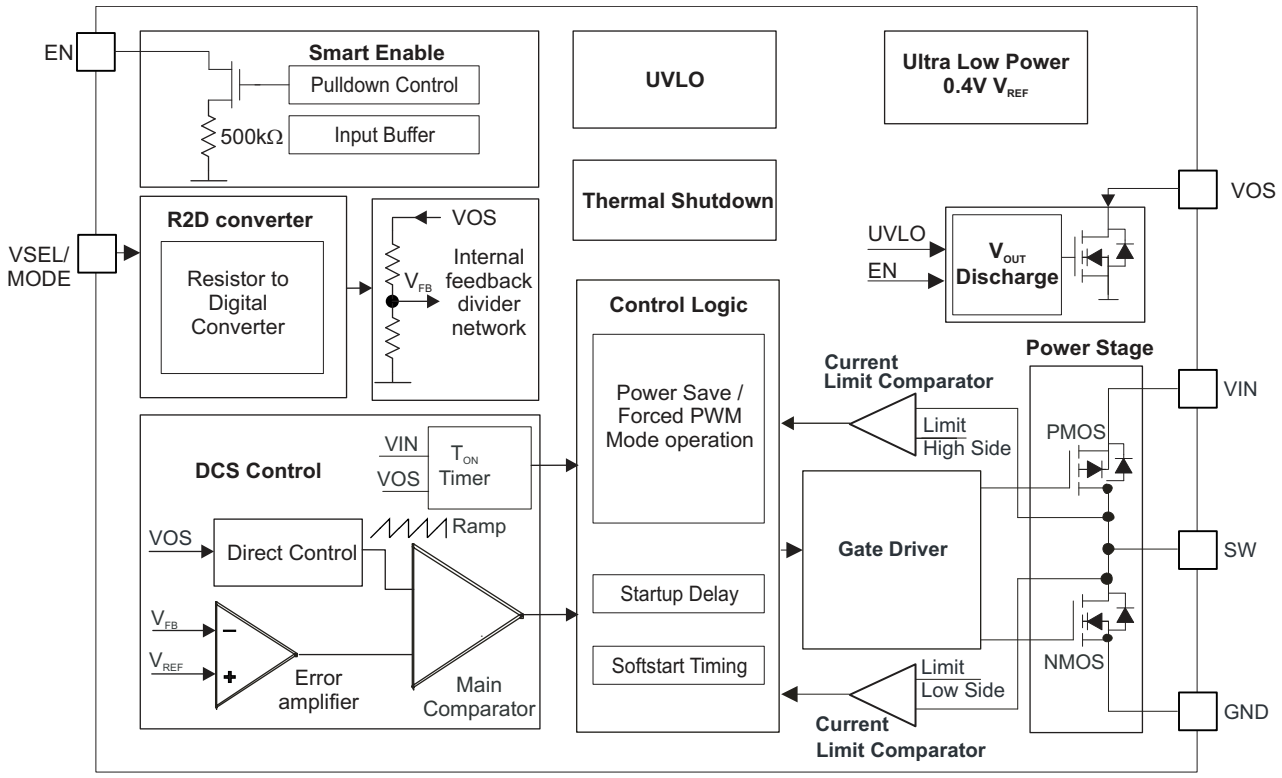



**Figure 8-1. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Smart Enable and Shutdown (EN)

An internal 500-kΩ resistor pulls the EN pin to GND and avoids the pin to be floating, which prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.2 Soft Start

Once the device has been enabled with EN high, it initializes and powers up its internal circuits, which occurs during the regulator start-up delay time, $t_{Startup\_delay}$. Once $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, $t_{ss}$. See Figure 8-2.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSEL value. $t_{Startup\_delay}$ is shortest with VSEL = 0 and longest with VSEL = 16. See Figure 9-42 to Figure 9-46.

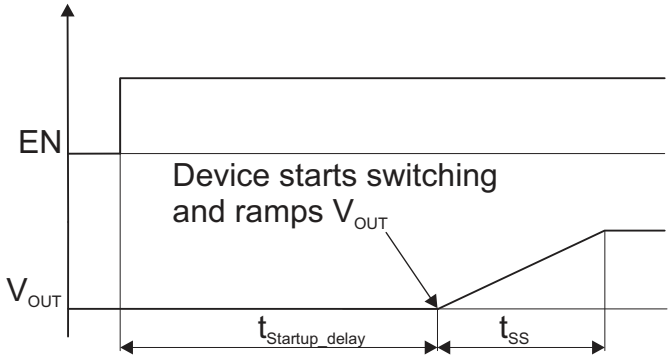



**Figure 8-2. Device Start-Up**

### 8.3.3 VSEL/MODE Pin

This pin has two functions: output voltage selection during start-up of the converter and operating mode selection. See Section 5.

#### *8.3.3.1 Output Voltage Selection (R2D Converter)*

The output voltage is set with a single external resistor connected between the VSEL/MODE pin and GND. Once the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor $R_{VSEL}$ within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. Once this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor.

After power up, the pin is configured as an input for mode selection. Therefore, the output voltage is set only once. If the mode selection function is used in combination with the VSEL function, ensure that there is no additional current path or capacitance greater than 30 pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. Table 6-2 lists the correct resistor values for $R_{VSEL}$ to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor, $R_{VSEL}$, is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Ensure that there is no other leakage path than the $R_{VSEL}$ resistor at the VSEL/MODE pin during an undervoltage lockout event. Otherwise, a false output voltage will be set.

Connecting VSEL/MODE to GND selects a pre-defined output voltage.

- TPS62800 = 0.7 V
- TPS62801 = 1.2 V
- TPS62802 = 1.8 V
- TPS62806 = 0.7 V
- TPS62807 = 1.2 V
- TPS62808 = 1.8 V

In this case, no external resistor is needed, which enables a smaller solution size.

#### *8.3.3.2 Mode Selection — Power Save Mode and Forced PWM Operation*

A low level at this pin selects power save mode operation, and a high level selects forced PWM operation. The mode can be changed during operation after the device has been powered up. The mode selection function is only available after the R2D converter has read out the external resistor.

### 8.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (maximum) with falling $V_{IN}$. The device starts at an input voltage of 1.75 V (maximum) rising $V_{IN}$. Once the device re-enters operation out of an undervoltage lockout condition, it behaves like being enabled. The internal control logic is powered up and the external resistor at the VSEL/MODE pin is read out.

### 8.3.5 Switch Current Limit and Short Circuit Protection

The TPS6280x integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, $I_{LIMF}$, trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low-side switch decreases below the low-side MOSFET current limit, $I_{LIMF}$, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

### 8.3.6 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. If $T_J$ exceeds the thermal shutdown temperature, $T_{SD}$, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When $T_J$ decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set $V_{OUT}$ (there is no R2D conversion of $R_{VSEL}$). The thermal shutdown is not active in power save mode.

### 8.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge feature is only active once the device has been enabled at least once since the supply voltage was applied. The output discharge function is not active if the device is disabled and the supply voltage is applied the first time.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO-}$.

## 8.4 Device Functional Modes

### 8.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 2.3 µA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device automatically enters PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency, $f_{sw}$, of typically 4 MHz or 1.5 MHz. The switching frequency in PWM mode is controlled and depends on $V_{IN}$ and $V_{OUT}$. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM ,mode is seamless with minimum output voltage ripple.

### 8.4.2 Forced PWM Mode Operation

After the device has powered up and ramped up $V_{OUT}$, the VSEL/MODE pin acts as an input. With a high level on VSEL/MODE pin, the device enters forced PWM mode and operates with a constant switching frequency over the entire load range, even at very light loads. This action reduces or eliminates interference with RF and noise sensitive circuits, but lowers efficiency at light loads.

### 8.4.3 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as D = $V_{OUT}$ / $V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point, which allows the conversion of small input to output voltage differences.

### 8.4.4 Optimized Transient Performance from PWM-to-PFM Mode Operation

For most converters, the load transient response in PWM mode is improved compared to PFM mode, since the converter reacts faster on the load step and actively sinks energy on the load release. Compare Figure 9-33 to Figure 9-32. As an additional feature, the TPS6280x automatically enters PWM mode for 16 cycles after a heavy load release to bring the output voltage back to the regulation level faster. After 16 cycles of PWM mode, the device automatically returns to PFM mode (if VSEL/MODE is driven low). See Figure 8-3. Without this optimization, the output voltage overshoot would be higher and would look like the $V_{OUT}$' trace. This feature is only active once the load is high enough and the converter operates in PWM mode.

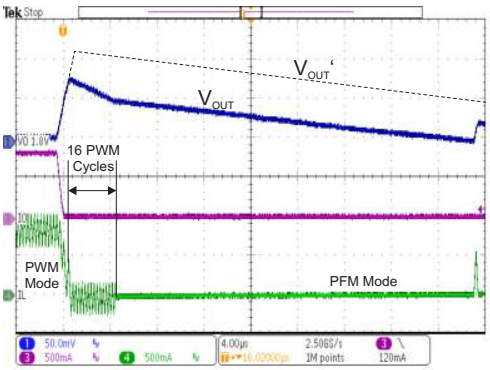



**Figure 8-3. Optimized Transient Performance from PWM-to-PFM Mode**

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 9.2 Typical Application

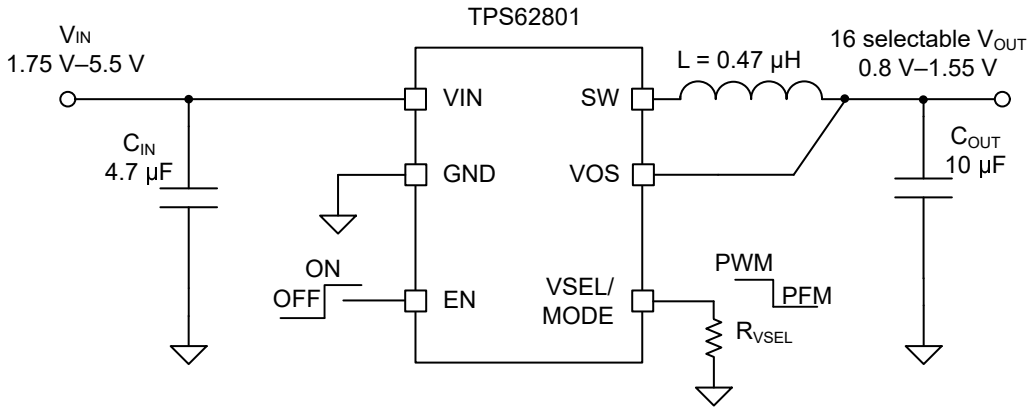



**Figure 9-1. TPS62801 Adjustable $V_{OUT}$ Application Circuit**

Additional circuits are shown in Section 9.3.

### 9.2.1 Design Requirements

Table 9-1 shows the list of components for the application circuit and the characteristic application curves

**Table 9-1. Components for Application Characteristic Curves**

| Reference | Description | Value | Size [L × W × T] | Manufacturer(1) |
|---|---|---|---|---|
| TPS62801 / 2 | Step down converter | | 1.05 mm × 0.70 mm × 0.4 mm maximum | Texas Instruments |
| $C_{IN}$ | Ceramic capacitor, GRM155R60J475ME47D | 4.7 µF | 0402 (1 mm × 0.5 mm × 0.6 mm maximum) | Murata |
| $C_{OUT}$ | Ceramic capacitor, GRM155R60J106ME15D | 10 µF | 0402 (1 mm × 0.5 mm × 0.65 mm maximum) | Murata |
| L | Inductor DFE18SANR47MG0L | 0.47 µH | 0603 (1.6 mm × 0.8 mm × 1.0 mm maximum) | Murata |

(1) See the *Third-party Products Disclaimer*.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPS62800 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62801 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62802 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62806 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62807 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62808 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### *9.2.2.2 Inductor Selection*

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$ and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with Equation 2, which is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, $I_{LIMF}$.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = switching frequency
- L = inductor value
- $\Delta I_L$ = peak-to-peak inductor ripple current
- $I_{Lmax}$ = maximum inductor current

Table 9-2 shows a list of possible inductors.

**Table 9-2. List of Possible Inductors**

| Inductance [µH] | Inductor Series | Size Imperial (Metric) | Dimensions L × W × T | Supplier(1) |
|---|---|---|---|---|
| 0.47 | DFE18SAN_G0 | 0603 (1608) | 1.6 mm × 0.8 mm × 1.0 mm maximum | Murata |
| 0.47 | HTEB16080F | 0603 (1608) | 1.6 mm × 0.8 mm × 0.6 mm maximum | Cyntec |
| 0.47 | HTET1005FE | 0402 (1005) | 1.0 mm × 0.5 mm × 0.65 mm maximum | Cyntec |
| 0.47 | TFM160808ALC | 0603 (1608) | 1.6 mm × 0.8 mm × 0.8 mm maximum | TDK |
| 1.0 | DFE201610E | 0806 (201610) | 2.0 mm × 1.6 mm × 1.0 mm maximum | Murata |

(1) See the *Third-party Products Disclaimer*.

#### 9.2.2.3 Output Capacitor Selection

The DCS-Control scheme of the TPS6280x allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple.

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 9-3 outlines possible inductor and capacitor value combinations.

**Table 9-3. Recommended LC Output Filter Combinations**

| Device | Nominal Inductor Value [µH] | Nominal Output Capacitor Value [µF] | | | |
|---|---|---|---|---|---|
| | | 4.7 µF | 10 µF | 2 × 10 µF | 22 µF |
| TPS62800, TPS62801 | 0.47(1) | √ | √(3) | √ | √ |
| TPS62802 | 0.47(1) | | √(3) | √ | √ |
| TPS62806, TPS62807, TPS62808 | 1.0(2) | √ | √(3) | √ | √ |

(1) An effective inductance range of 0.33 µH to 0.82 µH is recommended. An effective capacitance range of 2 µF to 26 µF is recommended.
(2) An effective inductance range of 0.7 µH to 1.2 µH is recommended. An effective capacitance range of 3 µF to 26 µF is recommended.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

#### 9.2.2.4 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-µF input capacitor is sufficient. When operating from a high impedance source, like a coin cell, a larger input buffer capacitor ≥ 10 µF is recommended to avoid voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall current consumption.

Table 9-4 shows a selection of input and output capacitors.

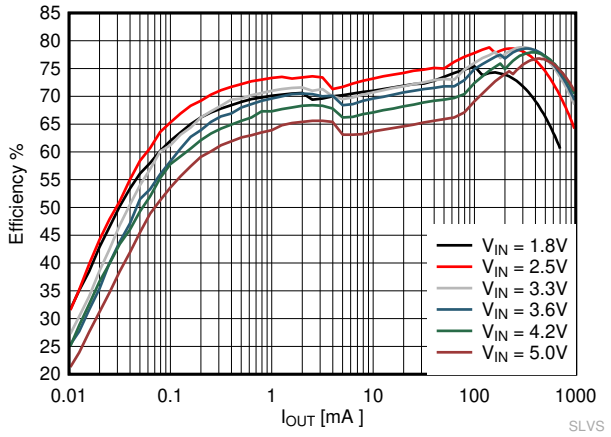
**Table 9-4. List of Possible Capacitors**

| Capacitance [µF] | Capacitor Part Number | Size Imperial (Metric) | Dimensions L × W × T | Supplier(1) |
|---|---|---|---|---|
| 4.7 | GRM155R60J475ME47D | 0402 (1005) | 1.0 mm × 0.5 mm × 0.6 mm maximum | Murata |
| 4.7 | GRM035R60J475ME15 | 0201 (0603) | 0.6 mm × 0.3 mm × 0.55 mm maximum | Murata |
| 10 | GRM155R60J106ME15D | 0402 (1005) | 1.0 mm × 0.5 mm × 0.65 mm maximum | Murata |

(1) See the *Third-party Products Disclaimer*.

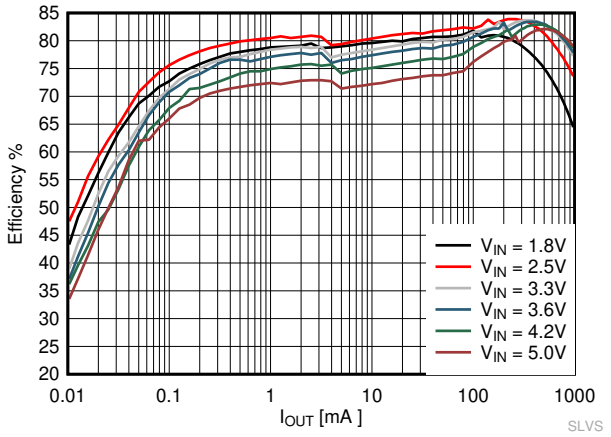
### 9.2.3 Application Curves

The conditions for the below application curves are $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V, and the components listed in Table 9-1, unless otherwise noted.



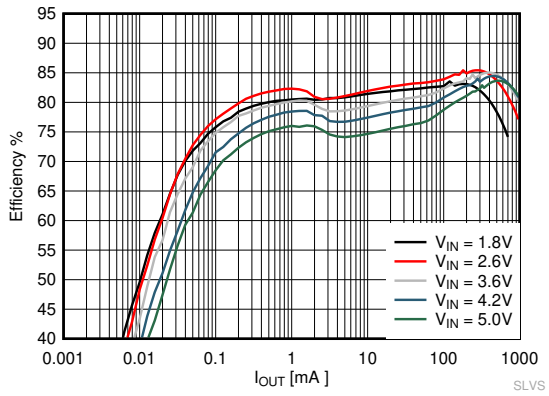

TPS62800 $R_{VSEL}$ = 10 kΩ to GND

**Figure 9-2. Efficiency Power Save Mode $V_{OUT}$ = 0.4 V**



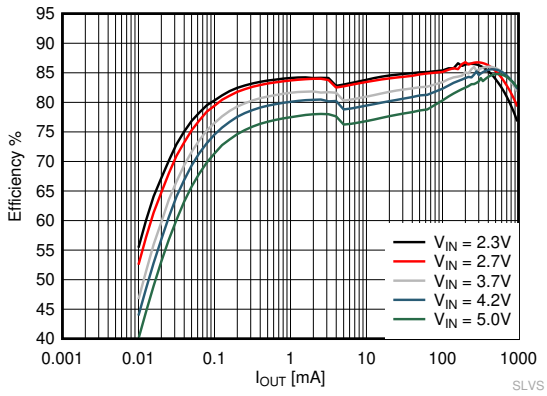

TPS62800 VSEL/MODE = GND

**Figure 9-3. Efficiency Power Save Mode $V_{OUT}$ = 0.7 V**



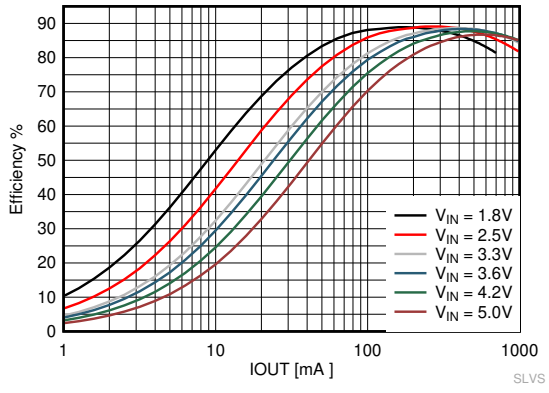

TPS62801 $R_{VSEL}$ = 10 kΩ to GND

**Figure 9-4. Efficiency Power Save Mode $V_{OUT}$ = 0.8 V**



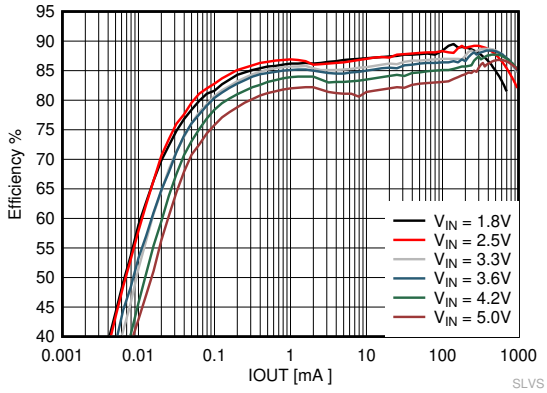

TPS62801 $R_{VSEL}$ = 15.4 kΩ to GND

**Figure 9-5. Efficiency Power Save Mode $V_{OUT}$ = 0.9 V**



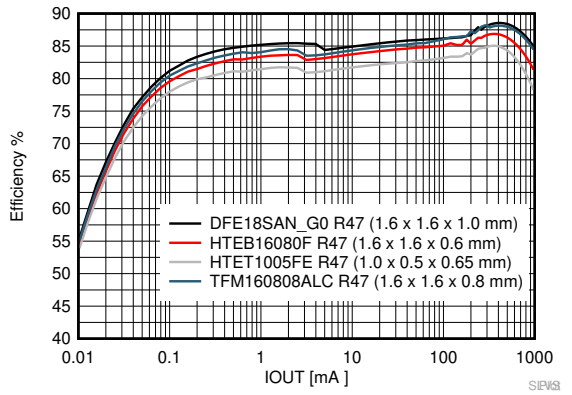

TPS62801 $R_{VSEL}$ = 56.2 kΩ
VSEL/MODE pin = high after start-up

**Figure 9-6. Efficiency Forced PWM Mode $V_{OUT}$ = 1.2 V**



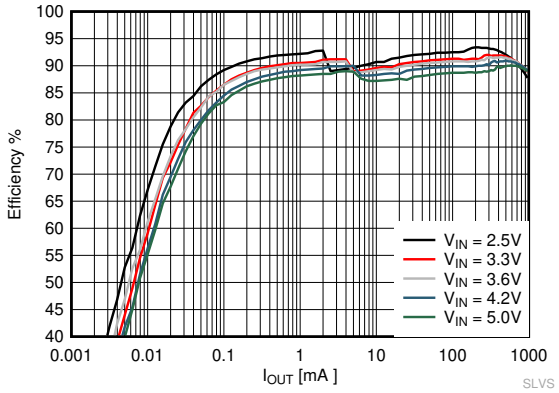

TPS62801 VSEL/MODE = GND

**Figure 9-7. Efficiency Power Save Mode $V_{OUT}$ = 1.2 V**



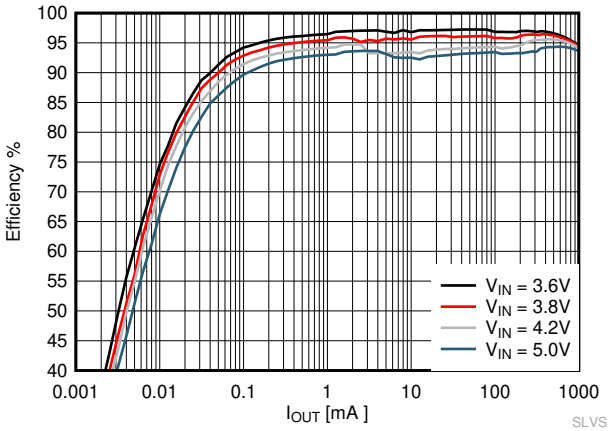

TPS62801 VSEL/MODE = GND, $V_{OUT}$ = 1.2 V

**Figure 9-8. Inductor Comparison**



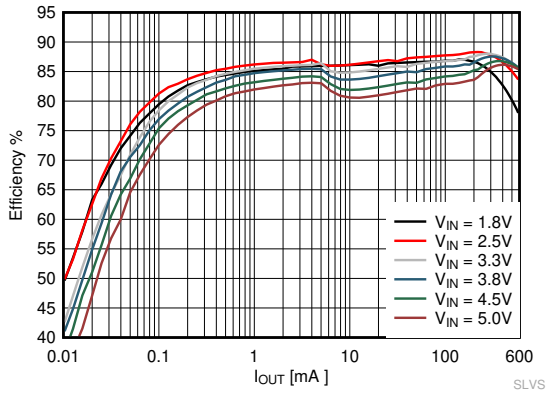

TPS62802 VSEL/MODE = GND

**Figure 9-9. Efficiency Power Save Mode $V_{OUT}$ = 1.8 V**



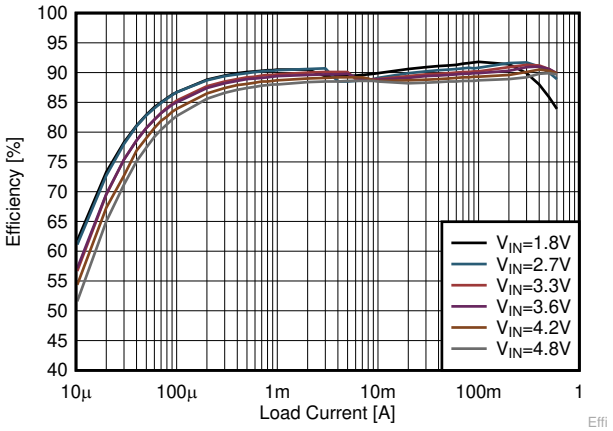

TPS62802 3.3 V $V_{OUT}$, VSEL/MODE = 249 k

**Figure 9-10. Efficiency Power Save Mode $V_{OUT}$ = 3.3 V**



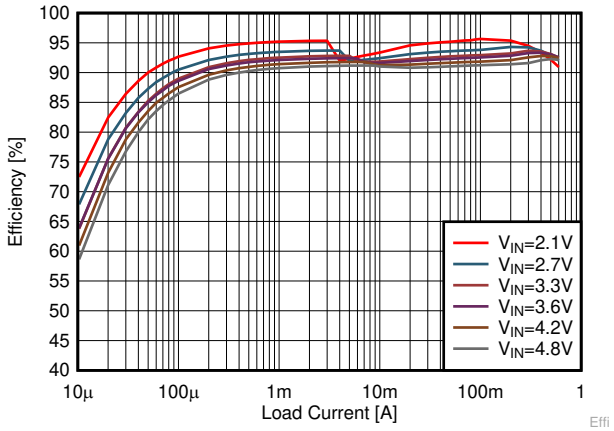

TPS62806 $V_{OUT}$ = 0.7 V, VSEL/MODE = GND
L = 1-µH DFE201610E

**Figure 9-11. Efficiency Power Save Mode $V_{OUT}$ = 0.7 V**



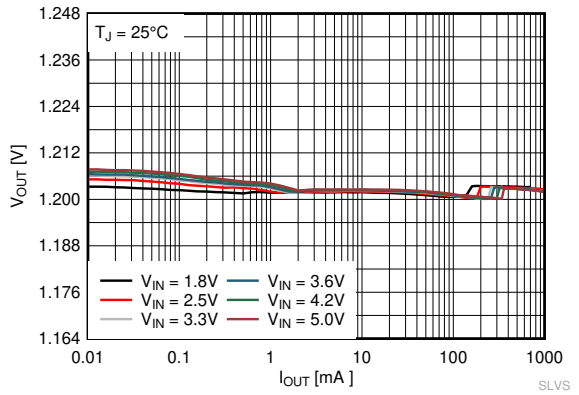

TPS62807 $V_{OUT}$ = 1.2 V, VSEL/MODE = GND
L = 1-µH DFE201610E

**Figure 9-12. Efficiency Power Save Mode $V_{OUT}$ = 1.2 V**



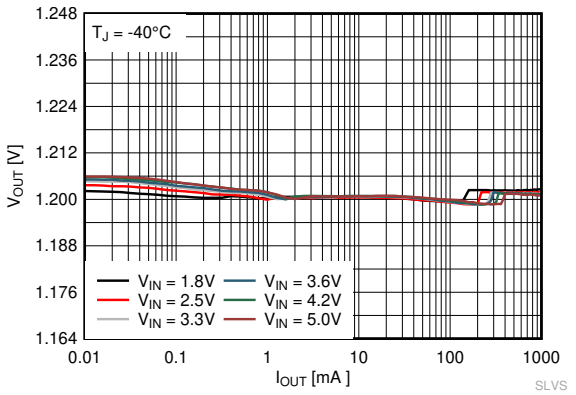

TPS62808 $V_{OUT}$ = 1.8 V, VSEL/MODE = GND
L = 1-µH DFE201610E

**Figure 9-13. Efficiency Power Save Mode $V_{OUT}$ = 1.8 V**



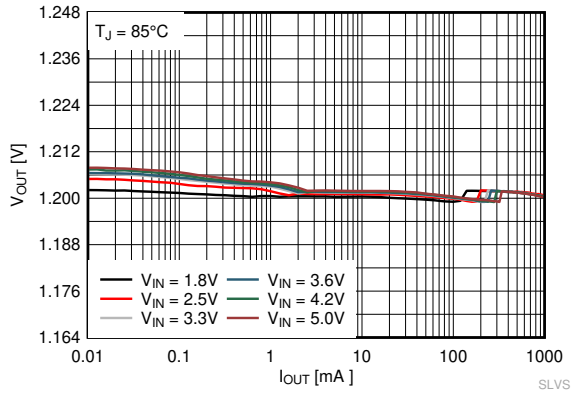

TPS62801 VSEL/MODE = GND
$V_{OUT}$ = 1.2 V PFM/PWM mode $T_J$ = 25°C

**Figure 9-14. Output Voltage vs Output Current**



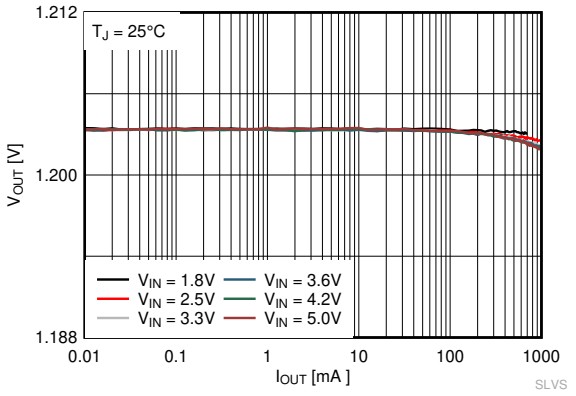

TPS62801 VSEL/MODE = GND
$V_{OUT}$ = 1.2 V PFM/PWM mode $T_J$ = –40°C

**Figure 9-15. Output Voltage vs Output Current**



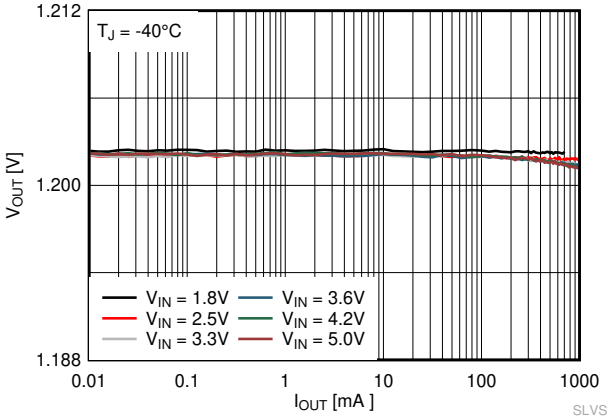

TPS62801 VSEL/MODE = GND
$V_{OUT}$ = 1.2 V PFM/PWM mode $T_J$ = 85°C

**Figure 9-16. Output Voltage vs Output Current**



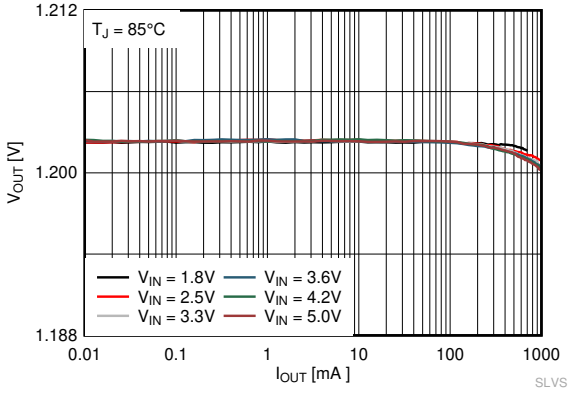

TPS62801 VSEL/MODE = high after start-up
$V_{OUT}$ = 1.2 V Forced PWM mode $T_J$ = 25°C

**Figure 9-17. Output Voltage vs Output Current**



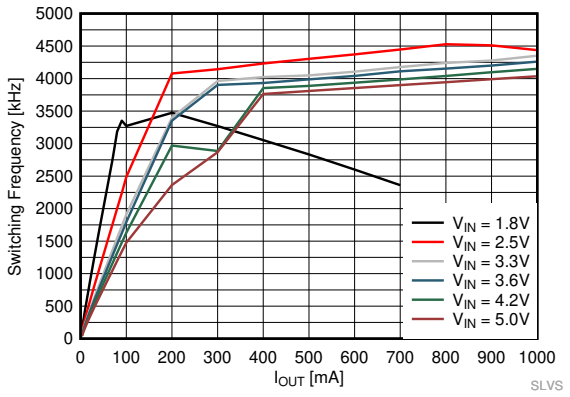

TPS62801 VSEL/MODE = high after start-up
$V_{OUT}$ = 1.2 V Forced PWM mode $T_J$ = –40°C

**Figure 9-18. Output Voltage vs Output Current**



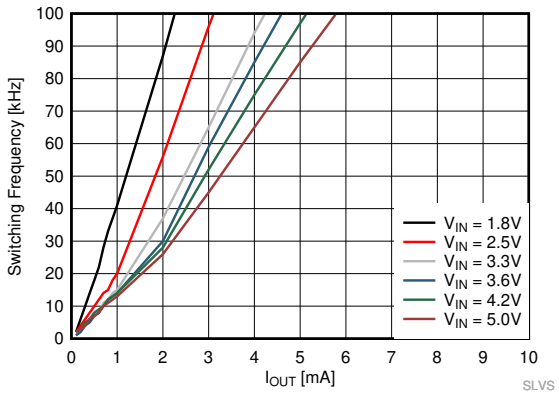

TPS62801 VSEL/MODE = high after start-up
$V_{OUT}$ = 1.2 V Forced PWM mode $T_J$ = 85°C

**Figure 9-19. Output Voltage vs Output Current**



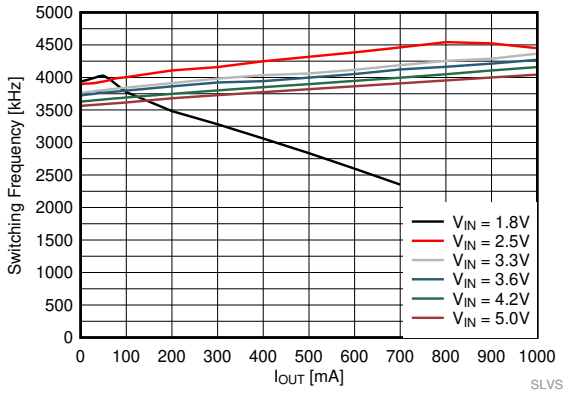

TPS62801 VSEL/MODE = GND
$V_{OUT}$ = 1.2 V PFM/PWM mode $T_J$ = 25°C

**Figure 9-20. Switching Frequency vs Output Current**



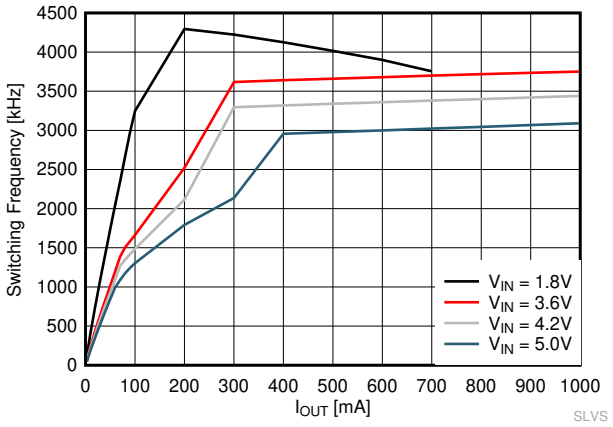

TPS62801 VSEL/MODE = GND
$V_{OUT}$ = 1.2 V PFM/PWM mode $T_J$ = 25°C

**Figure 9-21. Switching Frequency (Zoom In)**



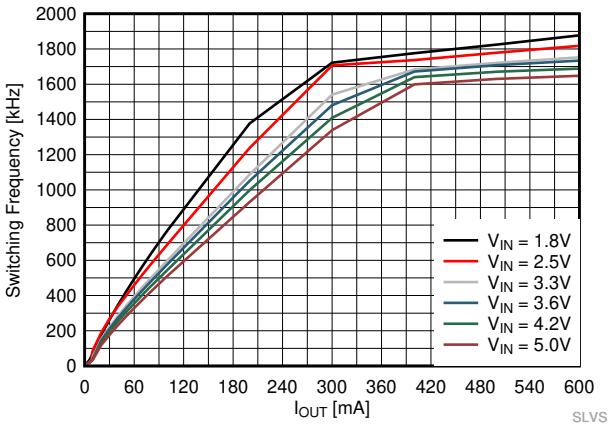

TPS62801 VSEL/MODE = high after start-up
$V_{OUT}$ = 1.2 V Forced PWM Mode $T_J$ = 25°C

**Figure 9-22. Switching Frequency vs Output Current**



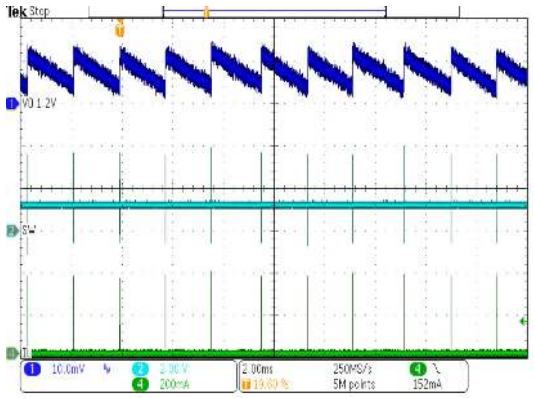

TPS62801 VSEL/MODE = 10 kΩ to GND
$V_{OUT}$ = 0.8 V PFM/PWM mode $T_J$ = 25°C

**Figure 9-23. Switching Frequency vs Output Current**



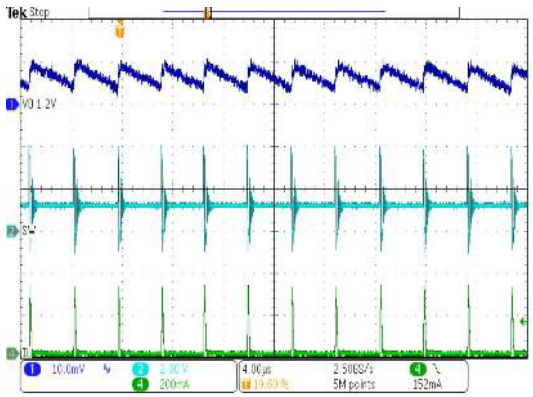

TPS62806 VSEL/MODE = GND L = 1 µH
$V_{OUT}$ = 0.7 V PFM/PWM mode $T_J$ = 25°C

**Figure 9-24. Switching Frequency vs Output Current**



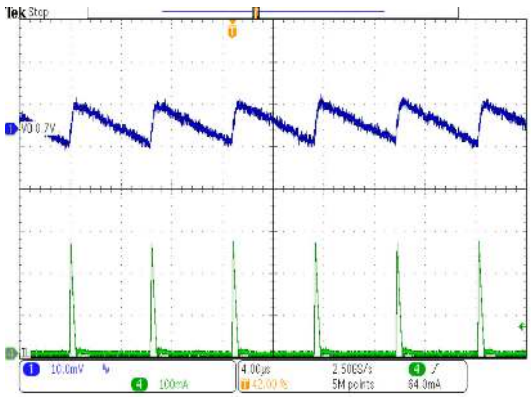

TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$I_{OUT}$ = 25 µA PFM mode

**Figure 9-25. Typical Operation Power Save Mode**



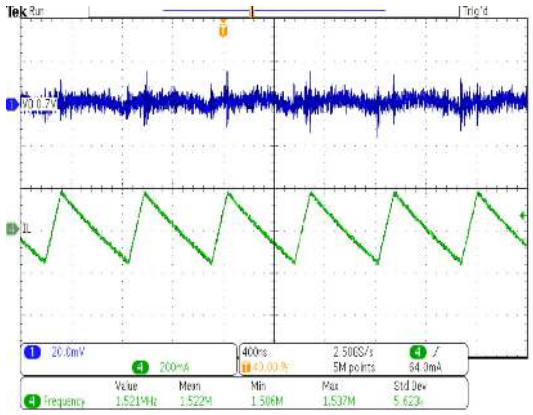
TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$I_{OUT}$ = 10 mA PFM mode

**Figure 9-26. Typical Operation Power Save Mode**



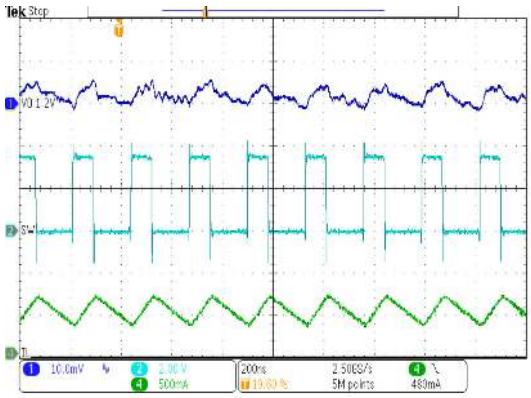
$V_{OUT}$ = 0.7 V $I_{OUT}$ = 10 mA VSEL/MODE = GND
$V_{IN}$ = 3.8 V PFM Mode, L = 1-µH DFE201610E

**Figure 9-27. TPS62806 Typical Operation Power Save Mode**



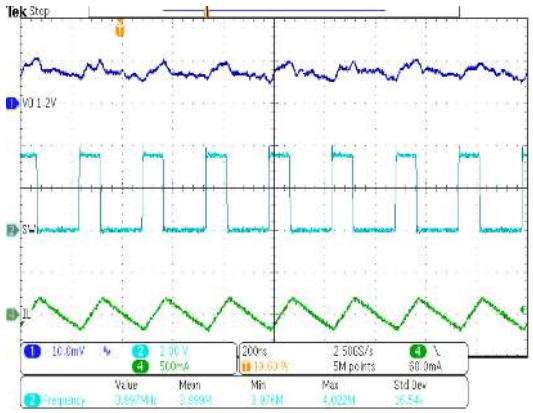
$V_{OUT}$ = 0.7 V $I_{OUT}$ = 0 mA VSEL/MODE = VIN (after start-up)
$V_{IN}$ = 3.8 V PFM Mode, L = 1-µH DFE201610E

**Figure 9-28. TPS62806 Typical Forced PWM Mode Operation (1.5 MHz)**



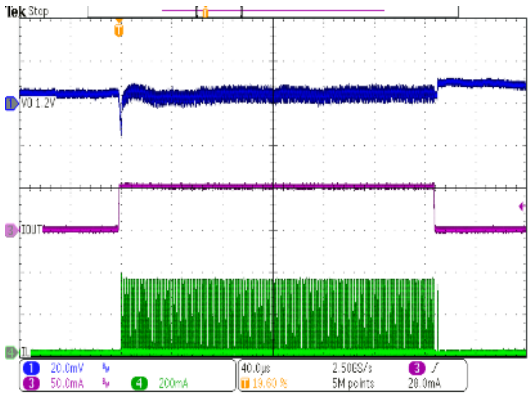
PWM mode $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$I_{OUT}$ = 500 mA

**Figure 9-29. TPS62801 Typical Operation PWM Mode**



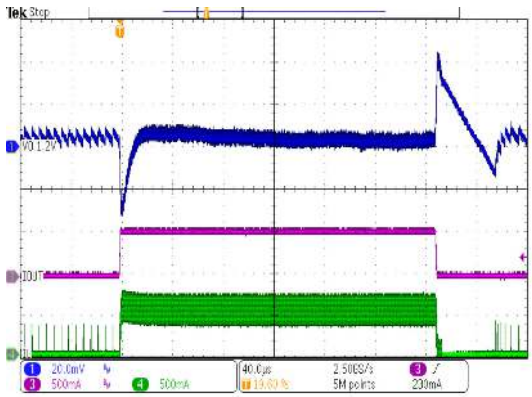
Forced PWM mode $V_{OUT}$ = 1.2 V $I_{OUT}$ = 0 mA
VSEL/MODE = VIN (after start-up)

**Figure 9-30. TPS62801 Typical Operation Forced PWM Mode**



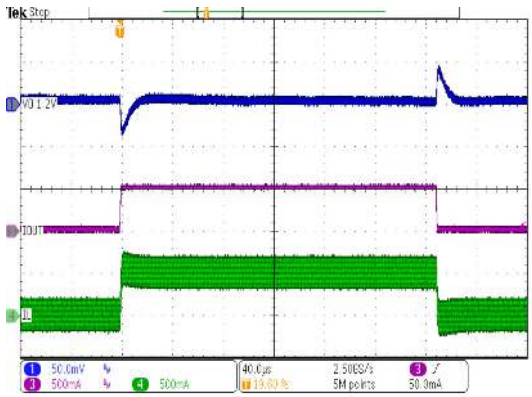
TPS62801 rise / fall time < 1 µs $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$I_{OUT}$ = 0 mA to 50 mA, PFM Mode

**Figure 9-31. Load Transient Power Save Mode**



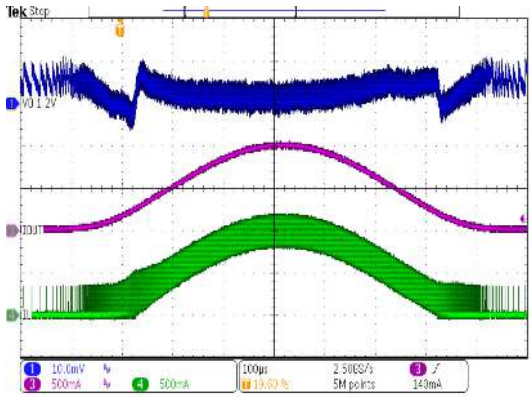
TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = GND
rise / fall time < 1 µs PFM / PWM mode
$I_{OUT}$ = 5 mA to 500 mA

**Figure 9-32. Load Transient Power Save Mode**



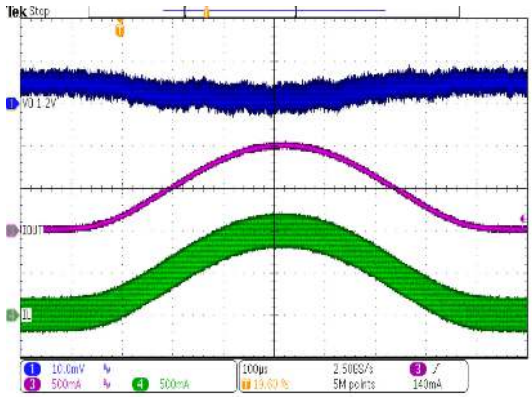
Forced $V_{OUT}$ = 1.2 V VSEL/MODE = VIN
PWM mode (after start-up)
rise / fall time < 1 µs $I_{OUT}$ = 5 mA to 500 mA

**Figure 9-33. TPS62801 Load Transient Forced PWM Mode**



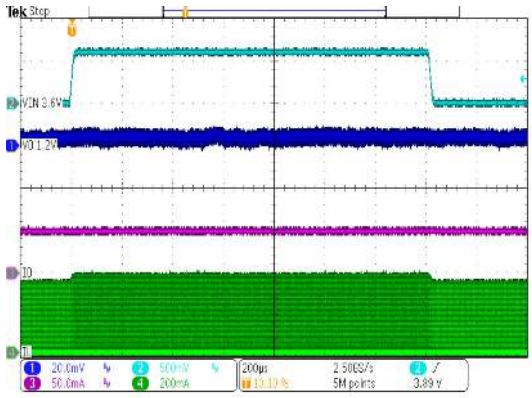
TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$I_{OUT}$ = 1 mA to 1 A 1 kHz PFM/PWM mode

**Figure 9-34. AC Load Sweep Power Save Mode**



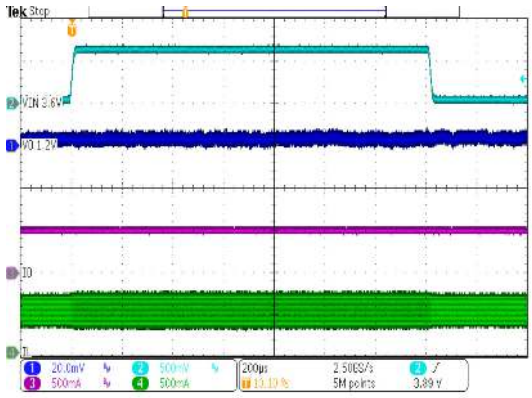
TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = VIN
$I_{OUT}$ = 1 mA to 1 A, 1 kHz (after start-up)
Forced PWM mode

**Figure 9-35. AC Load Sweep Forced PWM Mode**



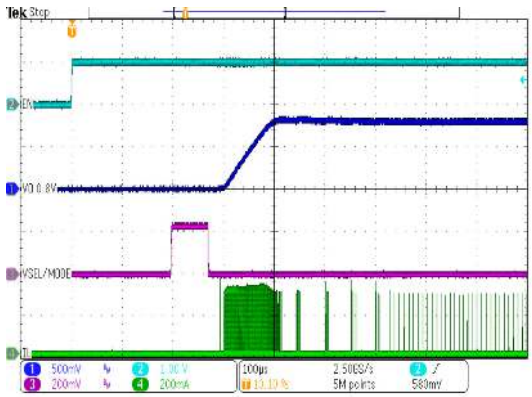
TPS62801 $V_{OUT}$ = 1.2 V $V_{IN}$ = 3.6 V to 4.2 V
rise / fall time = 10 µs $I_{OUT}$ = 50 mA

**Figure 9-36. Line Transient PFM Mode**



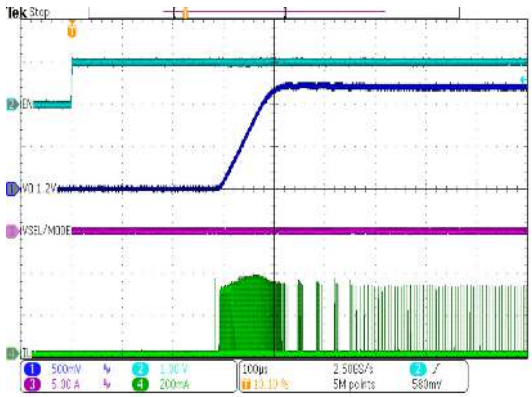
TPS62801 $V_{OUT}$ = 1.2 V $V_{IN}$ = 3.6 V to 4.2 V
rise / fall time = 10 µs $I_{OUT}$ = 500 mA

**Figure 9-37. Line Transient PWM Mode**



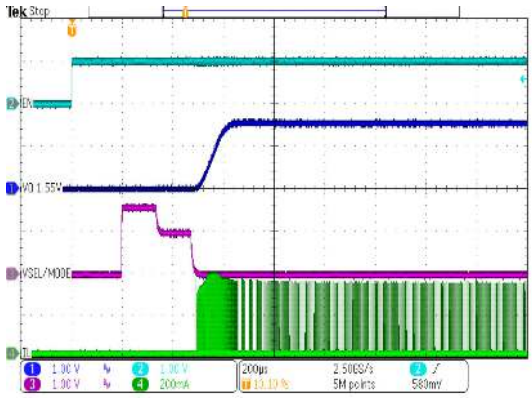

$V_{OUT}$ = 0.8 V VSEL/MODE = Low (through $R_{VSEL}$)
$R_{VSEL}$ = 10 kΩ $R_{Load}$ = 220 Ω

**Figure 9-38. TPS62801 Start-Up, $V_{OUT}$ = 0.8 V**



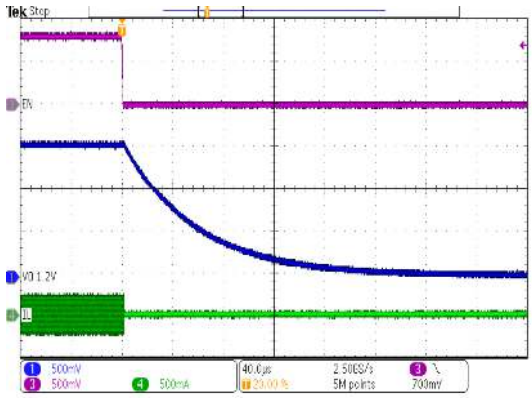

TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = GND
$R_{Load}$ = 220 Ω

**Figure 9-39. Start-Up, $V_{OUT}$ = 1.2 V**



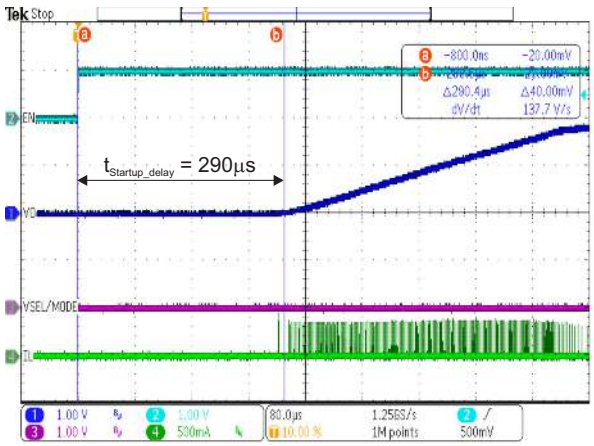

$V_{OUT}$ = 1.55 V VSEL/MODE = Low (through $R_{VSEL}$)
$R_{Load}$ = 220 Ω $R_{VSEL}$ = 249 kΩ

**Figure 9-40. TPS62801 Start-Up, $V_{OUT}$ = 1.55 V**



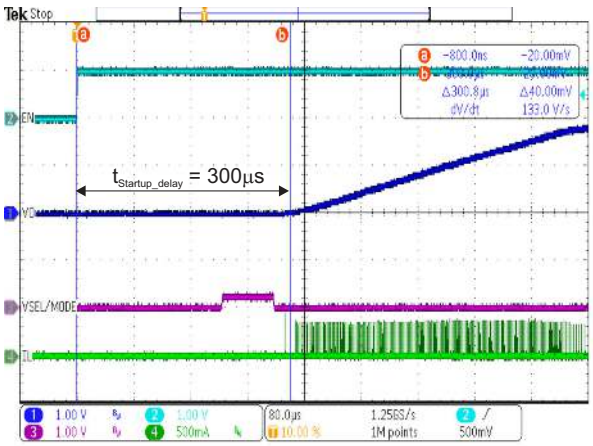

TPS62801 $V_{OUT}$ = 1.2 V VSEL/MODE = $V_{IN}$
EN = high to low No load

**Figure 9-41. Output Discharge**



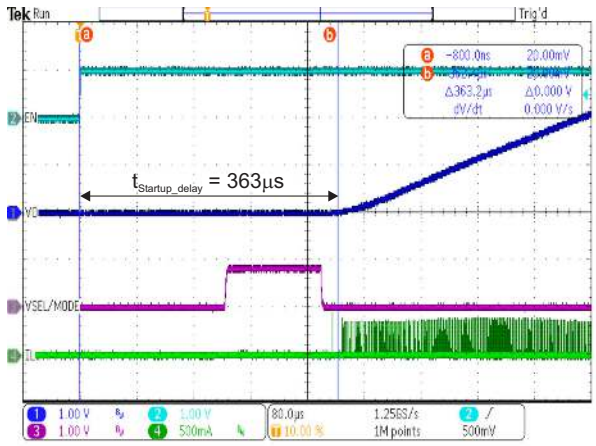

VSEL/MODE = GND

**Figure 9-42. Start-Up Delay Time, VSEL = 0**



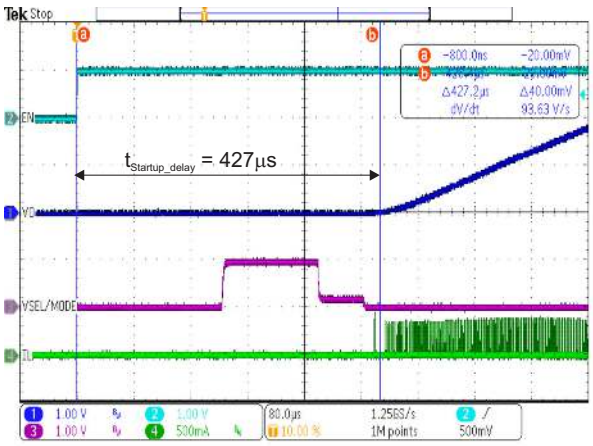

$R_{VSEL}$ = 10 kΩ

**Figure 9-43. Start-Up Delay Time, VSEL = 1**



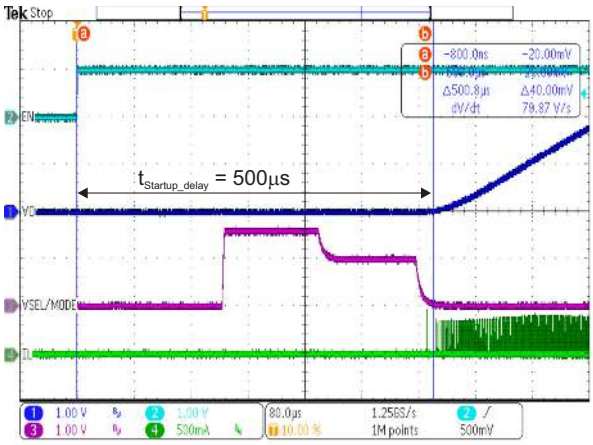

$R_{VSEL}$ = 36.5 kΩ

**Figure 9-44. Start-Up Delay Time, VSEL = 7**




$R_{VSEL}$ = 44.2 kΩ

**Figure 9-45. Start-Up Delay Time, VSEL = 8**




$R_{VSEL}$ = 249 kΩ

**Figure 9-46. Start-Up Delay Time, VSEL = 16**

## 9.3 System Examples

This section shows additional circuits for various output voltages.

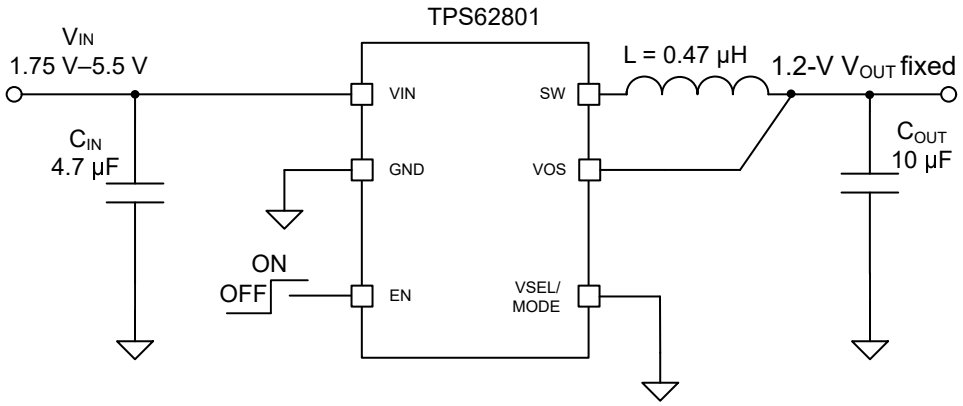



**Figure 9-47. TPS62801 VSEL Connected to GND for 1.2-V Fixed $V_{OUT}$**

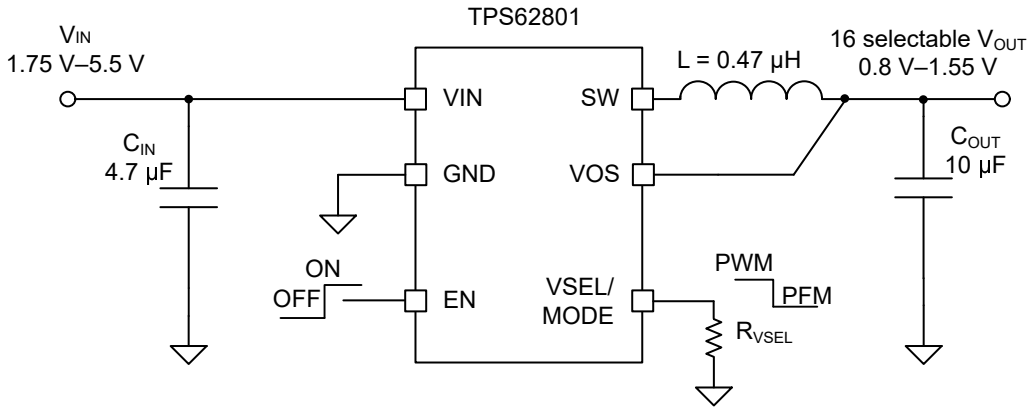



**Figure 9-48. TPS62801 Adjustable $V_{OUT}$ Application Circuit**

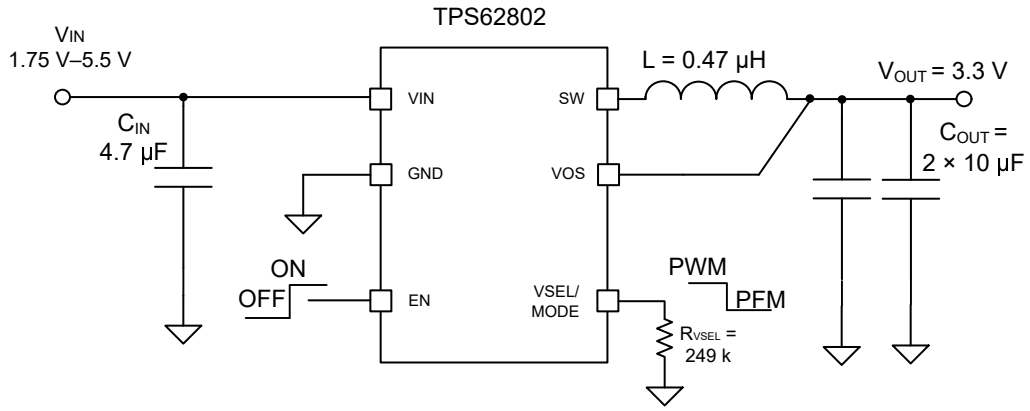



**Figure 9-49. TPS62802 Adjustable 3.3-V $V_{OUT}$ Application Circuit**

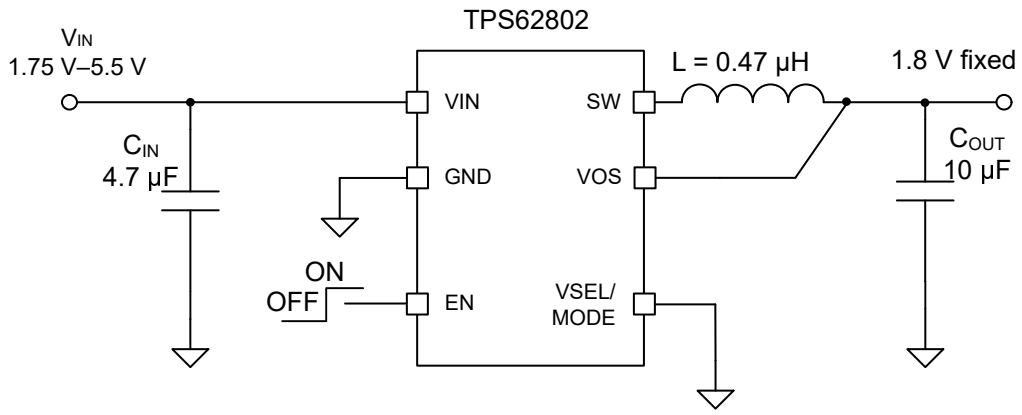



**Figure 9-50. TPS62802 VSEL Connected to GND for 1.8-V Fixed $V_{OUT}$**

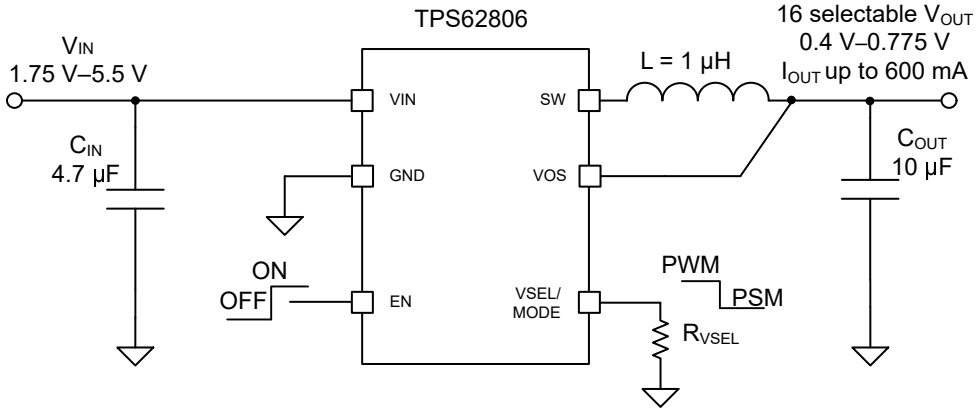



**Figure 9-51. TPS62806 Adjustable $V_{OUT}$ Application Circuit**

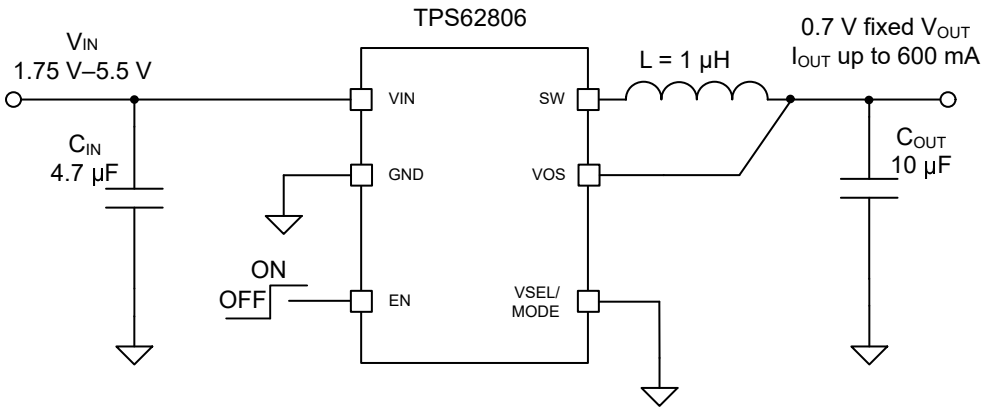



**Figure 9-52. TPS62806 VSEL Connected to GND for 0.7-V Fixed $V_{OUT}$**

# 10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS6280x.

# 11 Layout

## 11.1 Layout Guidelines

The pinout of TPS6280x has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as $C_{IN}$, $C_{OUT}$, and L. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603) size capacitors and a 0402 (1005) size inductor. A solution size smaller than 5 $mm^2$ can be achieved with a fixed output voltage.

- As for all switching power supplies, the layout is an important step in the design. Take care in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the VIN and GND pins of the IC. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (for example, SW line) or other noise sources.

## 11.2 Layout Example

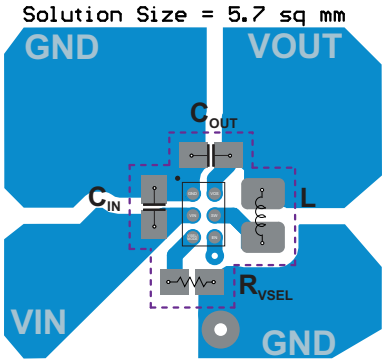



**Figure 11-1. PCB Layout Example**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.1.2 Development Support

#### *12.1.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPS62800 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62801 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62802 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62806 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62807 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62808 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62800YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | - | Samples |
| TPS62801YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | + | Samples |
| TPS62801YKAT | ACTIVE | DSBGA | YKA | 6 | 250 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | + | Samples |
| TPS62802YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | X | Samples |
| TPS62802YKAT | ACTIVE | DSBGA | YKA | 6 | 250 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | X | Samples |
| TPS62806YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | J | Samples |
| TPS62806YKAT | ACTIVE | DSBGA | YKA | 6 | 250 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | J | Samples |
| TPS62807YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | L | Samples |
| TPS62807YKAT | ACTIVE | DSBGA | YKA | 6 | 250 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | L | Samples |
| TPS62808YKAR | ACTIVE | DSBGA | YKA | 6 | 3000 | RoHS & Green | SAC396 \| SNAGCU | Level-1-260C-UNLIM | -40 to 125 | V | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

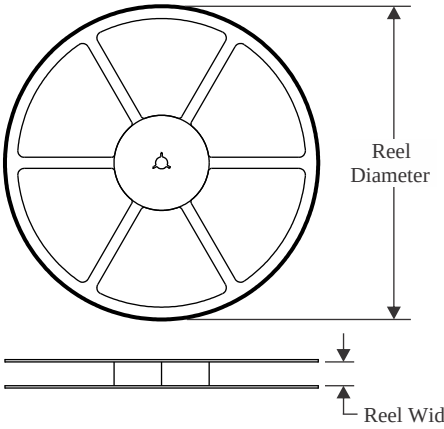
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

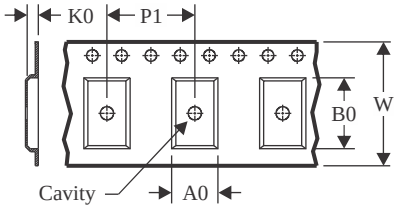
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

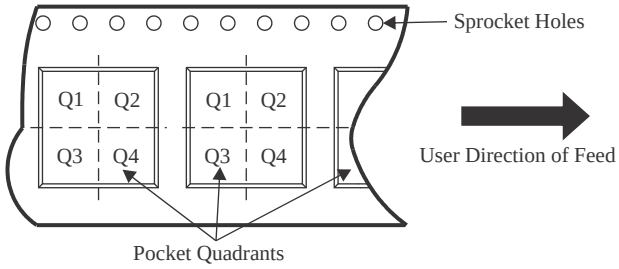



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

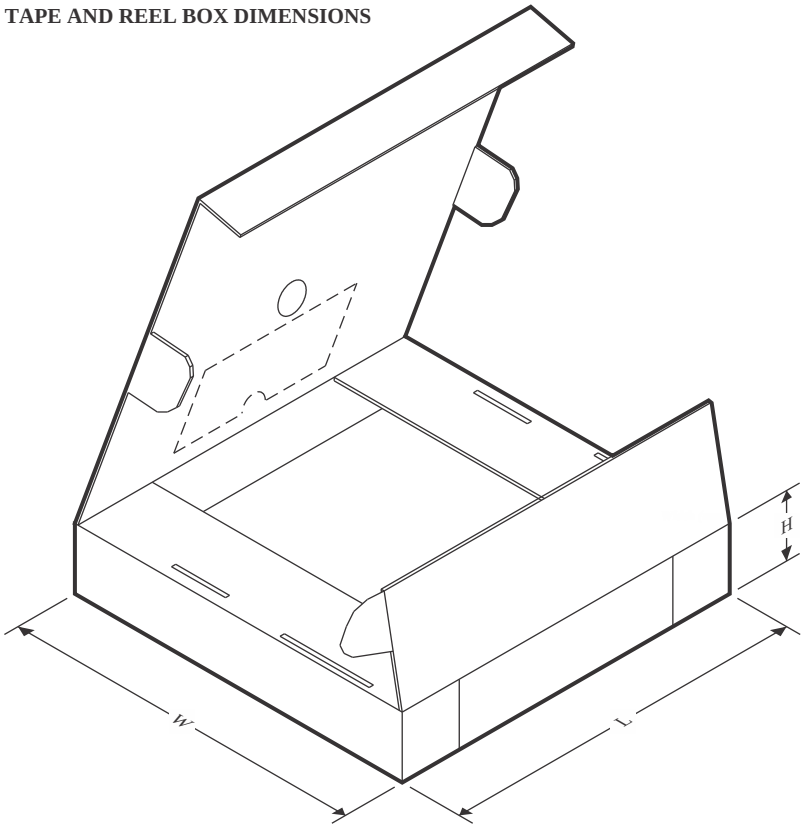
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62800YKAR | DSBGA | YKA | 6 | 3000 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62801YKAR | DSBGA | YKA | 6 | 3000 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62801YKAR | DSBGA | YKA | 6 | 3000 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62801YKAT | DSBGA | YKA | 6 | 250 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62801YKAT | DSBGA | YKA | 6 | 250 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62802YKAR | DSBGA | YKA | 6 | 3000 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62802YKAR | DSBGA | YKA | 6 | 3000 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62802YKAT | DSBGA | YKA | 6 | 250 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62806YKAR | DSBGA | YKA | 6 | 3000 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62806YKAT | DSBGA | YKA | 6 | 250 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62806YKAT | DSBGA | YKA | 6 | 250 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62807YKAR | DSBGA | YKA | 6 | 3000 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62807YKAT | DSBGA | YKA | 6 | 250 | 178.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62807YKAT | DSBGA | YKA | 6 | 250 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |
| TPS62808YKAR | DSBGA | YKA | 6 | 3000 | 180.0 | 8.4 | 0.81 | 1.16 | 0.46 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

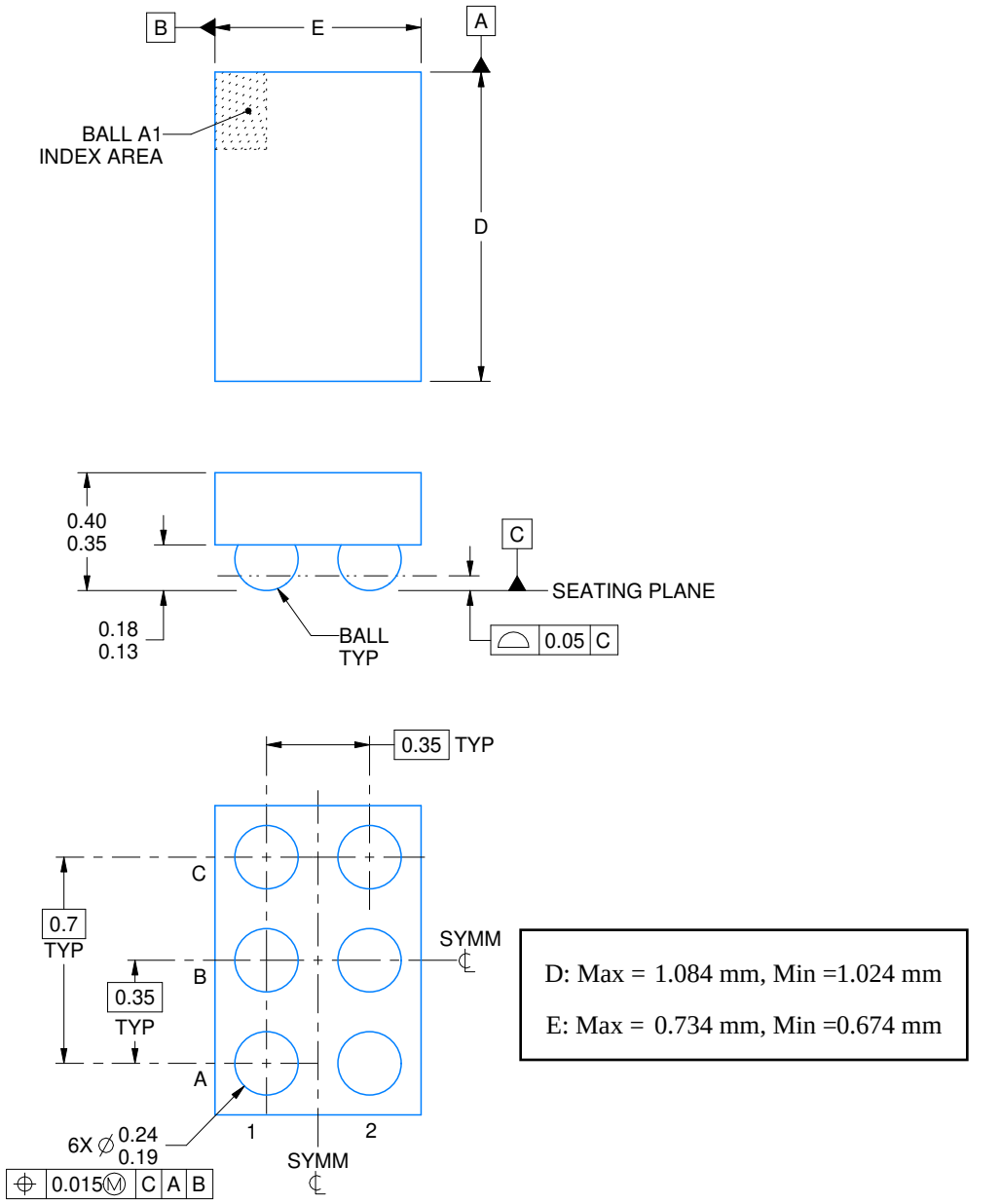
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62800YKAR | DSBGA | YKA | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62801YKAR | DSBGA | YKA | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62801YKAR | DSBGA | YKA | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| TPS62801YKAT | DSBGA | YKA | 6 | 250 | 220.0 | 220.0 | 35.0 |
| TPS62801YKAT | DSBGA | YKA | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62802YKAR | DSBGA | YKA | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62802YKAR | DSBGA | YKA | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| TPS62802YKAT | DSBGA | YKA | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62806YKAR | DSBGA | YKA | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62806YKAT | DSBGA | YKA | 6 | 250 | 220.0 | 220.0 | 35.0 |
| TPS62806YKAT | DSBGA | YKA | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62807YKAR | DSBGA | YKA | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| TPS62807YKAT | DSBGA | YKA | 6 | 250 | 220.0 | 220.0 | 35.0 |
| TPS62807YKAT | DSBGA | YKA | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62808YKAR | DSBGA | YKA | 6 | 3000 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## YKA0006

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

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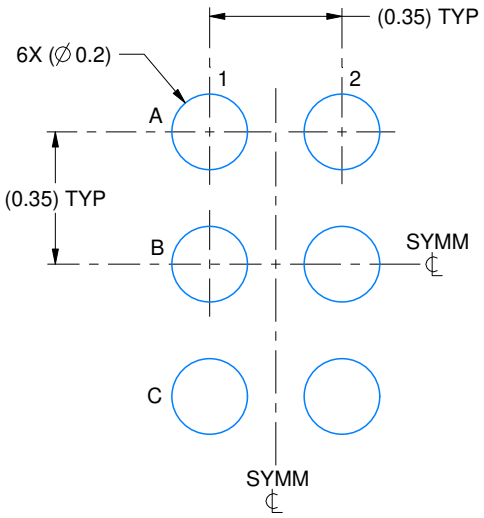
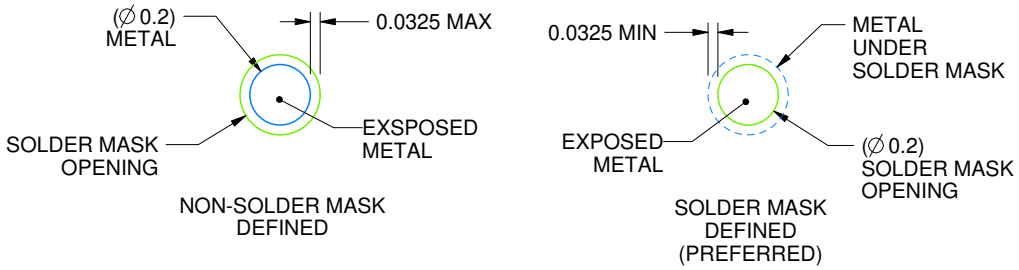
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X




SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

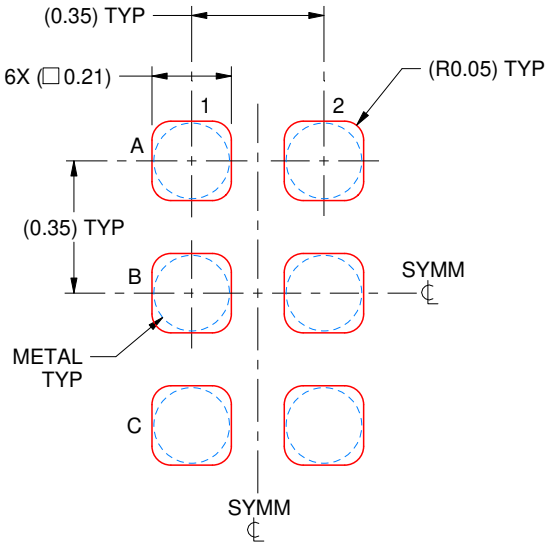
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YKA0006

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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