Preliminary Data Sheet No. PD60130-K

International
IOR Rectifier

IR2122(S)

CURRENT SENSING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- $\overline{\text{FAULT}}$ lead indicates shutdown has occured
- Output out of phase with input

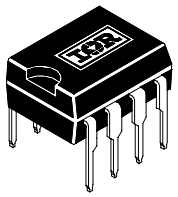
Description

The IR2122(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

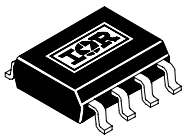
Product Summary

V_{OFFSET}	600V max.
I_O+/-	110 mA / 110 mA
V_{OUT}	10 - 20V
V_{CSth}	500 mV
$t_{on/off}$ (typ.)	250 & 200 ns

Packages

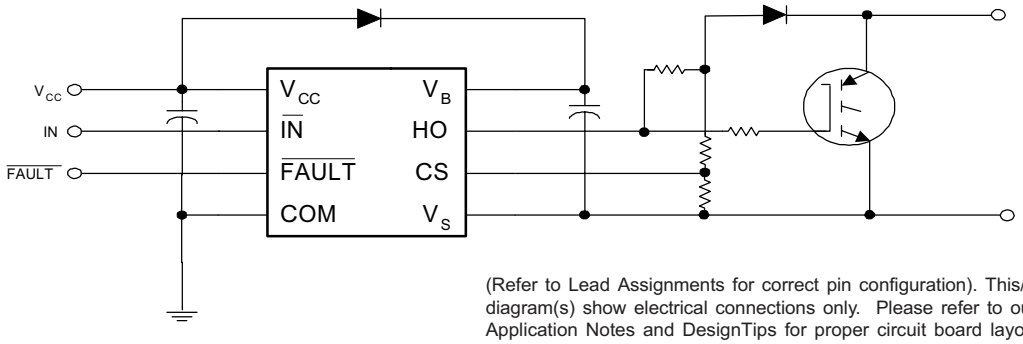


8-Lead PDIP



8-Lead SOIC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic Supply Voltage	-0.3	25	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_B + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R_{THJA}	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	V_S + 13	V_S + 20	V
V_S	High Side Floating Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Logic Supply Voltage	13	20	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{FLT}	$\overline{\text{FAULT}}$ Output Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_S + 5	
T_A	Ambient Temperature	-40	150	℃

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

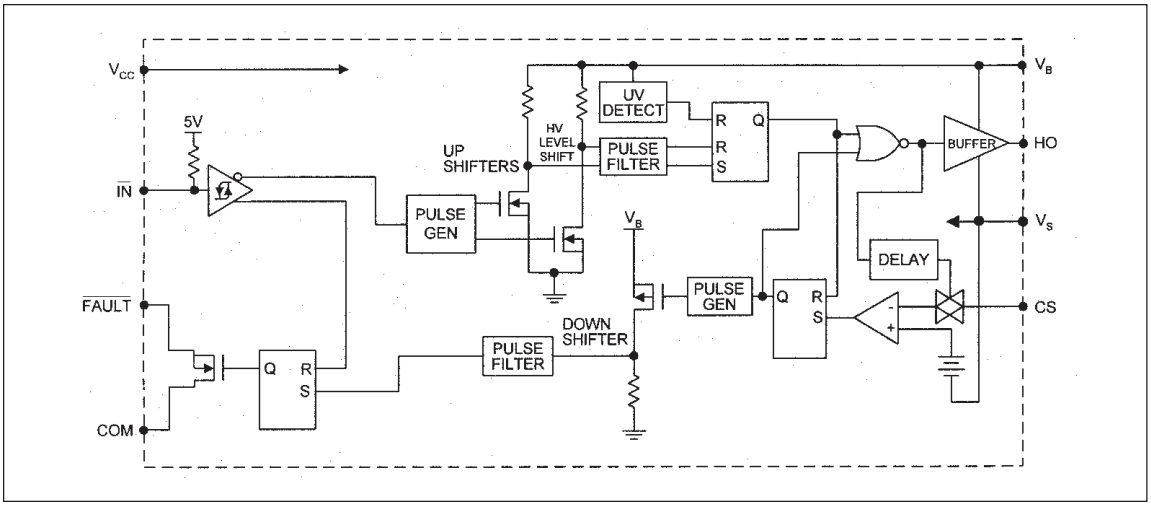
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	250	—	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	200	—		V_S = 600V
t_r	Turn-On Rise Time	—	250	—		C_L = 1000 pF
t_f	Turn-Off Fall Time	—	250	—		C_L = 1000 pF
t_{bl}	Start-Up Blanking Time	500	900	—		
t_{cs}	CS Shutdown Propagation Delay	—	350	—		
t_{flt}	CS to $\overline{\text{FAULT}}$ Pull-Up Propagation Delay	—	450	—		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” Input Voltage (OUT = LO)	3.0	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “1” Input Voltage (OUT = HI)	—	—	0.8		V_{CC} = 10V to 20V
V_{CSTH+}	CS Input Positive Going Threshold	350	500	650	mV	V_{CC} = 10V to 20V
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50		V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	150	350	µA	V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	60	120		V_{IN} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current	—	7.0	15		V_{IN} = 0V
I_{IN-}	Logic “0” Input Bias Current	—	—	1.0		V_{IN} = 5V
I_{CS+}	“High” CS Bias Current	—	—	1.0		V_{CS} = 3V
I_{CS-}	“High” CS Bias Current	—	—	1.0		V_{CS} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	10.0	11.4	13.0	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	9.5	10.4	12.5		
I_{O+}	Output High Short Circuit Pulsed Current	110	130	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	110	130	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

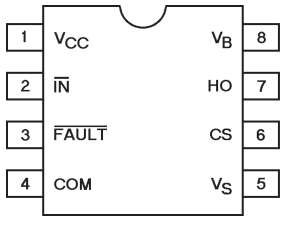
Functional Block Diagram



Lead Definitions

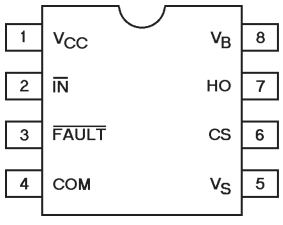
Lead Symbol	Description
V_{CC}	Logic and gate drive supply
$\overline{IN}$	Logic input for gate driver output (HO), out of phase with HO
$\overline{FAULT}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Lead Assignments



8 Lead PDIP

IR2122



8 Lead SOIC

IR2122S

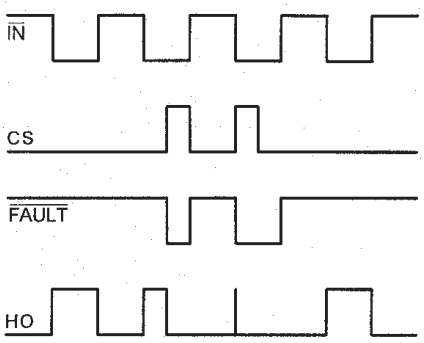


Figure 1. Input/Output Timing Diagram

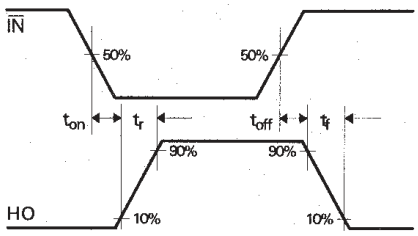


Figure 2. Switching Time Waveform Definition

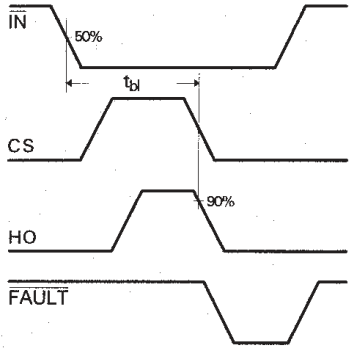


Figure3. Start-up Blanking Time Waveform Definitions

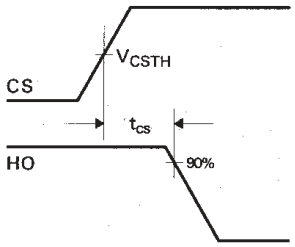


Figure 4. CS Shutdown Waveform Definitions

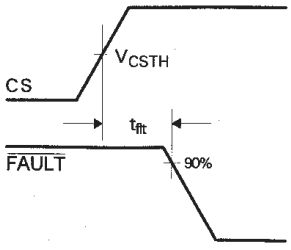
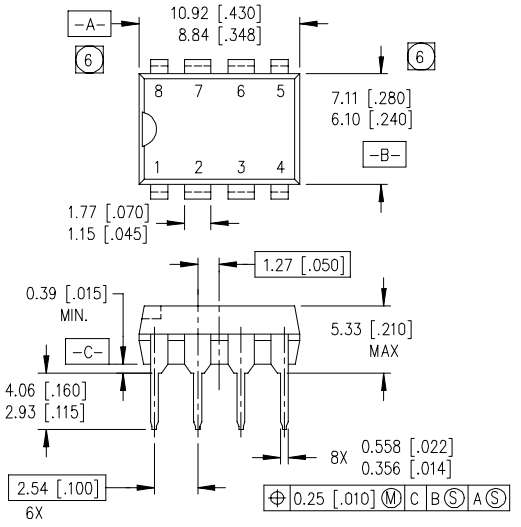
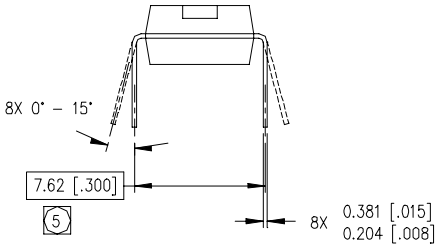


Figure 5. CS to FAULT Waveform Definitions

Case outlines

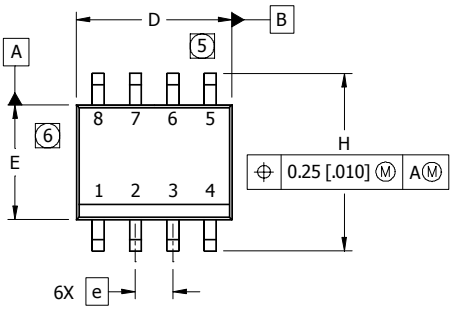


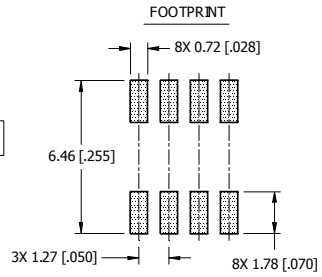
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



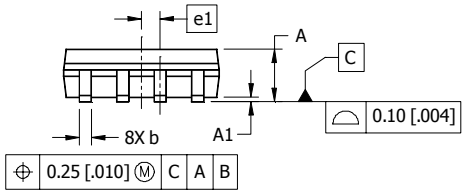
8-Lead PDIP

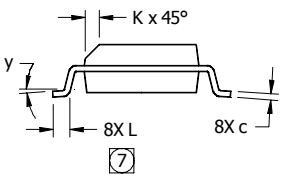
01-6014
01-3003 01 (MS-001AB)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°





NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)