TLC2274-HT Advanced LinCMOS™ Rail-to-Rail Operational Amplifier

1 Features

- Qualified for Automotive Applications
- Qualified in Accordance With AEC-Q100
- Output Swing Includes Both Supply Rails
- Low Noise: 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current: 1 pA Typical
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth: 2.2 MHz Typical
- High Slew Rate: 3.6 V/µs Typical
- Low Input Offset Voltage 2500-µV Max at T_A = 25°C
- Macromodel Included

2 Applications

- Supports Extreme Temperature Applications:
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Extreme (–40°C to 150°C) Temperature Range [(1)]
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability
  - Texas Instruments' high temperature products use highly-optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures. All devices are characterized and qualified for 1000 hours continuous operating life at maximum rated temperature.

(1) Custom temperature ranges available

3 Description

The TLC2274 is a quadruple operational amplifier from Texas Instruments. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC2274 offers 2 MHz of bandwidth and 3 V/µs of slew rate for higher speed applications. These device offers comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC2274 has a noise voltage of 9nV/√Hz, two times lower than competitive solutions.

The TLC2274, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, this device works well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this device a great choice when interfacing with analog-to-digital converters (ADCs). This family is fully characterized at 5 V and ±5 V.

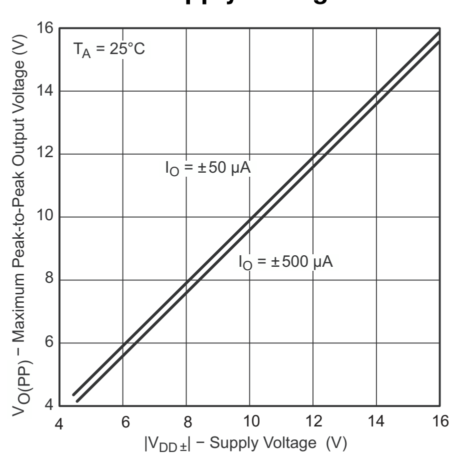
It offers increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the device to be used in a wider range of applications.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC2274-HT	TSSOP (14)	6.60 mm × 5.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Maximum Peak-to-Peak Output Voltage vs Supply Voltage



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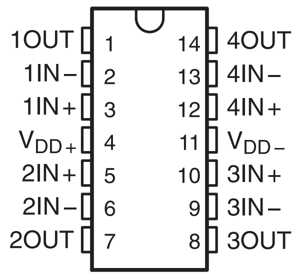
4 Revision History

DATE	REVISION	NOTES
January 2015	*	Initial release.

5 Pin Configuration and Functions

PW PACKAGE
(TOP VIEW)



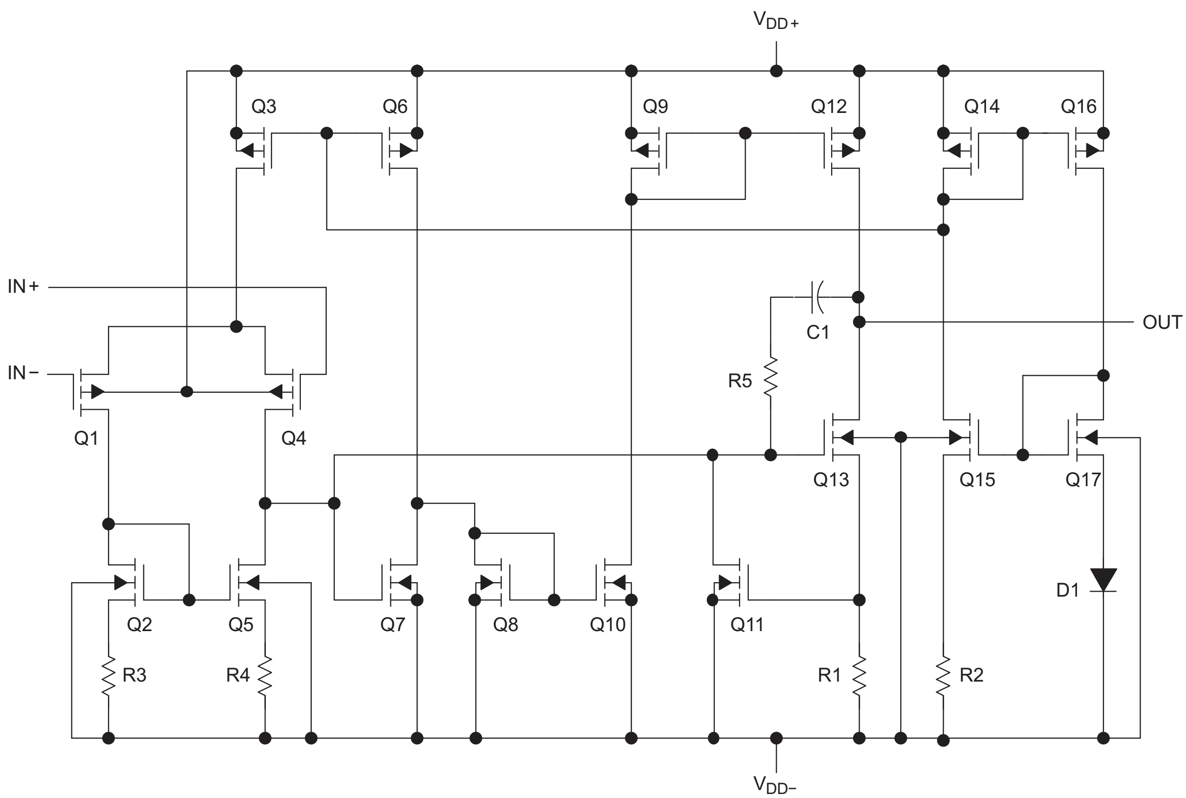


Figure 1. Equivalent Schematic (Each Amplifier)

Table 1. Actual Device Component Count[(1)]

COMPONENT	TLC2274
Transistors	76
Resistors	52
Diodes	18
Capacitors	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD+}	Supply voltage[2]			8	V
V_{DD-}	Supply voltage[2]			–8	V
V_{ID}	Differential input voltage[3]		–16	16	V
V_I	Input voltage[2]	Any input	V_{DD-} – 0.3	V_{DD+}	V
I_I	Input current	Any input	–5	5	mA
I_O	Output current		–50	50	mA
	Total current into V_{DD+}		–50	50	mA
	Total current out of V_{DD-}		–50	50	mA
	Duration of short-circuit current at (or below) 25°C[4]		Unlimited		
T_A	Operating free-air temperature		–40	150	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 s			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
(3) Differential voltages are at I_{N+} with respect to I_{N-}. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2500	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage	±2.2	±8	V
V_I	Input voltage	V_{DD-}	V_{DD+} −1.5	V
V_{IC}	Common-mode input voltage	V_{DD-}	V_{DD+} −1.5	V
T_A	Operating free-air temperature	−40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC2274 PW 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.6	
ψ_{JT}	Junction-to-top characterization parameter	2.4	
ψ_{JB}	Junction-to-board characterization parameter	47.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500	μV
				Full range			3000	
αV_{IO}	Temperature coefficient of input offset voltage			25°C to 125°C		2		μV/°C
	Input offset voltage long-term drift (2)			25°C		0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			7000	
I_{IB}	Input bias current			25°C		1		pA
				Full range				
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	$\|V_{IO}\|$ ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		
				Full range	4.84			
		I_{OH} = −1 mA		25°C	4.25	4.65		
				Full range	4.20			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15	
				Full range			0.16	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5	
				Full range			1.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V,	R_L = 10 kΩ (3)	25°C	10	35		V/mV
				Full range	8			
			R_L = 1 MΩ (3)	25°C		175		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		dB
				Full range	69			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		4.4	6	mA
				Full range			6	

(1) Full range is −40°C to 150°C for thisl part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V

6.6 Operating Characteristics, V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF (2)	R_L = 10 kΩ (2)	25°C	2.3	3.6		V/μs
				Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50		nV/√Hz
		f = 1 kHz		25°C		9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		μV
		f = 0.1 to 10 Hz		25°C		1.4		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5V to 2.5V, R_L = 10 kΩ, f = 20 kHz (2)	A_V = 1	25°C		0.0013%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF (2)	R_L = 10 kΩ (2)	25°C		2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2V, R_L = 10 kΩ (2)	A_V = 1, C_L = 100 pF (2)	25°C		1		MHz
t_s	Settling time	A_V = -1, Step = 0.5V to 2.5V, R_L = 10 kΩ (2) C_L = 100 pF (2)	To 0.1%	25°C		1.5		μs
			To 0.01%			2.6		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ	C_L = 100 pF (2)	25°C		50°		
	Gain margin			25°C		10		dB

(1) Full range is −40°C to 150°C for this part.
(2) Referenced to 2.5 V

6.7 Electrical Characteristics, $V_{DD\pm}$ = ±5 V

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, R_S = 50 Ω	V_O = 0 V	25°C		300	2500	μV
				Full range			3000	
$αV_{IO}$	Temperature coefficient of input offset voltage			25°C to 125°C		2		μV/°C
	Input offset voltage long-term drift (2)			25°C		0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			7000	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			7000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	$\|V_{IO}\|$ ≤ 5 mV	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99		V
		I_O = −200 μA		25°C	4.85	4.93		
				Full range	4.84			
		I_O = −1 mA		25°C	4.25	4.65		
				Full range	4.20			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA	25°C		−4.99		V
		V_{IC} = 0 V,	I_O = 500 μA	25°C	−4.85	−4.91		
				Full range	−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		
				Full range	−3.45			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V,	R_L = 10 kΩ	25°C	20	50		V/mV
				Full range	16			
			R_L = 1 MΩ	25°C		300		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	AV = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = -5 V to 2.7 V, V_O = 0 V,	R_S = 50 Ω	25°C	75	80		dB
				Full range	73			
k_{SVR}	Supply voltage rejection ratio ($ΔV_{DD}/ΔV_{IO}$)	V_{DD} = ±2.2 V to ±8 V, V_{IC} = 0V,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 0 V,	No load	25°C		4.4	6	mA
				Full range			6	

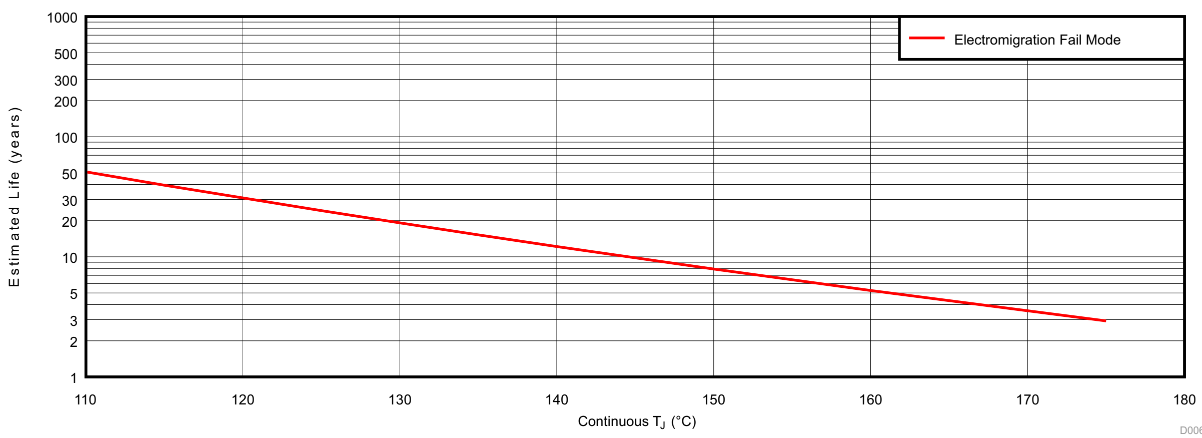
(1) Full range is −40°C to 150°C for this part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6.8 Operating Characteristics, $V_{DD\pm}$ = ±5 V

at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A[(1)]	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ	C_L = 100 pF	25°C	2.3	3.6		V/μs
				Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50		nV/√Hz
		f = 1 kHz		25°C		9		
$V_{N(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		μV
		f = 0.1 to 10 Hz		25°C		1.4		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ	25°C		2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ	A_V = 1, C_L = 100 pF	25°C		0.54		MHz
t_s	Settling time	A_V = -1, Step = -2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5		μs
			To 0.01%			3.2		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°		
	Gain margin			25°C		10		dB

(1) Full range is −40°C to 150°C for this part.



A. See data sheet for *Absolute Maximum Ratings* and minimum *Recommended Operating Conditions*.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 2. TLC2274EPWRQ1 Operating Life Derating Chart

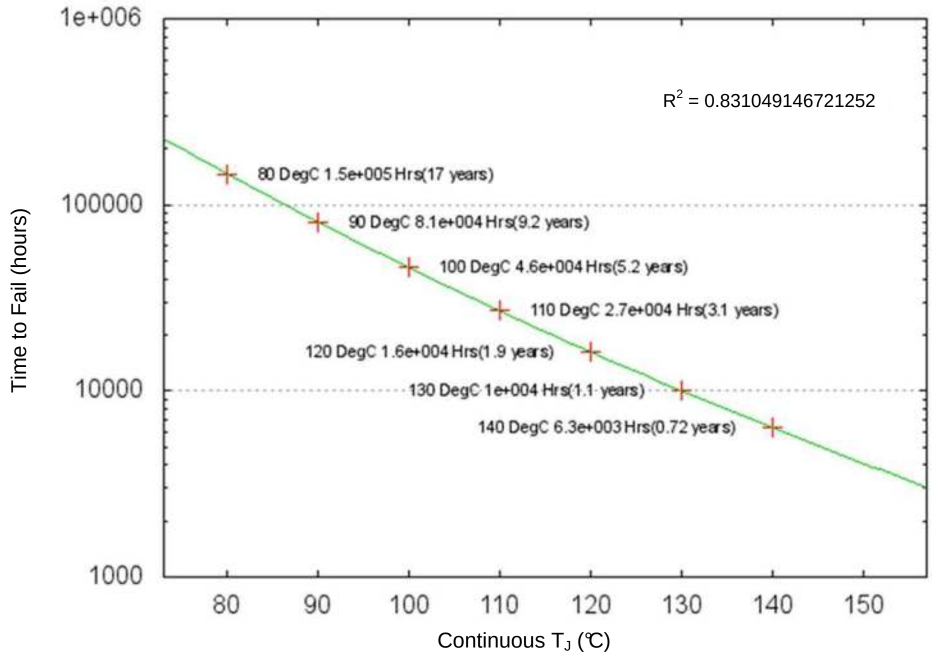


Figure 3. Estimated Wire Bond Life

6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

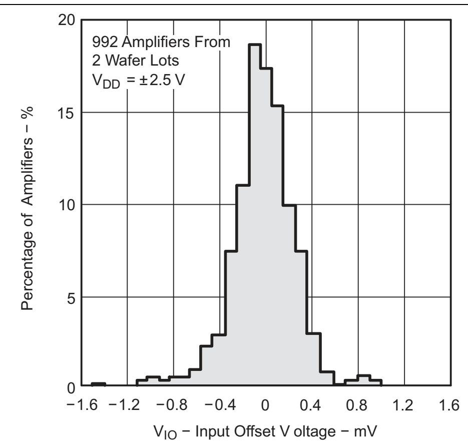


Figure 4. Distribution of TLC2274 Input Offset Voltage

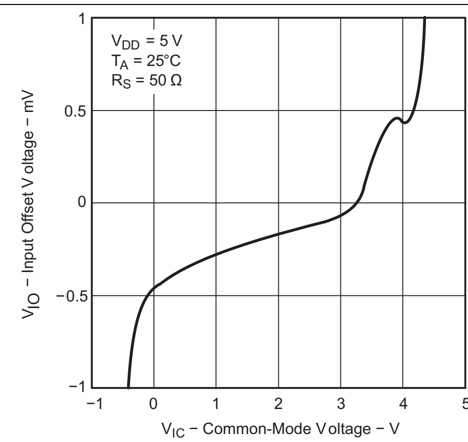


Figure 5. Input Offset Voltage vs Common-Mode Voltage

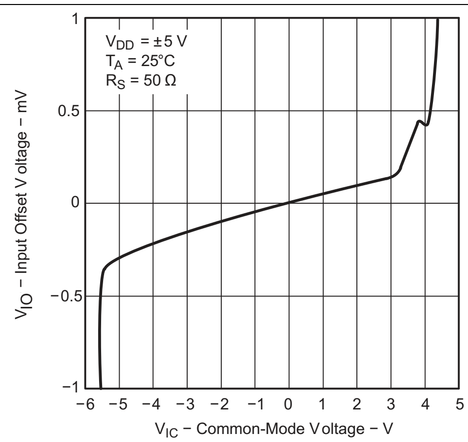


Figure 6. Input Offset Voltage vs Common-Mode Voltage

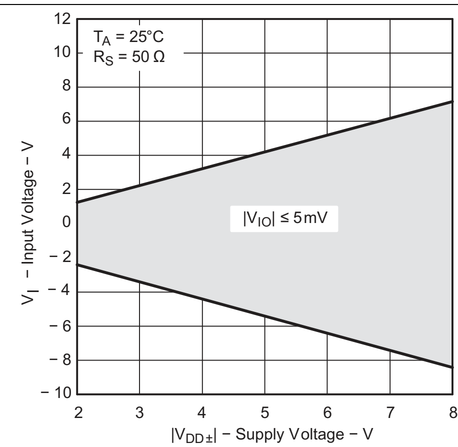


Figure 7. Input Voltage vs Supply Voltage

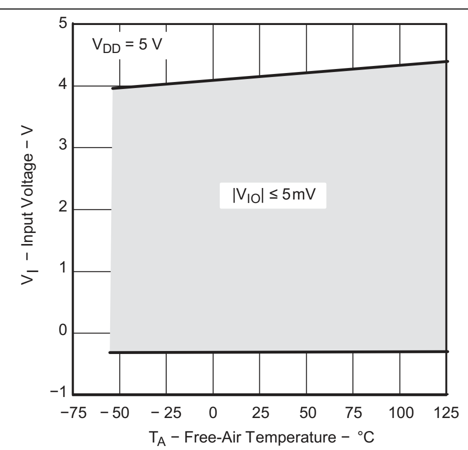


Figure 8. Input Voltage vs Free-Air Temperature

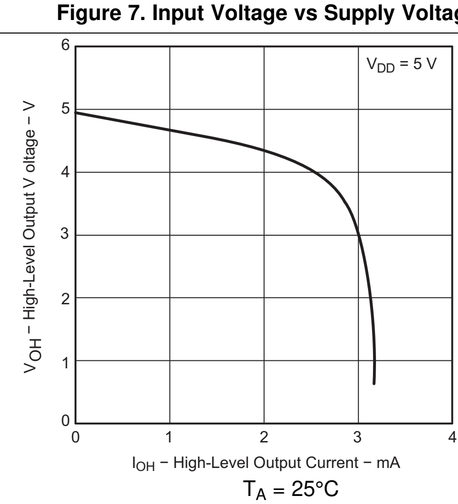


Figure 9. High-Level Output Voltage vs High-Level Output Current

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

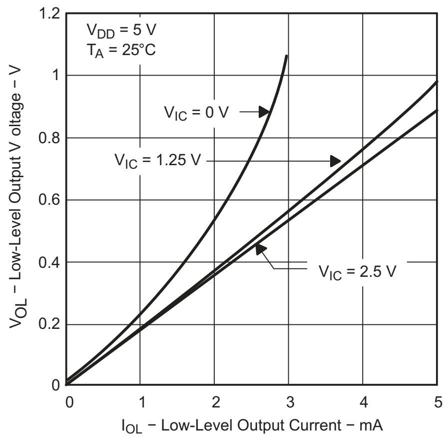


Figure 10. Low-Level Output Voltage vs Low-Level Output Current

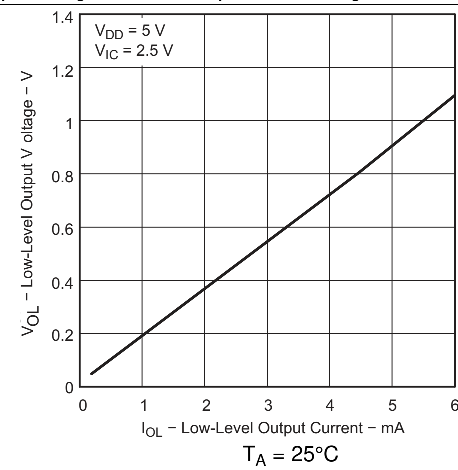


Figure 11. Low-Level Output Voltage vs Low-Level Output Current

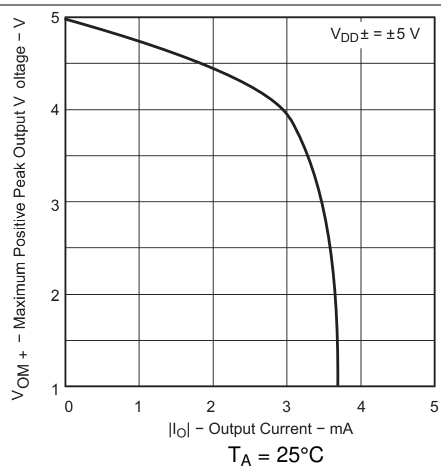


Figure 12. Maximum Positive Peak Output Voltage vs Output Current

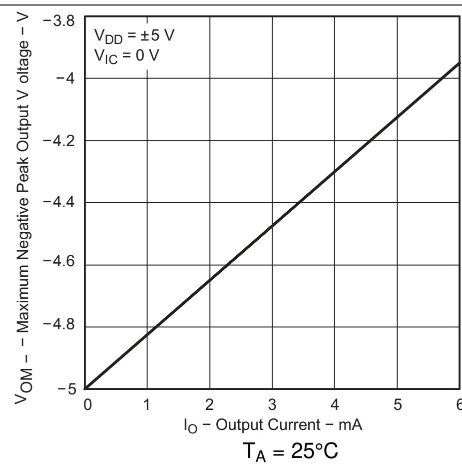


Figure 13. Maximum Negative Peak Output Voltage vs Output Current

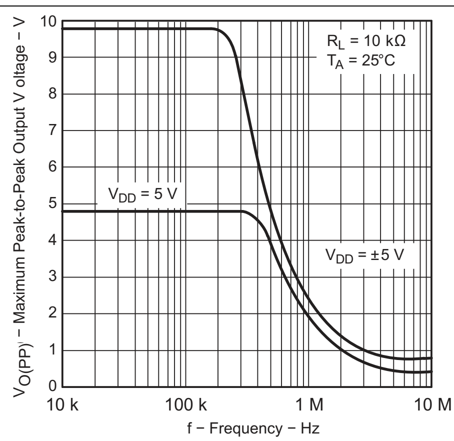


Figure 14. Maximum Peak-to-Peak Output Voltage vs Frequency

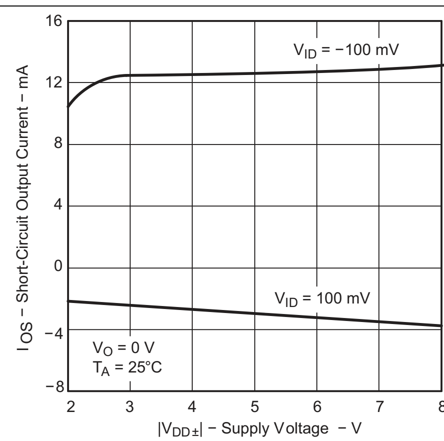


Figure 15. Short-Circuit Output Current vs Supply Voltage

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

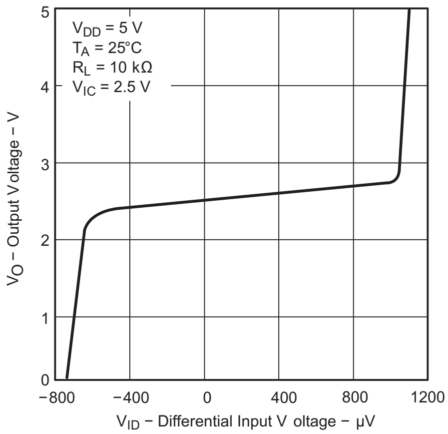


Figure 16. Output Voltage vs Differential Input Voltage

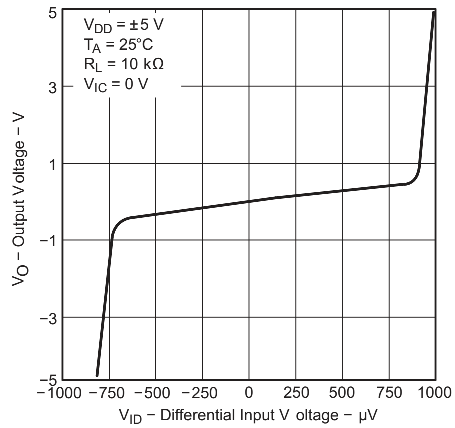


Figure 17. Output Voltage vs Differential Input Voltage

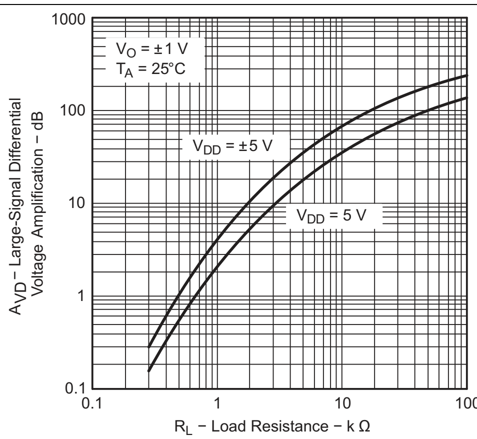


Figure 18. Large-Signal Differential Voltage Amplification vs Load Resistance

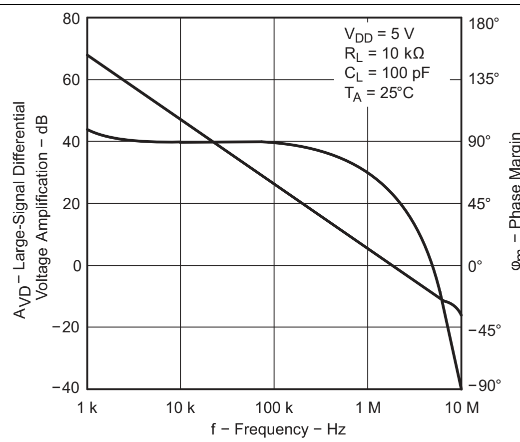


Figure 19. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

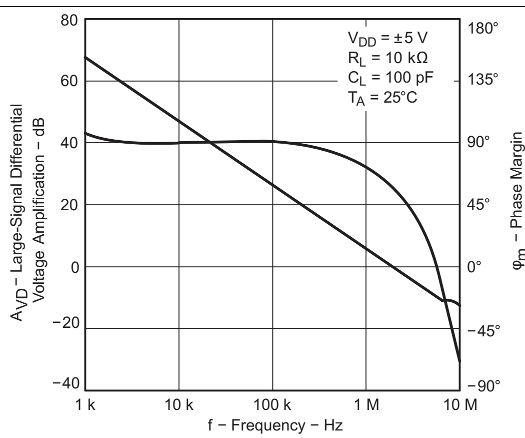
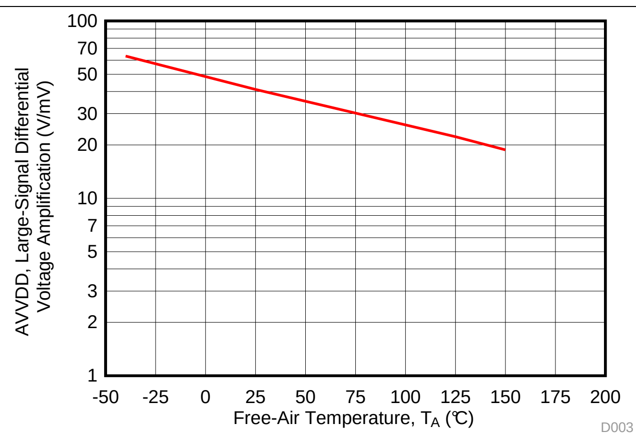


Figure 20. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency



V_{DD} = 5 V V_{IC} = 2.5 V V_O = 1 to 4 V
R_L = 10 kΩ

Figure 21. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

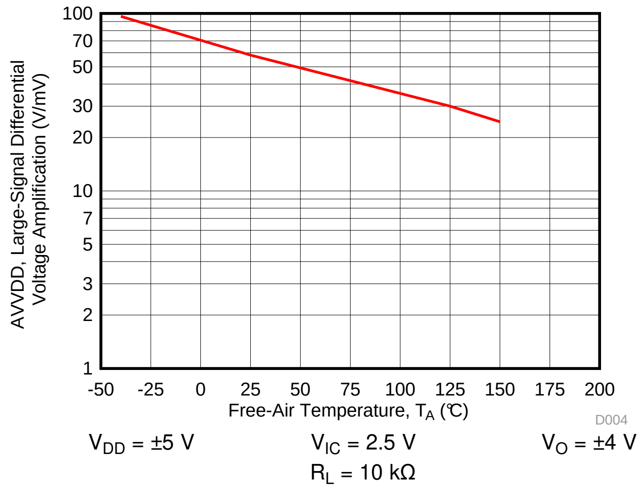


Figure 22. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

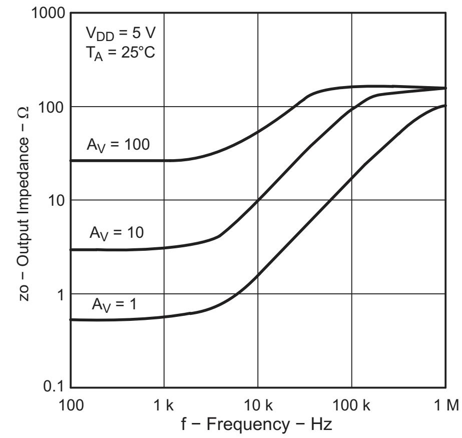


Figure 23. Output Impedance vs Frequency

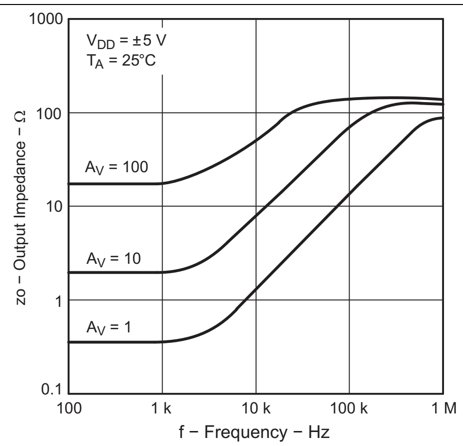


Figure 24. Output Impedance vs Frequency

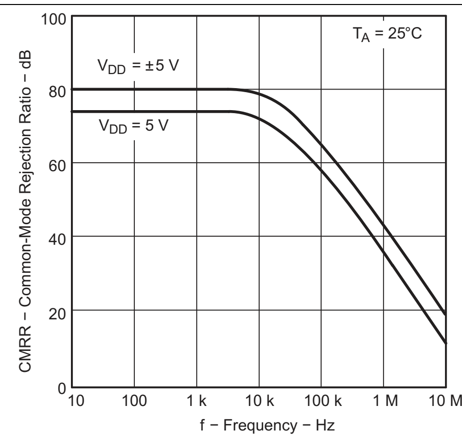


Figure 25. Common-Mode Rejection Ratio vs Frequency

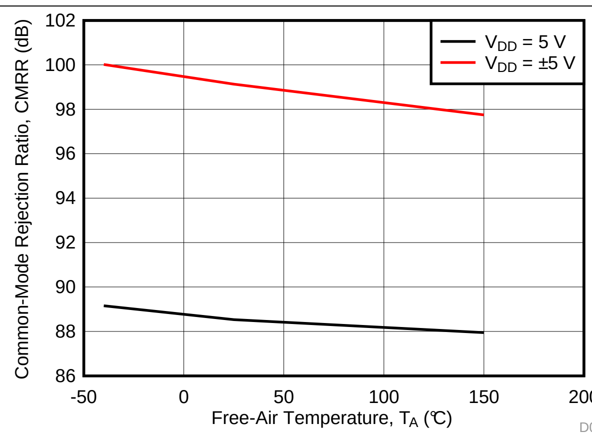


Figure 26. Common-Mode Rejection Ratio vs Free-Air Temperature

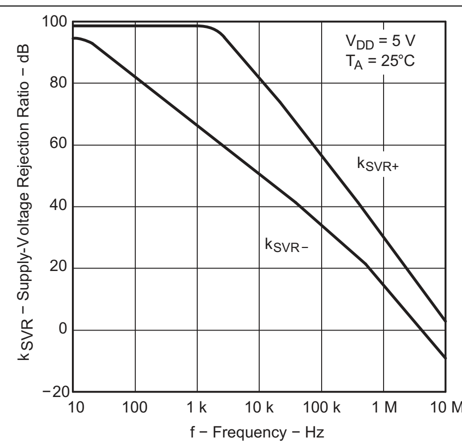


Figure 27. Supply-Voltage Rejection Ratio vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

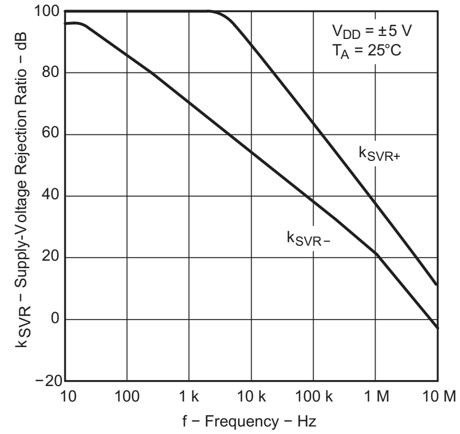
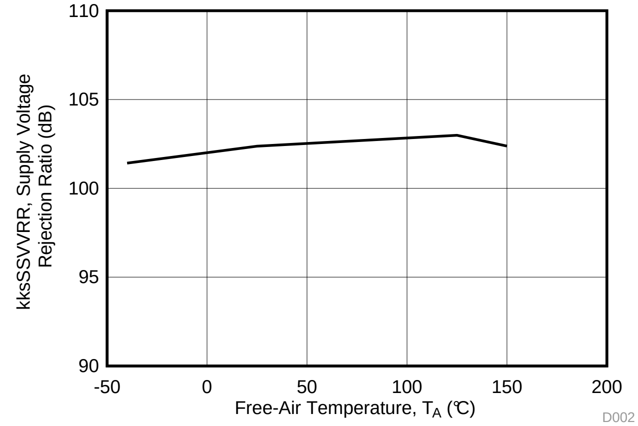


Figure 28. Supply-Voltage Rejection Ratio vs Frequency



$V_{DD\pm}$ = ±2.2 to ±8 V V_O = 0 V

Figure 29. Supply-Voltage Rejection Ratio vs Free-Air Temperature

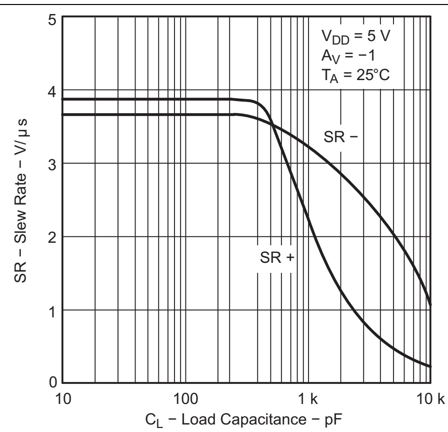
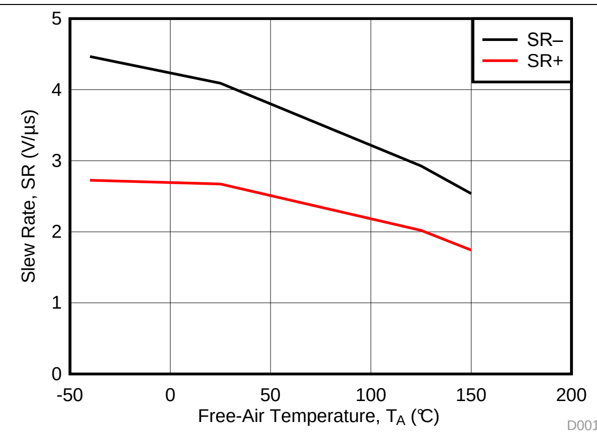


Figure 30. Slew Rate vs Load Capacitance



V_{DD} = 5 V R_L = 10 kΩ C_L = 100 pF
A_V = 1

Figure 31. Slew Rate vs Free-Air Temperature

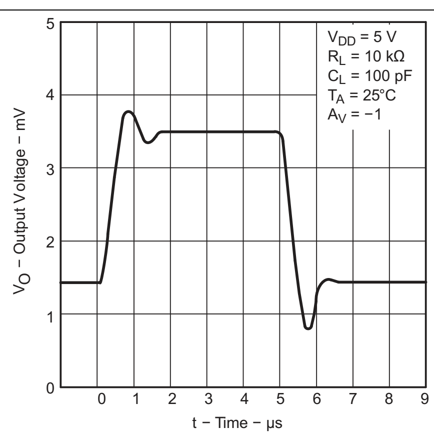


Figure 32. Inverting Large-Signal Pulse Response

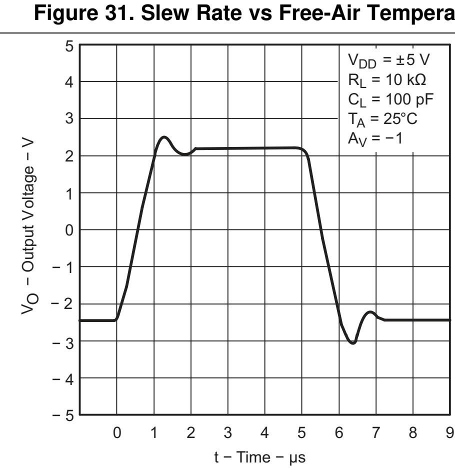


Figure 33. Inverting Large-Signal Pulse Response

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

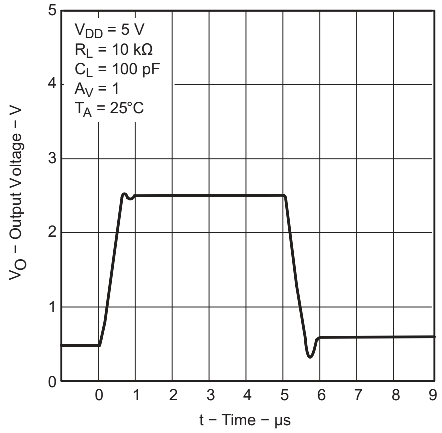


Figure 34. Voltage-Follower Large-Signal Pulse Response

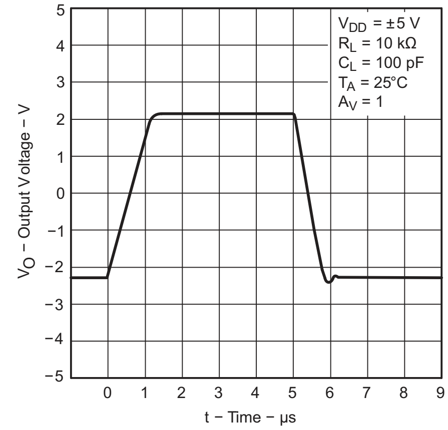


Figure 35. Voltage-Follower Large-Signal Pulse Response

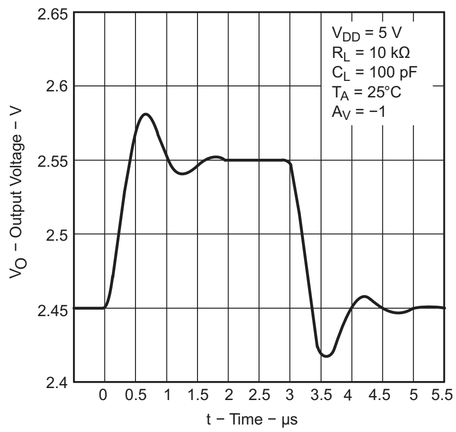


Figure 36. Inverting Small-Signal Pulse Response

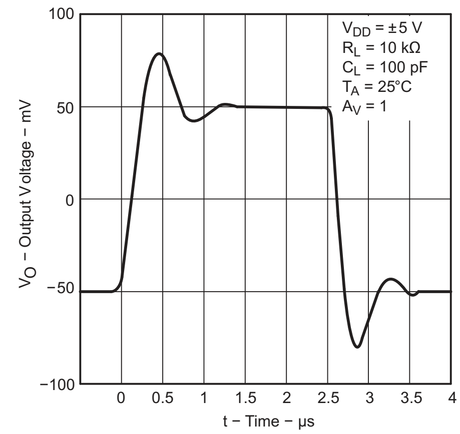


Figure 37. Inverting Small-Signal Pulse Response

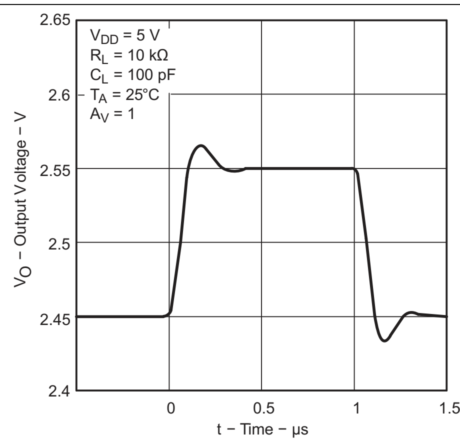


Figure 38. Voltage-Follower Small-Signal Pulse Response

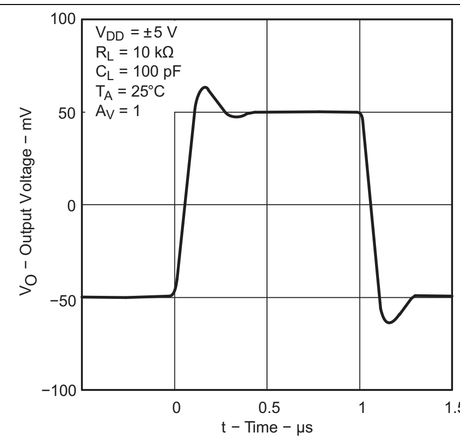


Figure 39. Voltage-Follower Small-Signal Pulse Response

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

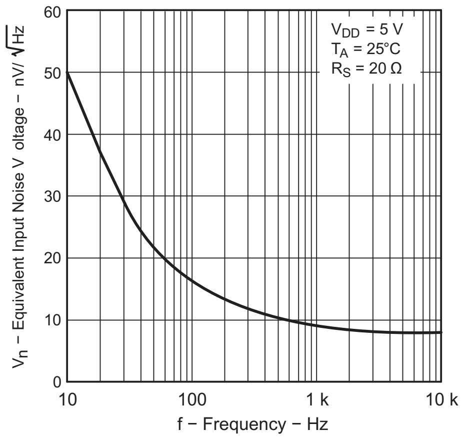


Figure 40. Equivalent Input Noise Voltage vs Frequency

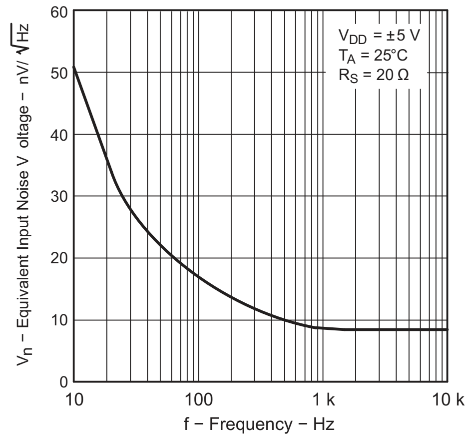


Figure 41. Equivalent Input Noise Voltage vs Frequency

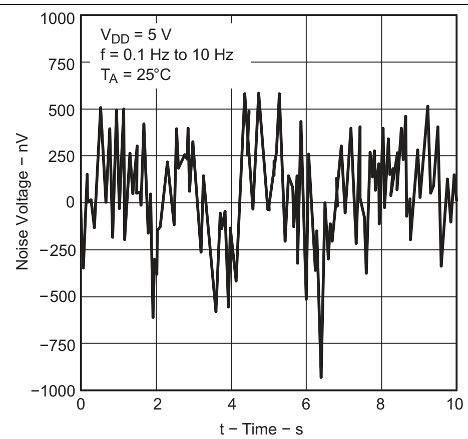


Figure 42. Noise Voltage Over a 10-s Period

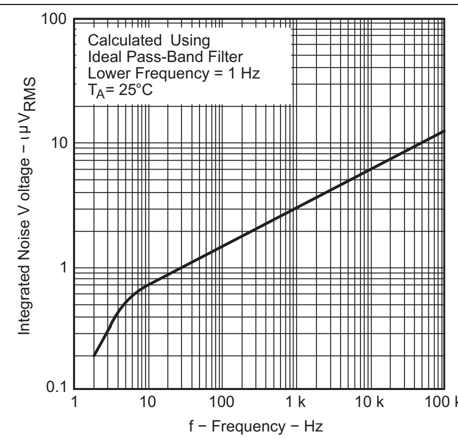


Figure 43. Integrated Noise Voltage vs Frequency

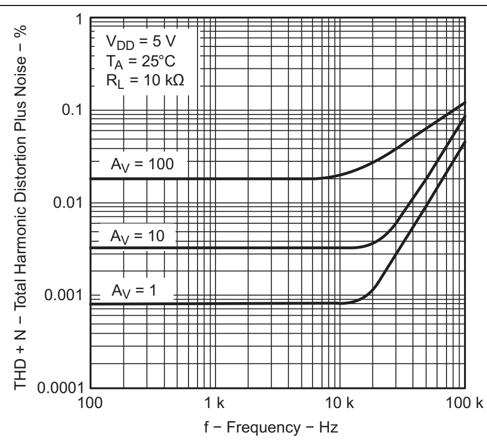


Figure 44. Total Harmonic Distortion Plus Noise vs Frequency

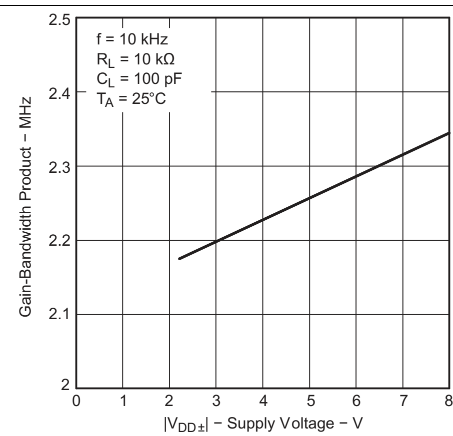


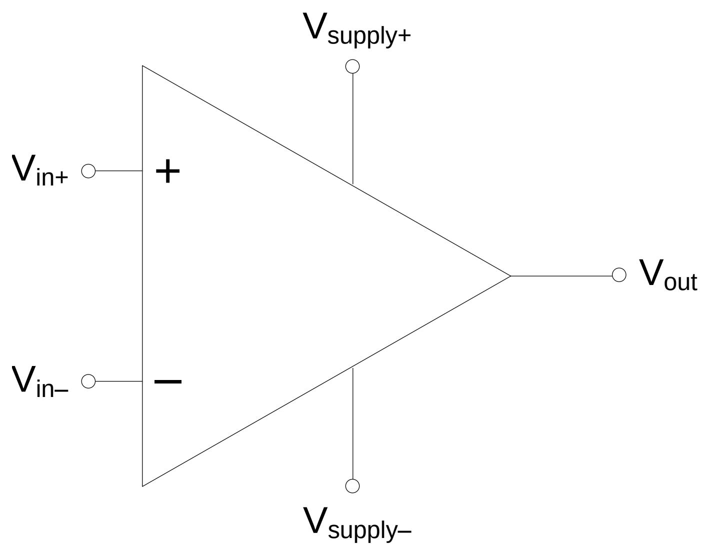
Figure 45. Gain-Bandwidth Product vs Supply Voltage

7 Detailed Description

7.1 Overview

The TLC2274 device exhibits rail-to-rail output performance for increased dynamic range in single- or split - supply applications. These device offers comparable ac performance while having better noise, input offset voltage and power dissipation than existing CMOS operational amplifiers. The TLC2274 device, exhibiting high input impedance and low noise, is excellent for small signal conditioning for high-impedance sources, such as piezoelectric transducers. It offers increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the device to be used in a wider range of applications.

7.2 Functional Block Diagram



7.3 Feature Description

These devices use the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages, very high input impedances, and extremely low input offset and bias currents. In addition, the rail-to-rail output feature with single- or split-supplies, makes this device a great choice when interfacing with analog-to-digital converters (ADCs).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

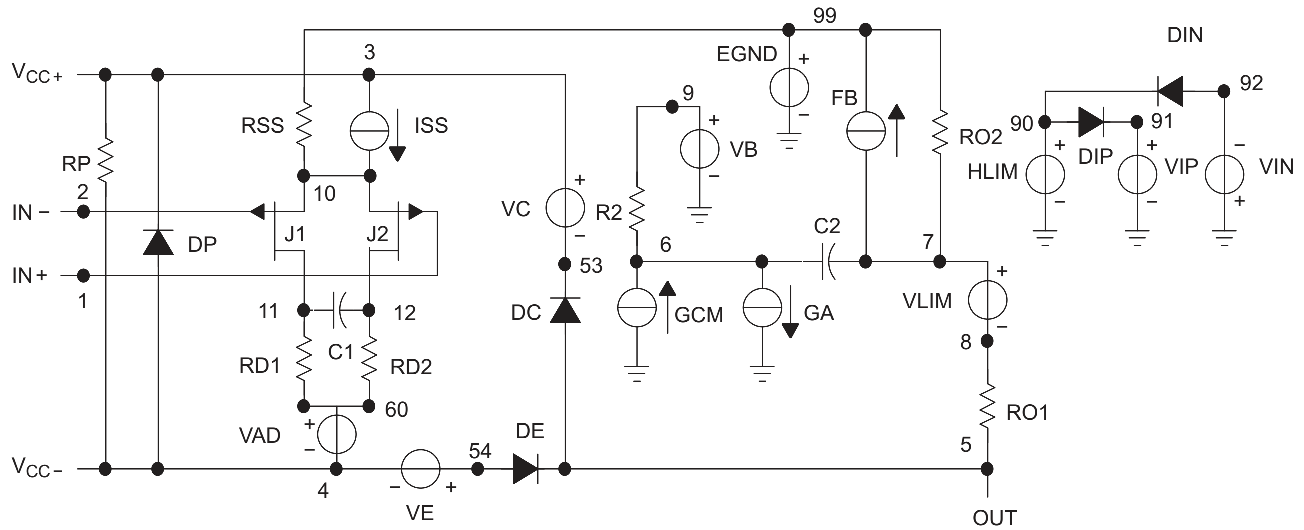
8.1.1 Macromodel Information

Macromodel information provided was derived using Microsim Parts, the model generation software used with Microsim PSpice. The Boyle macromodel [1] and subcircuit in Figure 46 are generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

Application Information (continued)




```
.SUBCKT TLC227x 1 2 3 4 5
        C1      11      1214E−12
        C2      6       760.00E−12
        DC      5       53DX
        DE      54      5DX
        DLP     90      91DX
        DLN     92      90DX
        DP      4       3DX
        EGND    99      0POLY (2) (3,0) (4,) 0 .5 .5
        FB      99      0POLY (5) VB VC VE VLP VLN 0
        + 984.9E3 −1E6 1E6 1E6 −1E6
        GA      6       011 12 377.0E−6
        GCM 0 6 10 99 134E−9
        ISS     3       10DC 216.OE−6
        HLIM    90      0VLIM 1K
        J1      11      210 JX
        J2      12      110 JX
        R2      6       9100.OE3

RD1     60      112.653E3
RD2     60      122.653E3
R01     8       550
R02     7       9950
RP      3       44.310E3
RSS     10      99925.9E3
VAD     60      4−.5
VB      9       0DC 0
VC 3 53 DC .78
VE      54      4DC .78
VLIM    7       8DC 0
VLP     91      0DC 1.9
VLN     0       92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 46. Boyle Macromodels and Subcircuit

8.2 Typical Application

The TLC2274 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 48 and Figure 49 show its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (Rnull = 0).

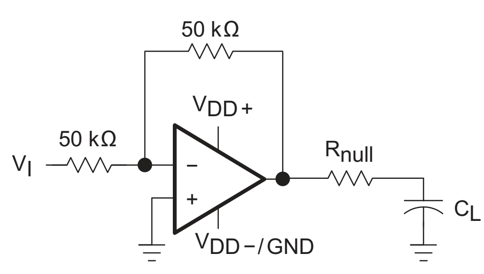


Figure 47. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

As per Equation 1:

Table 2. Design Parameters

Improvement in Phase Margin	UGBW (kHz)	R null (Ω)	CL (pF)
0	1000	0	1000
7.15	1000	20	1000
17.43	1000	50	1000
32.12	1000	100	1000

8.2.2 Detailed Design Procedure

A smaller series resistor (R_{null}) at the output of the device (see Figure 47) improves the gain and phase margins when driving large capacitive loads. Figure 48 and Figure 49 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, Equation 1 can be used.

$$\Delta\varphi_{m1} = \tan^{-1} (2 \times \pi \times UGBW \times R_{null} \times C_L) \quad (1)$$

where

- Δφm1 = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- Rnull = Output series resistance
- CL = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 47). To use equation 1, UGBW must be approximated from Figure 47. Using Equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 51. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. Using Figure 47, with Equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

8.2.3 Application Curves

T_A = 25°C

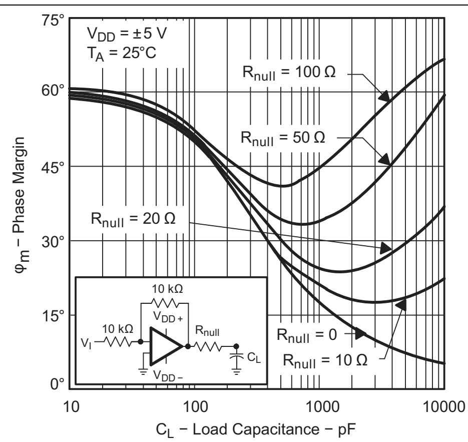


Figure 48. Phase Margin vs Load Capacitance

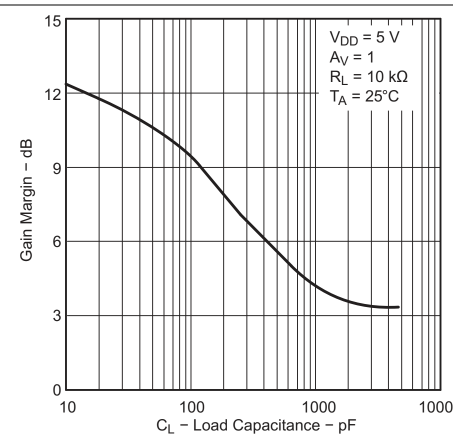


Figure 49. Gain Margin vs Load Capacitance

T_A = 25°C

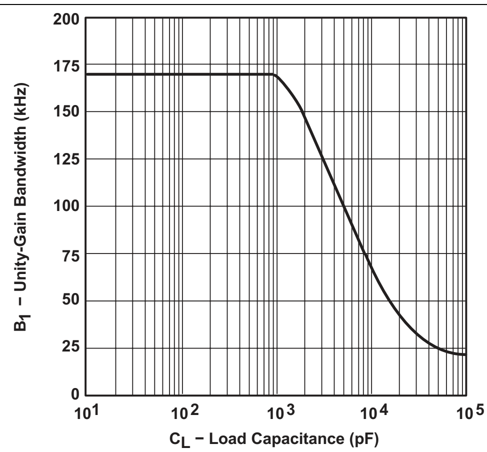


Figure 50. Unity-Gain Bandwidth vs Load Capacitance

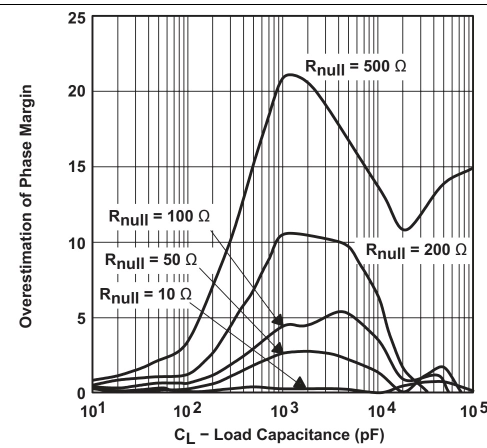


Figure 51. Overestimation of Phase Margin vs Load Capacitance

9 Power Supply Recommendations

TLC2274 operates from ±2.2- to ±8-V. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Parameters which vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

The TLC2274 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the TLC2274. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

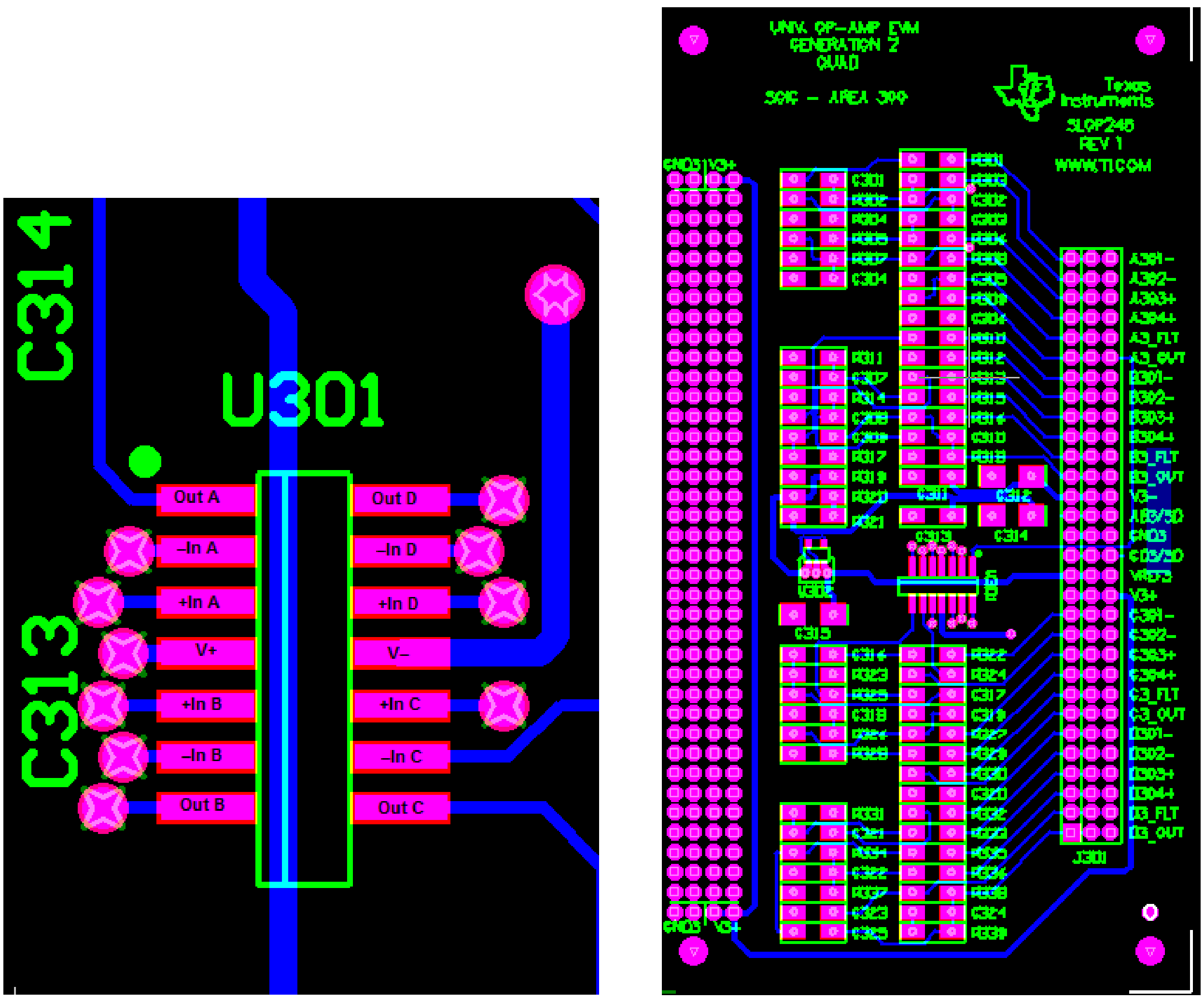


Figure 52. Board Layout Example

11 Device and Documentation Support

11.1 Trademarks

LinCMOS is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274EPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2274EQ1	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC2274-HT :

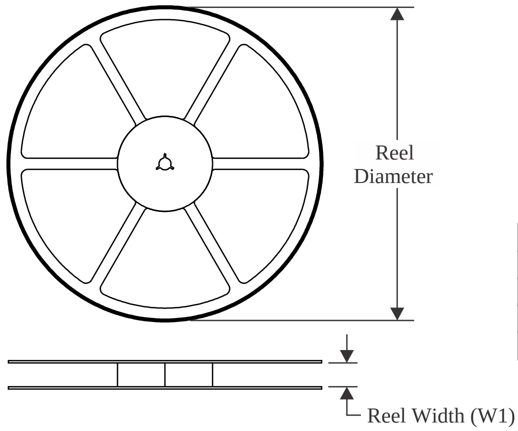
- Catalog: TLC2274
- Automotive: TLC2274-Q1
- Enhanced Product: TLC2274-EP
- Military: TLC2274M

NOTE: Qualified Version Definitions:

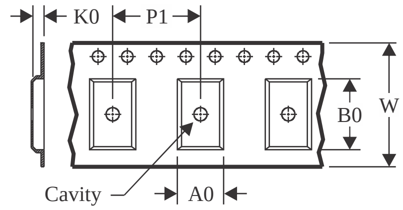
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

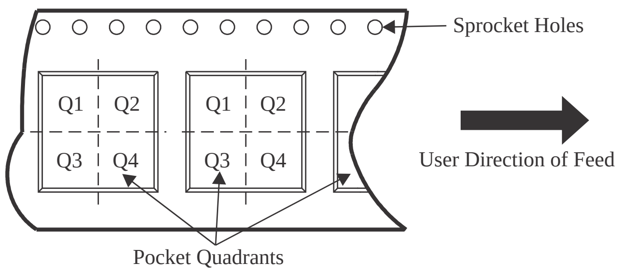


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

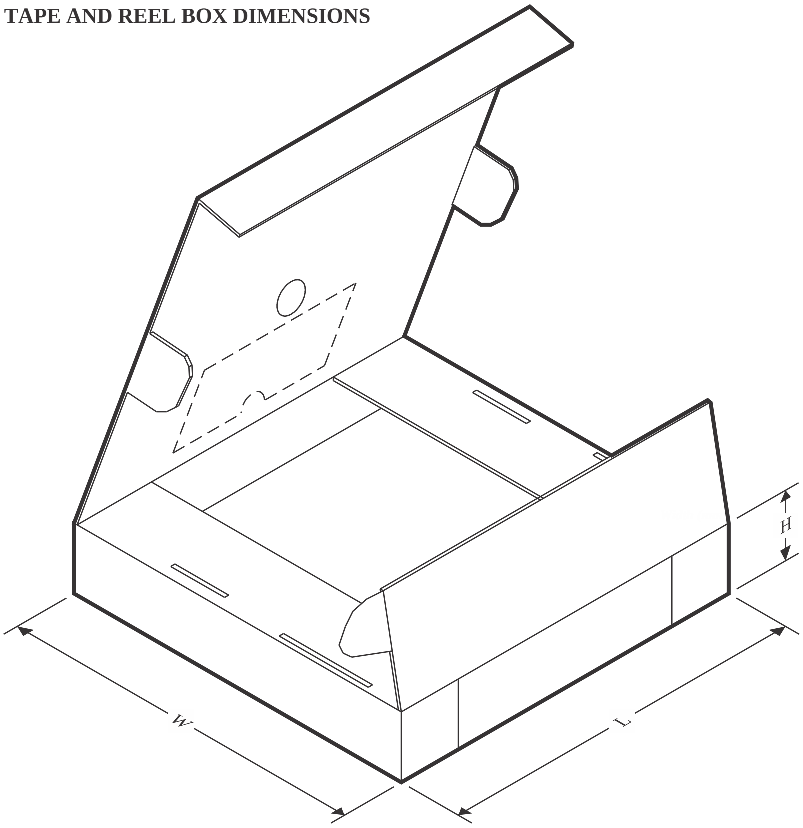
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274EPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

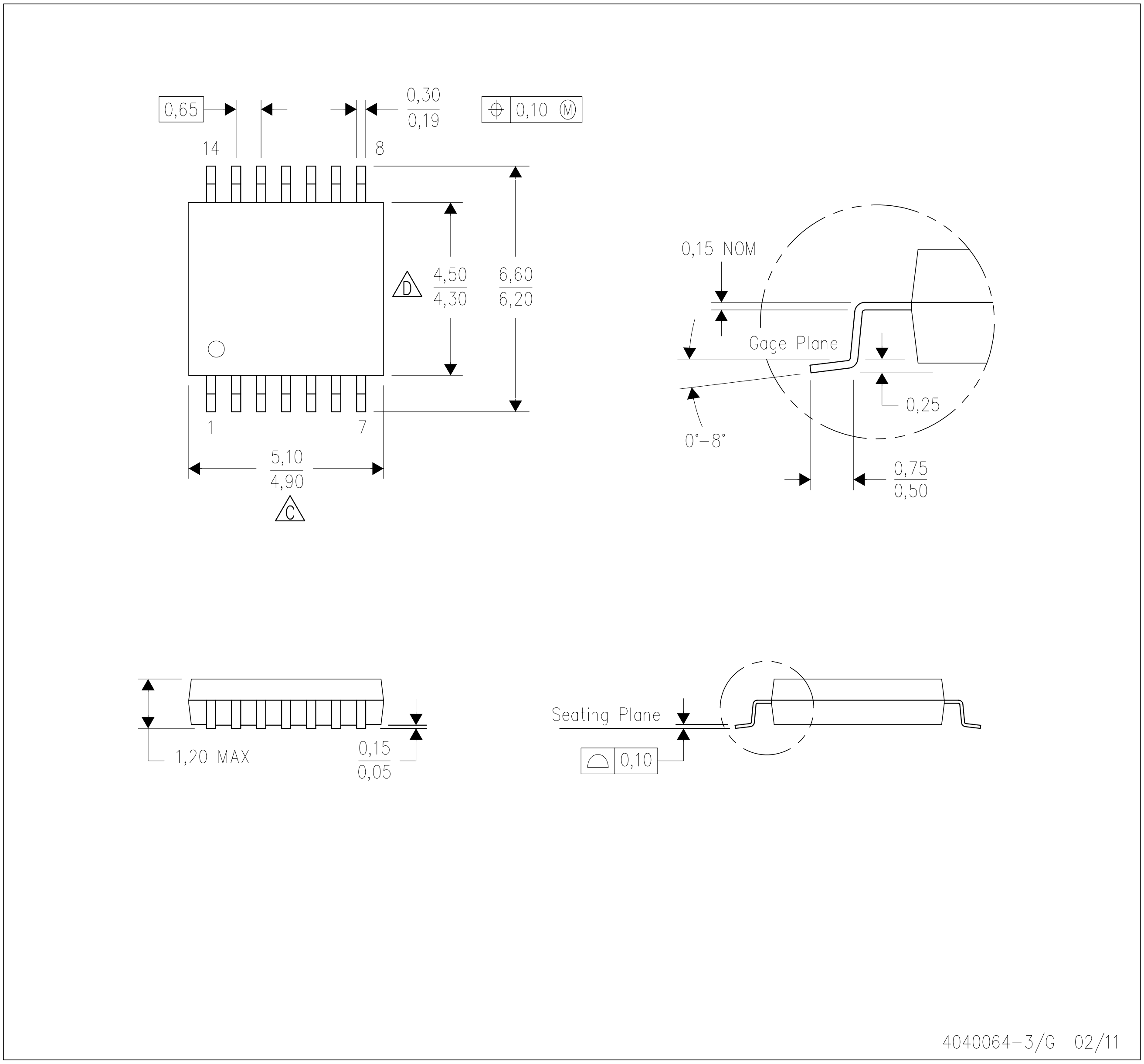
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2274EPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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