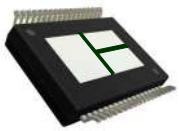
VNH7070AY

Automotive fully integrated H-bridge motor driver

Datasheet - production data



PowerSSO-36 TP

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH7070AY	72 mΩ typ (per leg)	20 A	38 V

- AEC-Q100 qualified
- Output current: 20 A
- 3 V CMOS compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- PWM operation up to 20 KHz
- Multisense monitoring functions
  - Analog motor current feedback
  - Chip temperature monitoring
  - Battery voltage monitoring
- Multisense diagnostic functions
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - High-side power limitation indication
  - Low-side overcurrent shutdown indication
  - Output short to V_{CC} detection
- Output protected against short to ground and short to V_{CC}
- Standby mode
- Half bridge operation
- Package: ECOPACK®

Description

The device is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches. All switches are designed using STMicroelectronics® well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dice are assembled in a PowerSSO-36 package equipped with three exposed islands for optimized dissipation performances. This package is specifically designed for the harsh automotive environment and offers improved thermal performance thanks to exposed die pads. A Multisense_EN pin is available to enable the MultiSense diagnostic. The input signals IN_A and IN_B can directly interface the microcontroller to select the motor direction and the brake condition. Two selection pins (SEL0 and SEL1) are available to address to the microcontroller the information available on the Multisense. The Multisense pin allows to monitor the motor current by delivering a current proportional to the motor current value and provides also the diagnostic feedback according to the implemeted truth table. When MultiSense_EN pin is driven low, MultiSense pin is in high impedance condition. The PWM, up to 20 KHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the LS_A and LS_B switches.

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1 Block diagram and pin description

Figure 1. Block diagram

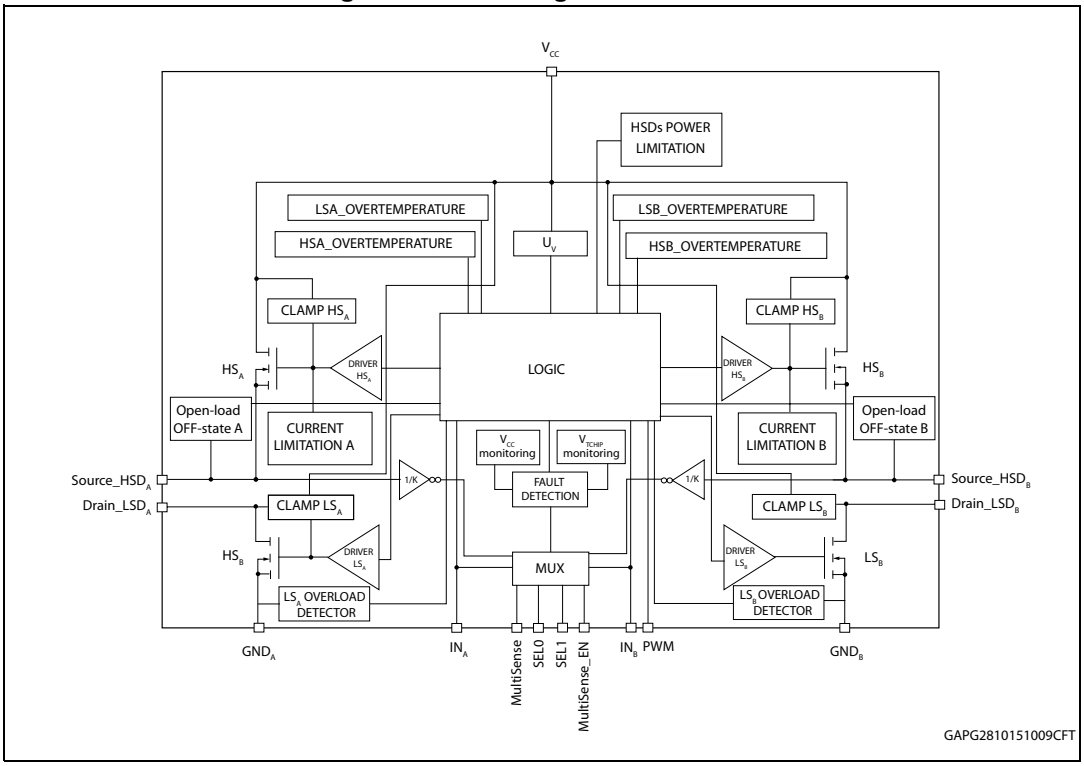


Table 1. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table.
Undervoltage	Shuts down the device for battery voltage below (4 V).
High-side and low-side clamp voltage	Protect the high-side and the low-side switches from high voltage on the battery line.
High-side and low-side driver	Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.
Current limitation	Limits the motor current in case of short circuit.
High-side and low-side overtemperature protection	In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die.
Low-side overcurrent detector	Detects when low-side current exceeds shutdown current and latches off the concerned low-side.
Fault detection	Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by a feedback on the MultiSense
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.

Table 1. Block description (continued)

Name	Description
Open-load in OFF-state	Signalize an open-load when the switches are off by a feedback on the MultiSense
T_{chip} monitoring	Provides a signal linked to the Chip temperature by a feedback on the MultiSense
V_{CC} monitoring	Provides a signal linked to the Chip temperature by a feedback on the MultiSense

Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	SOURCE_HSx	DRAIN_LSx	INPUTx, PWM SELx MultiSense_EN
Floating	Not allowed	X	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	X	Through 15 kΩ resistor

Figure 2. Configuration diagram (top view)

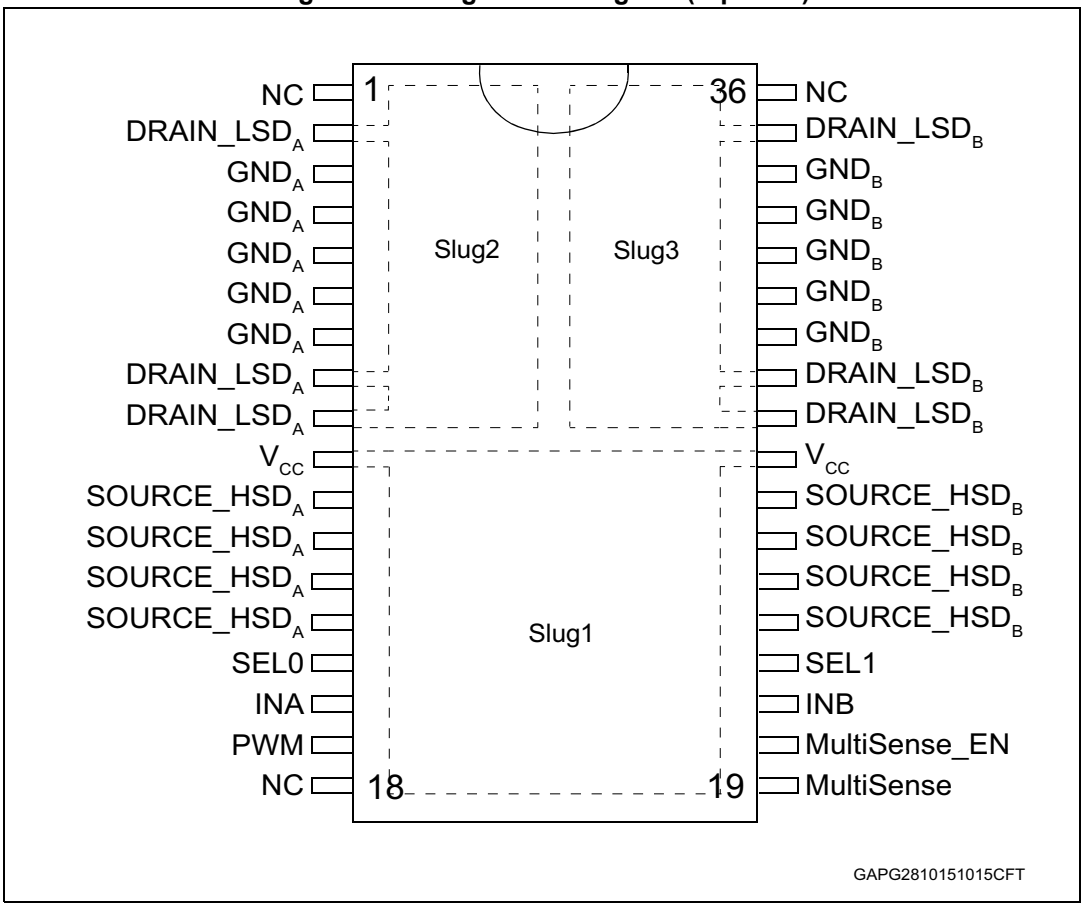


Table 3. Pin definitions and functions

Pin N°	Symbol	Function
1, 18, 36	NC	Not connected.
10, 27	V_{CC}, Heat slug1	Drain of high-side switches and power supply voltage.
16	IN_A	Clockwise input.
17	PWM	PWM input.
19	MultiSense	Output of current sense and diagnostic feedback
20	MultiSense_EN	Enables the MultiSense diagnostic pin
15	SEL0	Address the MultiSense multiplexer
22	SEL1	Address the MultiSense multiplexer
21	IN_B	Counter clockwise input.
28, 29, 35	$Drain\_LSD_B$, Heat Slug3	Drain of low-side switch B.
23, 24, 25, 26	$Source\_HSD_B$	Source of high-side switch B
30, 31, 32, 33, 34	GND_B	Source of low-side switch B.
2, 8, 9	$Drain\_LSD_A$, Heat Slug2	Drain of low-side switch A.
11, 12, 13, 14	$Source\_HSD_A$	Source of high-side switch A
3, 4, 5, 6, 7	GND_A	Source of low-side switch A.

Table 4. Pin functions description

Name	Description
V_{CC}	Battery connection.
GND	Power ground.
$Source\_LSD_A$ $Source\_LSD_B$(1)	Power connections to the motor or the bridge configuration: Source HSD_A and Drain LSD_A must be externally connected; Source HSD_B and Drain LSD_B must be externally connected.
IN_A IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, Brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible. This pin turns ON the low-side driver according to the IN_A and IN_B settings (see *Table 13*). Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor.
SEL_0 SEL_1	Active high compatible with 3 V and 5 V CMOS output pin; they addresses the Multisense multiplexer

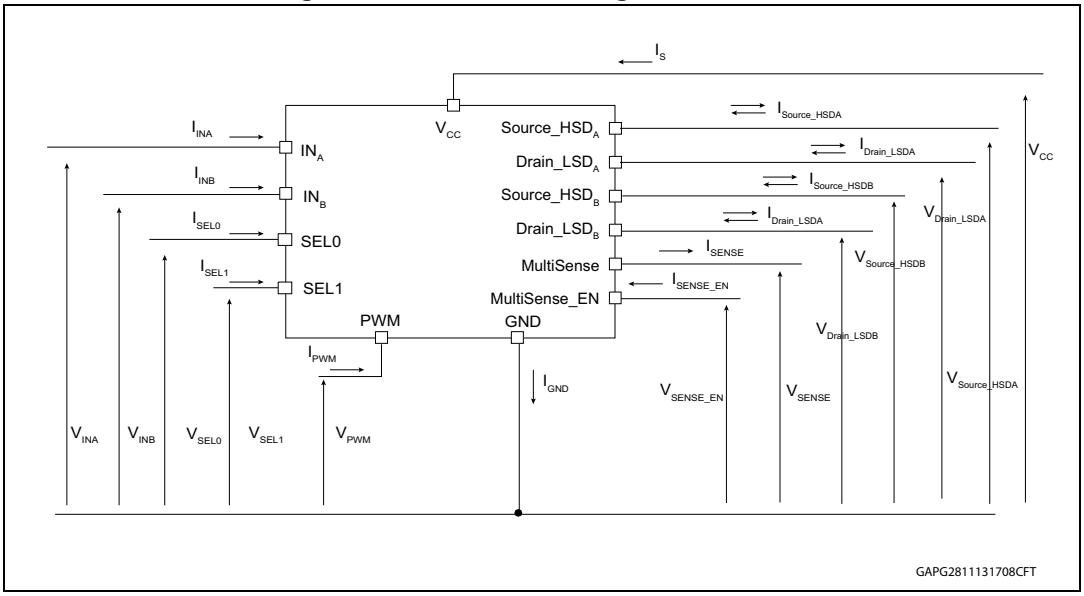
Table 4. Pin functions description (continued)

Name	Description
MultiSense	Multiplexed Analog Signal. It delivers a current proportional to the load or a voltage proportional to the V_{CC} voltage or a voltage proportional to the chip temperature whenever the MultiSense_EN is set to high. The desired signal is chosen via SEL0 and SEL1 levels. The MultiSense pin supplies as well a Fault Flag when a fault is detected on the selected path A or B.
MultiSense_EN	Active high compatible with 3 V and 5 V CMOS output pin. It enables the MultiSense diagnostic pin.

1. If the device is used in Bridge configuration we indicate: Source_HSD_A = Drain_LSD_A = OUT_A; Source HSD_B = Drain LSD_B = OUT_B; OUT_A and OUT_B are the power connections to the motor.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	38	V
$-V_{CC}$	Reverse V_{CC} supply voltage	0.3	V
I_{max}	DC output current (continuous)	Internally limited	A
I_R	Reverse output current (continuous)(1)	-16	A
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2 2010 Test B clamped to 40 V; R_L = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
I_{IN}	Input current (IN_A and IN_B pins)	-1 to 10	mA
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{PWM}	PWM Input current		
I_{SENSE_EN}	MultiSense_EN DC input current	-1 to 1.5	mA
I_{SENSE}	CS pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	CS pin DC output current in reverse (V_{CC} < 0 V)	-20	

Table 5. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human body model: R = 1.5 kΩ; C = 100 pF) – IN_A,IN_B, PWM – MultiSense, SEL0, SEL1, MultiSense_EN – V_{CC} – Output	 2 2 4 4	kV
T_c	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. Based on the internal wires capability.

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter		Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (per leg) (JEDEC JESD 51-8)	HSD	4	°C/W
		LSD	4.3	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		See *Section 9.1.1*	°C/W

2.3 Electrical characteristics

V_{CC} = 7 V up to 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 7. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4		28	V
I_S	Supply current	Off-state standby IN_A = IN_B = PWM = 0; $SEL_{0,1}$ = 0; T_j = 25 °C; V_{CC} = 13 V; MultiSense_EN = 0			1	µA
		Off-state standby(1); IN_A = IN_B = PWM = 0; $SEL_{0,1}$ = 0; V_{CC} = 13 V; T_j = 85 °C; MultiSense_EN = 0			1	µA
		Off-state standby; IN_A = IN_B = PWM = 0; $SEL_{0,1}$ = 0; V_{CC} = 13 V; T_j = 125 °C; MultiSense_EN = 0			3	µA
		Off-state (no standby) IN_A = IN_B = PWM = 0; $SEL_{0,1}$ = 1; MultiSense_EN = 0		2	4	mA
		On-state: IN_A or IN_B = 5V; PWM = 1; $SEL_{0,1}$ = 0; Multisense_EN=0; No Load		3.5	6	mA
t_{D_STBY}(2)	Standby mode blanking time	V_{CC} = 13 V; IN_A = IN_B = MultiSense_EN = 0 V; PWM = SEL_1 = 0 V; V_{SEL0} from 5 V to 0 V.	60	300	550	µs
R_{ONHS}	Static high-side resistance	I_{OUTx} = 3.5 A; T_j = 25 °C		42		mΩ
		I_{OUTx} = 3.5 A; T_j = - 40 °C to 150 °C			85	mΩ
		V_{CC} = 4 V; I_{OUT} = 3.5 A; T_j = 25 °C		42		mΩ
R_{ONLS}	Static low-side resistance	I_{OUTx} = 3.5 A; T_j = 25 °C		30		mΩ
		I_{OUTx} = 3.5 A; T_j = - 40 °C to 150 °C			60	mΩ
		V_{CC} = 4 V; I_{OUT} = 3.5 A; T_j = 25 °C		30		mΩ
V_f	High-side free-wheeling diode forward voltage	I_{OUTx} = -5 A; T_j = 150 °C		0.7	0.9	V
$I_{L(off)}$	Off-State Output current of one leg	T_j = 25 °C; V_{CC} = 13V; V_{OUTA} = 0 or V_{OUTB} = 0; IN_A = IN_B = PWM = 0	0		1	µA
		T_j = 125°C; V_{CC} = 13V; V_{OUTA} = 0 or V_{OUTB} = 0; IN_A = IN_B = PWM = 0	0		3	µA
$I_{L(off)h}$	Off-state output current of one leg with other HSD on	IN_A = PWM = 0; IN_B = 5 V; V_{CC} = 13 V; V_{OUTA} = 0	20		60	µA

1. Parameter guaranteed by design and characterization; not subject to production test.
2. To power on the device from standby, it is recommended to: toggle INA or INB or SEL0 or SEL1 or Multisense_EN from 0 to 1 first to come out from STBY mode; toggle PWM from 0 to 1 with a delay of 20 µs this avoids any overstress on the device in case of existing short-to-battery.

Table 8. Logic inputs (V_{cc}=7 V up to 28 V;-40 °C< T_j<150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
V_{IH}	Input high level voltage		2.1			V
V_{IHYST}	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		V
I_{INL}	Input current	V_{IN} = 0.9 V	1			µA
I_{INH}	Input current	V_{IN} = 2.1 V			10	µA
SEL_0, SEL_1 (V_{CC} = 7 V up to 18 V; -40 °C < T_j < 150 °C)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{SEL} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{SEL} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{SEL} = 1 mA	5.3		7.2	V
		I_{SEL} = -1 mA		-0.7		V
PWM (V_{CC} = 7 V up to 28 V; -40 °C < T_j < 150 °C)						
V_{PWM}	Input low level voltage				0.9	V
I_{PWM}	Low level input current	V_{PWM} = 0.9 V	1			µA
V_{PWM}	Input high level voltage		2.1			V
I_{PWMH}	High level input current	V_{PWM} = 2.1 V			10	µA
$V_{PWM(hyst)}$	Input hysteresis voltage		0.2			V
V_{PMWCL}	Input clamp voltage	I_{PWM} = 1 mA	5.3		7.2	V
		I_{PWM} = -1 mA		-0.7		V
SENSE_EN (V_{CC} = 7 V up to 18 V; -40 °C < T_j < 150 °C)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{SEn} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{SEn} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clump voltage	I_{SEn} = 1 mA	5.3		7.5	V
		I_{SEn} = -1 mA		-0.7		V

Table 9. Switching (V_{CC} = 13 V; R_{LOAD} = 2.6 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$f^{(1)}$	PWM frequency		0		20	kHz
$t_{d(on)}$	Turn-on delay time	Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*)		25		µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*)		15		µs
t_r	Rise time	See *Figure 5*		0.7	1.5	µs
t_f	Fall time	See *Figure 5*		0.2	0.5	µs
t_{cross}	Low-side turn-on delay time	See *Figure 7*	40	160	300	µs

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Protections and diagnostics (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{USD}	Undervoltage shutdown	V_{CC} falling			4	V
$V_{USDreset}$	Undervoltage shutdown reset	V_{CC} rising			5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
I_{LIM_HSD}	High-side current limitation	V_{CC} = 13 V	20	29	40	A
		4 V < V_{CC} < 18 V			40	A
I_{SD_LSD}	Shutdown LS current		25	38	54	A
t_{SD_LSD}	Time to shutdown for the low-side	IN_A = IN_B = 0; PWM = 5 V (see *Figure 8*)		5		µs
V_{CL_HSD}	High-side clamp voltage (V_{CC} to OUT_A = 0 or OUT_B = 0)	I_{OUT} = 100 mA; t_{clamp} = 1 ms; I_{clamp} = 100 mA	38	46		V
V_{CL_LSD}	Low-side clamp voltage (OUT_A = V_{CC} or OUT_B = V_{CC} to GND)	I_{OUT} = 100 mA; t_{clamp} = 1 ms; I_{clamp} = 100 mA	38	46		V
T_{TSD_HSD}	High-side thermal shutdown temperature	IN_x = 2.1 V	150	175	200	°C
T_{TR_HSD}	High-side thermal reset temperature		135			°C
T_{HYST_HSD}	High-side thermal hysteresis (T_{TSD_HSD} - T_{TR_HSD})			7		°C
T_{TSD_LSD}	Low-side thermal shutdown temperature	IN_x = 0 V, PWM = 5 V	150	175	200	°C

Table 10. Protections and diagnostics (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CL}	Total clamp voltage (V_{CC} to GND)	I_{OUT} = 100 mA; t_{clamp} = 1 ms; I_{clamp} = 100 mA	38	46	52	V
V_{OL}	OFF-state open-load voltage detection threshold	IN_A = IN_B = 0; PWM = 0; MultiSense_EN = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V for CHA; V_{SEL0} = 0 V; V_{SEL1} = 0 V for CHB	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	IN_A = IN_B = 0; V_{OUTx} = V_{OL}; PWM = 0; MultiSense_EN = 5 V; SEL_0 = 1; SEL_1 = 0 for CHA; SEL_0 = 0; SEL_1 = 0 for CHB	-100		-15	µA
ΔT_{j_SD}(1)	Dynamic temperature			60		°C
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 4*)	V_{INA} = 5 V to 0 V; IN_B = 0; PWM = 0; V_{SEL0} = 5 V; V_{SEL1} = 0 V; SENSE_EN = 1; I_{OUTA} = 0 A; V_{OUTA} = 4 V	40	160	300	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	IN_A = IN_B = 0; PWM = 0; V_{SENSE_EN} = 5 V; V_{OUTx} = 0 V to 4 V; SEL_0 = 1; SEL_1 = 0 for CHA; SEL_0 = 0; SEL_1 = 0 for CHB (see *Figure 11*)		5	30	µs
$t_{Latch\_RST\_HD}$(1)	Input reset time for high-side fault unlatch	V_{INx} = 5 V to 0 V; H_{SDx} faulting (see *Figure 9*)	3	10	20	µs
$t_{Latch\_RST\_LS}$(1)	Input reset time for low-side fault unlatch	V_{INx} = 0 V to 5 V; L_{SDx} faulting (see *Figure 10*)	3	10	20	µs

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 11. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
		V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUTx} = 0.05 A; V_{SENSE} = 0.5 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	665	1900		
K_0	I_{OUT}/I_{SENSE}	I_{OUTx} = 0.2 A; V_{SENSE} = 0.5 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	1083	1900	2716	
K_1	I_{OUT}/I_{SENSE}	I_{OUTx} = 3.5 A; V_{SENSE} = 4 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	1420	1680	1940	
K_2	I_{OUT}/I_{SENSE}	I_{OUTx} = 5.5 A; V_{SENSE} = 4 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	1480	1690	1900	
dK_{OL}/K_{OL} (1)	Analog sense current drift	I_{OUTx} = 0.05 A; V_{SENSE} = 0.5 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	-25		25	%
dK_0/K_0 (1)	Analog sense current drift	I_{OUTx} = 0.2 A; V_{SENSE} = 0.5 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	-21		21	%
dK_1/K_1 (1)	Analog sense current drift	I_{OUTx} = 3.5 A; V_{SENSE} = 4 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150 °C	-5		5	%
dK_2/K_2 (1)	Analog sense current drift	I_{OUTx} = 5.5 A; V_{SENSE} = 4 V; V_{SENSE_EN} = 5 V; T_j = -40 °C to 150°C	-4		4	%
I_{SENSE0}	MultiSense leakage current	IN_A = IN_B = PWM = 0 V; SEL_0 = SEL_0 = SEn = 0 V; T_j = -40 °C to 150°C (standby)	0		0.5	µA
		SEn = 5 V; IN_A = IN_B = 5 V; PWM = 0 V; legX diagnostic selected; I_{OUTx} = 0 A E.g. – LegA: SEL_0 = 5 V; SEL_1 = 0 V; I_{OUTA} = 0 A; I_{OUTB} = 5 A – LegB: SEL_0 = 0 V; SEL_1 = 0 V; I_{OUTA} = 5 A; I_{OUTB} = 0 V	0		5	µA
		SEn = 5 V; PWM = 0 V; legX diagnostic selected; HSx OFF E.g.: – LegA: SEL_0 = 5 V; SEL_1 = 0 V; IN_A = 0 V; IN_B = 5 V; I_{OUTB} = 5 A – LegB: SEL_0 = 0 V; SEL_1 = 0 V; IN_A = 5 V; IN_B = 0 V; I_{OUTA} = 5 A	0		5	µA

Table 11. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ; V_{SEn} = 5 V – E.g: OUT_A in open-load; V_{INA} = 0 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V; I_{OUTA} = 0 A; V_{OUTA} = 4 V	5		7	V
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{INA} = 5 V; V_{INB} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V; R_{SENSE} = 2.7 kΩ I_{OUTx} = 5 A		5		V
V_{SENSE_SAT}	MultiSense saturation voltage	V_{CC} = 7 V; V_{SEn} = 5 V; R_{SENSE} = 10 kΩ; V_{INA} = 5 V; V_{INB} = 0 V; I_{OUTA} = 5.5 A; V_{SEL0} = 5 V; V_{SEL1} = 0 V; T_j = 150 °C	5			V
I_{SENSE_SAT}(1)	MultiSense saturation current	V_{CC} = 13 V; V_{SENSE} = 4 V; V_{SEn} = 5 V; V_{INA} = 5 V; V_{INB} = 0 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V; T_j = 150°C	4.6			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 13 V; V_{SENSE} = 4 V; V_{SEn} = 5 V; V_{INA} = 5 V; V_{INB} = 0 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V; T_j = 150°C	8.7			A
I_{SENSEH}	MultiSense current in fault condition	9 V < V_{CC} < 18 V; V_{SENSE} = 5 V; MultiSense in fault condition	10	20	30	mA
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SENSE_EN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{INA} = V_{INB} = 0 V; R_{SENSE} = 1 kΩ; T_j = -40 °C	2.277	2.371	2.465	V
		V_{SENSE_EN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{INA} = V_{INB} = 0 V; R_{SENSE} = 1 kΩ; T_j = 25 °C	1.948	2.033	2.119	V
		V_{SENSE_EN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{INA} = V_{INB} = 0 V; R_{SENSE} = 1 kΩ; T_j = 125 °C	1.401	1.486	1.572	V
dV_{SENSE_TC}/dT (1)	Temperature coefficient	T_j = -40 °C to 150 °C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC}/dT * (T - T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SENSE_EN} = 5 V; V_{SEL0} = V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function		$V_{SENSE\_VCC} = V_{CC}/4$				

Table 11. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MultiSense timings (Multiplexer transition times)(2)						
t_{D_AtoB}	Multisense transition delay from legA to legB	V_{INA} = 5 V to 0 V, V_{INB} = 5 V V_{sense_EN} = 5 V V_{sel0} = 5 V to 0 V V_{sel1} = 0 V R_{sense} = 1 KOhm I_{OUTA} = 150 mA I_{OUTB} = 6 A			20	µs
t_{D_BtoA}	Multisense transition delay from legB to legA	V_{INB} = 5 V to 0 V, V_{INA} = 5 V V_{sense_EN} = 5 V V_{sel0} = 0 V to 5 V V_{sel1} = 0 V R_{sense} = 1 KOhm I_{OUTB} = 150 mA I_{OUTA}= 6 A			20	µs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{INA} = 5 V; V_{SENSE_EN} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 0 V to 5 V; I_{OUTA} = 2.5 A; R_{SENSE} = 1 kΩ;			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{INA} = 5 V; V_{SENSE_EN} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V to 0 V; I_{OUTA} = 2.5 A; R_{SENSE} = 1 kΩ;			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{INA} = 5 V; V_{SENSE_EN} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUTA} = 2.5 A; R_{SENSE} = 1 kΩ;			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{INA} = 5 V; V_{SENSE_EN} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUTA} = 2.5 A; R_{SENSE} = 1 kΩ;			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125 °C; V_{SENSE_EN} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ;			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125 °C; V_{SENSE_EN} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ;			20	µs
MultiSense timings (CurrentSense mode)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of V_{SENSE_EN}	V_{INA} = 5 V; V_{INB} = 0 V; V_{SENSE_EN} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω; V_{PWM} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V			60	µs

Table 11. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of V_{SENSE_EN}	V_{INA} = 5 V; V_{INB} = 0 V; V_{SENSE_EN} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω; V_{PWM} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V			20	µs
MultiSense timings (chip temperature sense mode)						
$t_{DSENSE2H}$	V_{SENSE_TC} setting time from rising edge of V_{SENSE_EN}	V_{SENSE_EN} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE2L}$	V_{SENSE_TC} setting time from falling edge of V_{SENSE_EN}	V_{SENSE_EN} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timing (V_{CC} voltage sense mode)						
$t_{DSENSE3H}$	V_{SENSE_VCC} setting time from rising edge of V_{SENSE_EN}	V_{SENSE_EN} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_VCC} setting time from falling edge of V_{SENSE_EN}	V_{SENSE_EN} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V R_{SENSE} = 1 kΩ			20	µs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. T_{DSTKON}

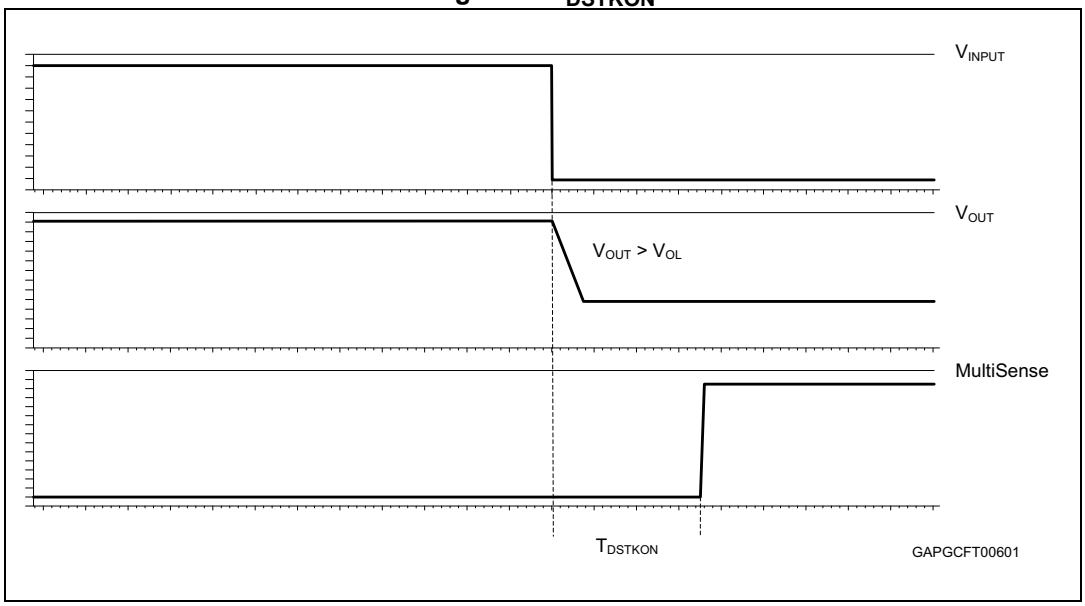


Figure 5. Definition of the low-side switching times

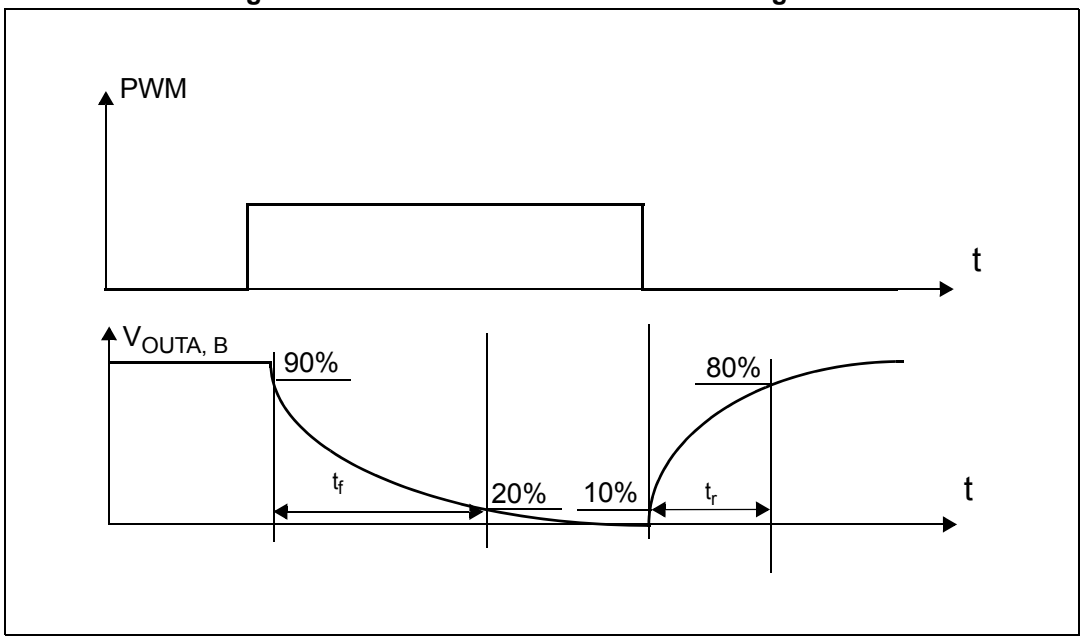


Figure 6. Definition of the high-side switching times

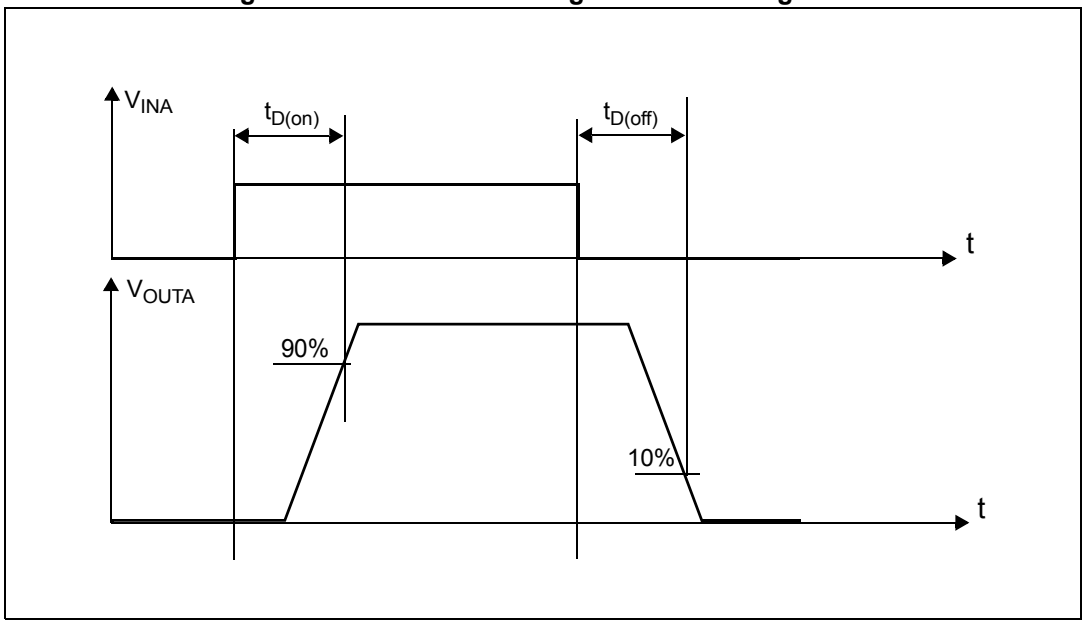


Figure 7. Low-side turn-on delay time

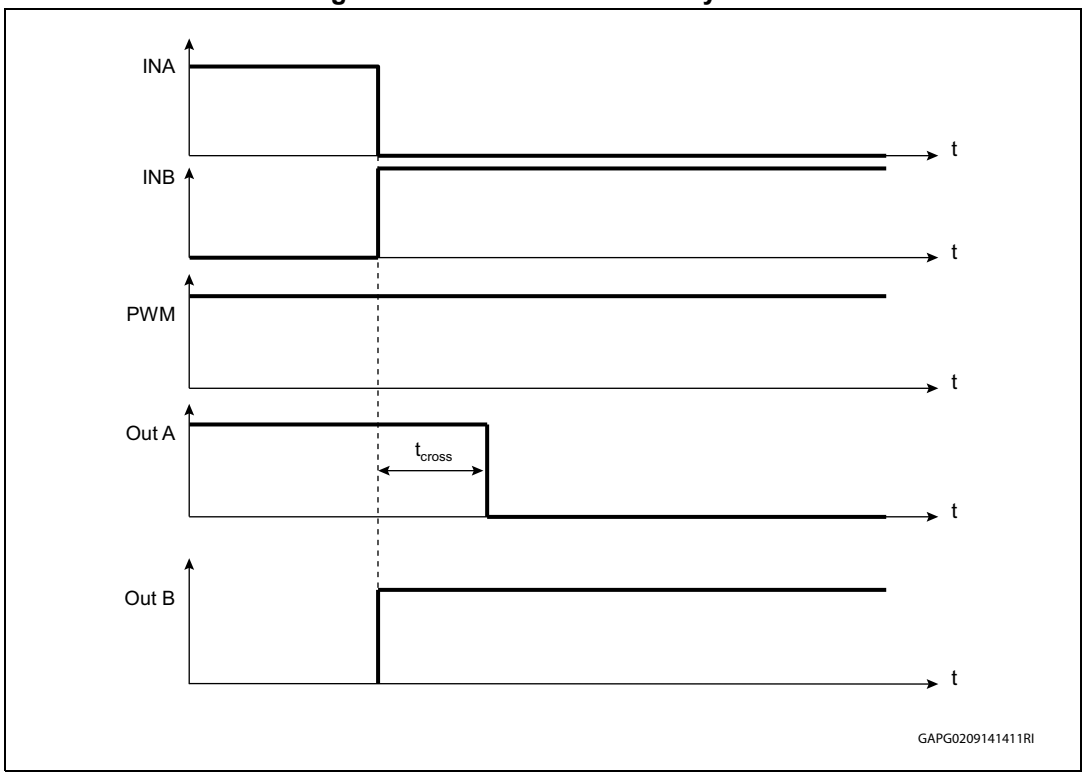
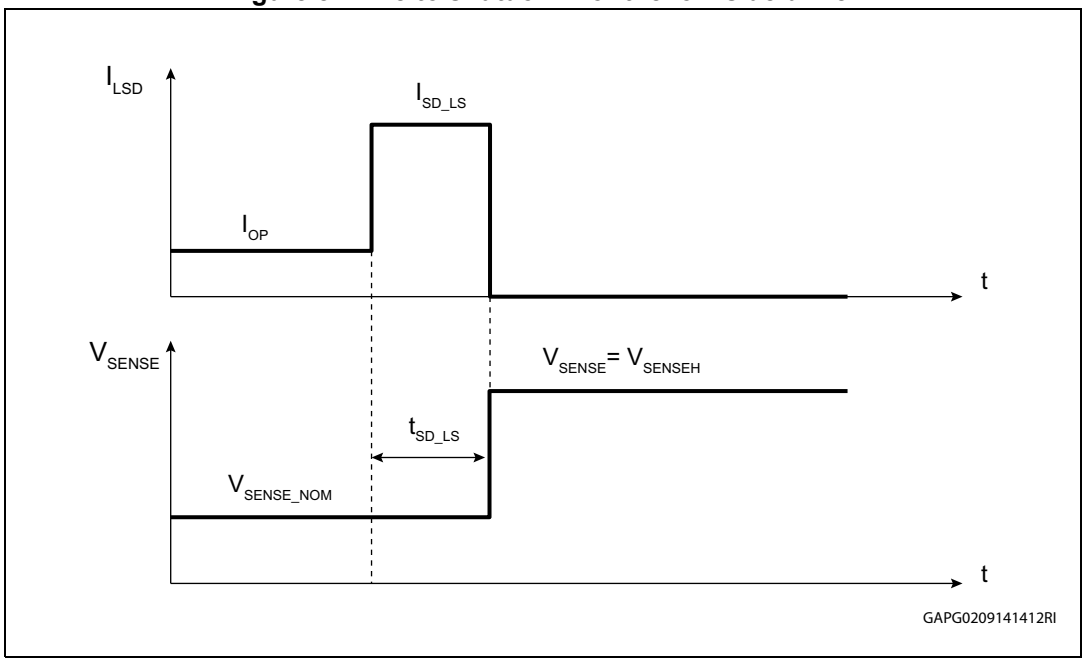
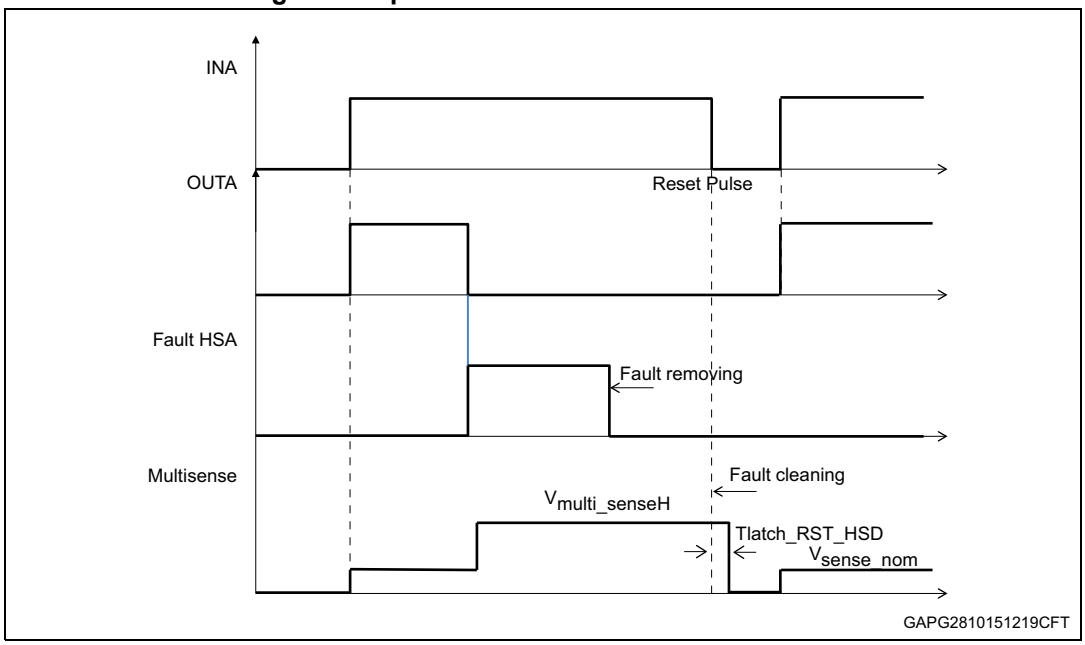


Figure 8. Time to shutdown for the low-side driver



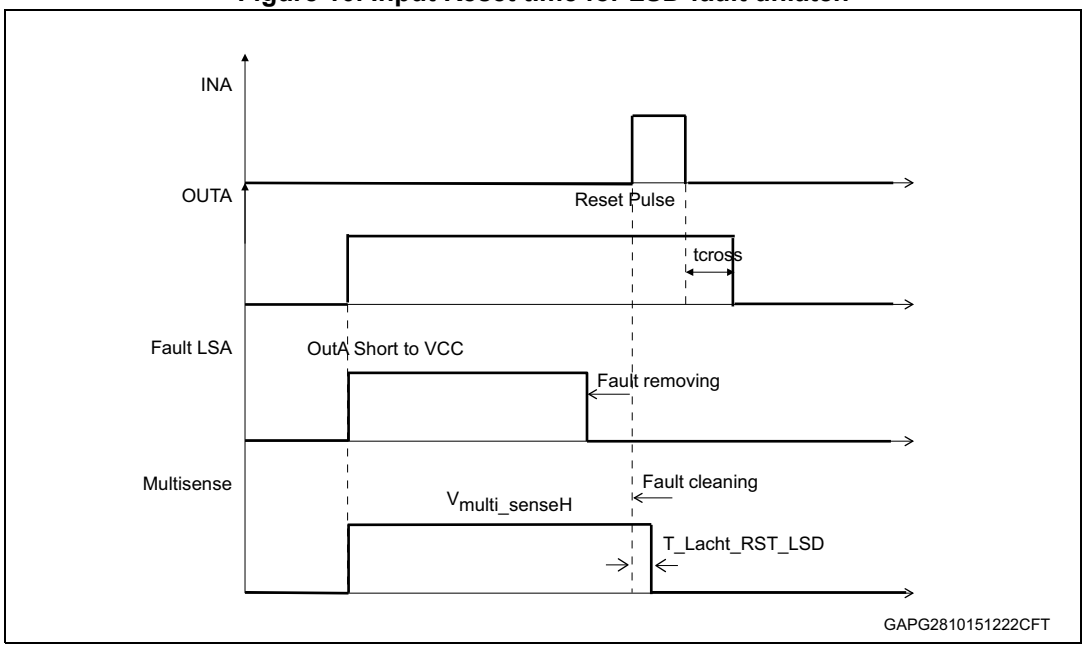
Note: MultiSense_EN=1

Figure 9. Input reset time for HSD-fault unlatch



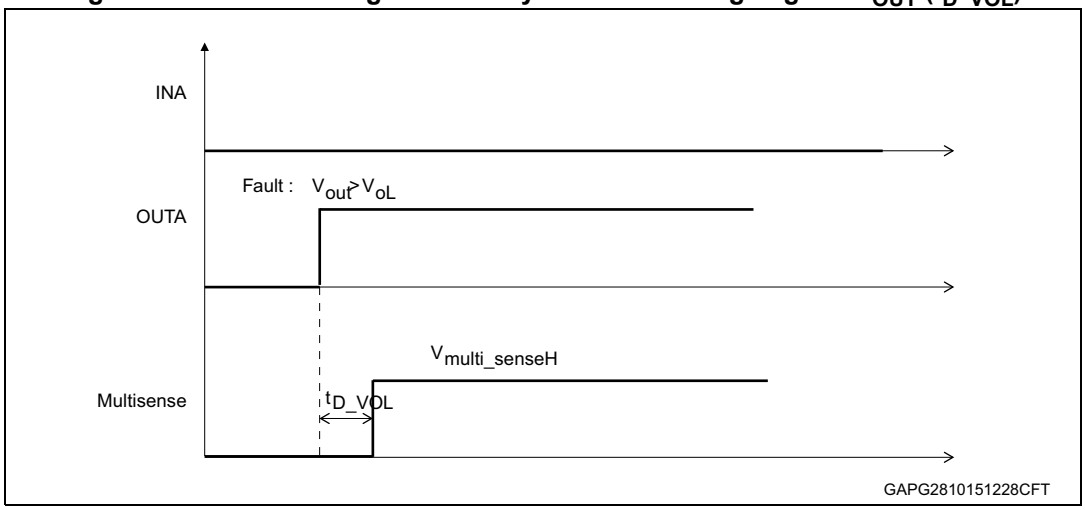
Note: MultiSense_EN=1

Figure 10. Input Reset time for LSD-fault unlatch



Note: MultiSense_EN = 1

Figure 11. OFF-state diagnostic delay time from rising edge of V_{OUT} (t_{D_VOL})



Note: MultiSense_EN = 1

Table 12. Operative condition - truth table

INA	INB	PWM	SEL0	SEL1	MS_EN	MS	HSA	LSA	HSB	LSB
0	0	1	0	0	1	High-Z	OFF	ON	OFF	ON
		1	1	0	1	High-Z	OFF	ON	OFF	ON
0	1	0	0	0	1	Current Monitoring HSB	OFF	OFF	ON	OFF
		1	0	0	1	Current Monitoring HSB	OFF	ON	ON	OFF
0	1	0	1	0	1	High-Z	OFF	OFF	ON	OFF
		1	1	0	1	High-Z	OFF	ON	ON	OFF
1	0	0	0	0	1	High-Z	ON	OFF	OFF	OFF
		1	0	0	1	High-Z	ON	OFF	OFF	ON
1	0	0	1	0	1	Current Monitoring HSA	ON	OFF	OFF	OFF
		1	1	0	1	Current Monitoring HSA	ON	OFF	OFF	ON
1	1	X	0	0	1	Current Monitoring HSB	ON	OFF	ON	OFF
			1	0	1	Current Monitoring HSA				
0	0	0	1	0	1	Off state diagnostic OUTA	OFF	OFF	OFF	OFF
0	0	0	0	0	1	Off state diagnostic OUTB	OFF	OFF	OFF	OFF
X(1)	X	X	0	1	1	Tchip Monitoring	—	—	—	—
X	X	X	1	1	1	Vcc Monitoring	—	—	—	—
X	X	X	X	X	0	High-Z(2)	—	—	—	—

1. X means that the value of the pin can be 0 or 1.
2. When IN_A = IN_B = PWM = SEL_0 = SEL_1 = MultiSense_EN = 0 device enters standby after T_{DSTBY}.

Table 13. On-state fault conditions - truth table

Digital Input pins(1)				MultiSense	Comment
INA	INB	PWM	SEL0		
0	0	1	0	VsenseH	LSB protection triggered; LSB latched off
0	0	1	1	VsenseH	LSA protection triggered; LSA latched off
0	1	X	0	VsenseH	HSB protection triggered; HSB latched off
0	1	1	1	VsenseH	LSA protection triggered; LSA latched off
1	0	1	0	VsenseH	LSB protection triggered; LSB latched off
1	0	X	1	VsenseH	HSA protection triggered; HSA latched off
1	1	X	0	VsenseH	HSB protection triggered; HSB latched off
1	1	X	1	VsenseH	HSA protection triggered; HSA latched off

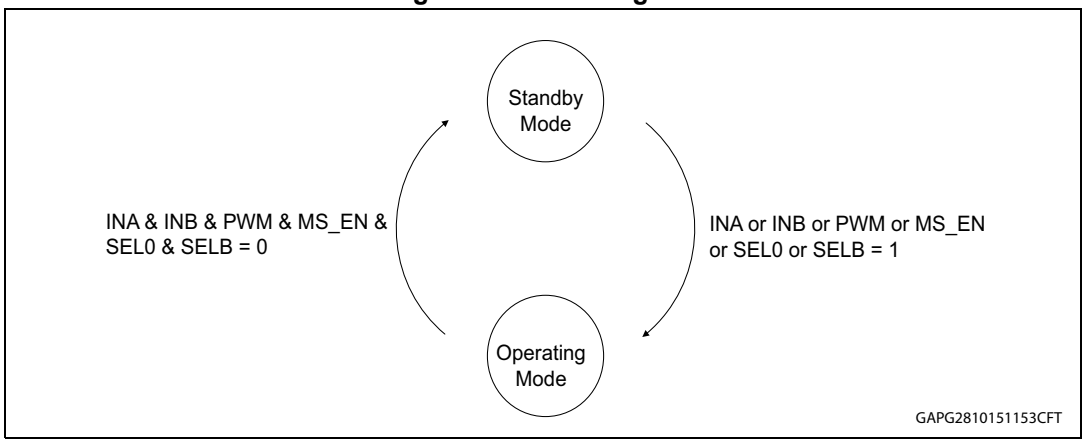
1. MultiSense_EN = 1 and SEL1 = 0 are mandatory for fault detection. Other logic combinations on digital input pins not reported on the above table do not allow to detect a latched-off channel.

Table 14. Off-state — truth table

INA	INB	SEL0	SEL1	PWM	OUTA	OUTB	MultiSense_EN	MultiSense	Description
Off-state diagnostic									
0	0	1	0	0	$V_{OUTA} > V_{OL}$	X	1	V_{SENSEH}	**Case 1: OUT_A shorted to V_{CC}** if no pull-up is applied. **Case 2: NO open-load** in full bridge configuration with an external pull-up on OUTB **Case 3: open-load** in half bridge configuration with an external pull-up on OUT_A (motor connected between Out and Ground)
					$V_{OUTA} < V_{OL}$	X	1	Hi-Z	**Case 1: open-load** in full Bridge configuration with an external pull-up on OUT_B **Case 2: NO open-load** in half Bridge configuration with external pull-up on OUT_A (motor connected between Out and Ground)
		0(1)(2)	0(1)(2)		X	$V_{OUTB} > V_{OL}$	1	V_{SENSEH}	**Case 1: OUT_B shorted to V_{CC}** if no pull-up is applied **Case 2: NO open-load** in full bridge configuration with external pull-up on OUT_A **Case 3: open-load** in half bridge configuration with external pull-up on OUT_B (motor connected between Out and Ground)
					X	$V_{OUTB} < V_{OL}$	1	Hi-Z	**Case1: open-load** in full Bridge configuration with an external pull-up on OUT_A **Case 2. NO open-load** in half Bridge configuration with external pull-up on OUT_B (motor connected between Out and Ground)

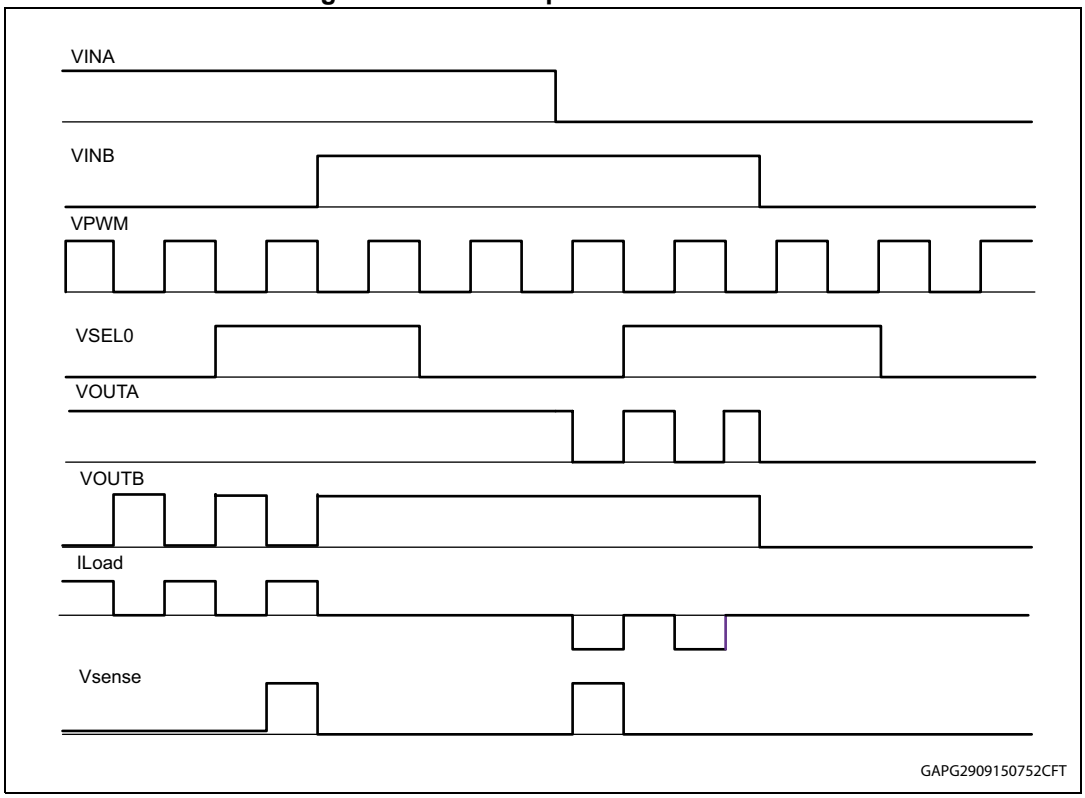
1. The device enters standby mode after $TD_{\_sdby}$.
2. To power on the device from standby, it is recommended to: toggle INA or INB or SEL0 or SEL1 from 0 to 1 first to come out from STBY mode; toggle PWM from 0 to 1 with a delay of 20 µs this avoids any overstress on the device in case of existing short-to-battery.

Figure 12. State diagram



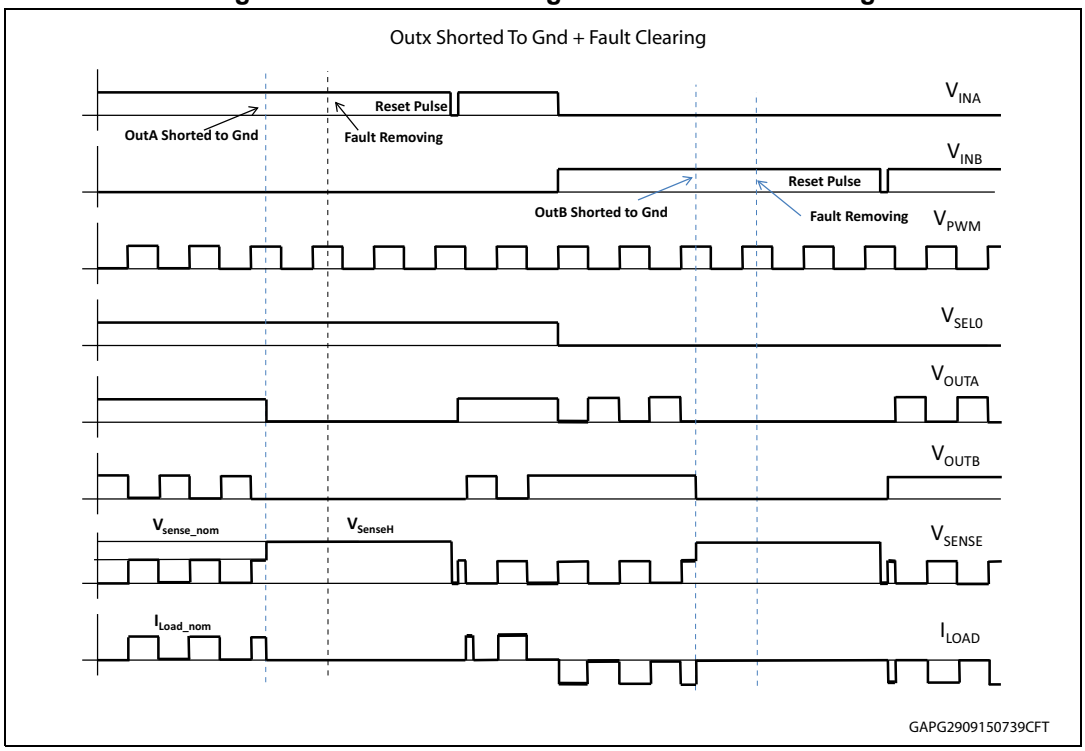
2.4 Waveforms

Figure 13. Normal operative conditions



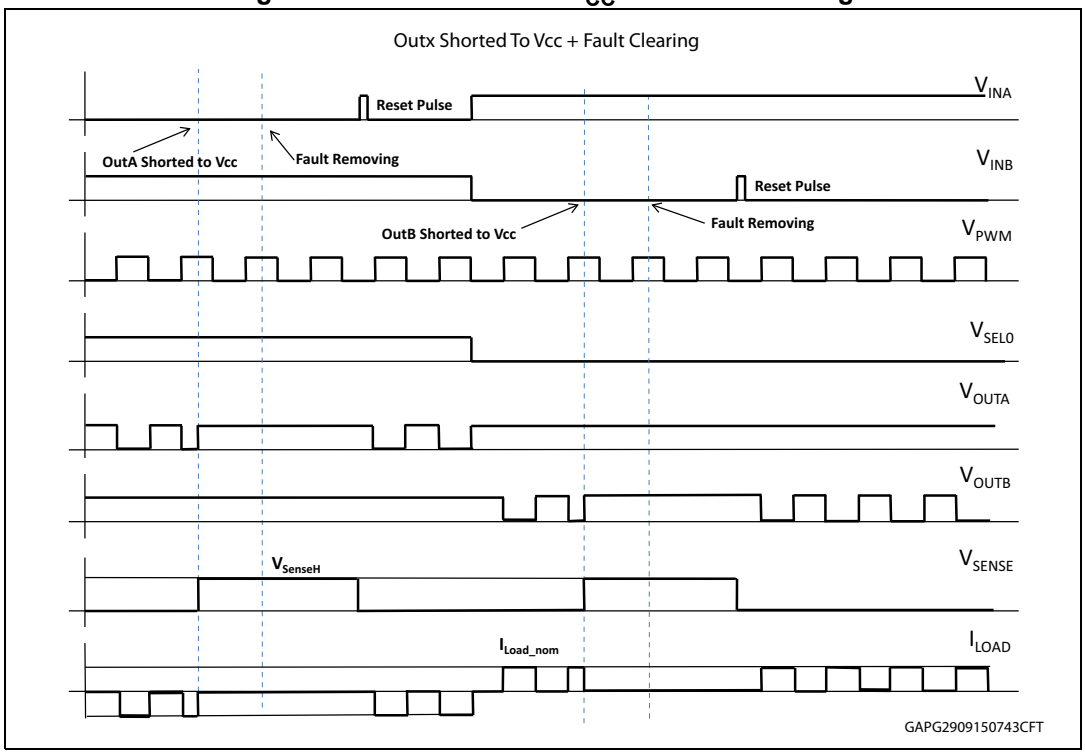
Note: MultiSense_EN = 1.

Figure 14. OUT shorted to ground and short clearing



Note: MultiSense_EN = 1

Figure 15. OUT shorted to V_{CC} and short clearing



Note: MultiSense_EN = 1

3 Protections

3.1 Power limitation (high-side driver)

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue. When Power Limitation is reached, The device enters in latch mode and generates the Fault Flag on Multisense=VsenseH when the faulty leg diagnostic is selected (please refer to *Table 13*).

3.2 Thermal shutdown (high-side and low-side)

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), the device enters in latch mode and generates the Fault Flag on Multisense = VsenseH (please refer to *Table 13*). The concerned high side can be switched ON again as soon as Tj drops below TTR_HSD, INX is set low for a duration > TLATCH_RST_HS and set high again.

3.3 Current limitation and over current detector

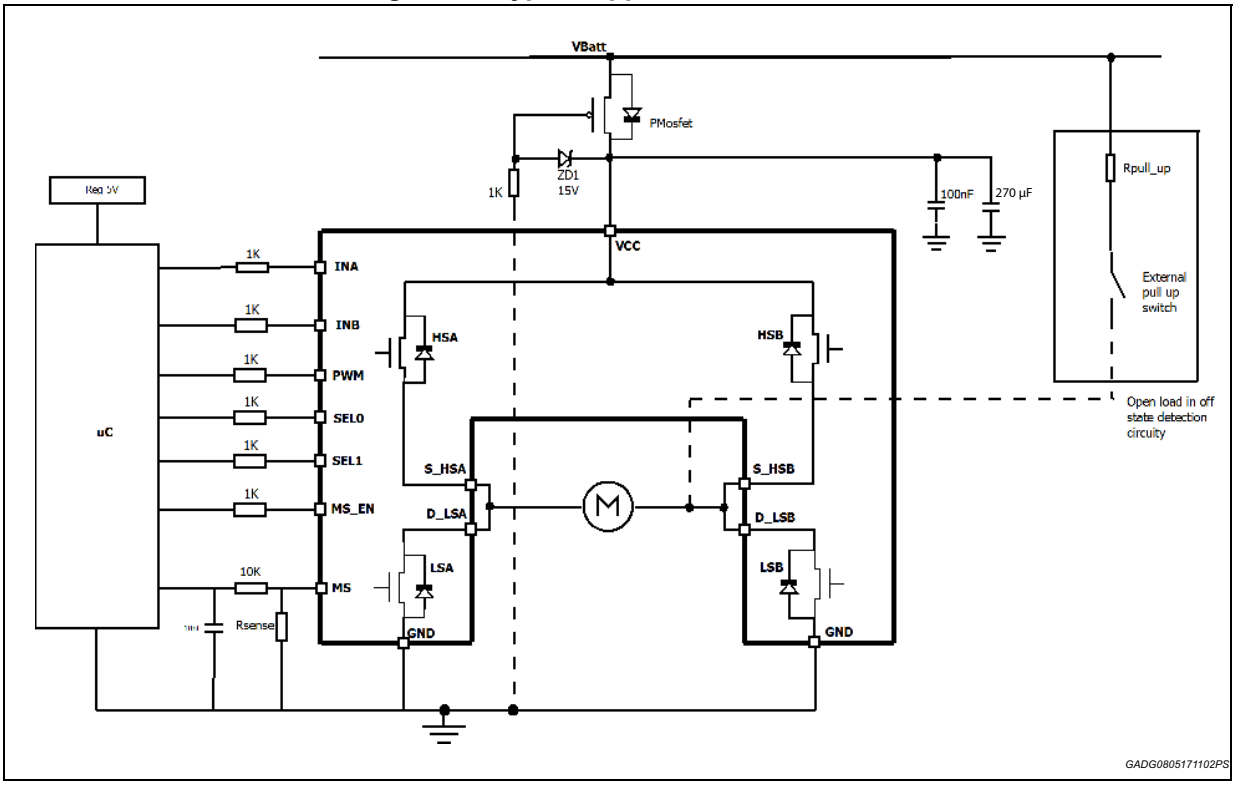
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. High-side current limitation: in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIM_HSD}, by operating the output power MOSFET in the active region.

Low-side overcurrent detector: this protection senses the current flowing in the low-side. If the current exceeds a safety level I_{SD_LS}, the device will switch off after a filtering time t_{sd_ld}.

In case of fault conditions caused by Power Limitation or overtemperature or open load/short to VCC in OFF state, the fault is indicated by the MultiSense pin being internally switched to a “current limited” voltage source pulled to level VSENSEH (please refer to *Table 13*).

4 Typical application schematic

Figure 16. Typical application schematic



Note: To protect the device against Battery disconnection with energized inductive load when the bridge driver goes into 3-state, suggested C(Vcc) is:

$$C(Vcc) = \frac{Emotor}{0.5 \cdot DVcc,\ max^2}$$

where:

Emotor = 19.4 mJ;

DVcc,max = Vcc_AMR - Vcc_max;

Vcc_AMR = 38 V;

Vcc_max = 26 V (Vcc at jump start);

C(Vcc) = 270 µF.

5 MultiSense operation

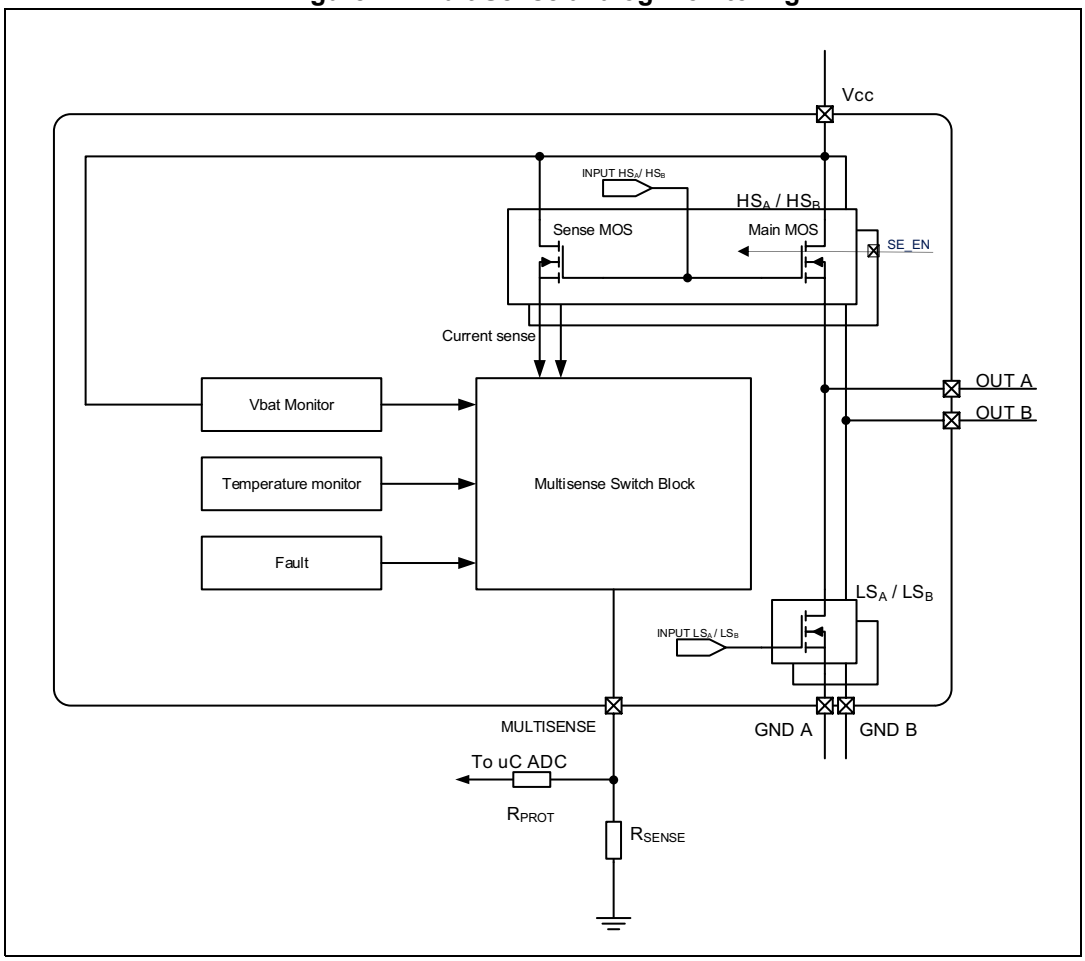
5.1 MultiSense analog monitoring

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage proportional to V_{CC}
- T_{CASE}: voltage proportional to chip temperature

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in MultiSense multiplexer addressing table.

Figure 17. MultiSense analog monitoring



5.2 Multisense diagnostics flag in fault conditions

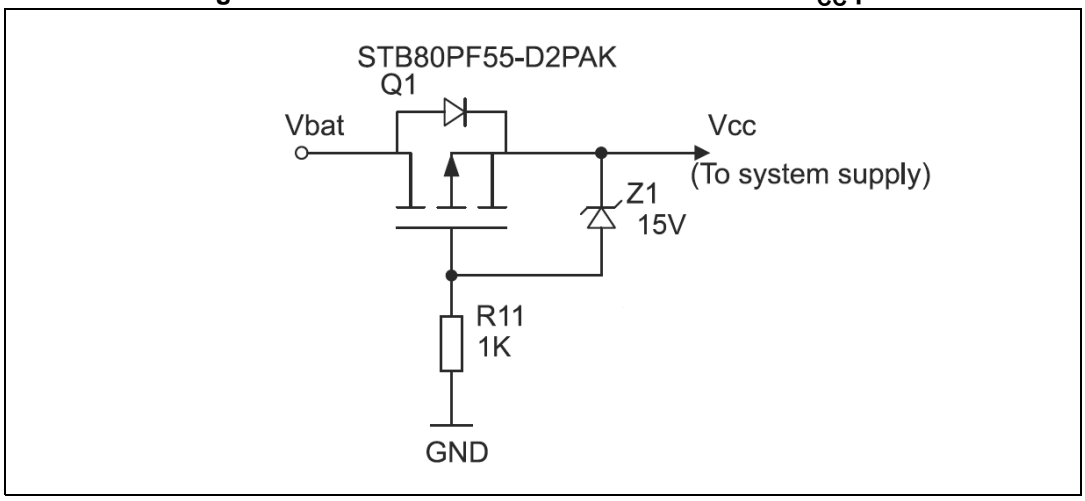
Multisense pin delivers fixed voltage (VSENSEH) with a certain current capability in case of:

- Fault condition on **activated high-side** (in ON state) triggered by Power Limitation, overtemperature protection, where MultiSense output is selected by SEL0 to high-side in fault state.
- Fault condition on a**ctivated low-side** (in ON state) triggered by overcurrent shutdown, overtemperature protection, where MultiSense output is selected by SEL0 to the same leg (of high-side) where low-side is in fault state.
- Short-circuit to VCC on **OUT in OFF state** (INA = INB = PWM = 0) selected by SEL0; Special care must be taken for the OUTB (SEL0 = 0) because the fixed voltage is available only before the device enters its stand-by mode after TD_STDBY (because all control signals are set to 0).
- In the configuration of **half bridge** (load connected between OUT and ground), when open-load appears on OUT in OFF state (selected by SEL0) with activated external pull-up resistor. Such condition causes an effect similar to the short circuit to V_{CC} on leg in OFF state (as mentioned in the above case, output voltage exceeds open-load threshold V_{OL}).

6 Reverse battery protection

The picture below shows a P-Channel MOSFET connected to the V_{CC} pin.

Figure 18. P-channel MOSFET connected to the V_{CC} pin



In normal operation the Zener diode plus the resistor generate a gate-source voltage enough to switch on the P-MOSFET. In case of reverse battery polarity: the P-Ch is switched off since its gate voltage is low. No current can flow in this state.

7 Open Load detection in off-state

The Open Load (OL) detection in off-state operates when output is deactivated (it means INA = INB = PWM = 0). Open load detection is performed by reading the MultiSense output. External (switched) pull-up resistor has to be used and dimensioned to pull output voltage above the maximum open load detection voltage (VOL MAX) when load is not connected.

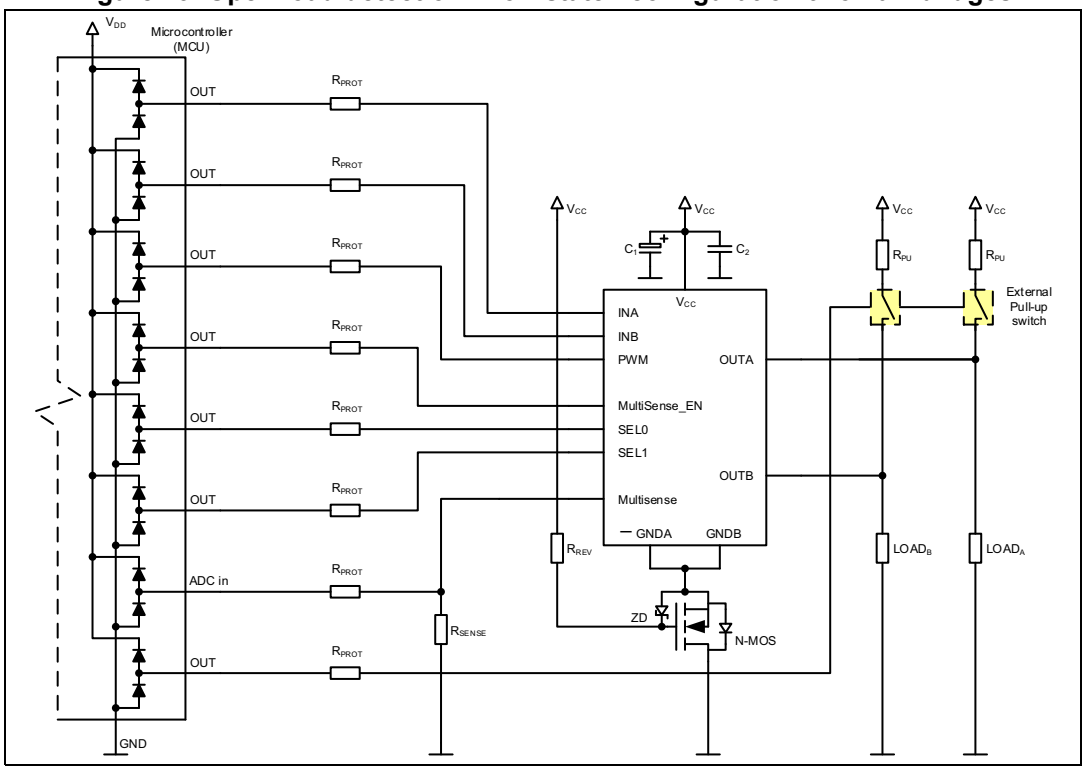
Possible conditions are specified in *Table 14*.

If pull up resistor is applied over switched circuitry, it allows to detect short to VCC from Open load.

Depending on the application setup, two cases can be applied:

- Half-bridge, with separate loads on OUTA and OUTB, open-load pull-up resistor R_{PU} is applied for each side; see an example in the figure below.

Figure 19. Open load detection in off-state - configuration two half-bridges

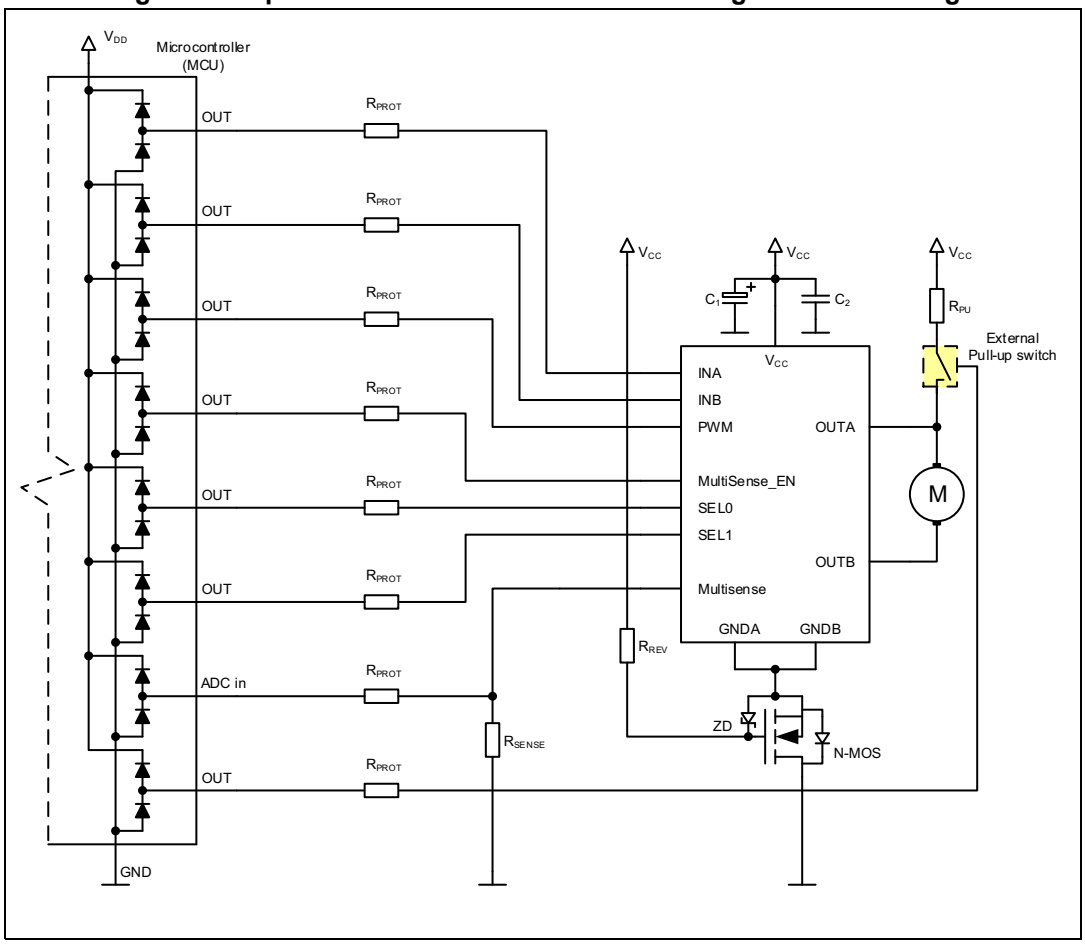


if the device is used in half bridge configuration, the R_{PU} value has to be:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{I_{L(off2)min[@VOLmax]}}$$

- Full bridge (load connected between OUTA and OUTB), only one pull-up resistor RPU is sufficient; see an example in the figure below.

Figure 20. Open load detection in off-state - configuration full-bridge



if the device is used in H-bridge configuration, the equation is:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{2xI_{L(off2)min[@VOLmax]}}$$

8 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the VCC pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 15: ISO 7637-2 electrical transient conduction along supply line*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), Section 4. The DUT is intended as the present device only, without components and accessed through VCC and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 15. ISO 7637-2 electrical transient conduction along supply line

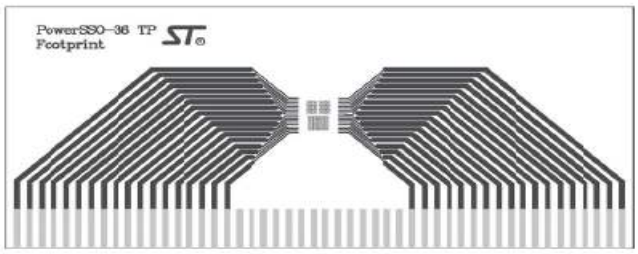
Test pulse 2011(E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle/pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S(1)		min.	max.	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4(2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		40 V	5 pulse	1 min		400 ms, 2 Ω

1. US is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E)
2. Test pulse from ISO 7637-2:2004(E)
3. With 40 V external suppressor referred to ground (-40 °C < T_J < 150 °C)

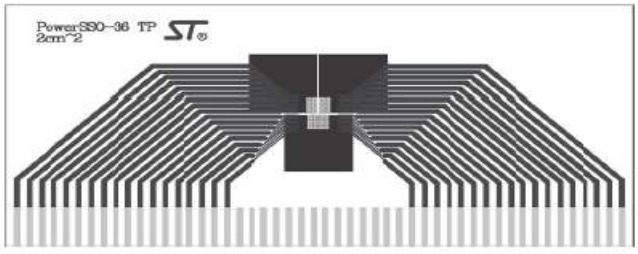
9 Package and PCB thermal data

9.1 PowerSSO-36 thermal data

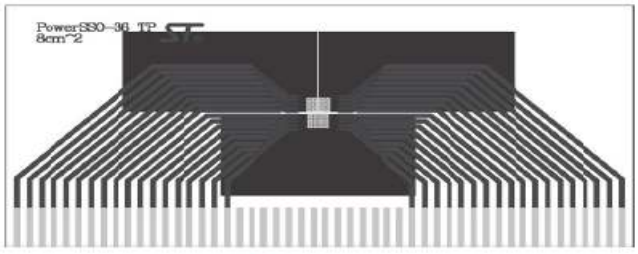
Figure 21. PowerSSO-36™ PC board



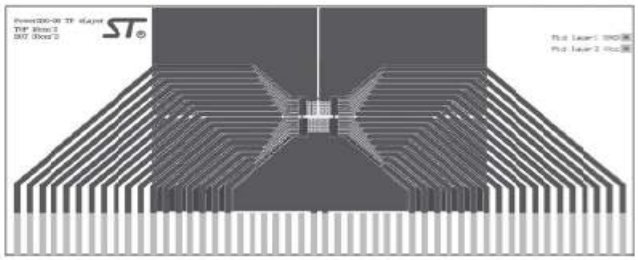
Double layers: footprint



Double layers: 2cm^2 of Cu



Double layers: 8cm^2 of Cu



Four layers: Cu on top layer: 16 cm^2; Cu on bottom layer: 32 cm^2; Cu on middle layer: total coverage

Note: Board finish thickness 1.6 mm +/- 10%, board double layers and four layers, board dimension 129x60, board material FR4, Cu thickness 0.070 mm (front and back side), thermal vias spaced on a 1.2 mm x 1.2 mm grid, Vias pad clearance thickness 0.2 mm, thermal via diameter 0.3 mm ± 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 4.1 mm x 6.5 mm.

Figure 22. Chipset configuration

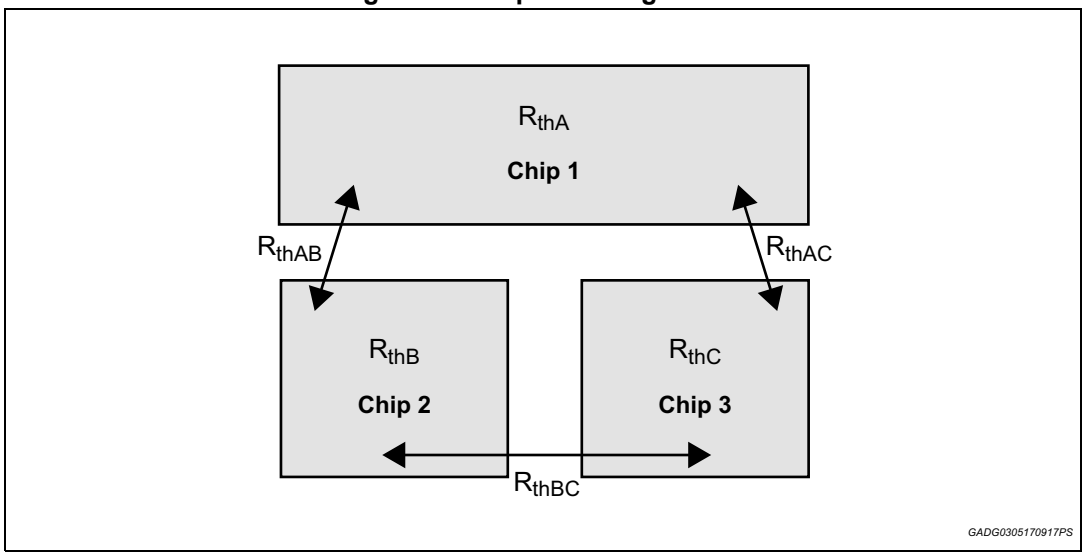


Figure 23. Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition

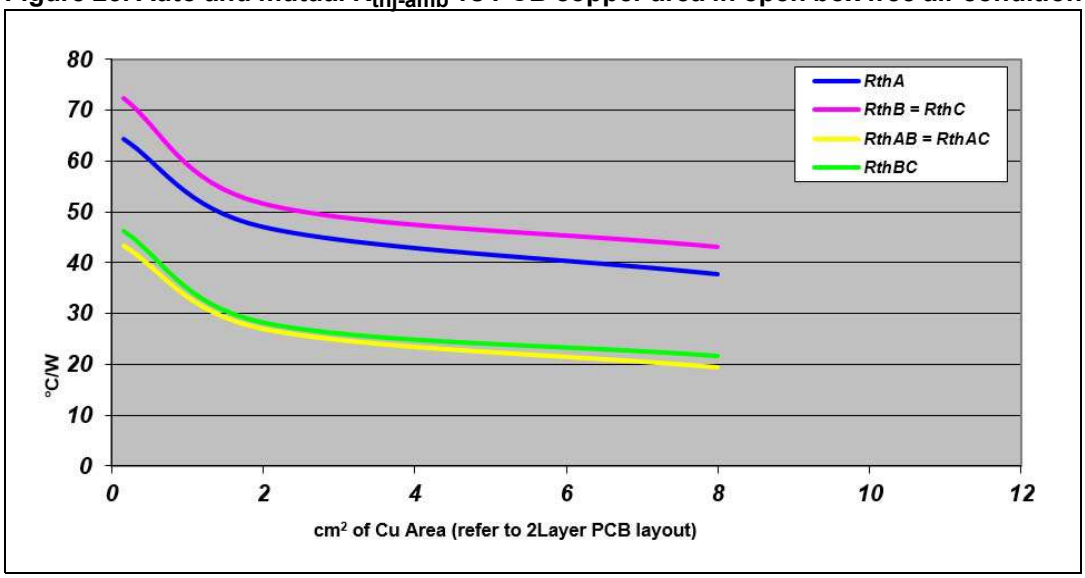


Table 16. Thermal resistance junction-ambient

	Footprint	Cu 2 cm^2	Cu 8 cm^2	4Layer
	°C/W			
RthA	64.4	47.1	37.8	24.1
RthB=RthC	72.4	51.7	43.2	30.2
RthAB=RthAC	43.3	26.8	19.3	10.8
RthBC	46.3	28.2	21.6	13.8

9.1.1 Thermal resistances definition (values according to the PCB heatsink area)

- RthHS = RthHSA = RthHSB = high-side chip thermal resistance junction to ambient (HSA or HSB in ON state)
- RthLS = RthLSA = RthLSB = low-side chip thermal resistance junction to ambient
- RthHSLS = RthHSALSB = RthHSBLSA = mutual thermal resistance junction to ambient between high-side and low-side chips
- RthLSLS = RthLSALSB = mutual thermal resistance junction to ambient between low-side chip.

Table 17. Thermal model for junction temperature calculation in steady-state conditions

Chip 1	Chip 2	Chip 3	Tjchip1	Tjchip2	Tjchip3
ON	OFF	ON	$P_{dchip1}.R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}$	$P_{dchip1}.R_{thAB} + P_{dchip3} . R_{thBC} + T_{amb}$	$P_{dchip1}.R_{thAC} + P_{dchip3} . R_{thC} + T_{amb}$
ON	ON	OFF	$P_{dchip1}.R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}$	$P_{dchip1}.R_{thAB} + P_{dchip2} . R_{thB} + T_{amb}$	$P_{dchip1}.R_{thAC} + P_{dchip2} . R_{thBC} + T_{amb}$
ON	OFF	OFF	$P_{dchip1}.R_{thA} + T_{amb}$	$P_{dchip1}.R_{thAB} + T_{amb}$	$P_{dchip1}.R_{thAC} + T_{amb}$
OFF	ON	ON	$(P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}$	$P_{dchip2}.R_{thB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$	$P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}$

9.2 Thermal Characterization during transients

$$T_{hs} = PD_{hs} \cdot Z_{hs} + Z_{hsls} \cdot (Pd_{lsA} + Pd_{lSB}) + T_{amb}$$

$$T_{lsA} = Pd_{lsA} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsB} \cdot Z_{lsls} + T_{amb}$$

$$T_{lsB} = Pd_{lsB} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsA} \cdot Z_{lsls} + T_{amb}$$

Figure 24. HSD thermal impedance junction ambient single pulse

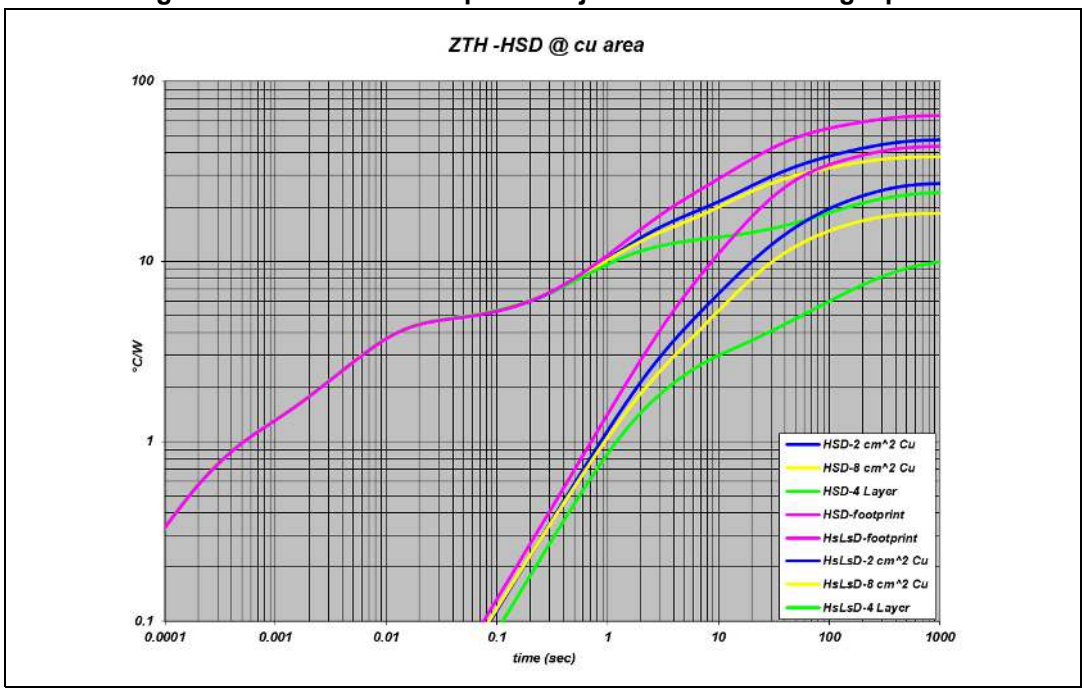


Figure 25. LSD thermal impedance junction ambient single pulse

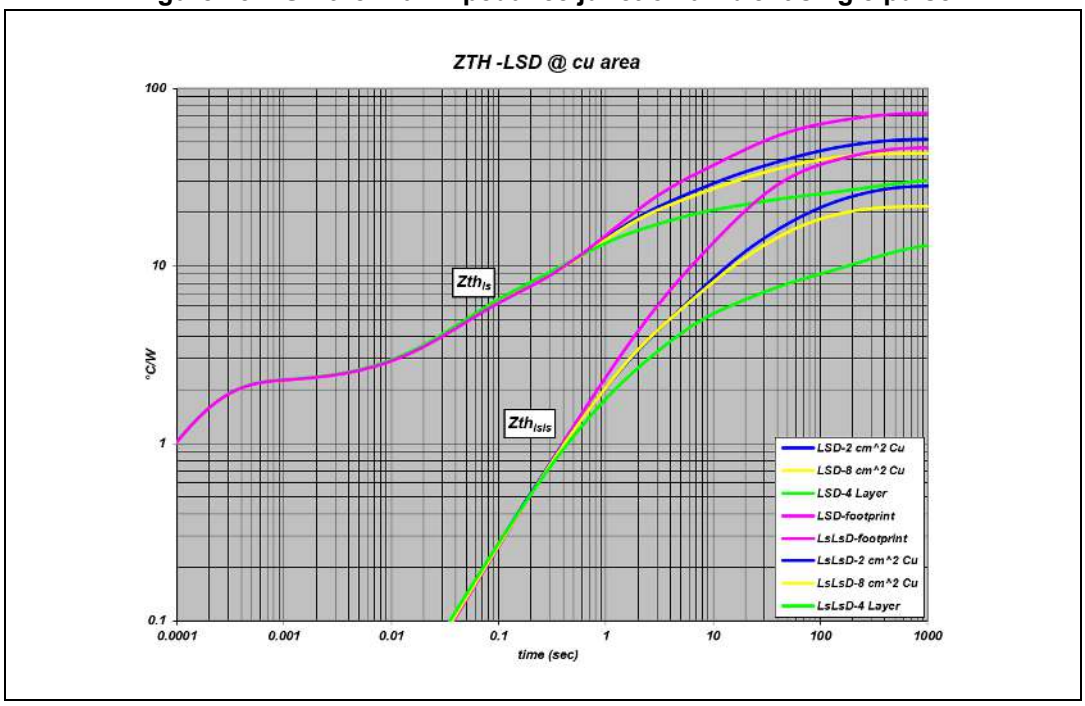


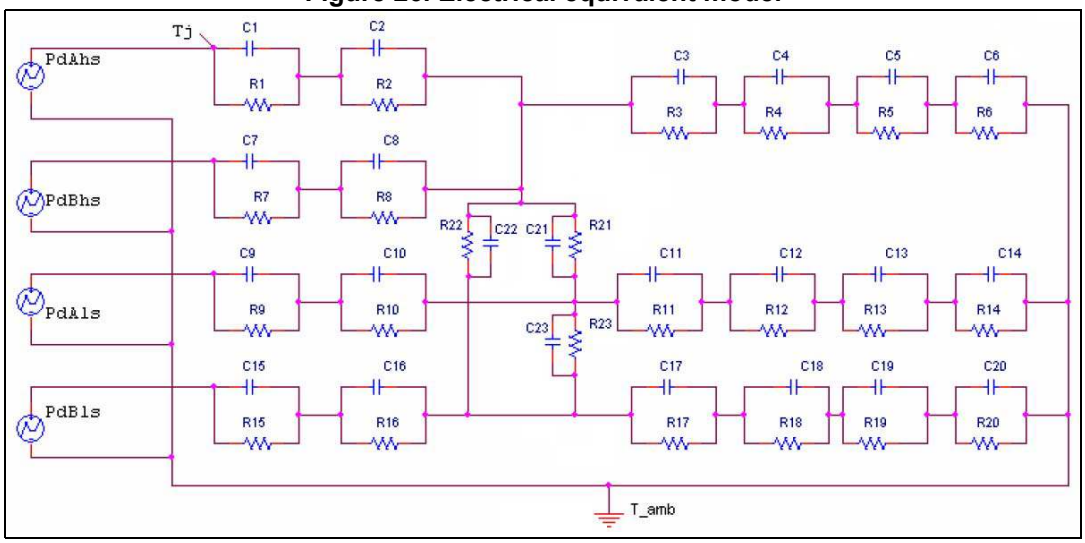
Table 18. Thermal parameters

Area/island (cm^2)	FP	2	8	4L
R1 (°C/W)	0.8			
R2 (°C/W)	3.7			
R3 (°C/W)	13	12	8.8	5.5
R4 (°C/W)	28	14	13	5
R5 (°C/W)	37	21	14	7
R6 (°C/W)	36	36	22	13
R7 (°C/W)	0.8			
R8 (°C/W)	3.7			
R9 (°C/W)	2.2			
R10 (°C/W)	3.2			
R11 (°C/W)	24	15.5	15.5	8.8
R12 (°C/W)	49	32	20	13
R13 (°C/W)	54	33	25	16
R14 (°C/W)	56	30	27	20
R15 (°C/W)	2.2			
R16 (°C/W)	3.2			
R17 (°C/W)	24	15.5	15.5	8.8
R18 (°C/W)	49	32	20	13
R19 (°C/W)	54	33	25	16
R20 (°C/W)	56	30	27	20
R21 (°C/W)	70	64	70	55
R22 (°C/W)	70	64	70	55
R23 (°C/W)	70	66	55	40
C1 (W·s/°C)	0.00028			
C2 (W·s/°C)	0.0018			
C3 (W·s/°C)	0.15	0.13	0.12	0.14
C4 (W·s/°C)	0.7	1.45	1.4	0.4
C5 (W·s/°C)	0.8	1.8	1.5	14
C6 (W·s/°C)	5	6	7.5	18
C7 (W·s/°C)	0.00028			
C8 (W·s/°C)	0.0018			
C9 (W·s/°C)	0.00007			
C10 (W·s/°C)	0.015			
C11 (W·s/°C)	0.08	0.07	0.07	0.06
C12 (W·s/°C)	0.35	0.3	0.37	0.26

Table 18. Thermal parameters (continued)

Area/island (cm^2)	FP	2	8	4L
C13 (W·s/°C)	0.55	1.4	1.2	1.4
C14 (W·s/°C)	2.8	5.4	3.2	20
C15 (W·s/°C)	0.00007			
C16 (W·s/°C)	0.015			
C17 (W·s/°C)	0.08	0.07	0.07	0.06
C18 (W·s/°C)	0.35	0.3	0.37	0.26
C19 (W·s/°C)	0.55	1.4	1.2	1.4
C20 (W·s/°C)	2.8	5.4	3.2	20
C21 (W·s/°C)	0.011	0.009	0.009	0.005
C22 (W·s/°C)	0.011	0.009	0.009	0.005
C23 (W·s/°C)	0.017	0.016	0.016	0.011

Figure 26. Electrical equivalent model



10 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

10.1 PowerSSO-36 TP package information

Figure 27. PowerSSO-36 TP package dimensions

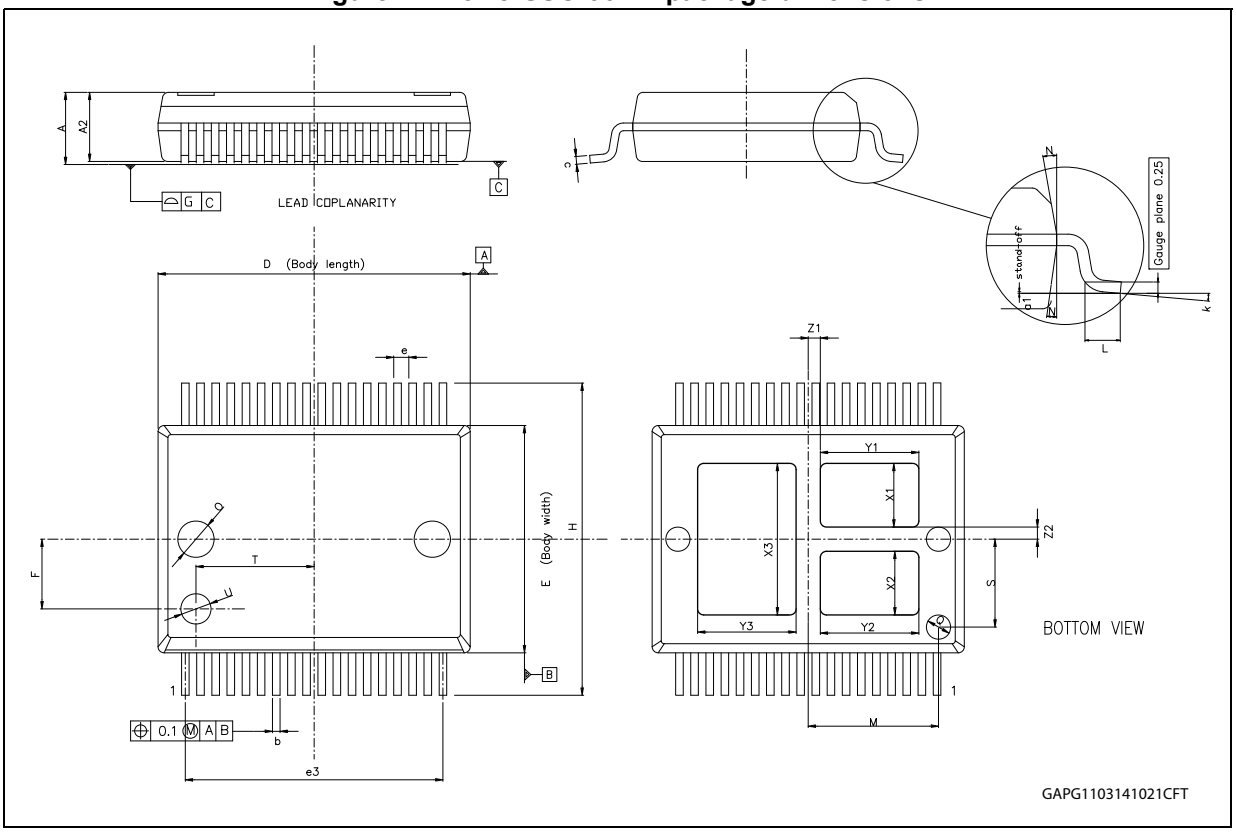
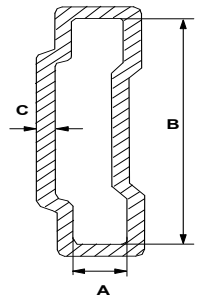


Table 19. PowerSSO-36 TP mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.1
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0 deg		8 deg
L	0.6		1
M		4.3	
N			10 deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X1	1.85		2.35
Y1	3		3.5
X2	1.85		2.35
Y2	3		3.5
X3	4.7		5.2
Y3	3		3.5
Z1		0.4	
Z2		0.4	

10.2 PowerSSO-36 TP packing information

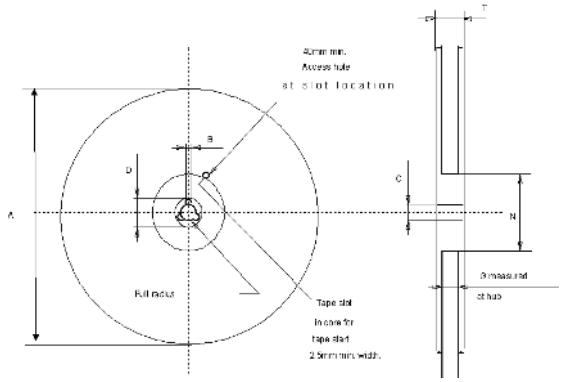
Figure 28. PowerSSO-36 TP tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 29. PowerSSO-36 TP tape and reel shipment (suffix "TR")



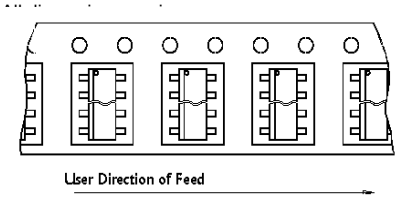
Reel dimensions

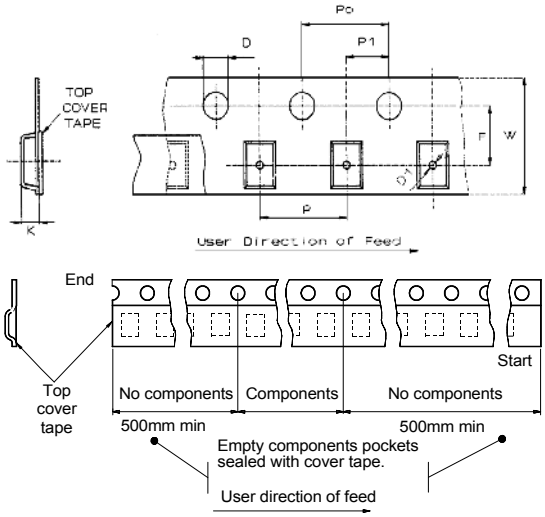
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

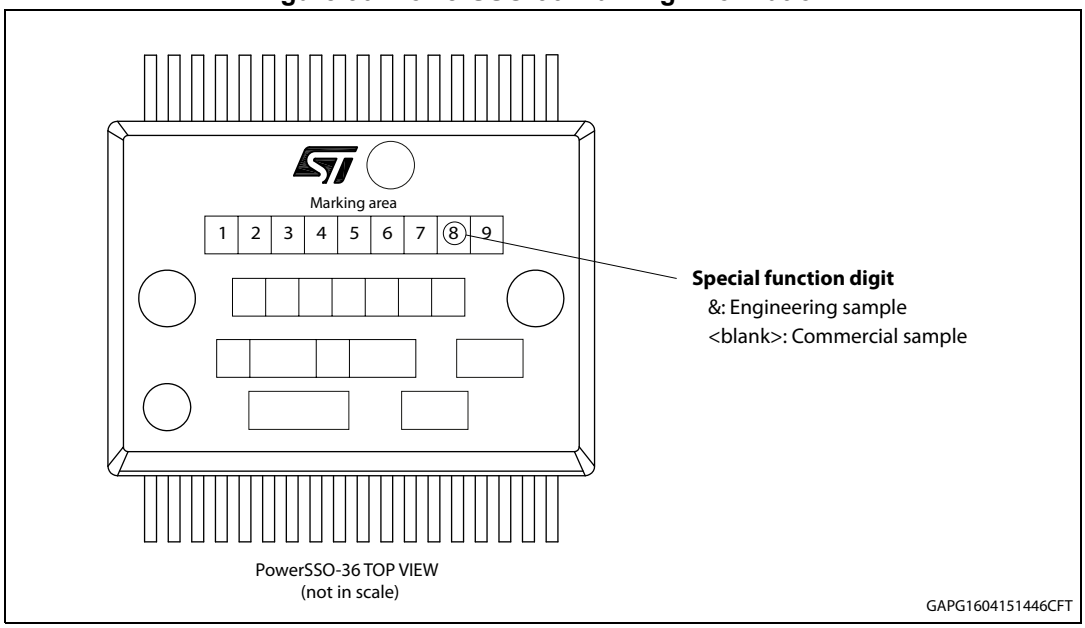
Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2





10.3 PowerSSO-36 marking information

Figure 30. PowerSSO-36 marking information



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

11 Order codes

Table 20. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36 TP	VNH7070AY	VNH7070AYTR

12 Revision history

Table 21. Document revision history

Date	Revision	Description of changes
13-Jul-2017	1	Initial release.
17-May-2018	2	Updated *Table 7: Power section*; *Table 10: Protections and diagnostics (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*; *Table 11: MultiSense (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*. Updated *Section 3.1: Power limitation (high-side driver)* and *Section 3.2: Thermal shutdown (high-side and low-side)*.
25-Jan-2019	3	Updated in cover page the first feature with “AEC-Q100 qualified”. Updated *Table 6*, *Table 11*, *Table 17* and *Figure 16*. Added *Figure 23*, *Table 16*, *Figure 24*, *Figure 25* and *Table 18*.
11-Feb-2019	4	In *Table 7* updated Typ. value for R_{ONHS} parameter. In *Table 11* updated Min. value for I_{OUT_SAT} parameter.
14-Mar-2019	5	Updated *Figure 23*, *Figure 24* and *Figure 25*. Updated *Table 16* and *Table 18*.