User's Guide

TPS65282 Buck Converter Evaluation Module User's Guide

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1 INTRODUCTION

This document presents the information required to operate the TPS65282 PMIC as well as the support documentation including schematic and bill of materials.

2 BACKGROUND

The TPS65282 PMIC contains a buck converter and two power switches. The buck converter is designed to provide an adjustable voltage with maximum 4-A continuous currents. The two power switches are designed to provide current limit at 75 mA - 2.7 A, while the current limit is available setting by external resistor.

As there are many possible options to set the converters, Table 2-1 presents the performance specification summary for the EVM.

Table 2-1. Summary of Performance

TEST CONDITIONS	PERFORMANCE
V_{IN} = 4.5 V to 18 V f_{SW} = 600 kHz (25°C ambient)	Buck : 5.0 V, up to 4 A Power Switch 1: 5.0 V, up to 2.7 A Power Switch 2: 5.0 V, up to 2.7 A

The evaluation module is designed to provide access to the features of the TPS65282. Some modifications can be made to this module to test performance at different input and output voltages, current and switching frequency. Please contact TI Field Applications Group for advice on these matters.

3 BOARD LAYOUT

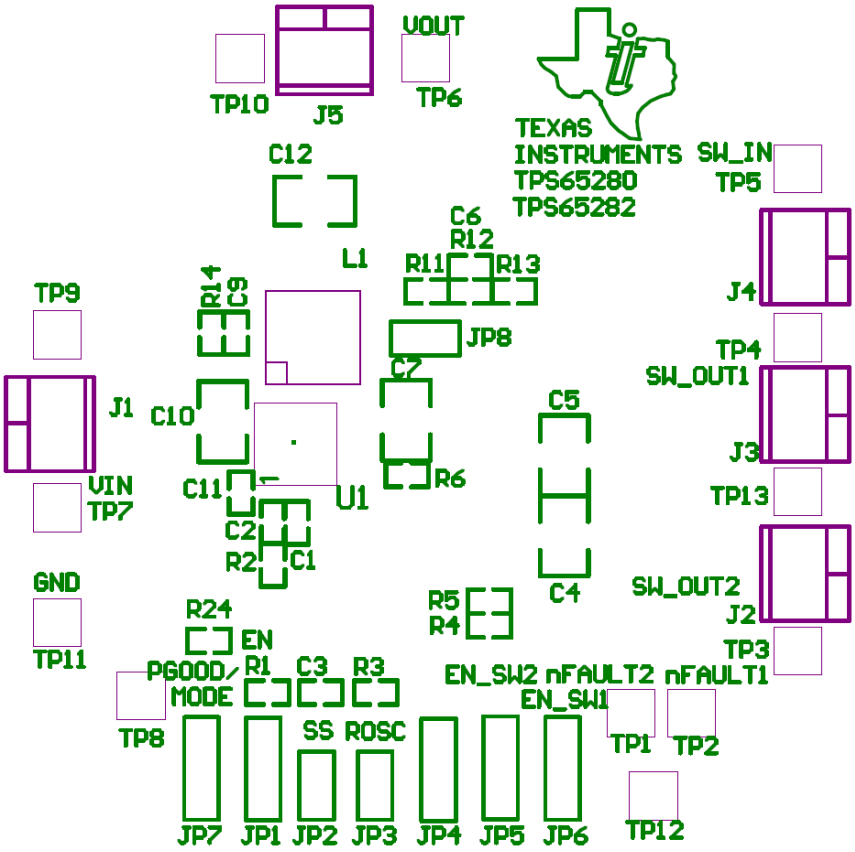

Figure 3-1. Placement (Top Layer)

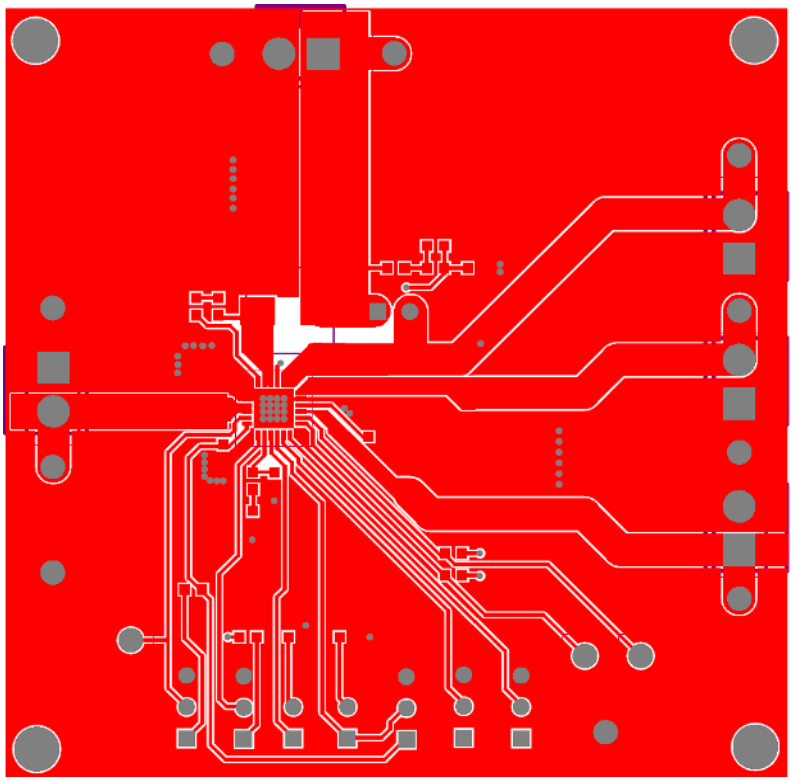

Figure 3-2. Board Layout (Top Layer)

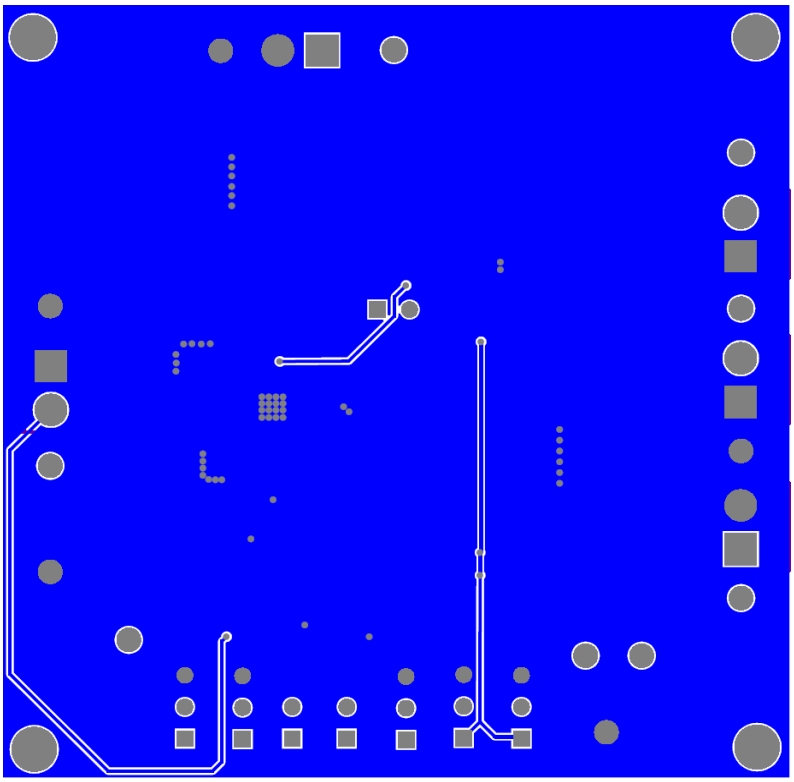

Figure 3-3. Board Layout (Bottom Layer – Ground Plane)

4 BENCH TEST SETUP CONDITIONS

4.1 Headers Description and Jumper Placement

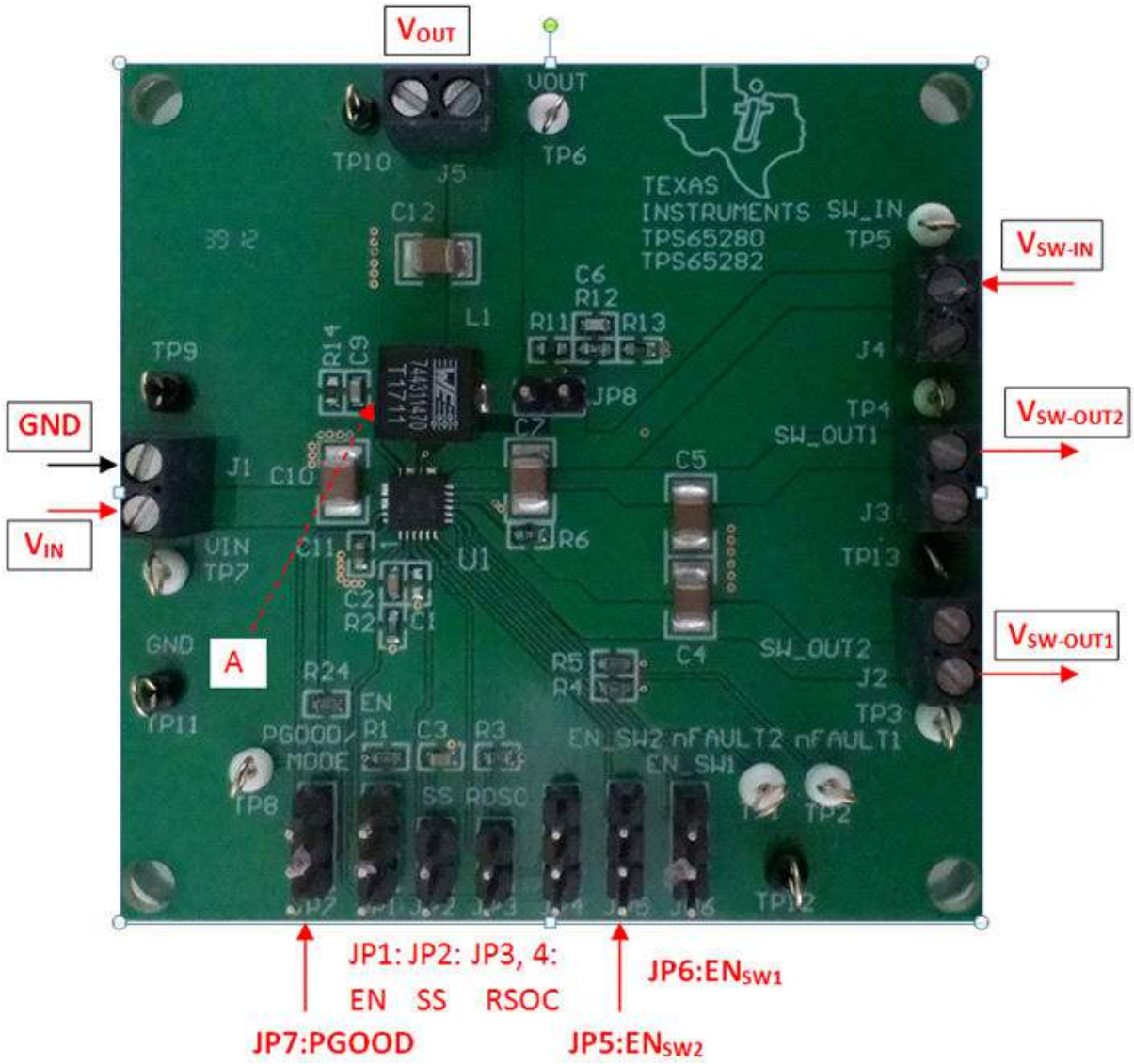

Figure 4-1. Headers Description and Jumper Placement

Test points:

1. LX of V_{OUT}

4.2 Jumpers and Switches

Table 4-1. Jumpers and Switches

NO.	FUNCTION	PLACEMENT	COMMENT
JP1	Buck Enable (EN)	Connect EN1 to GND to disable V_{OUT1}, connect EN1 to V_{IN} through a resistor to enable V_{OUT1}; Leave open to enable V_{OUT1}.	
JP2	Soft Start (SS)	Connect a external cap to this pin to program the soft start time of the buck converter; leave this pin open to have default 1-ms soft start time.	
JP3, 4	Switching Frequency	Connect a resistor to this pin to set the switching frequency; leave it open to set F_{SW} to 600 kHz; connect it to ground to set F_{SW} to 300 kHz.	
JP5	Switch 2 Enable	Connect this pin to high enable power switch 2; connect it to ground to disable power switch 2; Leave it open to enable power switch through internal 1.25-MΩ pull up resistor.	Not recommend to leave open
JP6	Switch 1 Enable	Connect this pin to high enable power switch 1; connect it to ground to disable power switch 1; Leave it open to enable power switch through internal 1.25-MΩ pull up resistor.	Not recommend to leave open
JP7	PGOOD Pull Up	Connect this pin to V7V force the PGOOD pull up. Connect this pin to GND there's no need to use this feature.	Not recommend to leave open

5 POWER-UP PROCEDURE

1. Apply 4.5 V - 18 V to JP7.
2. Toggle JP1 to enable V_{OUT1}.
3. Toggle JP6 and JP5 to enable switch 1 and switch 2.
4. Apply load to the output connectors.

6 SCHEMATIC AND BILL OF MATERIALS

The following pages contain the schematic and BOM.

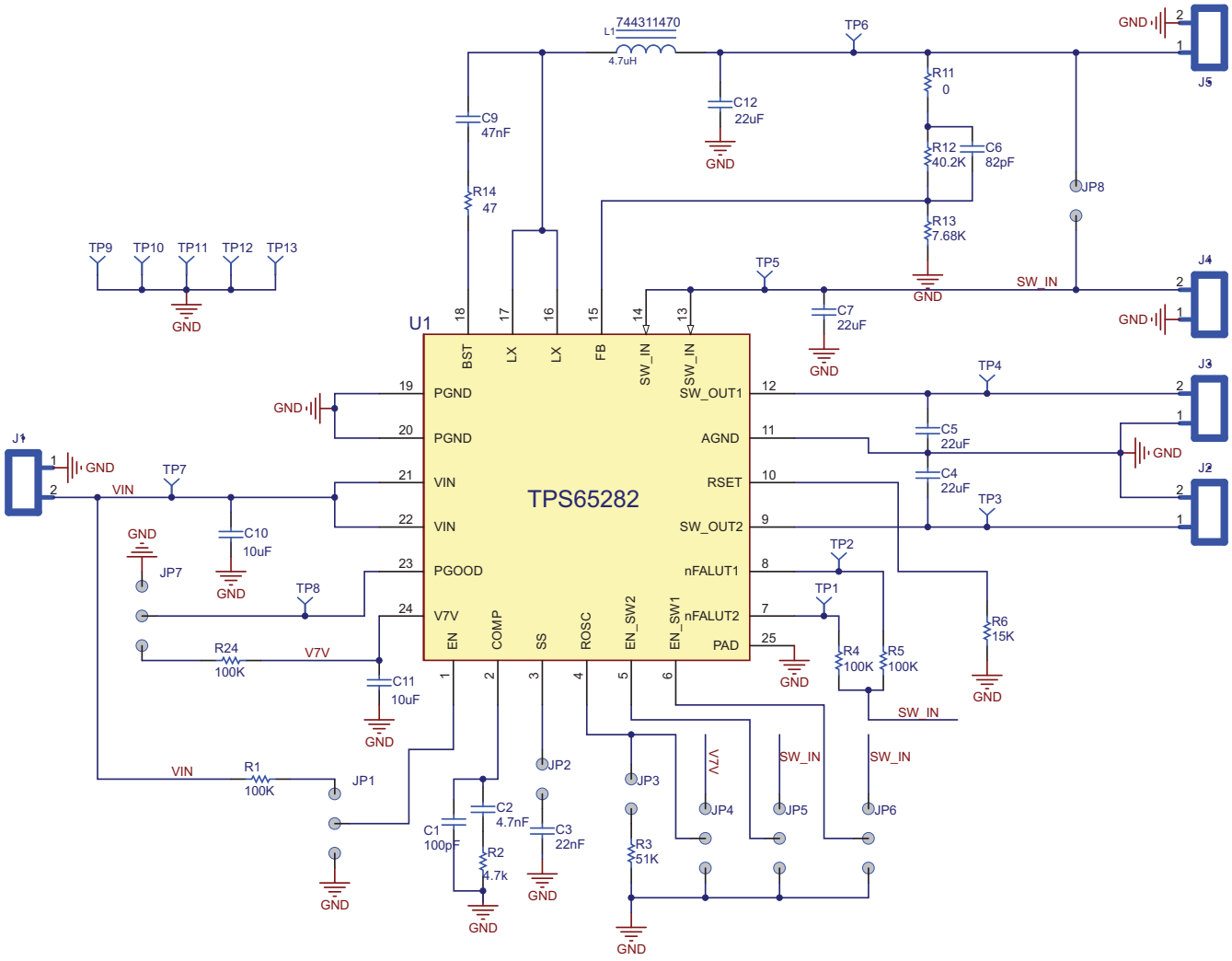

Figure 6-1. TPS65282EVM Schematic

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2013) to Revision A (May 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265