Data Sheet, Rev. 1.51, Nov. 2005

AN985B/BX

CardBus-to-Ethernet LAN Controller

Communications

Never stop thinking.

Edition 2005-11-30

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Previous Version:

Page/Date	Subjects (major changes since last revision)
2005-09-13	Rev. 1.51: when changed to the new Infineon format
2005-11-30	Minor change. Included Green package information

Trademarks

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1 General Description

The AN985B/BX is a high performance CARDBUS Fast Ethernet controller with a integrated physical layer interface for 10BASE-T and 100BASE-TX applications. The AN983B/BX is the environmentally friendly “green” package version.

The AN985B/BX was designed with 0.25um CMOS technology to provide glueless 32-bit bus master interface for CARDBUS, boot ROM interface and CSMA/CD protocol for Fast Ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detections.

The AN985B/BX provides both half-duplex and full-duplex operations, as well as support for full-duplex flow control.

It provides long FIFO buffers for transmission and reception, and an early interrupt mechanism to enhance performance.

The AN985B/BX also supports ACPI and CARDBUS compliant power management functions and Magic Packet wake-up event.

2 System Block Diagram

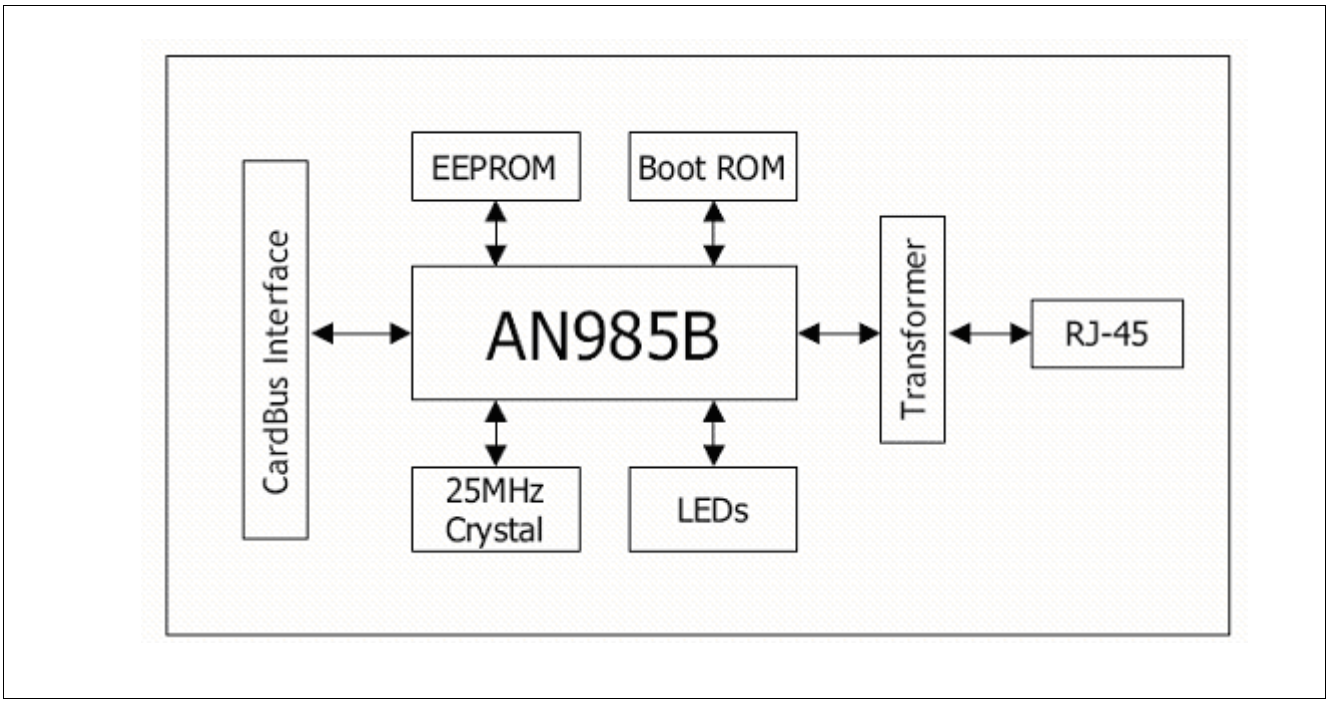


Figure 1 System Diagram of the AN985B/BX

3 Features

Industry standard

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Supports for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- CARDBUS Interface
- ACPI and PCI power management Ver.1.1 compliant

- Supports PC98 wake on LAN

FIFO

- Provides two independent long FIFOs with 2k bytes each for transmission and reception
- Pre-fetch up to two transmit packets to minimize inter frame gap (IFG) to 0.96 μs
- Retransmit collided packet without reload from host memory within 64 bytes
- Automatically retransmit FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet

CARDBUS I/F

- Provides 32-bit PCI bus master data transfer
- Supports CARDBUS clock with frequency from 0 Hz to 33 MHz
- Supports network operation with CARDBUS system clock from 20 MHz to 33 MHz
- Performance meter, CARDBUS bus master latency timer, for tuning the threshold to enhance performance
- Burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization
- Memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- Supports big or little endian byte ordering

EEPROM/Boot ROM I/F

- Write-able Flash ROM and EPROM as boot ROM with size up to 128 KB
- CARDBUS to access boot ROM by byte, word, or double word
- Re-write Flash boot ROM through I/O port by programming register
- Serial interface for read/write 93C46/66 EEPROM
- Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C46/66 after PCI reset de-asserted in PCI environment
- CIS data is recalled from 93C66 to AN985B/BX PC internal SRAM to speed up CIS access in CARDBUS environment

MAC/Physical

- Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- Full -duplex operation on both 100 Mbit/s and 10 Mbit/s modes
- Auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbit/s
- Transmits wave-shaper, receive filters, and adaptive equalizer
- MLT-3 transceivers with DC restoration for Base-line wander compensation
- MAC and Transceiver (TXCVR) loop-back modes for diagnostic
- Built in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- External transmitting transformer with turn ratio 1:1
- External receiving transformer with turn ratio 1:1

LED Display

- 3 LEDs display scheme provided:
  - 100 Mbit/s (on) or Speed 10 (off)
  - Link (keeps on when link ok) or Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)
- 4 LEDs displayed scheme provided:
  - 100 Mbit/s and Link (keep on when link and 100 Mbit/s)
  - 10 Mbit/s and Link (keep on when link and 10 Mbit/s)
  - Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

Miscellaneous

- 128-pin QFP package for CARDBUS interface.

4 Block Diagram

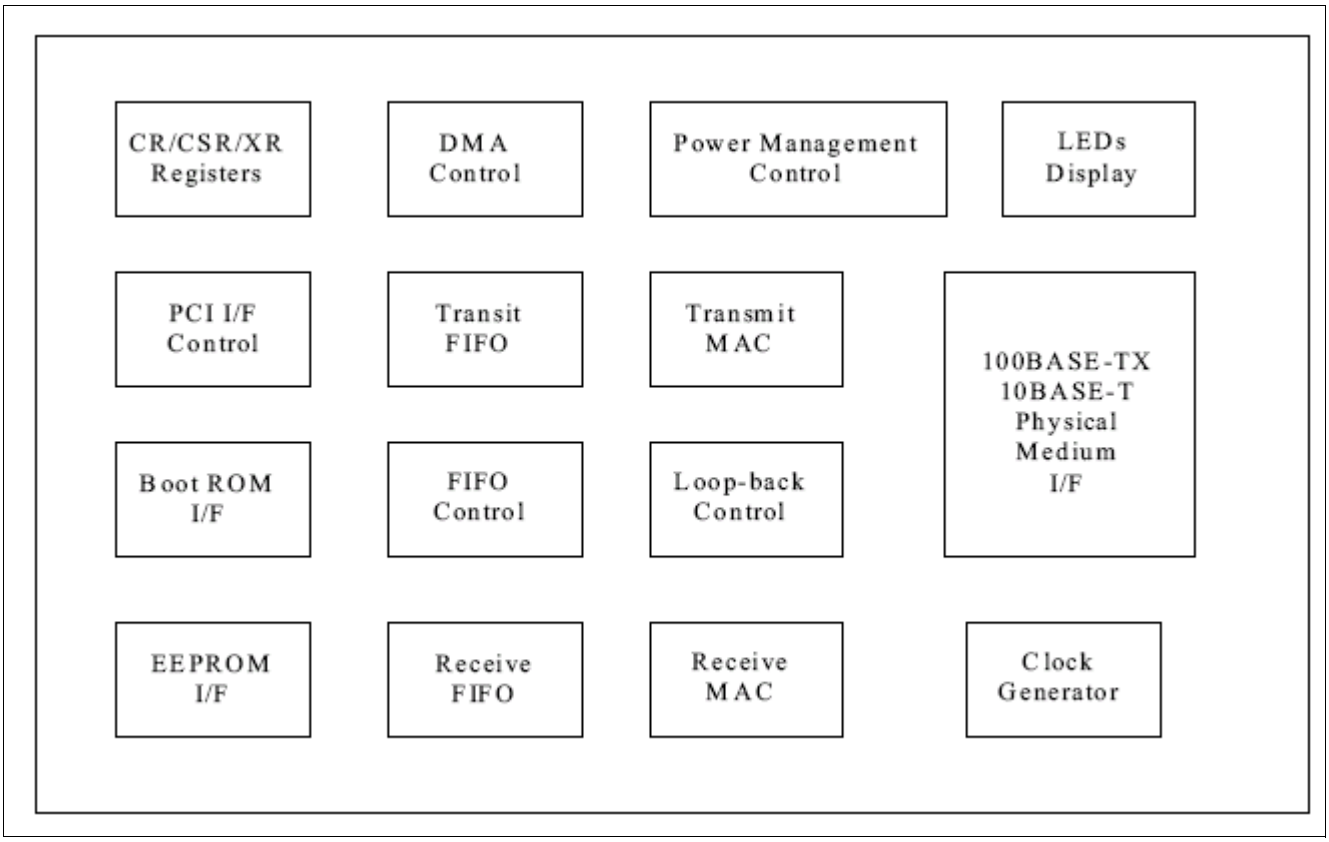


Figure 2 Block Diagram of the AN985B/BX

5 Pin Assignment Diagram

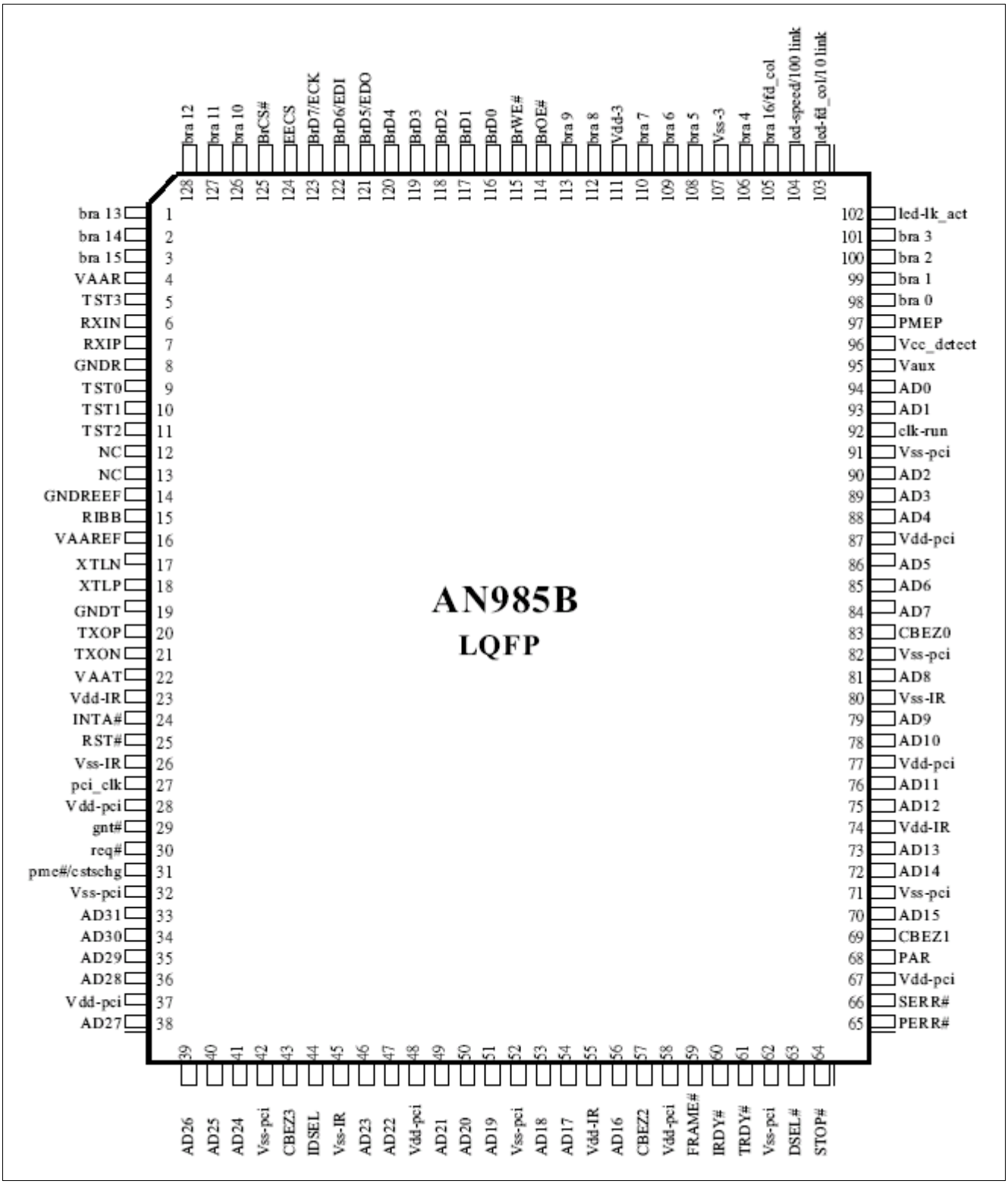


Figure 3 Pin Assignment (top view)

5.1 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

6 Pin Description

Table 3 Pin Definitions and Functions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
PCI Interface				
24	INTA#	O/D		**CARDBUS Interrupt Request** AN985B/BX asserts this signal when one of the interrupt events occurs.
25	RST#	I		**CARDBUS Signal to Initialize the AN985B/BX** The active reset signal should be sustained for at least 100μs to guarantee that the AN985B/BX has completed the initializing activity. During the reset period, all the output pins of AN985B/BX will be set to tri-state and all the O/D pins are floated.
27	CLK	I		**This CARDBUS Clock Inputs to AN985B/BX for CARDBUS Relative Circuits as the Synchronized Timing Base with CARDBUS** The Bus signals are recognized on the rising edge of CARDBUS-CLK. In order to let the network operate properly, the frequency range of the CARDBUS-CLK is limited to between 20 MHz and 33 MHz when the network is operating.
29	GNT#	I		**CARDBUS Bus Granted** This signal indicates that the bus request of AN985B/BX has been accepted.
30	REQ#	O		**CARDBUS Bus Request** Bus master device wants to get bus access right
31	PME#/CSTSCHG	I/O		**Power Management Event** The Power Management Event signal is an open drain, active low signal for CARDBUS(PME#). When WOL-bit 18 of CSR is set into “1”, this means that the AN985B/BX is set into Wake On LAN mode. In this mode, when the AN985B/BX receives a Magic Packet frame from network then the AN985B/BX will active this signal too. In the Wake On LAN mode, when LWS-bit (bit 17) of CSR18 is set to “1” this means the LAN-WAKE signal is a HP-style signal, otherwise it is an IBM-style signal.

Table 3 Pin Definitions and Functions (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
33	AD-31	I/O		**Multiplexed Address Data Pin of CARDBUS Bus**
34	AD-30			
35	AD-29			
36	AD-28			
38	AD-27			
39	AD-26			
40	AD-25			
41	AD-24			
46	AD-23			
47	AD-22			
49	AD-21			
50	AD-20			
51	AD-19			
53	AD-18			
54	AD-17			
56	AD-16			
70	AD-15			
72	AD-14			
73	AD-13			
75	AD-12			
76	AD-11			
78	AD-10			
79	AD-9			
81	AD-8			
84	AD-7			
85	AD-6			
86	AD-5			
88	AD-4			
89	AD-3			
90	AD-2			
93	AD-1			
94	AD-0			
43	C-BEB3	I/O		**Bus Command and Byte Enable**
57	C-BEB2			
69	C-BEB1			
83	C-BEB0			
44	IDSEL	I		**Initialization Device Select** This signal is asserted when the host issues the configuration cycles to the AN985B/BX.
59	FRAME#	I/O		**Begin and Duration of Bus Access** Driven by master device

Table 3 Pin Definitions and Functions (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
60	IRDY#	I/O		**Master Device is Ready to Data Transaction**
61	TRDY#	I/O		**Slave Device is Ready to Data Transaction**
63	DEVSEL#	I/O		**Device Select** Device select, target is driving to indicate the address is decoded
64	STOP#	I/O		**Stop the Current Transaction** Target device requests the master device to stop the current transaction
65	PERR#	I/O		**Data Parity Error** Data parity error is detected, driven by the agent receiving data
66	SERR#	O/D		**Address Parity Error**
68	PAR	I/O		**Parity** Parity, even parity (AD [31:0] + C/BE [3:0]); master drives par for address and write data phas; target drives par for read data phase
92	Clk-run	I/O, O/D		**Clock Run for CARDBUS System** In the normal operation situation, Host should assert this signal to indicate to AN985B/BX about the normal situation. On the other hand, when Host deasserts this signal the clock is going down to a non-operating frequency. When AN985B/BX recognizes the deasserted status of clk-run, then it will assert clk-run to request Host to maintain the normal clock operation. When the clk-run function is disabled then the AN985B/BX will set clk-run in tri-state.
BOOTROM/EEPROM Interface				
98	BrA0	I/O		**ROM Data Bus** Provides up to 128kB EPROM or Flash-ROM application space.
99	BrA1			
100	BrA2			
101	BrA3			
106	BrA4			
108	BrA5			
109	BrA6			
110	BrA7			
112	BrA8			
113	BrA9			
126	BrA10			
127	BrA11			
128	BrA12			
1	BrA13			
2	BrA14			
3	BrA15			
105	BrA16			

Table 3 Pin Definitions and Functions (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
116	BrD0	O		**BootROM Data Bus Bit (0~7)** Inputs/Output data for AN985B/BX EDO: Data Output of serial EEPROM EDI: Data Input of serial EEPROM ECK: Clock input of serial EEPROM The AN985B/BX outputs clock signal to EEPROM.
117	BrD1			
118	BrD2			
119	BrD3			
120	BrD4			
121	BrD5/EDO	O/I		
122	BrD6/EDI	O/O		
123	BrD7/ECK	O/O		
124	EECS	O		**Chip Select of Serial EEPROM**
125	BrCS#	O		**BootROM Chip Select**
114	BrOE#	O		**BootROM Read Enable for Flash ROM Application**
115	BrWE#	O		**BootROM Write Enable for Flash ROM Application**
Physical Interface				
18	XTLP	I		**Crystal Inputs** To be connected to a 25 MHz crystal.
17	XTLN			
6	RXIN	I		**Differentials Receive Inputs** The differentials receive inputs of 100BASE-TX or 10BASE-T, these pins are directly inputted from Magnetic.
7	RXIP			
20	TXOP	O		**Differential Transmit Outputs** The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins are directly outputted to Magnetic.
21	TXON			
15	RIBB	I		**Reference Bias Resistor** To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
9	TST0	I		**Test Pin**
10	TST1			
11	TST2			
5	TST3			
12	NC	O		**Not Connected**
13	NC			
LED Display and Miscellaneous				
102	Led-Act	O		**4 LED Mode: LED Display for Activity Status** This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected.
	(Led-lnk/act)	O		**(3 LED Mode): LED Display for Link and Activity Status** Link and Activity
103	Led-10Lnk	O		**4 LED Mode: LED Display for 10 Mbit/s Speed** This pin will be driven on continually when the 10 Mbit/s network operating speed is detected.
	(Led-fd/col)	O		**(3 LED Mode): LED Display for Full Duplex or Collision Status** full duplex/collision

Table 3 Pin Definitions and Functions (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
104	Led-100Lnk	O		**4 LED Mode: LED Display for 100 Mbit/s Speed** This pin will be driven on continually when the 100 Mbit/s network operating speed is detected.
	(Led-speed)	O		**(3 LED Mode): LED Display for 100 Mbit/s or 10 Mbit/s speed** speed 100(on)/10(off)
105	Led-Fd/Col	O		**4 LED Mode: LED Display for Full Duplex or Collision Status** This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration.
	bra(16)	O		**(3 LED Mode):bra 16**
95	Vaux	I		**When this pin is asserted, it indicates an auxiliary power source is supported.** ACPI purpose, for detecting the auxiliary power source. This pin should be or-wired connected to: 1) 3.3 V when 3.3 Vaux support, or 2) 5 V when 5 Vaux support from 3-way switch.
96	Vcc-detect	I		**When this pin is asserted, it indicates PCI power source is supported.** ACPI purpose, for detecting the main power is remained or not. This pin should be connected to PCI bus power source +5 V.
97	PMEP	O		**High pulse/low pulse 50ms**
Digital Power Pins				
26, 32, 42, 45, 52, 62, 71, 80, 82, 91, 107	$V_{ss\text{-}pci}$, $V_{ss\text{-}IR}$, $V_{ss\text{-}3}$			
23, 28, 37, 48, 55, 58, 67, 74, 77, 87, 111	$V_{dd\text{-}pci}$, $V_{dd\text{-}IR}$, $V_{dd\text{-}3}$, Connect to 3.3 V			
Analog Power Pins				
4,16,22	V_{AAR}, V_{AAREF}, V_{AAT}, 3.3 V			
8,14,19	GNDR, GNDREF, GNDT			

7 Functional Descriptions

7.1 Network Packet Buffer Management

7.1.1 Descriptor Structure Types

For networking operations, the AN985B/BX transmits the data packet from transmitting buffers in host memory to AN985B/BX's transmitting FIFO and receives the data packet from AN985B/BX's receiving FIFO to receive buffers in host memory. The descriptors that the AN985B/BX supports to build in host memory are used as the pointers of these transmitting and receiving buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the AN985B/BX and are shown as below. The type selections are controlled by bit 24 of RDES1 and the bit 24 of TDES1.

The transmitting and receiving buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

- Ring structure

There are two buffers per descriptor in the ring structure. Support receives early interrupt.

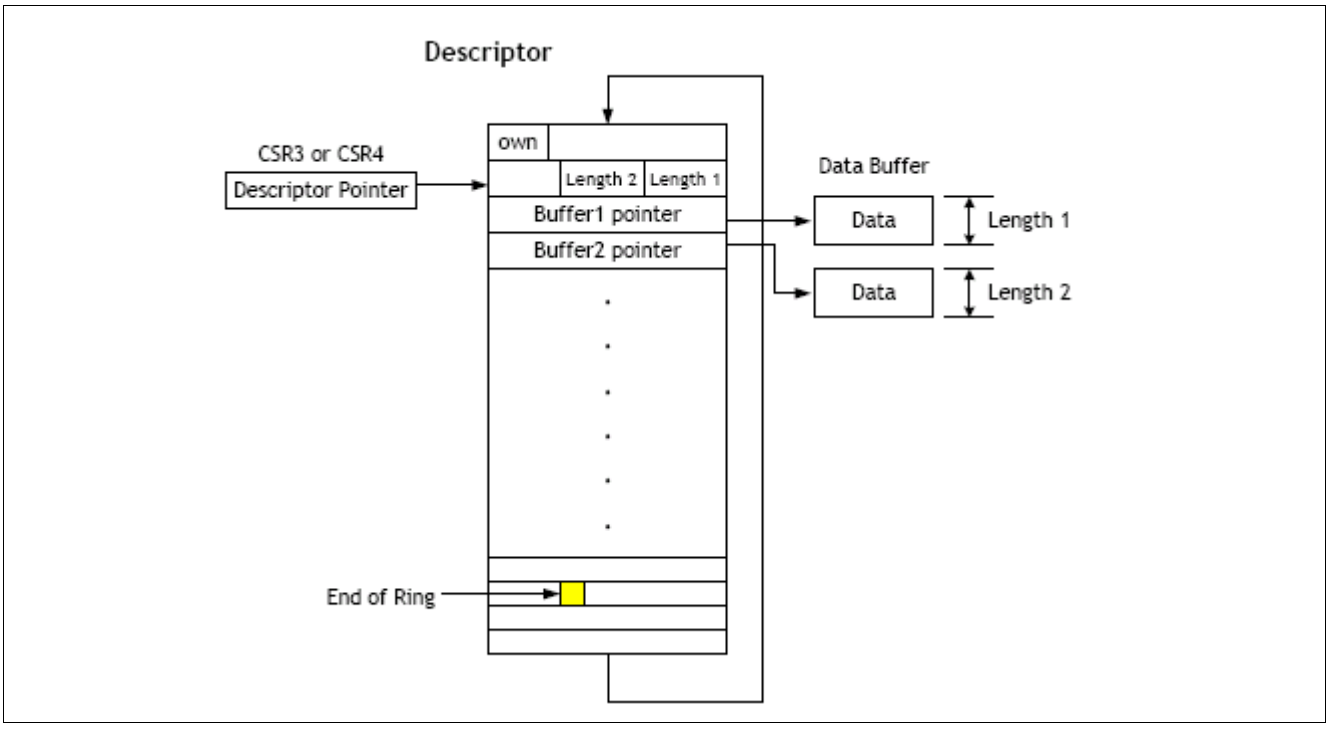


Figure 4 Ring Structure of Frame Buffer

- Chain structure

There is only one buffer per descriptor in the chain structure.

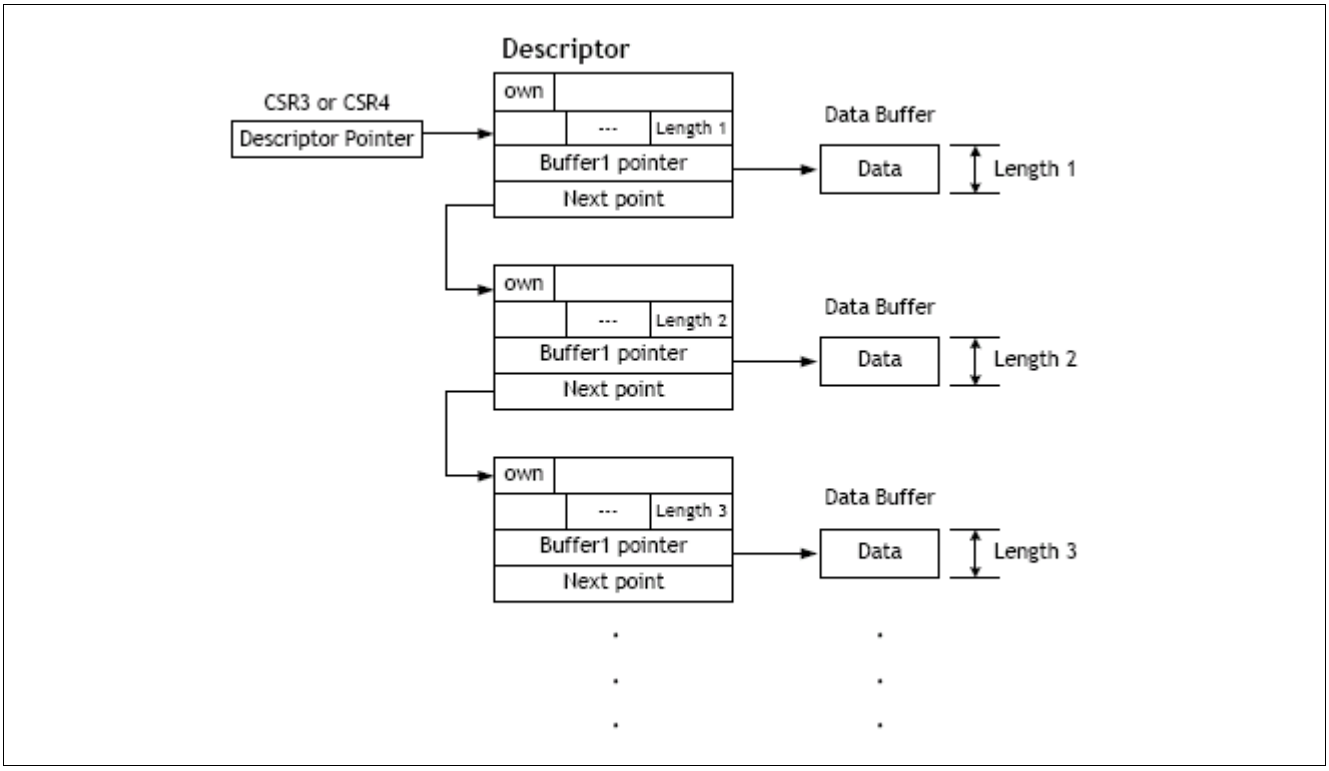


Figure 5 Chain Structure of Frame Buffer

7.1.2 The Point of Descriptor Management

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

- Transmit Descriptor Pointers

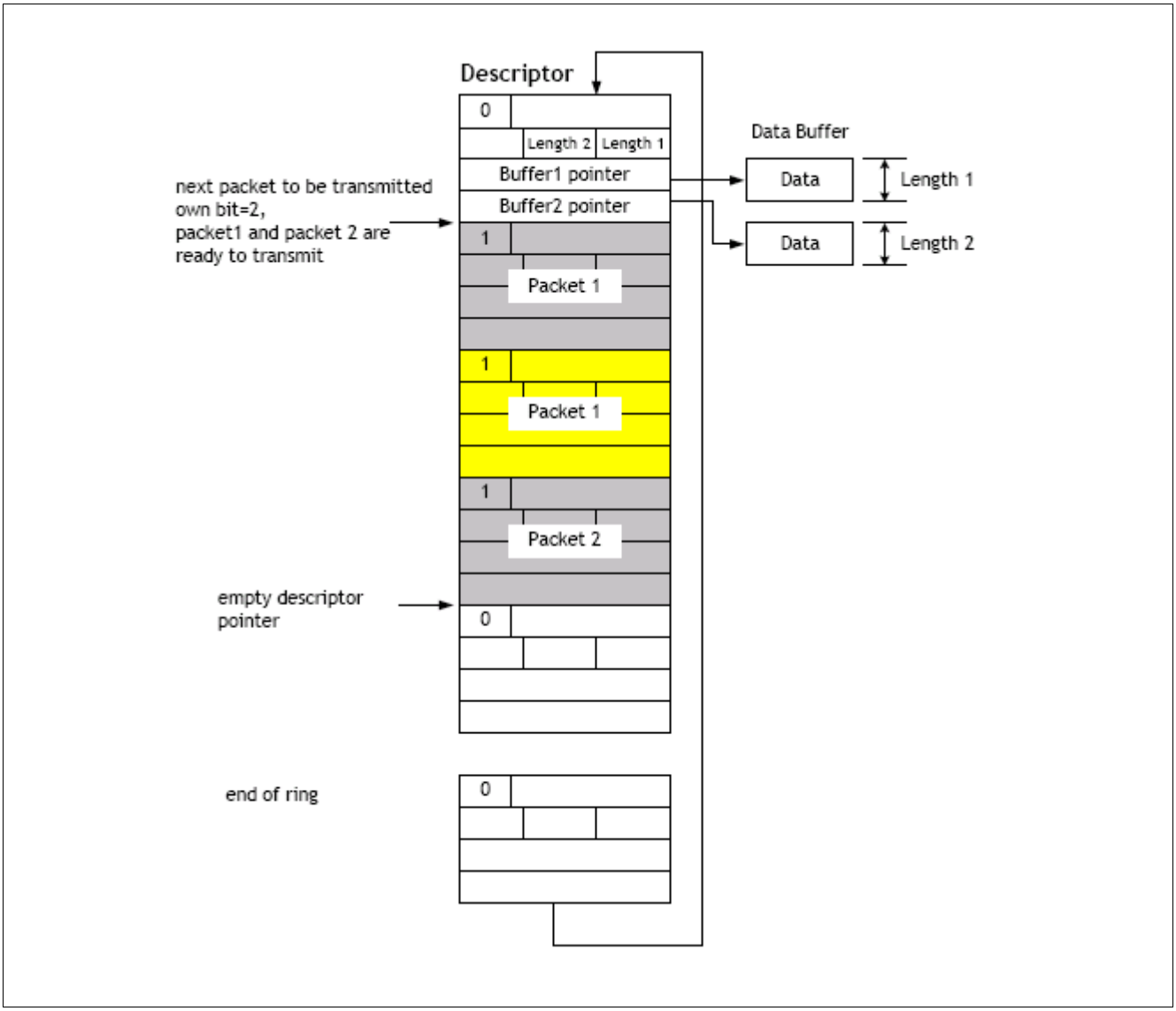


Figure 6 Transmit Pointers for Descriptor Management

- Receive Descriptor Pointers

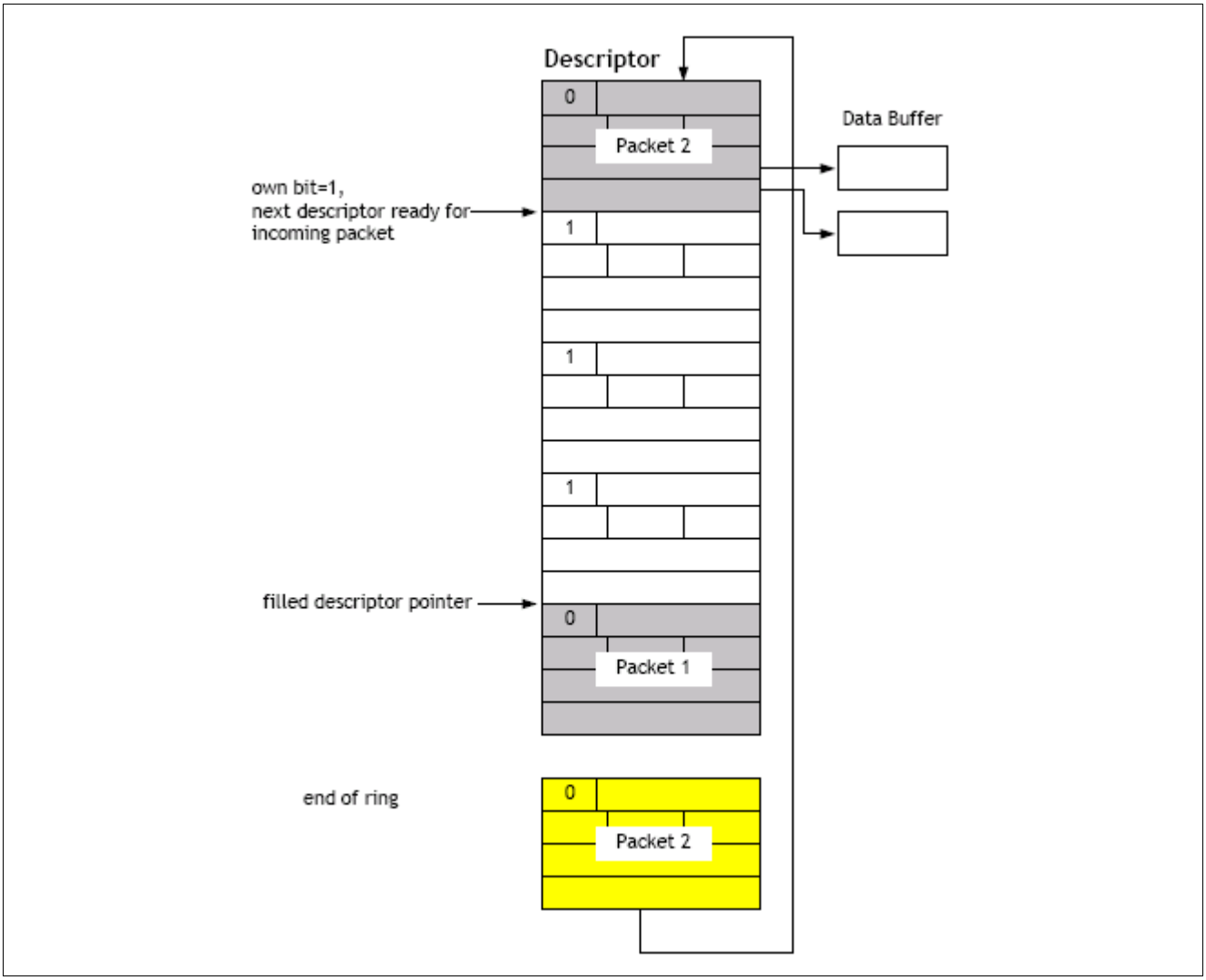


Figure 7 Receive Pointers for Descriptor Management

7.2 Transmit Scheme and Transmit Early Interrupt

7.2.1 Transmit Flow

The flow of packet transmit is shown below.

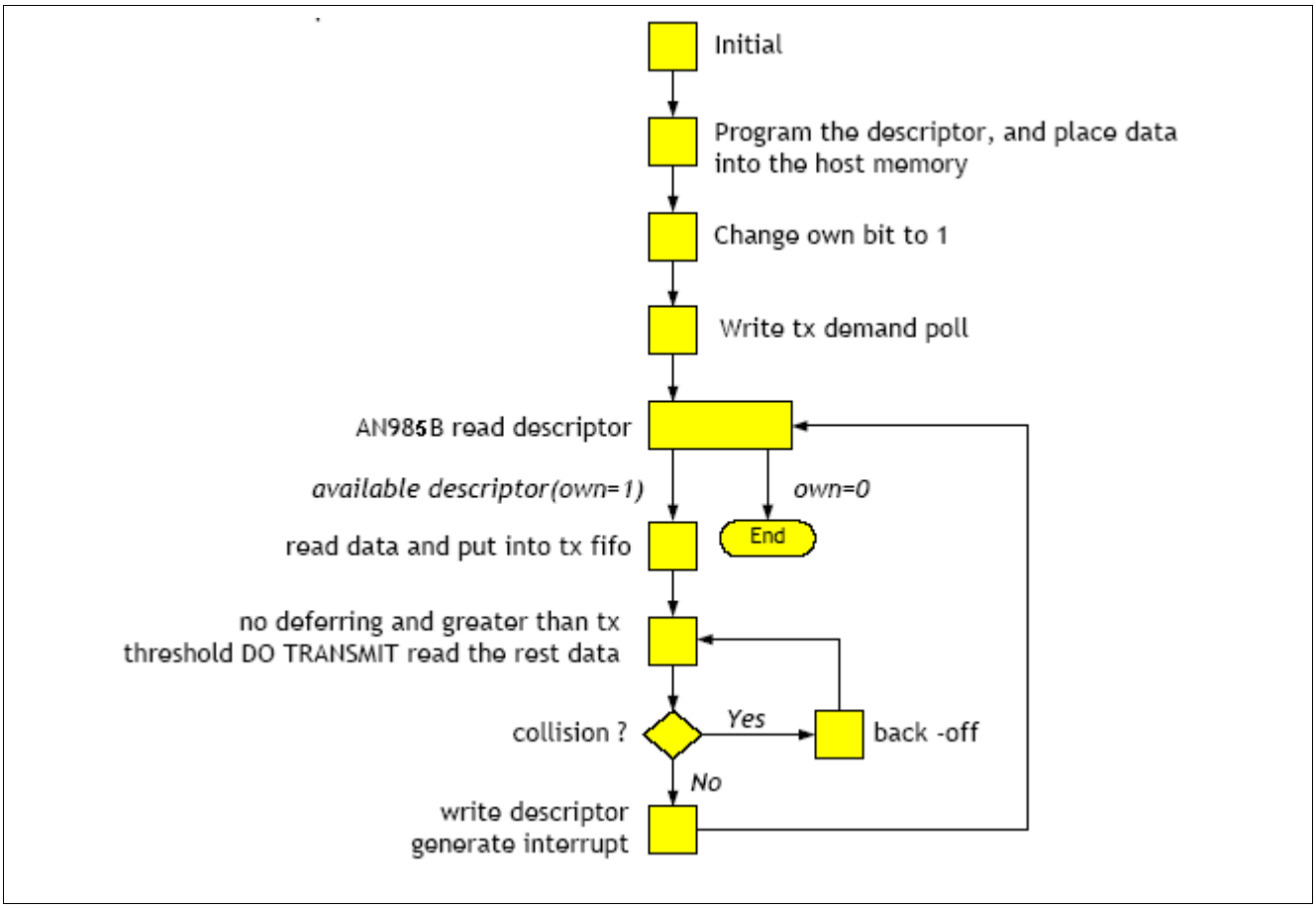


Figure 8 Transmit Flow

7.2.2 Transmit Pre-fetch Data Flow

- Transmit FIFO size = 2K-byte
- Two packets in the FIFO at the same time
- Meet the transmit min. back-to-back

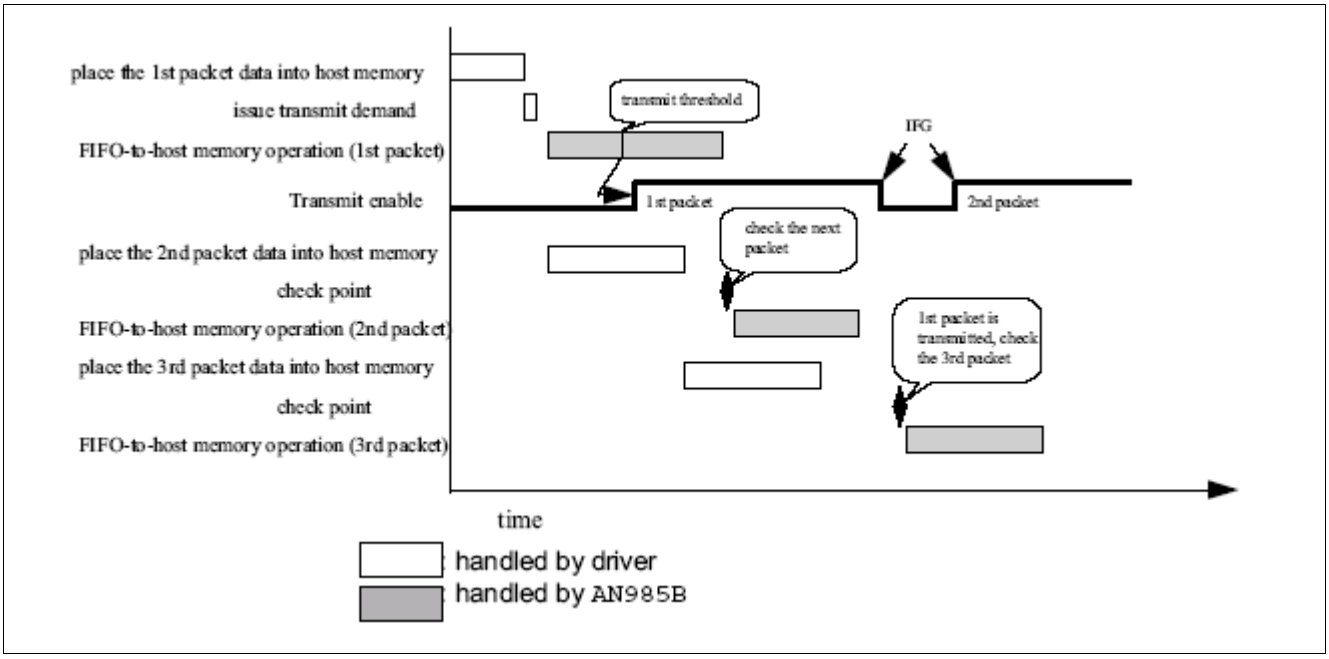


Figure 9 Transmit Data Flow of Pre-fetch Data

7.2.3 Transmit Early interrupt Scheme

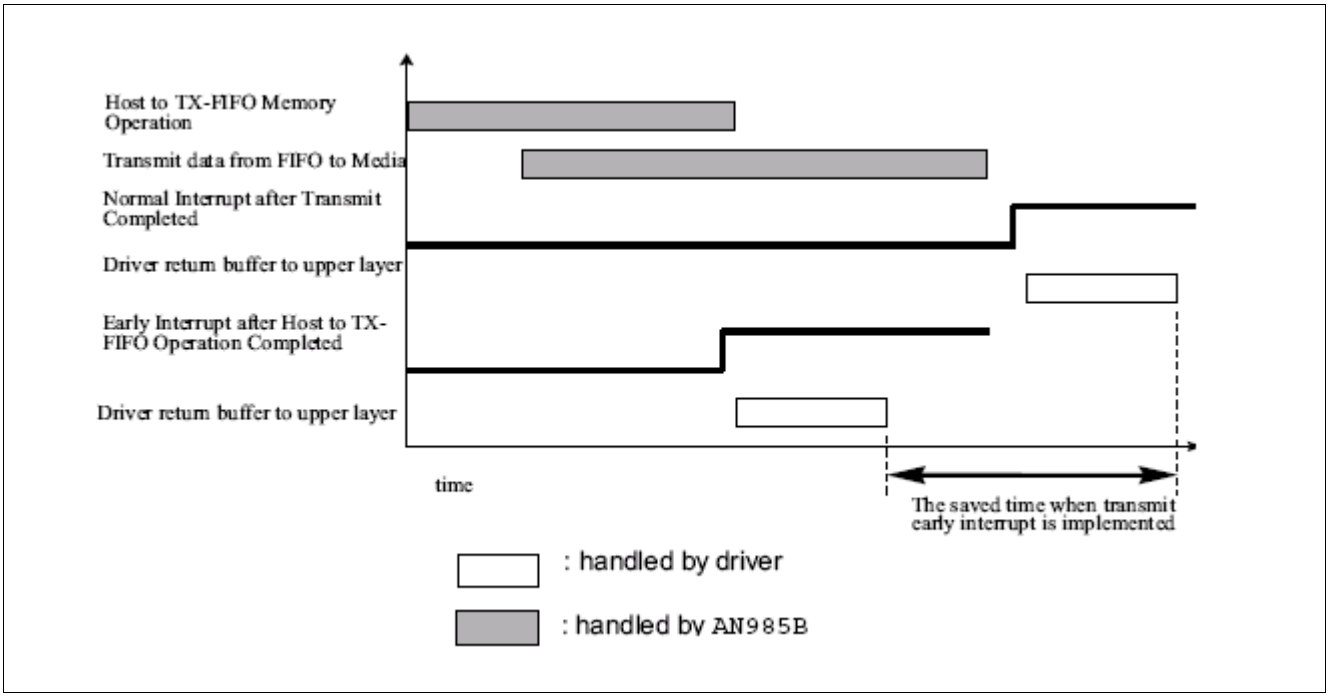


Figure 10 Transmit Normal Interrupt and Early Interrupt Comparison

7.3 Receive Scheme and Receive Early Interrupt Scheme

The following figure shows the difference of timing without early interrupt and with early interrupt.

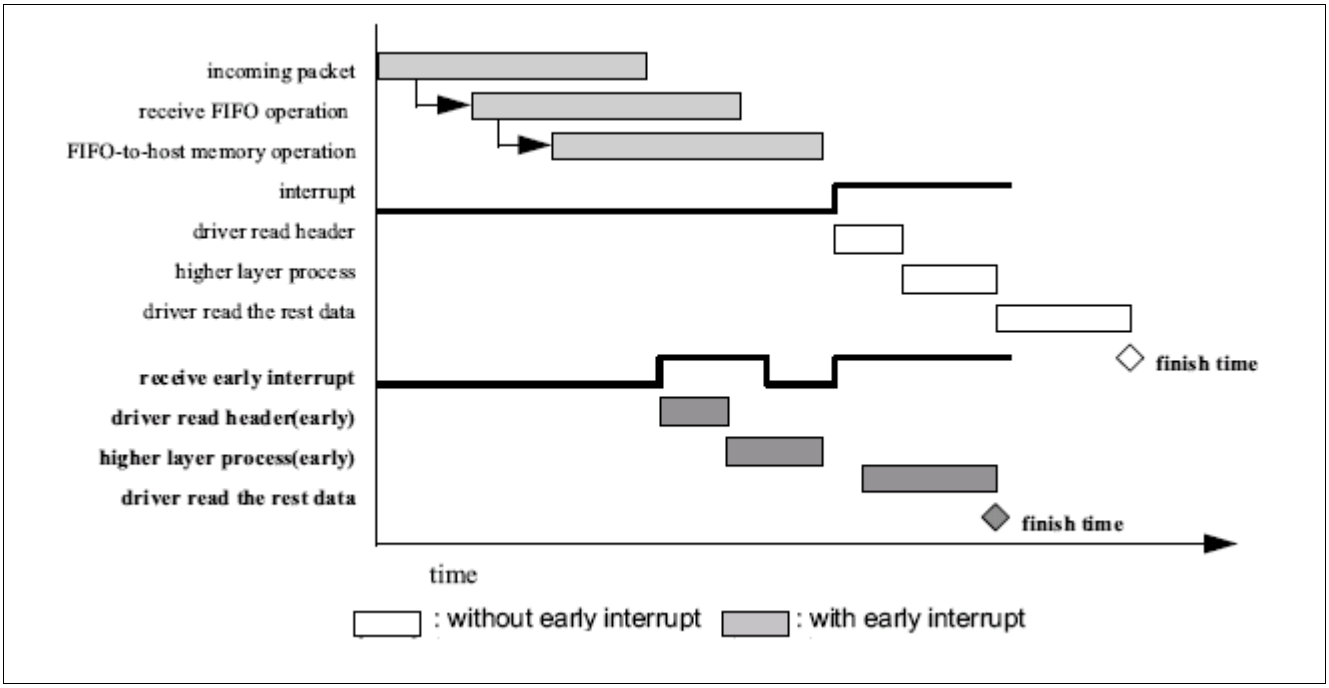


Figure 11 Receive Data Flow (without early interrupt and with early interrupt)

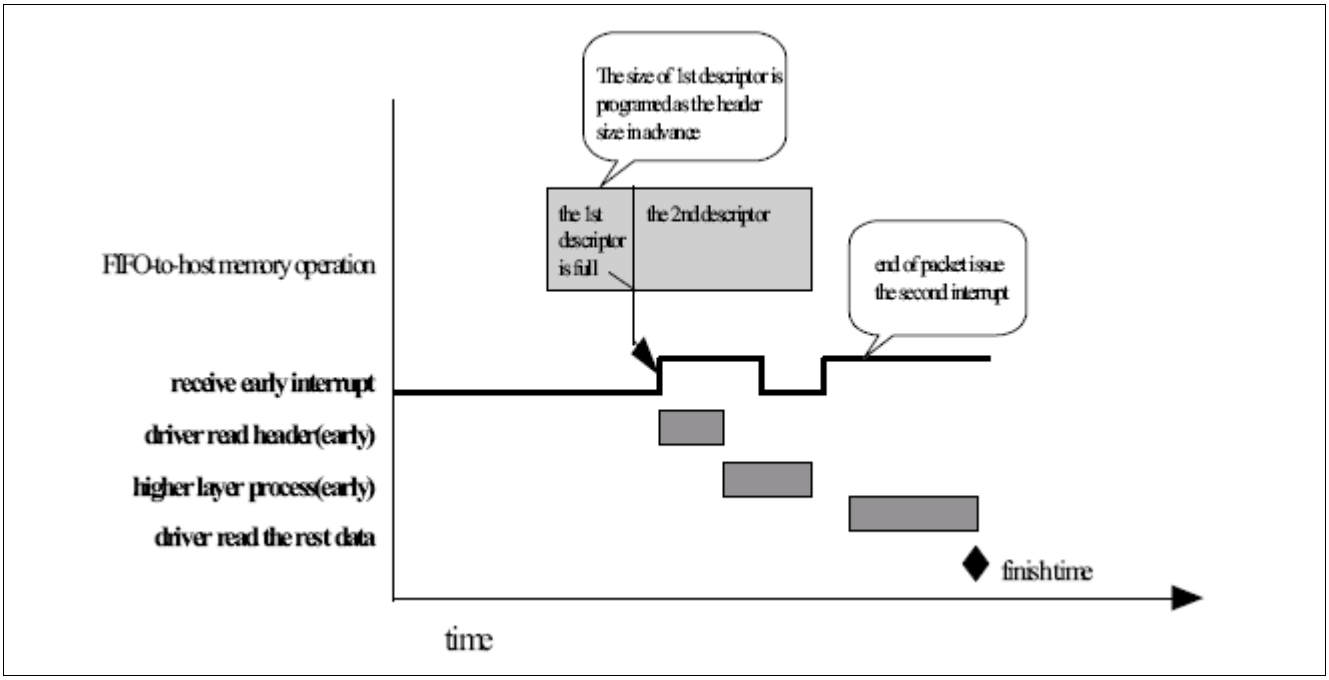


Figure 12 Detailed Receive Early Interrupt Flow

7.4 Network Operation

7.4.1 MAC Operation

The MAC (Media Access Control) portion of AN985B/BX, incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

Table 4 Format

Field	Description
Preamble	A 7-byte field of (10101010b)
Start Frame Delimiter	A 1-byte field of (10101011b)
Destination Address	A 6-byte field
Source Address	A 6-byte field
Length/Type	A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format.IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field
Data	46[1)] ~ 1500 bytes of data information
CRC	A 32-bit cyclic redundant code for error detection

1) If padding is disabled (TDES1 bit23), the data field may be shorter than 46 bytes.

Transmit Data Encapsulation

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEE802.3u, clause 24.
2. After the CRC field of the MAC frame, the AN985B/BX inserts the TR code according to the IEE802.3u, clause 24.

Receive Data Decapsulation

When operating in 100BASE-TX mode the AN985B/BX detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the AN985B/BX will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the AN985B/BX will report a CRC error.

Deferring

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the AN985B/BX will reset the IFG1 time counter and restart to monitor the channel for an idle again.
2. IFG2 time (32-bit time): After counting the IFG2 time the AN985B/BX will access the channel even though a carrier has been sensed on the network.

Collision Handling

The scheduling of re-transmissions is determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the AN985B/BX delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the nth re-transmission attempt is chosen as a uniform distributed integer r in the range:

$0 \leq r < 2^k$, where k = min (n, 10)

7.4.2 Transceiver Operation

The transceiver portion of the AN985B/BX, integrates the IEEE802.3u compliant functions of PCS (physical coding sub-layer), PMA (physical medium attachment) sub-layer, PMD (physical medium dependent) sub-layer for 100BASE-TX, the IEEE802.3 compliant functions of Manchester encoding/decoding and a transceiver for 10BASE-T. All the functions and operation schemes are described in the following sections:

7.4.2.1 100BASE-TX Transmit Operation

Regarding the 100BASE-TX transmission, the transceiver provides transmission functions PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1:1.

Data Code-Groups Encoder

In normal MII mode application, the transceiver receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the transceiver on the rising edge of Tx-clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.

Idle Code-Groups

In order to establish and maintain the clock synchronization, the transceiver needs to keep transmitting signals to medium. The transceiver will generate Idle code-groups for transmission when there is no real data MAC wants to send.

Start-of-Stream Delimiter-SSD (/J/K/)

In a transmission stream, the first 16 nibbles are MAC preamble. In order to let a partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the transceiver will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

End-of-Stream Delimiter-ESD (/T/R/)

In order to indicate the termination of the normal data transmissions, the transceiver will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.

Scrambling

All the encoded data (including the idle, SSD, and ESD code-groups) is passed to data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.

Data Conversion of Parallel to Serial, NRZ to NRZI, NRZI to MLT3

After being scrambled, the transmission data with 5B type in 25 MHz will be converted to a serial bit stream in 125 MHz by the parallel to serial function. After serialization, the transmission serial bit stream will be further converted from NRZ to NRZI format. After NRZI is converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easy to meet the FCC specification of EMI.

Wave-Shaper and Media Signal Driver

In order to reduce the energy of the harmonic frequency of transmission signals, the transceiver provides the wave-shaper prior to the line driver to smoothen but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals including the 100BASE-TX and 10BASE-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with a single one.

7.4.2.2 100BASE-TX Receiving Operation

Regarding the 100BASE-TX receiving operation, the transceiver provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with turn's ratio of 1:1. It includes the adaptive equalizer, baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ, and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

Adaptive Equalizer and Baseline Wander

The high-speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are dependent on the signal frequency, cable type, cable length and the connectors of the cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to perform these functions.

MLT3 to NRZI Decoder and PLL for Data Recovery

After receiving the proper MLT3 signals, the transceiver converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125 MHz are passed to the Phase Lock Loop circuits to extract out the original data and the synchronous clock.

Data Conversions of NRZI to NRZ and Serial to Parallel

After data recovery, the signals will be passed to the NRZI to NRZ converter to generate the 125 MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing.

De-scrambling and Decoding of 5B/4B

The parallel 5B type data is passed to the de-scrambler and 5B/4B decoder to return their original MII nibble type data.

Carrier Sensing

Carrier Sense (CRS) signal is asserted when the transceiver detects any 2 non-contiguous zeros within any 10bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or reception. But in full duplex mode, CRS is asserted only during packet reception.

7.4.2.3 10BASE-T Transmission Operation

It includes the parallel to serial converter, Manchester Encoder, Link test function, Jabber function, the transmit wave-shaper, and line driver described in the section of "Wave-Shaper and Media Signal Driver" of "100BASE-T Transmission Operation". It also provides Collision detection and SQE test for half duplex application.

7.4.2.4 10BASE-T Receive Operation

It includes the carrier sense function, receiving filter, PLL for clock and data recovering, Manchester decoder, and serial to parallel converter.

7.4.2.5 Loop-back Operation of Transceiver

The transceiver provides internal loop-back (also called transceiver loop-back) operation for both the 100BASE-TX and 10BASE-T operations. Setting bit 14 of PHY register 0 to 1 can enable the loop-back operation. In this loop-back operation, PHY will not transmit packets (but PHY will still send MLT3 for Idle).

In the 100BASE-TX internal loop-back operation, the data comes from the transmit output of NRZ to NRZI converter then loops-back to the receiving path into the input of NRZI to NRZ converter.

In the 10BASE-T loop-back operation, the data is through transmitting path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receiving path.

7.4.2.6 Full Duplex and Half Duplex Operation of Transceiver

The transceiver can operate for either full duplex or half duplex network application. In full duplex, both transmission and reception can be operated simultaneously. Under full duplex mode, collision (COL) signal is ignored and carrier sense (CRS) signal is asserted only when the transceiver is receiving.

In half duplex mode, either transmission or reception can be operated at one time. Under half duplex mode, collision signal is asserted when transmitted and received signals collided and carrier sense asserted during transmission and reception.

7.4.2.7 Auto-Negotiation Operation

The Auto-Negotiation function is designed to provide the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through bit 12 of PHY register 0.

The Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses (FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partners' capabilities, which are determined by PHY, register 4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex
2. 100BASE-TX half duplex
3. 10BASE-T full duplex
4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled, FLPs will be transmitted and the Auto-Negotiation function will process. Otherwise, the Auto-Negotiation will not occur until the bit 12 of PHY register 0 is set to 1. When the Auto-Negotiation is disabled, the Network Speed and Duplex Mode are selected by programming PHY register 0.

7.4.2.8 Power Down Operation

To reduce the power consumption the transceiver is designed with power down feature, which can save the power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separated, the transceiver can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other is operating.

7.4.3 Flow Control in Full Duplex Application

The PAUSE function operation is used to inhibit transmission of data frames for a specified period of time. The AN985B/BX supports full duplex protocol of IEEE802.3x. To support the PAUSE function, the AN985B/BX implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and execute the relative requests accordingly. When the Full Duplex mode and PAUSE functions are selected after Auto-Negotiation is completed, the AN985B/BX enables the PAUSE function for flow control of full duplex applications. In this section we will describe how the AN985B/BX implements the PAUSE function.

MAC Control Frame and PAUSE Frame

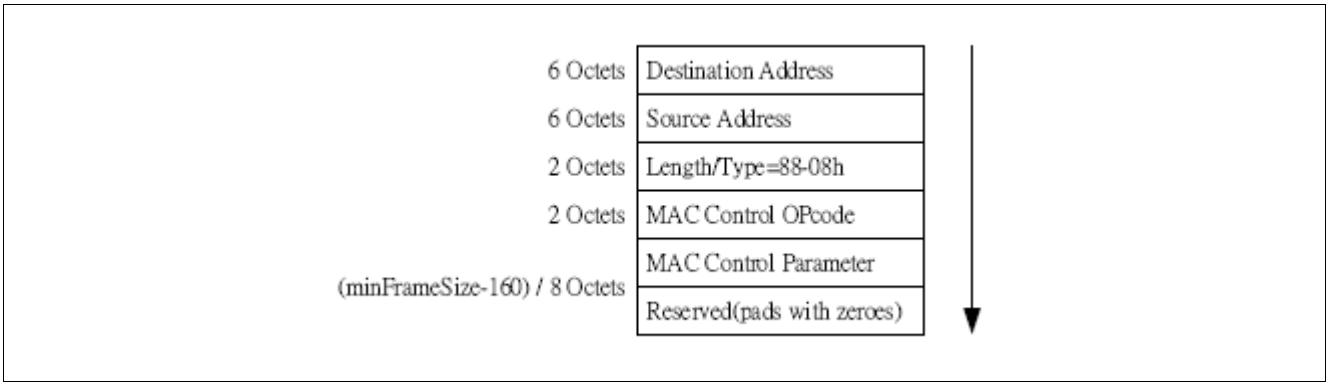


Figure 13 MAC Control Frame Format

The MAC Control frame is distinguished from other MAC frames only by their Length/Type field identifier. The MAC Control Opcode defined in MAC Control Frame format for PAUSE function is 0001_H. Also, the PAUSE time is specified in the MAC Control Parameters field with 2 Octets, unsigned integer, in the units of Slot-Times. The range of possible PAUSE time is 0 to 65535 Slot-Times.

So, a valid PAUSE frame issued by a MAC control client (could be a switch or a bridge) which will contain:

1. The destination address set equal to the globally assigned 48 bit mulitcast address 01-80-C2-00-00-01, or equal to the unicast address which the MAC control client wishes to inhibit its transmission of data frames
2. Filled MAC Control Opcode field with 0001_H
3. 2 Octets of PAUSE time specified in the MAC Control parameter field to indicate the length of time for which the destination is wished to inhibit data frame transmission

Receive Operation for PAUSE Function

Upon reception of a valid MAC Control frame, the AN985B/BX will start a timer for the length of time specified by the MAC Control Parameters field. When the timer value reaches zero then the AN985B/BX ends PAUSE state. However, a PAUSE frame should not affect the transmission of a frame that has been submitted to the MAC (started Transmit out of the MAC and can't be interrupted). On the other hand, the AN985B/BX shall not begin to transmit a frame more than one Slot-Times after receiving a valid PAUSE frame with a non-zero PAUSE time. If the AN985B/BX receives a PAUSE frame with a zero PAUSE time value, the AN985B/BX ends the PAUSE state immediately.

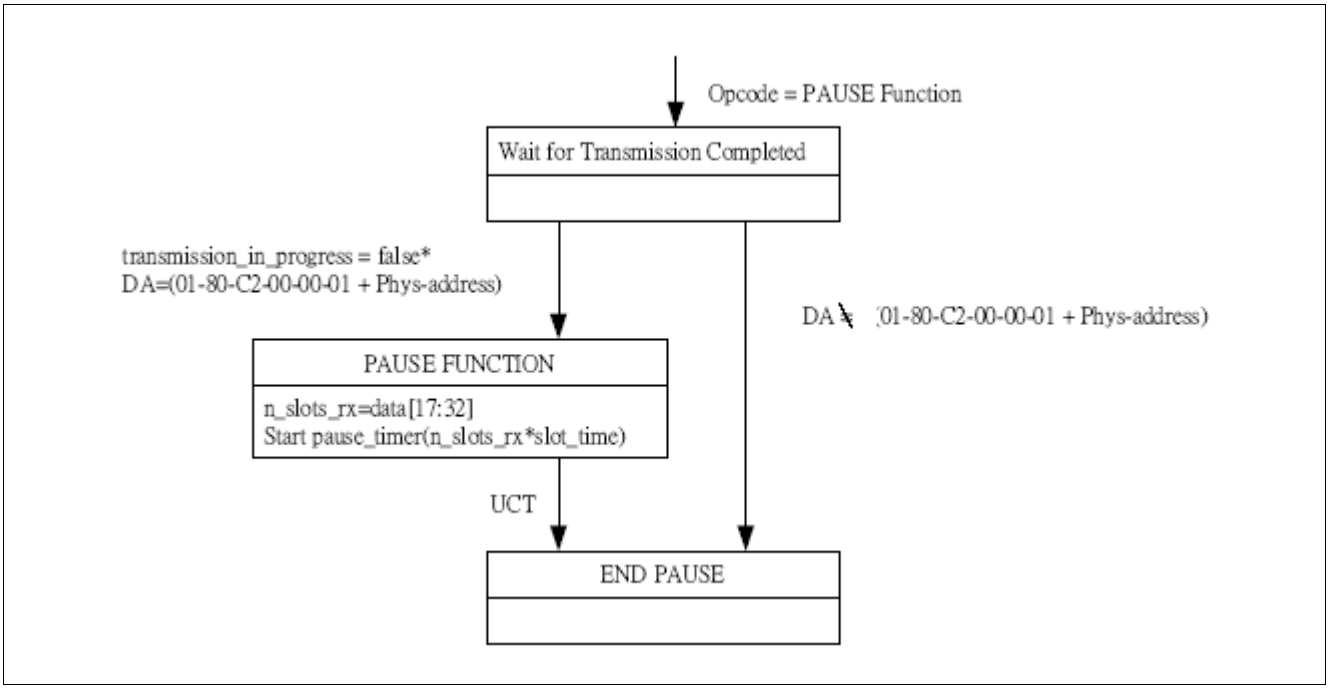


Figure 14 PAUSE Operation Receive State Diagram

7.5 LED Display Operation

The AN985B/BX provides two LED schemes one is three-LED which provides display pins for Link test status/Activity status, Speed mode, and Full duplex/Collision status. These pins can directly drive the LED device; the other is four-LED schemes which provide link100, link10, act, fd/col. The detail descriptions about the operation are described in the Pin Description section.

7.6 Reset Operation

7.6.1 Reset Whole Chip

There are two ways to reset the AN985B/BX. First, hardware reset, the AN985B/BX can be reset via RST# pin. For ensuring proper reset operation, at least 100us active Reset input signal is required. Second, software reset, when bit 0 of CSR0 register is set to 1, the AN985B/BX will reset entire circuits and registers to default values then clear the bit 0 of CSR0 to 0.

7.6.2 Reset Transceiver Only

When bit 15 of XR0 register is set to 1, the transceiver will reset entire circuits and register contents to default value then clear the bit 15 of XR0 to 0.

7.7 Wake on LAN Function

The AN985B/BX can assert a signal to wake up the system when it receives a Magic Packet from the network. The Wake on LAN operation is described as follows:

7.7.1 The Magic Packet Format

- Valid destination address that can pass the address filter of the AN985B/BX
- The payload of frame must include at least 6 contiguous ‘FF’ followed immediately by 16 repetitions of IEEE address
- The frame can contain multiple ‘six FF + sixteen IEEE address’ patterns
- CRC OK

7.7.2 The Wake on LAN Operation

The Wake on LAN enable function is controlled by bit 18 of CSR18; it is loaded from the EEPROM after reset or programmed by a driver to enable Wake on LAN function. If the bit 18 of CSR18 is set and the AN985B/BX receives a Magic Packet, it will assert the PME# signal (drive to low) to indicated is receiving a wake up frame as well as to set the PME status bit (the bit 15 of CSR20).

7.8 ACPI Power Management Function

The AN985B/BX has a built-in capability for Power Management (PM), which controlled by the host system

The AN985B/BX will provide:

- Compatibility with Device Class Power Management Reference Specification, Rev1.09
- Compatibility with ACPI specification, Rev 1.0
- Compatibility with CARDBUS Bus Power Management Interface Specification, Rev 1.1
- Compatibility with AMD Magic Packet™ Technology.
- Compatibility with CARDBUS CLKRUN scheme.

7.8.1 Power States

DO (Fully On)

In this state the AN985B/BX operates at full functionality and consumes its normal power. While in the D0 state, if the CARDBUS clock is lower than 16 MHz, the AN985B/BX may not receive or transmit frames properly.

D1

In this state the AN985B/BX doesn't response to any accesses, except if configuration space and full function contexts are in place. The only network operation the AN985B/BX can initiate is a wake-up event.

D2

In this state the AN985B/BX only responds to access configuration space and full function context in place. The AN985B/BX can't transmit or receive, even the wake-up frame.

$D3_{cold}$ (Power Removed)

In this state all function context is lost. When power is restored, the function will return to D0.

$D3_{hot}$ (Software Visible D3)

When the AN985B/BX is brought back to D0 from $D3_{hot}$ the software must perform a full initialization.

The AN985B/BX in the $D3_{hot}$ state responds to configuration cycles as long as power and clocks are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

Table 5 Power State

Device State	CARDBUS-Bus State	Function Context	Clock	Power	Supported Actions to Function	Supported Actions from Function
D0	B0	Full function context in place	Full speed	Full power	Any CARDBUS transaction	Any CARDBUS transaction or interrupt
D1	B0, B1	Configuration maintained. No Tx and Rx except wake-up events	Stopped to Full speed	–	CARDBUS configuration access	Only wake-up events
D2	B0, B1, B2	Configuration maintained. No Tx and Rx	Stopped to Full speed	–	CARDBUS configuration access (B0, B1)	–
D3hot	B0, B1, B2	Configuration lost, full initialization required upon return to D0	Stopped to Full speed	–	CARDBUS configuration access (B0, B1)	–
D3cold	B3	All configurations lost. Power-on defaults in place on return to D0	No clock	No power	Power-on reset	–

8 Registers and Descriptors Description

There are three kinds of registers designed for AN985B/BX. They are AN985B/BX configuration registers, CARDBUS control/status registers, and Transceiver control/status registers.

The AN985B/BX configuration registers are used to initialize and configure the AN985B/BX for identifying and querying the AN985B/BX.

The CARDBUS control/status registers are used to communicate between host and AN985B/BX. Host can initialize, control, and read the status of the AN985B/BX through the mapped I/O or memory address space.

Regarding the registers of transceiver portion of AN985B/BX, there are 11 basic registers with 16bits supporting for AN985B/BX. It includes 7 basic registers which are defined according to the clause 22 “Reconciliation Sub-layer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mbit/s and 100 Mbit/s Auto-Negotiation on twisted pair” of IEEE802.3u standard. The AN985B/BX also provides receiving and transmitting descriptors for packet buffering and management. These descriptors are described in the following section

8.1 AN985B/BX Configuration Registers

Table 6 Registers Address Space

Module	Base Address	End Address	Note
Configuration	0000 0000_H	0000 $00C4_H$	Xxxxx

Table 7 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
LID_CR0	Loaded Identification Number of Device and Vendor	00_H	36
CSD_CR1	Configuration Command and Status	04_H	36
CC_CR2	Class Code and Revision Number	08_H	38
LT_CR3	Latency Timer	$0C_H$	38
IOBA_CR4	I/O Base Address	10_H	39
MBA_CR5	Memory Base Address	14_H	40
CIS_CR10	Card Information Structure	28_H	40
SID_CR11	Subsystem ID and Vendor ID	$2C_H$	41
BRBA_CR12	Boot ROM Base Address	30_H	41
CP_CR13	Capabilities Pointer	34_H	41
CI_CR15	Configuration Interrupt	$3C_H$	42
DS_CR16	Driver Space for Special Purpose	40_H	43
SIG_CR32	Signature	80_H	43
PMR0_CR48	Power Management Register 0	$C0_H$	44
PMR1_CR49	Power Management Register 1	$C4_H$	46

The register is addressed wordwise.

Table 8 Registers Access ConditionsRegisters Access Conditions

Access Condition Short Name	Dependency
	= $_B$.

Standard abbreviations:

Table 9 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified

Table 9 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 10 Registers Clock Domains

Clock Short Name	Description

8.1.1 AN985B/BX Configuration Registers Descriptions

Offset	b31----------b16		b15----------b0		
00h	Device ID*		Vendor ID*		
04h	Status		Command		
08h	Base Class Code	Subclass	----------	Revision#	Step#

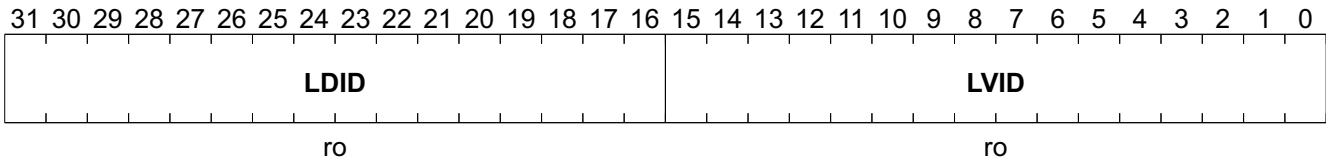
Offset	b31----------b16		b15----------b0	
0ch	------	------	Latency timer	Cache line size
10h	Base I/O address			
14h	Base memory address			
18h~24h	Reserved			
28h	ROM-im*	Address space offset*		Add-indi*
2ch	Subsystem ID*		Subsystem vendor ID*	
30h	Boot ROM base address			
34h	Reserved			
38h	Reserved			
3ch	Max_Lat*	Min_Gnt*	Interrupt pin	Interrupt line
40h	Reserved		Driver Space	Reserved
80h	Signature of AN985B/BX			
c0h	PMC		Next_Item_Ptr	Cap_ID
c4h	Reserved		PMCSR	

Note: Automatically recalled from EEPROM when CARDBUS reset is deserted.

1. *CIS(28_H) is a read-only register.*
2. *DS(40_H), bit 15-8, is read/write able register.*
3. *SIG(80_H) is hard wired register, read only.*

Loaded Identification Number of Device and Vendor

LID_CR0	Offset	Reset Value
Loaded Identification Number of Device and Vendor	00_H	From $EEPROM_H$

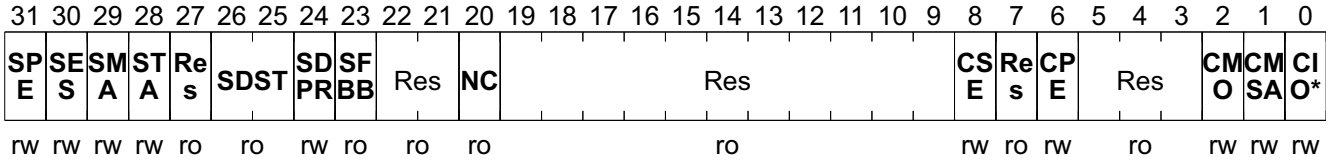


Field	Bits	Type	Description
LDID	31:16	ro	**Loaded Device ID** The device ID number loaded from serial EEPROM.
LVID	15:0	ro	**Loaded Vendor ID** The vendor ID number loaded from serial EEPROM.

Reset Value loaded from EEPROM

Configuration Command and Status

CSD_CR1	Offset	Reset Value
Configuration Command and Status	04_H	$0290\ 0000_H$

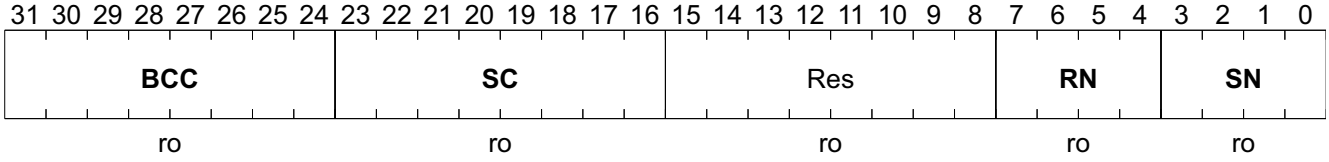


Field	Bits	Type	Description
SPE	31	rw	**Status of Parity Error** 1_B , means that AN985B/BX detected a parity error. This bit will be set in this condition even if the parity error response (bit 6 of CR1) is disabled.
SES	30	rw	**Status of System Error** 1_B , means that AN985B/BX asserted the system error pin
SMA	29	rw	**Status of Master Abort** 1_B , means that AN985B/BX received a master abort and terminated a master transaction
STA	28	rw	**Status of Target Abort** 1_B , means that AN985B/BX received a target abort and terminated a master transaction
Res	27	ro	**Reserved**
SDST	26:25	ro	**Status of Device Select Timing** The timing of the assertion of device select. 01_B , means a medium assertion of $\overline{\text{DEVSEL\#}}$
SDPR	24	rw	**Status of Data Parity Report** 1: when three conditions are met: AN985B/BX asserted parity error - $\overline{\text{PERR\#}}$ or it detected parity error asserted by other device. AN985B/BX is operating as a bus master. 5AN985B/BX's parity error response bit (bit 6 of CR1) is enabled.
SFBB	23	ro	**Status of Fast Back-to-Back** Always 1, since AN985B/BX has the ability to accept fast back-to-back transactions.
Res	22:21	ro	**Reserved**
NC	20	ro	**New Capabilities** This bit indicates that whether the AN985B/BX provides a list of extended capabilities, such as CARDBUS power management. 0_B , the AN985B/BX doesn't provide New Capabilities 1_B , the AN985B/BX provides the CARDBUS management function
Res	19:9	ro	**Reserved**
CSE	8	rw	**Command of System Error Response** 1_B , enable system error response. AN985B/BX will assert $\overline{\text{SERR\#}}$ when it find a parity error on the address phase.
Res	7	ro	**Reserved**

Field	Bits	Type	Description
CPE	6	rw	**Command of Parity Error Response** 0_B , disable parity error response. AN985B/BX will ignore any detected parity error and keep on its operating. Default value is 0. 1_B , enable parity error response. AN985B/BX will assert system error (bit 13 of CSR5) when a parity error is detected.
Res	5:3	ro	**Reserved**
CMO	2	rw	**Command of Master Operation Ability** 0_B , disable the bus master ability 1_B , enable the CARDBUS bus master ability. Default value is 1 for normal operation.
CMSA	1	rw	**Command of Memory Space Access** 0_B , disable the memory space access ability 1_B , enable the memory space access ability
CIOSA	0	rw	**Command of I/O Space Access** 0_B , disable the I/O space access ability 1_B , enable the I/O space access ability

Class Code and Revision Number

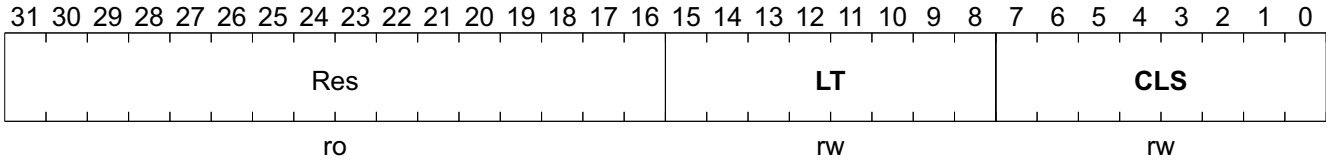
CC_CR2	Offset	Reset Value
Class Code and Revision Number	**08_H**	**$0200\ ????_H$**



Field	Bits	Type	Description
BCC	31:24	ro	**Base Class Code** It means AN985B/BX is network controller.
SC	23:16	ro	**Subclass Code** It means AN985B/BX is a Fast Ethernet Controller.
Res	15:8	ro	**Reserved**
RN	7:4	ro	**Revision Number** Identifies the revision number of AN985B/BX.
SN	3:0	ro	**Step Number** Identifies the AN985B/BX steps within the current revision.

Latency Timer

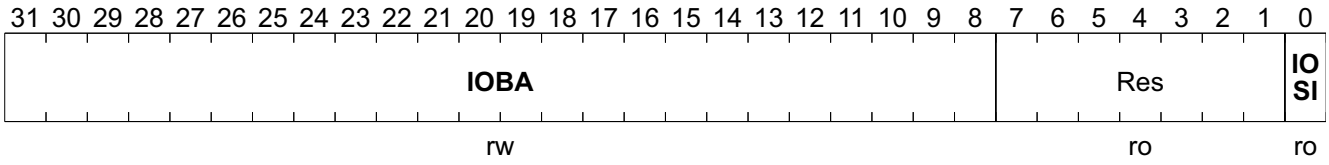
LT_CR3	Offset	Reset Value
Latency Timer	**$0C_H$**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:16	ro	**Reserved**
LT	15:8	rw	**Latency Timer** This value specifies the latency timer of the AN985B/BX in units of CARDBUS bus clock. Once the AN985B/BX asserts FRAME#, the latency timer starts to count. If the latency timer expires and the AN985B/BX still asserted FRAME#, then the AN985B/BX will terminate the data transaction as soon as its GNT# is removed.
CLS	7:0	rw	**Cache Line Size** This value specifies the system cache line size in units of 32-bit double words (DW). The AN985B/BX supports 8, 16, and 32 DW of cache line size. This value is used by the AN985B/BX driver to program the cache alignment bits (bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented CARDBUS commands; say memory-read-line, memory-read-multiple, and memory-write-and-invalidate.

I/O Base Address

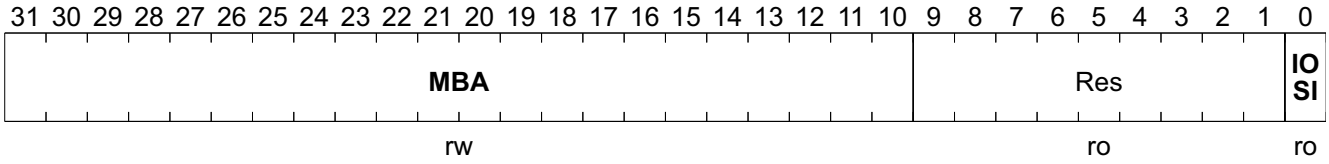
IOBA_CR4	Offset	Reset Value
I/O Base Address	**10_H**	**$0000\ 0001_H$**



Field	Bits	Type	Description
IOBA	31:8	rw	**I/O Base Address** This value indicate the base address of CARDBUS control and status register (CSR0~28).
Res	7:1	ro	**Reserved**
IOSI	0	ro	**I/O Space Indicator** 1_B , means that the configuration registers map into the I/O space

Memory Base Address

MBA_CR5	Offset	Reset Value
Memory Base Address	14_H	$0000\ 0000_H$

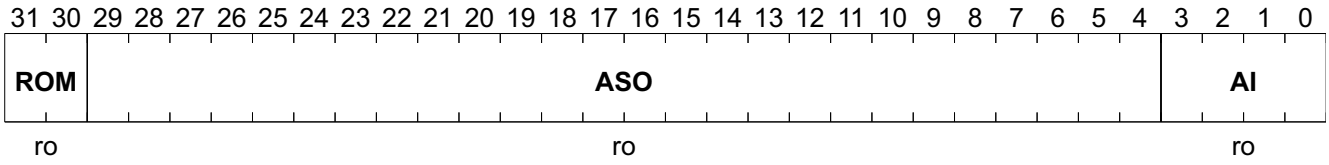


Field	Bits	Type	Description
MBA	31:10	rw	**Memory Base Address** This value indicates the base address of CARDBUS control and status register (CSR0~28).
Res	9:1	ro	**Reserved**
IOSI	0	ro	**Memory Space Indicator** 1_B , means that the configuration registers map into the I/O space

Card Information Structure

This register is used to point one of the possible address spaces where the CIS begins. This register is designed for CARDBUS environment. It's data is auto-loaded from the serial EEPROM after power on or hardware reset.

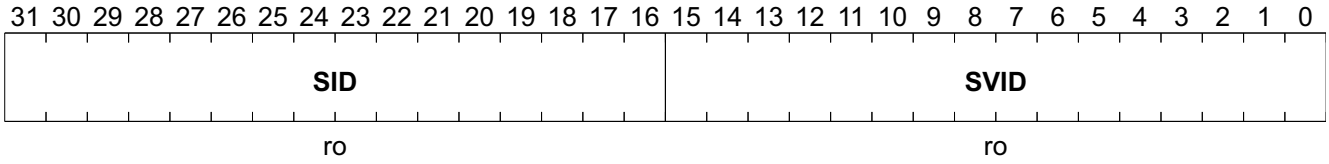
CIS_CR10	Offset	Reset Value
Card Information Structure	28_H	From $EEPROM_H$



Field	Bits	Type	Description
ROM	31:30	ro	**ROM Image** This ROM image value is applied when the CIS is stored in a boot ROM. This value is loaded from serial EEPROM.
ASO	29:4	ro	**Address Space Offset** This value indicates the offset within the address space. The address space is specified by address space indicator(bit 2~0 of CR10).
AI	3:0	ro	**Address Space Indicator** This value indicates the location where the CIS address space begins. 111_B , means that the CIS begins in the boot ROM space. $others_B$, makes all the bits of CIS reset to 0

Subsystem ID and Vendor ID

SID_CR11	Offset	Reset Value
Subsystem ID and Vendor ID	$2C_H$	From EEPROM$_H$

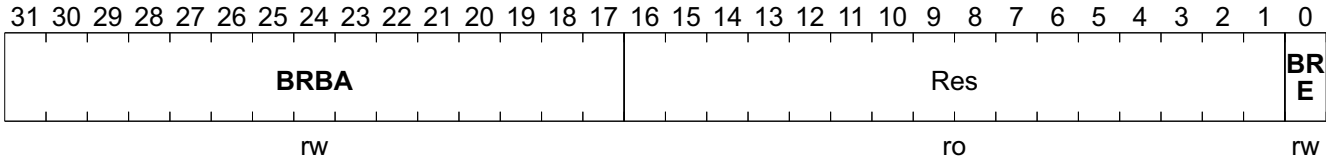


Field	Bits	Type	Description
SID	31:16	ro	**Subsystem ID** This value is loaded from EEPROM after power on or hardware reset.
SVID	15:0	ro	**Subsystem Vendor ID** This value is loaded from EEPROM after power on or hardware reset.

Boot ROM Base Address

This register should be initialized before accessing the boot ROM space. (Write ffffffff$_H$ return fffe0001$_H$)

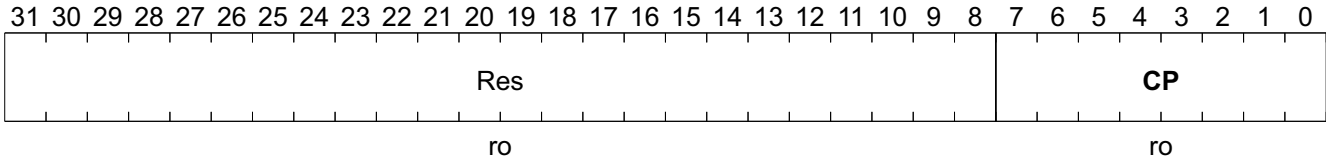
BRBA_CR12	Offset	Reset Value
Boot ROM Base Address	30_H	XXXX 0000$_H$



Field	Bits	Type	Description
BRBA	31:17	rw	**Boot ROM Base Address** This value indicates the address mapping of boot ROM field. Besides, it also defines the boot ROM size. The value of bit 17~10 is set to 0 for AN985B/BX to support up to 256 KB of boot ROM.
Res	16:1	ro	**Reserved**
BRE	0	rw	**Boot ROM Enable** The AN985B/BX really enables its boot ROM access only if both the memory space access bit (bit 1 of CR1) and this bit are set to 1. 1_B , enable Boot ROM (Combines with bit 1 of CR1)

Capabilities Pointer

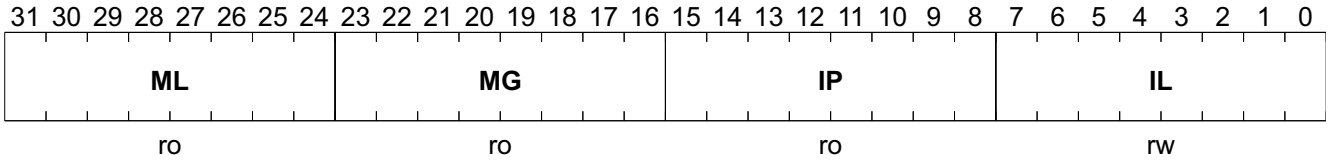
CP_CR13	Offset	Reset Value
Capabilities Pointer	34_H	0000 00C0$_H$



Field	Bits	Type	Description
Res	31:8	ro	**Reserved**
CP	7:0	ro	**Capabilities Pointer**

Configuration Interrupt

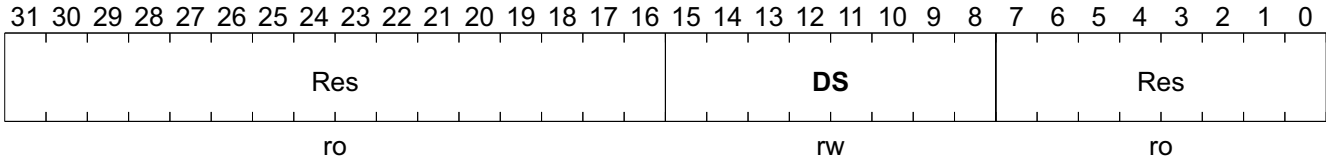
CI_CR15	Offset	Reset Value
Configuration Interrupt	**$3C_H$**	**$XXXX\ 01XX_H$**



Field	Bits	Type	Description
ML	31:24	ro	**Max. Lat Register** This value indicates “how often” the AN985B/BX needs to access to the CARDBUS bus in the units of 250 ns. This value is loaded from serial EEPROM after power on or hardware reset. *Note: Automatically recalled from EEPROM.*
MG	23:16	ro	**Min. Gnt Register** This value indicates how long the AN985B/BX needs to retain the CARDBUS bus ownership whenever it initiates a transaction, in the units of 250 ns. This value is loaded from serial EEPROM after power on or hardware reset. *Note: Automatically recalled from EEPROM.*
IP	15:8	ro	**Interrupt Pin** This value indicates which of the four interrupt request pins that AN985B/BX is connected.Always 01_H: means the AN985B/BX connects to $\overline{\text{INTA}}$#
IL	7:0	rw	**Interrupt Line** This value indicates which of the system interrupt request lines the $\overline{\text{INTA}}$# of AN985B/BX is routed to. The BIOS will fill this field when it initializes and configures the system. The AN985B/BX driver can use this value to determine priority and vector information.

Driver Space for Special Purpose

DS_CR16	Offset	Reset Value
Driver Space for Special Purpose	40_H	0000 XX00$_H$

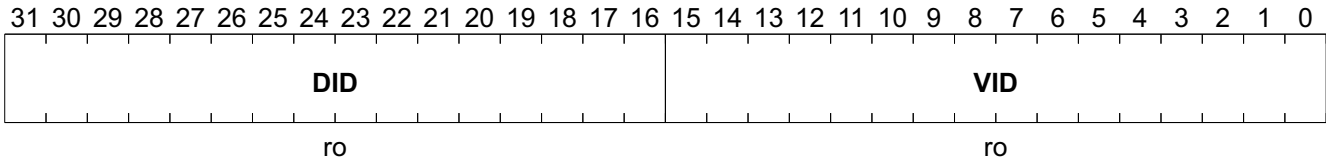


Field	Bits	Type	Description
Res	31:16	ro	**Reserved**
DS	15:8	rw	**Driver Space for special purpose** Since this area won't be cleared in the software reset. The AN985B/BX driver can use this rw area for special purpose.
Res	7:0	ro	**Reserved**

Signature of AN985B/BX

Hard wired register, read only

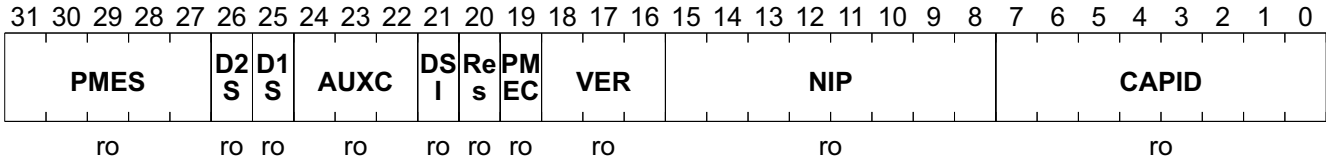
SIG_CR32	Offset	Reset Value
Signature	80_H	0985 1317$_H$



Field	Bits	Type	Description
DID	31:16	ro	**Device ID** The device ID number of AN985B/BX.
VID	15:0	ro	**Vendor ID** The vendor ID number of ADM Technology Corp.

Power Management Register 0

PMR0_CR48	Offset	Reset Value
Power Management Register 0	$C0_H$	$FE82\ 0001_H$

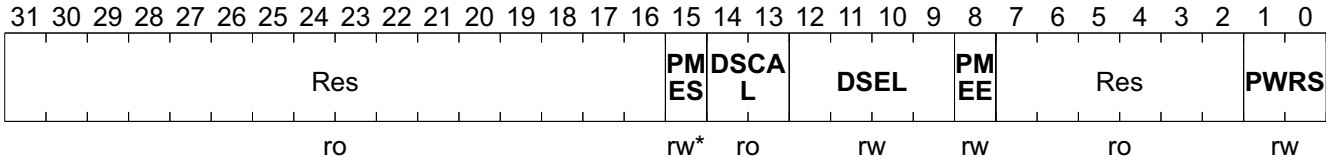


Field	Bits	Type	Description
PMES	31:27	ro	**PME Support** The AN985B/BX will assert $\overline{\text{PME}}$#/CSTSCHG signal while in the D0, D1, D2, D3 power state. The AN985B/BX supports Wake-up from the above states.
D2S	26	ro	**D2 Support** The AN985B/BX supports D2 Power Management State.
D1S	25	ro	**D1 Support** The AN985B/BX supports D1 Power Management State.
AUXC	24:22	ro	**Aux Current** These three bits report the maximum 3.3 Vaux current requirements for AN985B/BX. If bit 31 of PMR0 is '1', the default value is 0101_B, means AN985B/BX need 100 mA to support remote wake-up in D3cold power state.
DSI	21	ro	**Device Specific Initialization** The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0_B , indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state
Res	20	ro	**Reserved**
PMEC	19	ro	**PME Clock** When "1" indicates that the AN985B/BX relies on the presence of the CARDBUS clock for $\overline{\text{PME}}$#/CSTSCHG operation. While "0" indicates the no CARDBUS clock is required for the AN985B/BX to generate $\overline{\text{PME}}$#/CSTSCHG.
VER	18:16	ro	**Version** The value of 010_B indicates that the AN985B/BX complies with Revision 1.0a of the CARDBUS Power Management Interface Specification.
NIP	15:8	ro	**Next Item Pointer** This value is always 0_H, indicates that there is no additional items in the Capabilities List.

Field	Bits	Type	Description
CAPID	7:0	ro	**Capability Identifier** This value is always 01_H, indicates the link list item as being CARDBUS Power Management Registers.

Power Management Register 1

PMR1_CR49	Offset	Reset Value
Power Management Register 1	$C4_H$	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:16	ro	**Reserved**
PMES	15	rw*	**PME Status** This bit is set when the AN985B/BX would normally assert the PME#/CSTSCHG signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a “1” to this bit will clear it and cause the AN985B/BX to stop asserting a PME#/CSTSCHG (if enabled). Writing a “0” has no effect. *Note: rw*: Read and Write Clear*
DSCAL	14:13	ro	**Data Scale** Indicates the scaling factor to be used when interpreting the value of the Data register.
DSEL	12:9	rw	**Data Select** This four-bit field is used to select which data is to be reported through the Data register and Data_Scale field.
PMEE	8	rw	**PME En** “1” enables the AN985B/BX to assert PME#/CSTSCHG. When “0” disables the PME#/CSTSCHG assertion. Magic packet default enable: Csr18 <18> and csr18 <19> are set ->csr13 <9> is set, then #pme asserts without impact of PME_En.
Res	7:2	ro	**Reserved**
PWRS	1:0	rw	**Power State** This two-bit field is used both to determine the current power state of the AN985B/BX and to set the AN985B/BX into a new power state. The definition of this field is given below. *Note: This field is auto cleared to D0 when power resumed.* 00_B **D0**, 01_B **D1**, 10_B **D2**, 11_B **D3hot**,

8.2 PCI /CARDBUS Control/Status Registers

Table 11 Registers Address Space

Module	Base Address	End Address	Note
PCI/CARDBUS	0000 0000_H	0000 $010C_H$	

Table 12 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
PAR_CSR0	CARDBUS Access Register	00_H	49
TDR_CSR1	Transmit Demand Register	08_H	50
RDR_CSR2	Receive Demand Register	10_H	52
RDB_CSR3	Receive Descriptor Base Address	18_H	52
TDB_CSR4	Transmit Descriptor Base Address	20_H	53
SR_CSR5	Status Register	28_H	53
NAR_CSR6	Network Access Register	30_H	57
IER_CSR7	Interrupt Enable Register	38_H	58
LPC_CSR8	Lost Packet Counter	40_H	61
SPR_CSR9	Serial Port Register	48_H	61
TMR_CSR11	General-Purpose Timer	58_H	62
WCSR_CSR13	Wake-up Control/Status Register	68_H	62
WTMR_CSR15	Watchdog Timer	78_H	65
ACSR5_CSR16	Assistant CSR5 (Status Register 2)	80_H	66
ACSR7_CSR17	Assistant CSR7 (Interrupt Enable Register 2)	84_H	67
CR_CSR18	Command Register	88_H	67
CARDBUSC_CSR19	CARDBUS Bus Performance Counter	$8C_H$	70
PMCSR_CSR20	Power Management Command and Status	90_H	70
WTDP_CSR21	Current Working Transmit Descriptor Pointer	94_H	72
WRDP_CSR22	Current Working Receive Descriptor Pointer	98_H	72
TXBR_CSR23	Transmit Burst Count/Time-out	$9C_H$	73
FROM_CSR24	Flash ROM (also the boot ROM) Port	$A0_H$	73
PAR0_CSR25	Physical Address Register 0	$A4_H$	74
PAR1_CSR26	Physical Address Register 1	$A8_H$	74
MAR0_CSR27	Multicast Address Register 0	AC_H	75
MAR1_CSR28	Multicast Address Register 1	$B0_H$	76
UAR0_CSR_29	Unicast Address Register 0	$B4_H$	77
UAR1_CSR_30	Unicast Address Register 1	$B8_H$	77
OMR	Operation Mode Register	FC_H	77
FER	Function Event Register	100_H	78
FEMR	Function Event Mask Register	104_H	79
FPSR	Function Present State Register	108_H	80
FFER	Function Force Event Register	$10C_H$	80

The register is addressed wordwise.

Standard abbreviations:

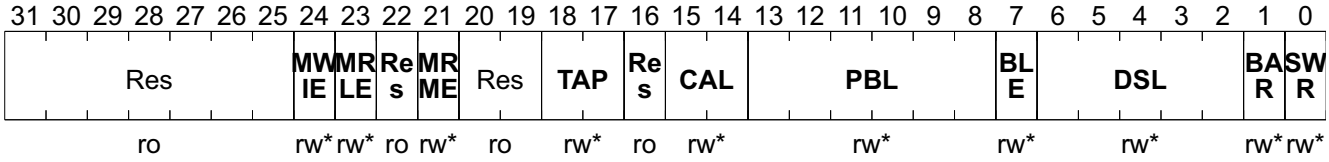
Table 13 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

8.2.1 PCI/CARDBUS Control/Status Registers Description

CARDBUS Access Register

PAR_CSR0	Offset	Reset Value
CARDBUS Access Register	00_H	$0000\ 1000_H$

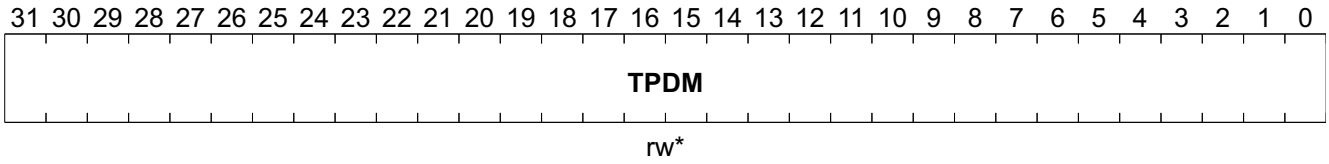


Field	Bits	Type	Description
Res	31:25	ro	**Reserved**
MWIE	24	rw*	**Memory Write and Invalidate Enable** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 0_B , disable AN985B/BX to generate memory write invalidate command and use memory write commands instead 1_B , enable AN985B/BX to generate memory write invalidate command. AN985B/BX will generate this command while writing full cache lines
MRLE	23	rw*	**Memory Read Line Enable** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 1_B , enable AN985B/BX to generate memory read line command while read access instruction reach the cache line boundary. If the read access instruction doesn't reach the cache line boundary then AN985B/BX uses the memory read command instead.
Res	22	ro	**Reserved**
MRME	21	rw*	**Memory Read Multiple Enable** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 1_B , enable AN985B/BX to generate memory read multiple commands while reading full cache line. If the memory is not cache aligned the AN985B/BX uses memory read command instead.
Res	20:19	ro	**Reserved**

Field	Bits	Type	Description
TAP	18:17	rw*	**Transmit Auto-polling in Transmit Suspended State** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 00_B , disable auto-polling (default) 01_B , polling own-bit every 200 μ s 10_B , polling own-bit every 800 μ s 11_B , polling own-bit every 1600 μ s
Res	16	ro	**Reserved**
CAL	15:14	rw*	**Cache Alignment, Address Boundary for Data Burst, Set after Reset** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 00_B , reserved (default) 01_B , 8 DW boundary alignment 10_B , 16 DW boundary alignment 11_B , 32 DW boundary alignment
PBL	13:8	rw*	**Programmable Burst Length** This value defines the maximum number of DW to be transferred in one DMA transaction. Value: 0 (unlimited), 1, 2, 4, 8, 16 (default), 32 *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.*
BLE	7	rw*	**Big or Little Endian Selection** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 0_B , little endian (e.g. INTEL) 1_B , big endian (only for data buffer)
DSL	6:2	rw*	**Descriptor Skip Length** Defines the gap between two descriptions in the units of DW. *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.*
BAR	1	rw*	**Bus Arbitration** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 0_B , receive higher priority 1_B , transmit higher priority
SWR	0	rw*	**Software Reset** *Note: rw*: Before writing the trasmitting and receiving operations should be stopped.* 1_B , reset all internal hardware except configuration registers. This signal will be cleared by AN985B/BX itself after it completed the reset process.

Transmit Demand Register

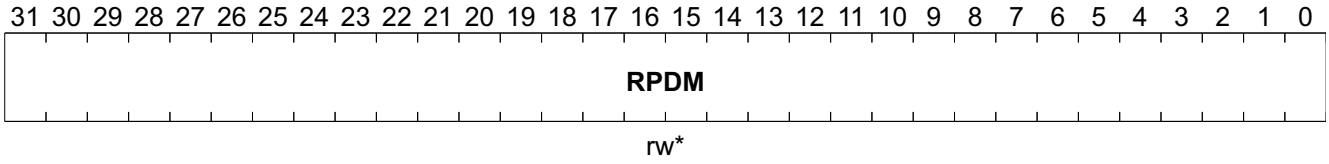
TDR_CSR1	Offset	Reset Value
Transmit Demand Register	08_H	FFFF FFFF$_H$



Field	Bits	Type	Description
TPDM	31:0	rw*	**Transmit Poll Demand** When written any value in suspended state, trigger read-tx-descriptor process and check the own-bit, if own-bit = 1, then start transmit process. *Note: rw*: Before writing the trasmitting process should be in the suspended state.*

Receive Demand Register

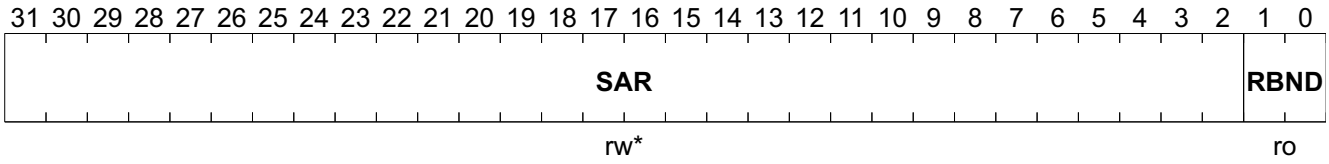
RDR_CSR2	Offset	Reset Value
Receive Demand Register	10_H	FFFF FFFF$_H$



Field	Bits	Type	Description
RPDM	31:0	rw*	**Receive Poll Demand** When written any value in suspended state, trigger the read-rx-descriptor process and check own-bit, if own- bit = 1, then start move data to buffer from FIFO. *Note: rw*: Before writing the receiving process should be in the suspended state.*

Receive Descriptor Base Address

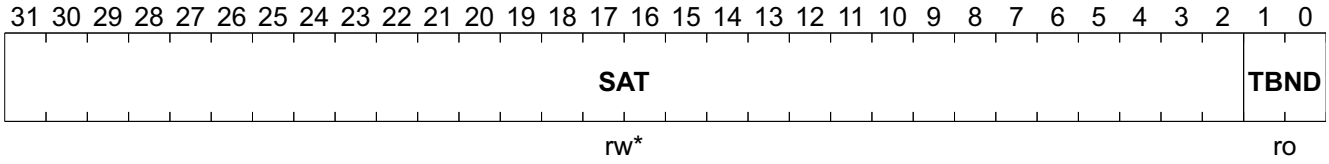
RDB_CSR3	Offset	Reset Value
Receive Descriptor Base Address	18_H	xxxx xxxx$_H$



Field	Bits	Type	Description
SAR	31:2	rw*	**Start Address of Receive Descriptor** *Note: rw*: Before writing the receiving process should be stopped.*
RBND	1:0	ro	**Must be 00, DW Boundary**

Transmit Descriptor Base Address

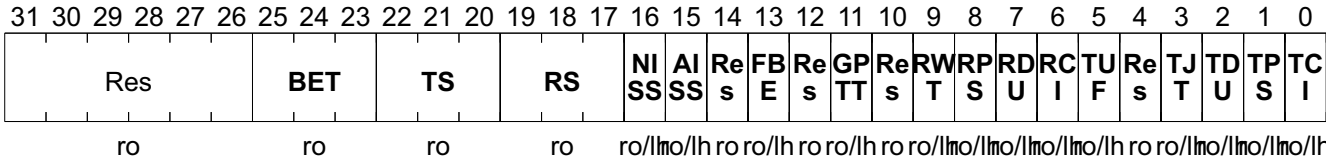
TDB_CSR4	Offset	Reset Value
Transmit Descriptor Base Address	20_H	xxxx xxxx$_H$



Field	Bits	Type	Description
SAT	31:2	rw*	**Start Address of Transmit Descriptor** *Note: rw*: Before writing the trasmitting process should be stopped.*
TBND	1:0	ro	**Must be 00, DW Boundary**

Status Register

SR_CSR5	Offset	Reset Value
Status Register	28_H	0000 0000$_H$



Field	Bits	Type	Description
Res	31:26	ro	**Reserved**
BET	25:23	ro	**Bus Error Type** This field is valid only when bit 13 of CSR5 (fatal bus error) is set. There is no interrupt generated by this field. 000_B , parity error 001_B , master abort 010_B , target abort 011_B , reserved $1xx_B$, reserved

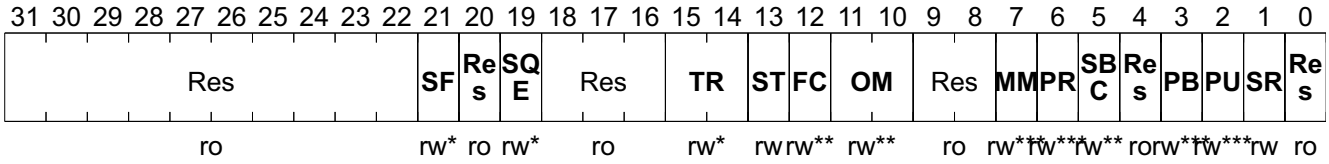
Field	Bits	Type	Description
TS	22:20	ro	**Transmit State** Report the current transmission state only, no interrupt will be generated. 000_B , stop 001_B , read descriptor 010_B , transmitting 011_B , FIFO fill read the data from memory and put into FIFO 100_B , reserved 101_B , reserved 110_B , suspended, unavailable transmit descriptor or FIFO overflow 111_B , write descriptor
RS	19:17	ro	**Receive State** Report current receive state only, no interrupt will be generated. 000_B , stop 001_B , read descriptor 010_B , check this packet and pre-fetch next descriptor 011_B , wait for receiving data 100_B , suspended 101_B , write descriptor 110_B , flush the current FIFO 111_B , FIFO drain. move data from receiving FIFO into memory
NISS	16	ro/lh	**Normal Interrupt Status Summary** It's set if any of below bits of CSR5 asserted. (Combines with bit 16 of ACSR5) bit0, transmit completed interrupt bit2, transmit descriptor unavailable bit6, receive descriptor interrupt *Note: LH = High Latching and cleared by writing 1*
AISS	15	ro/lh	**Abnormal Interrupt Status Summary** It's set if any of below bits of CSR5 asserted. (Combines with bit 15 of ACSR5) bit1, transmit process stopped bit3, transmit jabber timer time-out bit5, transmit under-flow bit7, receive descriptor unavailable bit8, receive processor stopped bit9, receive watchdog time-out bit11, general purpose timer time-out bit13, fatal bus error *Note: LH = High Latching and cleared by writing 1*
Res	14	ro	**Reserved**
FBE	13	ro/lh	**Fatal Bus Error** *Note: LH = High Latching and cleared by writing 1* 1_B , while any of parity error master abort, or target abort is occurred (see bits 25~23 of CSR5). AN985B/BX will disable all bus access. The way to recover parity error is by setting software reset.
Res	12	ro	**Reserved**

Field	Bits	Type	Description
GPTT	11	ro/lh	**General Purpose Timer Time-out** Base on CSR11 timer register. *Note: LH = High Latching and cleared by writing 1*
Res	10	ro	**Reserved**
RWT	9	ro/lh	**Receive Watchdog Time-out** Based on CSR15 watchdog timer register. *Note: LH = High Latching and cleared by writing 1*
RPS	8	ro/lh	**Receive Process Stopped** Receive state = stop *Note: LH = High Latching and cleared by writing 1*
RDU	7	ro/lh	**Receive Descriptor Unavailable** *Note: LH = High Latching and cleared by writing 1* 1_B , while the next receive descriptor can't be applied by AN985B/BX. The receive process is suspended in this situation. To restart the receive process the ownership bit of next receive descriptor should be set to AN985B/BX and a receive poll demand command should be issued (or a new recognized frame is received, if the receive poll demand is not issued).
RCI	6	ro/lh	**Receive Completed Interrupt** *Note: LH = High Latching and cleared by writing 1* 1_B , while a frame reception is completed
TUF	5	ro/lh	**Transmit Under-Flow** *Note: LH = High Latching and cleared by writing 1* 1_B , while the transmit FIFO had an under-flow condition happened during transmitting. The transmit process will enter the suspended state and report the under-flow error on bit1 of TDES0
Res	4	ro	**Reserved**
TJT	3	ro/lh	**Transmit Jabber Timer Time-out** *Note: LH = High Latching and cleared by writing 1* 1_B , while the transmit jabber timer expired. The transmit processor will enter the stop state and the transmit jabber time-out flag of bit 14 of TDES0 will be asserted
TDU	2	ro/lh	**Transmit Descriptor Unavailable** *Note: LH = High Latching and cleared by writing 1* 1_B , while the next transmit descriptor can't be applied by AN985B/BX. The transmission process is suspended in this situation. To restart the transmission process the ownership bit of next transmit descriptor should be set to AN985B/BX and if the transmit automatic polling is not enabled then a transmit poll demand command should be issued.
TPS	1	ro/lh	**Transmit Process Stopped** *Note: LH = High Latching and cleared by writing 1* 1_B , while transmit state = stop

Field	Bits	Type	Description
TCI	0	ro/lh	**Transmit Completed Interrupt** *Note: LH = High Latching and cleared by writing 1* 1_B , means a frame transmission is completed while bit 31 of TDES1 is asserted in the first transmit descriptor of the frame

Network Access Register

NAR_CSR6	Offset	Reset Value
Network Access Register	30_H	$0008\ 0040_H$

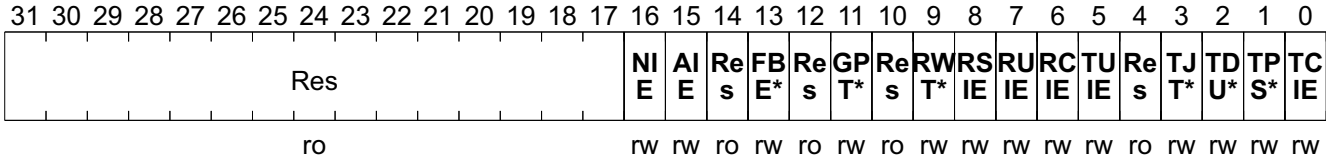


Field	Bits	Type	Description
Res	31:22	ro	**Reserved**
SF	21	rw*	**Store and Forward for Transmit** *Note: w* = only write when the transmit processor stopped.* 0_B , disable 1_B , enable ignore the transmit threshold setting
Res	20	ro	**Reserved**
SQE	19	rw*	**SQE Disable** *Note: w* = only write when the transmit processor stopped.* 0_B , enable SQE function for 10BASE-T operation. The AN985B/BX provides SQE test function for 10BASE-T half duplex operation 1_B , disable SQE function
Res	18:16	ro	**Reserved**
TR	15:14	rw*	**Transmit Threshold Control** *Note: w* = only write when the transmit processor stopped.* 00_B , 128-byte (100 Mbit/s) 72-byte (10 Mbit/s) 01_B , 256-byte (100 Mbit/s) 96-byte (10 Mbit/s) 10_B , 512-byte (100 Mbit/s) 128-byte (10 Mbit/s) 00_B , 1024-byte (100 Mbit/s) 160 -byte (10 Mbit/s)
ST	13	rw	**Stop Transmit** 0_B , stop (default) 1_B , start
FC	12	rw**	**Force Collision Mode** *Note: w** = only write when the transmit and receive processor both stopped.* 0_B , disable 1_B , generate collision when transmit (for test in loop-back mode)

Field	Bits	Type	Description
OM	11:10	rw**	**Operating Mode** *Note: w** = only write when the transmit and receive processor both stopped.* 00_B , normal 01_B , MAC loop-back 10_B , reserved 11_B , reserved
Res	9:8	ro	**Reserved**
MM	7	rw***	**Multicast Mode** *Note: w*** = only write when the receive processor stopped.* 1_B , receive all multicast packets
PR	6	rw***	**Promiscuous Mode** *Note: w*** = only write when the receive processor stopped.* 0_B , receive only the right destination address packets 1_B , receive any good packet
SBC	5	rw**	**Stop Back-off Counter** *Note: w** = only write when the transmit and receive processor both stopped.* 0_B , back-off counter is not effected by carrier 1_B , back-off counter stop when carrier is active and resume when carrier drop.
Res	4	ro	**Reserved**
PB	3	rw***	**Pass Bad Packet** *Note: w*** = only write when the receive processor stopped.* 0_B , filters all bad packets 1_B , receives any packets if pass address filter, including runt packets, CRC error, truncated packets... For receiving all bad packets, the bit 6 of CSR6 should be set to 1.
PU	2	rw***	**Pass Unicast Mode** *Note: w*** = only write when the receive processor stopped.* 1_B , back-off counter stop when carrier is active and resume when carrier drop.
SR	1	rw	**Start/Stop Receive** 0_B , receive processor will enter stop state after the current reception frame completed. This value is effective only when the receive processor is in the running or suspending state. Notice: In “Stop Receive” state the PAUSE packet and Remote Wake Up packet won’t be affected and can be received if the corresponding function is enabled. 1_B , receive processor will enter running state
Res	0	ro	**Reserved**

Interrupt Enable Register

IER_CSR7	Offset	Reset Value
Interrupt Enable Register	**38_H**	**$0000\ 0000_H$**

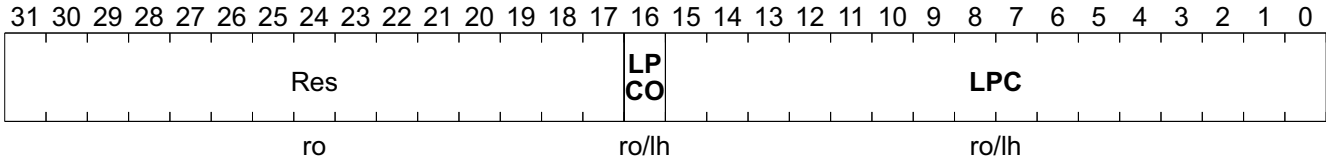


Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
NIE	16	rw	**Normal Interrupt Enable** 1_B , enable all the normal interrupt bits (see bit16 of CSR5)
AIE	15	rw	**Abnormal Interrupt Enable** 1_B , enable all the abnormal interrupt bits (see bit15 of CSR5)
Res	14	ro	**Reserved**
FBEIE	13	rw	**Fatal Bus Error Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable fatal bus error interrupt
Res	12	ro	**Reserved**
GPTIE	11	rw	**General Purpose Timer Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable general-purpose timer expired interrupt
Res	10	ro	**Reserved**
RWTIE	9	rw	**Receive Watchdog Time-out Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable receive watchdog time-out interrupt
RSIE	8	rw	**Receive Stopped Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable receive stopped interrupt
RUIE	7	rw	**Receive Descriptor Unavailable Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable receive descriptor unavailable interrupt
RCIE	6	rw	**Receive Completed Interrupt Enable** 1_B , combine this bit and bit 16 of CSR7 to enable receive completed interrupt
TUIE	5	rw	**Transmit Under-flow Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable transmit under-flow interrupt
Res	4	ro	**Reserved**
TJTTIE	3	rw	**Transmit Jabber Timer Time-out Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable transmit jabber timer time-out interrupt
TDUIE	2	rw	**Transmit Descriptor Unavailable Interrupt Enable** 1_B , combine this bit and bit 16 of CSR7 to enable transmit descriptor unavailable interrupt

Field	Bits	Type	Description
TPSIE	1	rw	**Transmit Processor Stopped Interrupt Enable** 1_B , combine this bit and bit 15 of CSR7 to enable transmit processor stopped interrupt
TCIE	0	rw	**Transmit Completed Interrupt Enable** 1_B , combine this bit and bit 16 of CSR7 to enable transmit completed interrupt.

Lost Packet Counter

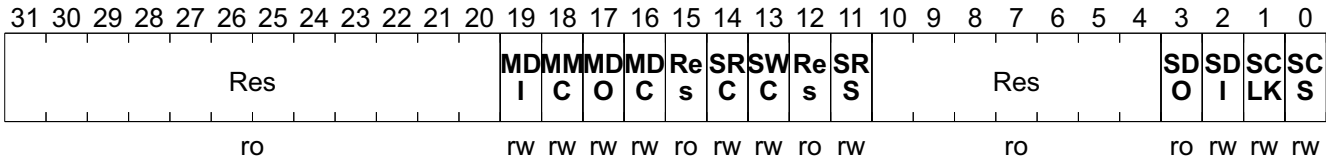
LPC_CSR8 **Offset** **Reset Value**
Lost Packet Counter **40_H** **$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
LPCO	16	ro/lh	**Lost Packet Counter Overflow** *Note: LH = High Latching and cleared by writing 1* 1_B , while lost packet counter overflowed. Cleared after read
LPC	15:0	ro/lh	**Lost Packet Counter** Increment the counter while packet discarded since there was no host receives descriptors available. Cleared after read. *Note: LH = High Latching and cleared by writing 1*

Serial Port Register

SPR_CSR9 **Offset** **Reset Value**
Serial Port Register **48_H** **$0004\ 000E_H$**

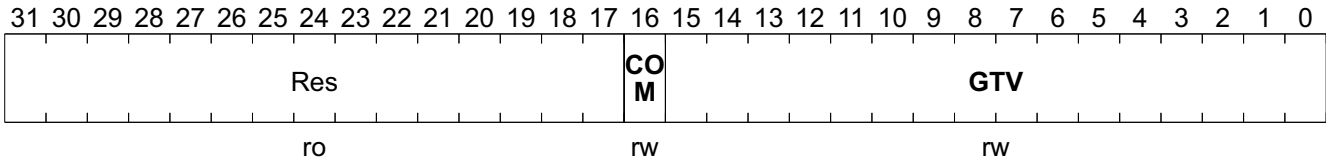


Field	Bits	Type	Description
Res	31:20	ro	**Reserved**
MDI	19	rw	**MII Management Data Input** Specified read data from the external PHY
MMC	18	rw	**MII Management Control** 0_B , Write operation to the external PHY 1_B , Read operation from the external PHY
MDO	17	rw	**MII Management Data Output** Specified Write Data to the external PHY

Field	Bits	Type	Description
MDC	16	rw	**MII Management Clock** 1_B , MII Management Clock is a output reference clock to the external PHY
Res	15	ro	**Reserved**
SRC	14	rw	**Serial EEPROM Read Control**
SWC	13	rw	**Serial EEPROM Write Control**
Res	12	ro	**Reserved**
SRS	11	rw	**Serial EEPROM Select**
Res	10:4	ro	**Reserved**
SDO	3	ro	**Serial EEPROM Data Out** This bit serially shifts data from the EEPROM to the AN985B/BX.
SDI	2	rw	**Serial EEPROM Data In** This bit serially shifts data from the AN985B/BX to the EEPROM.
SCLK	1	rw	**Serial EEPROM Clock** High/Low this bit to provide the clock signal for EEPROM.
SCS	0	rw	**Serial EEPROM Chip Select** 1_B , selects the serial EEPROM chip

General-Purpose Timer

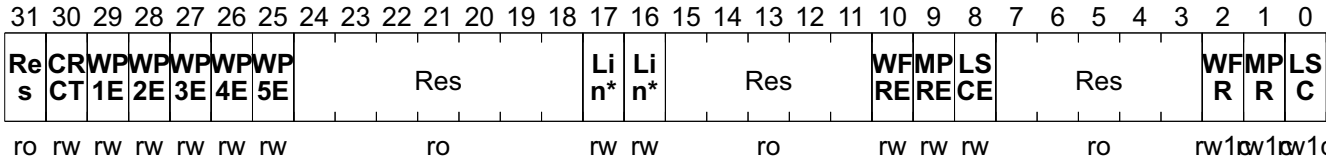
TMR_CSR11	Offset	Reset Value
General-Purpose Timer	**58_H**	**0000 0000$_H$**



Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
COM	16	rw	**Continuous Operation Mode** 1_B , sets the general-purpose timer in continuous operating mode
GTV	15:0	rw	**General-Purpose Timer Value** Sets the counter value. This is a countdown counter with the cycle time of 204 μ s.

Wake-up Control/Status Register

WCSR_CSR13	Offset	Reset Value
Wake-up Control/Status Register	**68_H**	**0000 00??$_H$**



Field	Bits	Type	Description
Res	31	ro	**Reserved**
CRCT	30	rw	**CRC-16 Type** 0_B , Initial contents = 0000h 1_B , Initial contents = FFFFh
WP1E	29	rw	**Wake-up Pattern n Matched Enable** n = 1 to 5
WP2E	28	rw	
WP3E	27	rw	
WP4E	26	rw	
WP5E	25	rw	
Res	24:18	ro	**Reserved**
LinkOFF	17	rw	**Link Off Detect Enable** The AN985B/BX will set the LSC bit of CSR13 after it has detected that link status is from ON to OFF.
LinkON	16	rw	**Link On Detect Enable** The AN985B/BX will set the LSC bit of CSR13 after it has detected that link status is from OFF to ON.
Res	15:11	ro	**Reserved**
WFRE	10	rw	**Wake-up Frame Received Enable** The AN985B/BX will include the “Wake-up Frame Received” event into wake-up events. If this bit is set, AN985B/BX will assert PMES bit of PMR1 after AN985B/BX has received a matched wake-up frame.
MPRE	9	rw	**Magic Packet Received Enable** The AN985B/BX will include the “Magic Packet Received” event into wake-up events. If this bit is set, AN985B/BX will assert PMES bit of PMR1 after AN985B/BX has received a Magic packet.
LSCE	8	rw	**Link Status Changed Enable** The AN985B/BX will include the “Link Status Changed” event into wake-up events. If this bit is set, AN985B/BX will assert PMES bit of PMR1 after AN985B/BX has detected a link status changed event.
Res	7:3	ro	**Reserved**
WFR	2	rw1c	**Wake-up Frame Received** *Note: rw1c: Read only and Write one cleared.* 1_B , Indicates AN985B/BX has received a wake-up frame. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset

Field	Bits	Type	Description
MPR	1	rw1c	**Magic Packet Received** *Note: rw1c: Read only and Write one cleared.* 1_B , Indicates AN985B/BX has received a magic packet. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset
LSC	0	rw1c	**Link Status Changed** *Note: rw1c: Read only and Write one cleared.* 1_B , Indicates AN985B/BX has detected a link status change event. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset

CSR14, WPDR – Wake-up Pattern Data Register

All six wake-up patterns filtering information are programmed through WPDR register. The filtering information is as follows:

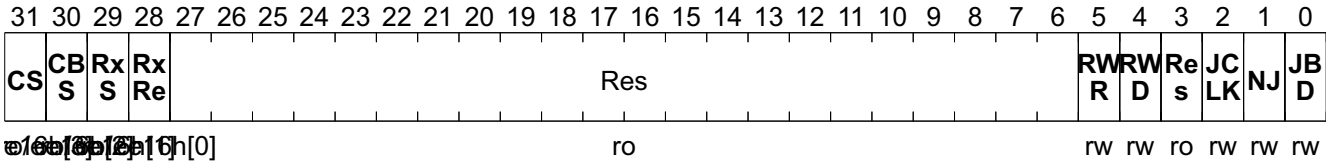
Offset	31-24	23-16	15-8	7-0
0000h	Wake-up pattern 1 mask bits 31:0			
0004h	Wake-up pattern 1 mask bits 63:32			
0008h	Wake-up pattern 1 mask bits 95:64			
000ch	Wake-up pattern 1 mask bits 127:96			
0010h	CRC16 of pattern 1		Reserved	Wake-up pattern 1 offset
0014h	Wake-up pattern 2 mask bits 31:0			
0018h	Wake-up pattern 2 mask bits 63:32			
001ch	Wake-up pattern 2 mask bits 95:64			
0020h	Wake-up pattern 2 mask bits 127:96			
0024h	CRC16 of pattern 2		Reserved	Wake-up pattern 2 offset
0028h	Wake-up pattern 3 mask bits 31:0			
002ch	Wake-up pattern 3 mask bits 63:32			
0030h	Wake-up pattern 3 mask bits 95:64			
0034h	Wake-up pattern 3 mask bits 127:96			
0038h	CRC16 of pattern 3		Reserved	Wake-up pattern 3 offset
003ch	Wake-up pattern 4 mask bits 31:0			
0040h	Wake-up pattern 4 mask bits 63:32			
0044h	Wake-up pattern 4 mask bits 95:64			
0048h	Wake-up pattern 4 mask bits 127:96			
004ch	CRC16 of pattern 4		Reserved	Wake-up pattern 4 offset
0050h	Wake-up pattern 5 mask bits 31:0			
0054h	Wake-up pattern 5 mask bits 63:32			
0058h	Wake-up pattern 5 mask bits 95:64			
005ch	Wake-up pattern 5 mask bits 127:96			
0060h	CRC16 of pattern 5		Reserved	Wake-up pattern 5 offset

1. CRC-16 polynomial: still pending

2. Offset value is from 0-255 (8-bit width).
3. To load the whole wake-up frame-filtering information, consecutive 25 long words write operation to CSR14 should be done.

Watchdog Timer

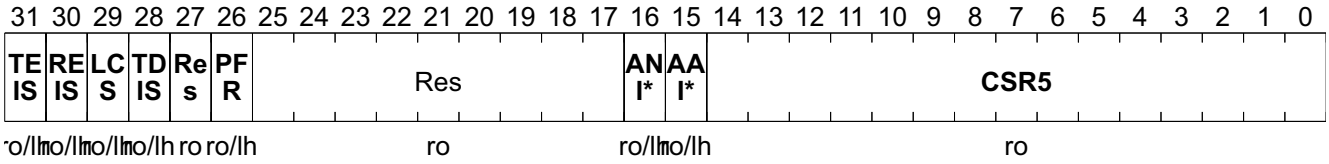
WTMR_CSR15	Offset	Reset Value
Watchdog Timer	78_H	$0000\ 0000_H$



Field	Bits	Type	Description
CS	31	ro/ee16h[3]	**Clock Save Mode** 0_B , clock stuck at 0 when clock save mode enable 1_B , clock stuck at 1 when clock save mode enable
CBS	30	ro/ee16h[2]	**CARDBUS Save Mode** 1_B , CARDBUS clock save mode enable
RxS	29	ro/ee16h[1]	**Rx Save Mode** 1_B , RX save mode enable
RxRe	28	ro/ee16h[0]	**Rx Clock Reverse Mode** 1_B , reverse (for NS HomePHY mode)
Res	27:6	ro	**Reserved**
RWR	5	rw	**Receive Watchdog Release** The time of release watchdog timer from last carrier deserted. 0_B , 24 bit-time 1_B , 48 bit-time
RWD	4	rw	**Receive Watchdog Disable** 0_B , If the receiving packet's length is longer than 2560 bytes the watchdog timer will be expired 1_B , disable the receive watchdog
Res	3	ro	**Reserved**
JCLK	2	rw	**Jabber Clock** 0_B , cut off transmission after 2.6 ms (100 Mbit/s) or 26 ms (10 Mbit/s) 1_B , cut off transmission after 2560 byte-time
NJ	1	rw	**Non-Jabber** 0_B , if jabber expired re-enable transmit function after 42 ms (100 Mbit/s) or 420 ms (10 Mbit/s) 1_B , immediately re-enable the transmit function after jabber expired
JBD	0	rw	**Jabber Disable** 1_B , disable transmit jabber function

Assistant CSR5 (Status Register 2)

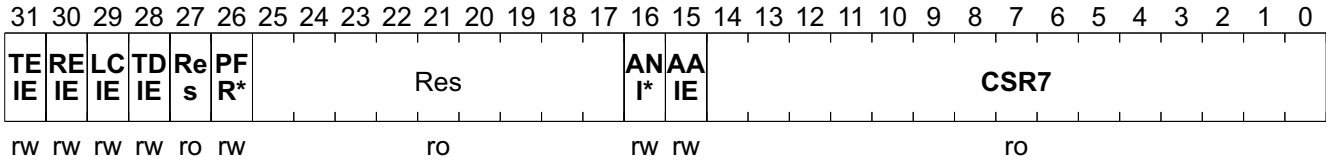
ACSR5_CSR16	Offset	Reset Value
Assistant CSR5 (Status Register 2)	**80_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
TEIS	31	ro/lh	**Transmit Early Interrupt Status** Transmit early interrupt status is set to 1 when Transmit early interrupt function is enabled (set bit 31 of CSR17 = 1) and the transmitted packet is moved completed from descriptors to TX-FIFO buffer. This bit is cleared by written with 1. *Note: LH = High Latching and cleared by writing 1*
REIS	30	ro/lh	**Receive Early Interrupt Status** Receive early interrupt status is set to 1 when Receive early interrupt function is enabled (set bit 30 of CSR17 = 1) and the received packet is fill up its first receive descriptor. This bit is cleared by written with 1. *Note: LH = High Latching and cleared by writing 1*
LCS	29	ro/lh	**Status of Link Status Change** *Note: LH = High Latching and cleared by writing 1*
TDIS	28	ro/lh	**Transmit Deferred Interrupt Status** *Note: LH = High Latching and cleared by writing 1*
Res	27	ro	**Reserved**
PFR	26	ro/lh	**PAUSE Frame Received Interrupt Status** *Note: LH = High Latching and cleared by writing 1* 1_B , indicates a PAUSE frame received when the PAUSE function is enabled
Res	25:17	ro	**Reserved**
ANISS	16	ro/lh	**Added Normal Interrupt Status Summary** *Note: LH = High Latching and cleared by writing 1* 1_B , any of the added normal interrupts happened
AAISS	15	ro/lh	**Added Abnormal Interrupt Status Summary** *Note: LH = High Latching and cleared by writing 1* 1_B , any of added abnormal interrupt happened
CSR5	14:0	ro	**This bits are the same as CSR5** You can access those status bits through either CSR5 or CSR16

Assistant CSR7 (Interrupt Enable Register 2)

ACSR7_CSR17	Offset	Reset Value
Assistant CSR7 (Interrupt Enable Register 2)	**84_H**	**$0000\ 0000_H$**



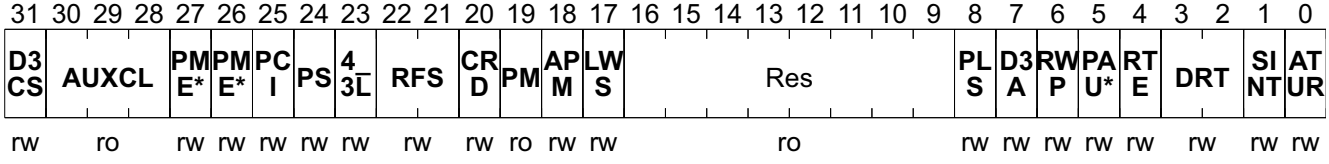
Field	Bits	Type	Description
TEIE	31	rw	**Transmit Early Interrupt Enable**
REIE	30	rw	**Receive Early Interrupt Enable**
LCIE	29	rw	**Link Status Change Interrupt Enable**
TDIE	28	rw	**Transmit Deferred Interrupt Enable**
Res	27	ro	**Reserved**
PFRIE	26	rw	**PAUSE Frame Received Interrupt Enable**
Res	25:17	ro	**Reserved**
ANISE	16	rw	**Added Normal Interrupt Summary Enable** 1_B , adds the interrupts of bit 30 and 31 of ACSR7 to the normal interrupt summary (bit 16 of CSR5)
AAIE	15	rw	**Added Abnormal Interrupt Summary Enable** 1_B , adds the interrupt of bit 26, 28 and 29 of ACSR7 to the abnormal interrupt summary
CSR7	14:0	ro	**This bits are the same as CSR7** You can access those status bits through either CSR7 or CSR16

Command Register

Bit 31 to Bit 16

Automatically recall from EEPROM

CR_CSR18	Offset	Reset Value
Command Register	**88_H**	**$A04C\ 0004_H$**



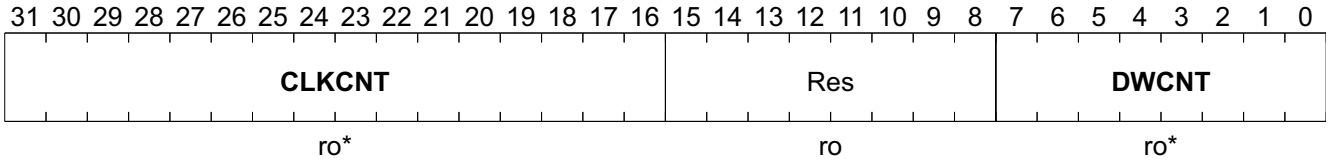
Field	Bits	Type	Description
D3CS	31	rw	**D3cold Support, Mapped to CR48<31>**

Field	Bits	Type	Description
AUXCL	30:28	ro	**Aux Current** Should be 0.
PMEPS	27	rw	**PMEP Select** 0_B , positive pulse 1_B , negative pulse
PMEPE	26	rw	**PMEP Pin Enable** 0_B , disable(for old board) 1_B , enable
PCI	25	rw	**PCI Pad** 0_B , apply CARDBUS Pad in CARDBUS Mode. No effect in PCI Mode 1_B , apply PCI Pad in CARDBUS Mode(for twinhead notebook)
PS	24	rw	**PMES Sticky** 0_B , pmez auto de-asserted: pmez will be disasserted by power up after wakeup event trigger. 1_B , pmez sticky: Vcc_detect has no impact to pmez disasserts
4_3L	23	rw	**4_3LED** 0_B , 3 LED scheme 1_B , 4 LED scheme
RFS	22:21	rw	**Receive FIFO Size Control** 00_B , reserved 01_B , reserved 10_B , 2K 11_B , 1K
CRD	20	rw	**Clock Run (clk-run pin) Disable** 1_B , disables the function of clock run supports to CARDBUS
PM	19	ro	**Power Management** Enables the AN985B/BX whether to activate the Power Management abilities. When this bit is set into “0” the AN985B/BX will set the Cap_Ptr register to zero, indicating no CARDBUS compliant power management capabilities.The value of this bit will be mapped to NC-bit 20 of CR1.In CARDBUS Power Management mode, the Wake-up events include “Wake-up Frame Received”, “Magic Packet Received” and “Link Status Changed” depends on the CSR13 settings.
APM	18	rw	**APM Mode** This bit is effective when PM (csr18 [19]) = 1.
LWS	17	rw	**Should be 0**
Res	16:9	ro	**Reserved**
PLS	8	rw	**PMEP Pulse Length Select** 0_B , long pulse 50ms 1_B , short pulse 100us for test purpose
D3A	7	rw	**D3_cold APM Mode Enable** PMEZ can be asserted without the impact of PME_EN
RWP	6	rw	**Reset Wake-up Pattern Data Register Pointer** 0_B , Normal 1_B , Reset

Field	Bits	Type	Description
PAUSE	5	rw	**PAUSE Function Control** To disable or enable the PAUSE function for flow control. The default value of PAUSE is decided by the result of Auto-Negotiation. Driver can force to enable or disable it after the Auto-Negotiation completed. 0_B , PAUSE function is disabled 1_B , PAUSE function is enabled
RTE	4	rw	**Receive Threshold Enable** 0_B , disable the receive FIFO threshold selection in bit 3~2 of this register, the receive threshold is set to 64-byte. 1_B , the receive FIFO threshold is enabled
DRT	3:2	rw	**Drain Receive Threshold** 00_B , 32 bytes (8 DW) 01_B , 64 bytes (16 DW) 10_B , store-and -forward 11_B , reserved
SINT	1	rw	**Software Interrupt**
ATUR	0	rw	**Automatically Transmit-Underrun Recovery** 1_B , enable automatically transmit-underrun recovery

CARDBUS Bus Performance Counter

CARDBUSC_CSR19	Offset	Reset Value
CARDBUS Bus Performance Counter	$8C_H$	$0000\ 0000_H$



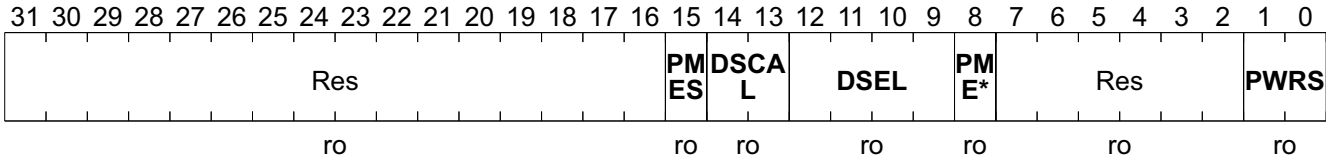
Field	Bits	Type	Description
CLKCNT	31:16	ro*	**Clock Count** The number of CARDBUS clock from read request asserted to access completed. This CARDBUS clock number is accumulated all the read command cycles from last CSR19 read to current CSR19 read. *Note: ro*: Read only and cleared by reading*
Res	15:8	ro	**Reserved**
DWCNT	7:0	ro*	**Double Word Count** The number of double word accessed by the last bus master. This double word number is accumulated all the bus master data transactions from last CSR19 read to current CSR19 read. *Note: ro*: Read only and cleared by reading*

ro = Read only and cleared by reading

Power Management Command and Status

(The same register value mapping to CR49-PMR1)

PMCSR_CSR20	Offset	Reset Value
Power Management Command and Status	90_H	$0000\ 0000_H$

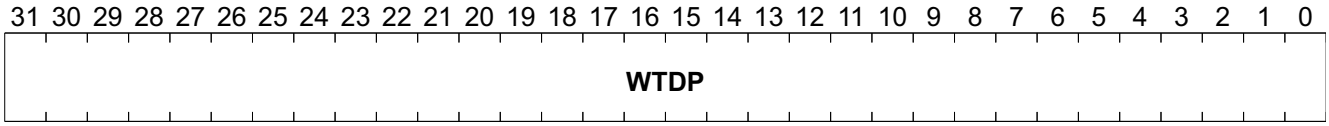


Field	Bits	Type	Description
Res	31:16	ro	**Reserved**

Field	Bits	Type	Description
PMES	15	ro	**PME_Status** This bit is set when the AN985B/BX would normally assert the PME# signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a “1” to this bit will clear it and cause the AN985B/BX to stop asserting a PME# (if enabled). Writing a “0” has no effect. Since the AN985B/BX doesn’t supports PME# from D3cold, this bit is defaulted to “0”.
DSCAL	14:13	ro	**Data_Scale** Indicates the scaling factor to be used when interpreting the value of the Data register. This field is required for any function that implements the Data register. Otherwise, it’s optional.The AN985B/BX doesn’t support Data register and Data_Scale.
DSEL	12:9	ro	**Data_Select** This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. This field is required for any function that implements the Data register. The AN985B/BX doesn’t support Data_Select.
PME_En	8	ro	**PME_En** “1” enables the AN985B/BX to assert PME#. When “0” disables the PME# assertion.This bit defaults to “0” if the function does not support PME# generation from D3cold.
Res	7:2	ro	**Reserved**
PWRS	1:0	ro	**PowerState** This two bit field is used both to determine the current power state of the AN985B/BX and to set the AN985B/BX into a new power state. The definition of this field is given below. 00_B - D0 01_B - D1 10_B - D2 11_B - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus, however the data is discarded a no state change occurs.

Current Working Transmit Descriptor Pointer

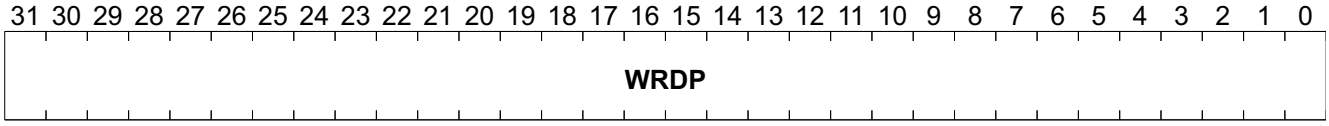
WTDP_CSR21	Offset	Reset Value
Current Working Transmit Descriptor Pointer	94_H	xxxx xxxx$_H$



Field	Bits	Type	Description
WTDP	31:0	ro	**Working Transmit Descriptor Pointer** The current working transmit descriptor pointer for driver's double-checking or other special purpose.

Current Working Receive Descriptor Pointer

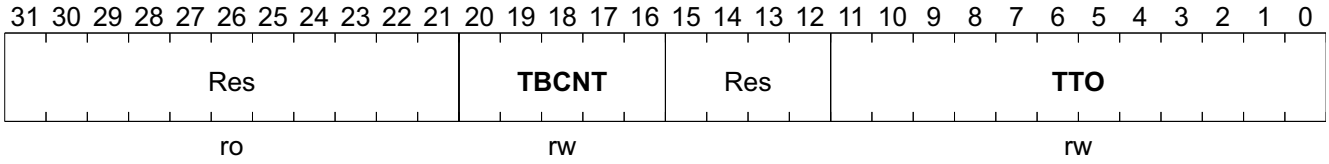
WRDP_CSR22	Offset	Reset Value
Current Working Receive Descriptor Pointer	98_H	xxxx xxxx$_H$



Field	Bits	Type	Description
WRDP	31:0	ro	**Working Receive Descriptor Pointer** The current working receive descriptor pointer for driver's double-checking or other special purpose.

Transmit Burst Count/Time-out

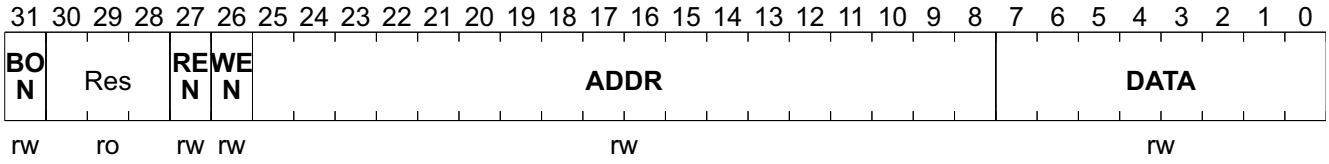
TXBR_CSR23 | **Offset** | **Reset Value**
Transmit Burst Count/Time-out | **$9C_H$** | **0000 0000$_H$**



Field	Bits	Type	Description
Res	31:21	ro	**Reserved**
TBCNT	20:16	rw	**Transmit Burst Count** After this number of consecutive successful transmit, transmit completed interrupt will be generated. Continuously do this function if no reset.
TTO	11:0	rw	**Transmit Time-Out = (deferred time + back-off time)** When the TDIE (bit28 of ACSR7) is set, the timer is decreased in unit of 2.56 μ s (100M) or 25.6 μ s (10M). If the timer expires before another packet transmit begin, then the TDIE interrupt will be generated.

Flash ROM (also the boot ROM) Port

FROM_CSR24 | **Offset** | **Reset Value**
Flash ROM (also the boot ROM) Port | **$A0_H$** | **8000 0000$_H$**



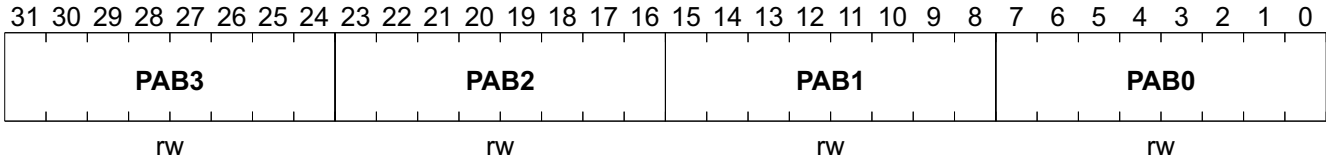
Field	Bits	Type	Description
BON	31	rw	**Bra16_on** This bit is no effective when 3_LED scheme applied. Driver needs to program this bit when 4_LED applied especially when boot rom read. 0_B , bra[16]=fd/col LED path 1_B , no effect to bar[16]
Res	30:28	ro	**Reserved**
REN	27	rw	**Read Enable** Clear if read data is ready in DATA, bit7-0 of FROM.
WEN	26	rw	**Write Enable** Cleared if write completed.

Field	Bits	Type	Description
ADDR	25:8	rw	**Flash ROM Address**
DATA	7:0	rw	**Read/Write Data of Flash ROM**

Physical Address Register 0

Automatically recall from EEPROM

PAR0_CSR25	Offset	Reset Value
Physical Address Register 0	**$A4_H$**	**xxxx xxxx$_H$**

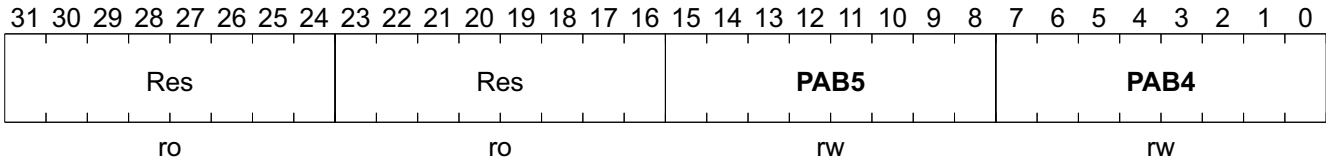


Field	Bits	Type	Description
PAB3	31:24	rw	**Physical Address Byte n** n = 0 to 3
PAB2	23:16	rw	
PAB1	15:8	rw	
PAB0	7:0	rw	

Physical Address Register 1

Automatically recall from EEPROM

PAR1_CSR26	Offset	Reset Value
Physical Address Register 1	**$A8_H$**	**xxxx xxxx$_H$**



Field	Bits	Type	Description
Res	31:24	ro	**Reserved**
Res	23:16	ro	**Reserved**
PAB5	15:8	rw	**Physical Address Byte 5**
PAB4	7:0	rw	**Physical Address Byte 4**

For example, physical address = 00-00-e8-11-22-33

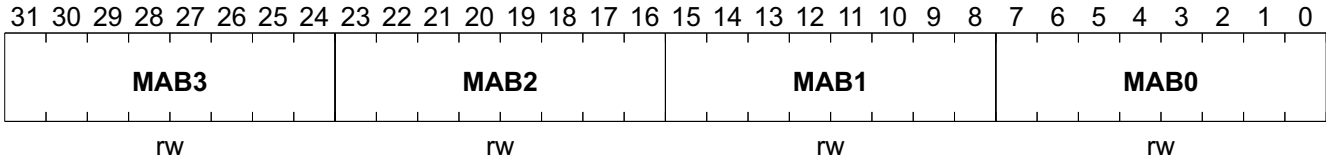
PAR0 = 11 e8 00 00

PAR1 = xx xx 33 22

PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bit19-17 = 000).

Multicast Address Register 0

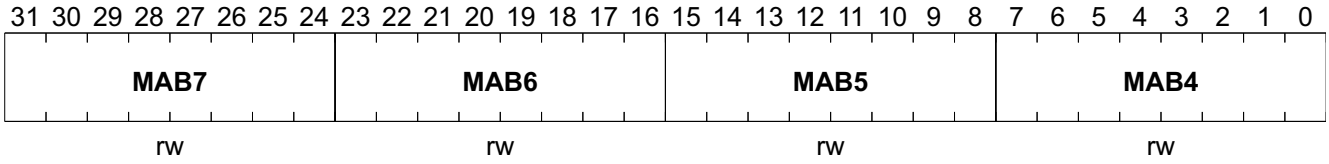
MAR0_CSR27	Offset	Reset Value
Multicast Address Register 0	AC_H	$0000\ 0000_H$



Field	Bits	Type	Description
MAB3	31:24	rw	**Multicast Address Byte n**
MAB2	23:16	rw	n = 0 to 3
MAB1	15:8	rw	
MAB0	7:0	rw	

Multicast Address Register 1

MAR1_CSR28	Offset	Reset Value
Multicast Address Register 1	$B0_H$	$0000\ 0000_H$

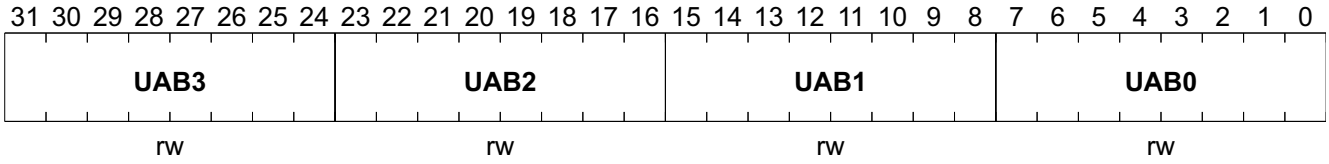


Field	Bits	Type	Description
MAB7	31:24	rw	**Multicast Address Byte 7 (hash table 63:56)**
MAB6	23:16	rw	**Multicast Address Byte 6 (hash table 55:48)**
MAB5	15:8	rw	**Multicast Address Byte 5 (hash table 47:40)**
MAB4	7:0	rw	**Multicast Address Byte 4 (hash table 39:32)**

MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bit19-17 = 000)

Unicast Address Register 0

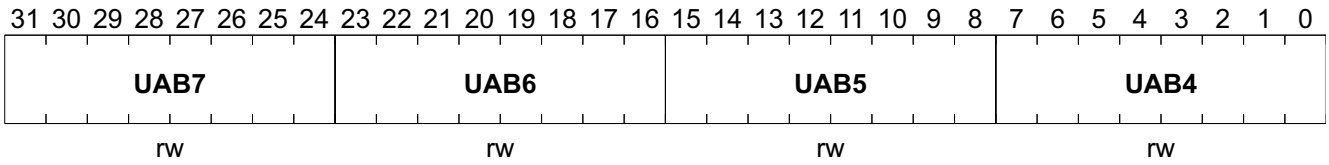
UAR0_CSR_29	Offset	Reset Value
Unicast Address Register 0	$B4_H$	$0000\ 0000_H$



Field	Bits	Type	Description
UAB3	31:24	rw	**Unicast Address Byte 3 (hash table 31:24)**
UAB2	23:16	rw	**Unicast Address Byte 2 (hash table 23:16)**
UAB1	15:8	rw	**Unicast Address Byte 1 (hash table 15:8)**
UAB0	7:0	rw	**Unicast Address Byte 0 (hash table 7:0)**

Unicast Address Register 1

UAR1_CSR_30	Offset	Reset Value
Unicast Address Register 1	$B8_H$	$0000\ 0000_H$



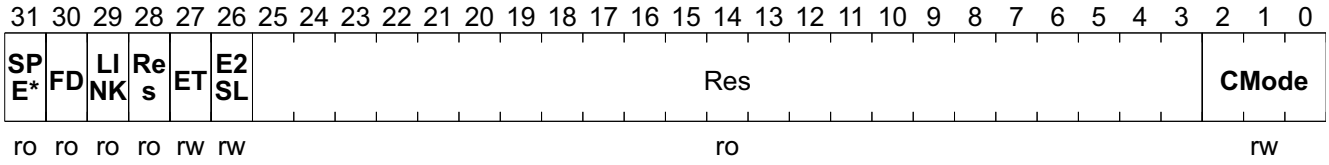
Field	Bits	Type	Description
UAB7	31:24	rw	**Unicast Address Byte 7 (hash table 63:56)**
UAB6	23:16	rw	**Unicast Address Byte 6 (hash table 55:48)**
UAB5	15:8	rw	**Unicast Address Byte 5 (hash table 47:40)**
UAB4	7:0	rw	**Unicast Address Byte 4 (hash table 39:32)**

Unicast64 Algorithm

The algorithm is the same with multicast64.

Operation Mode Register

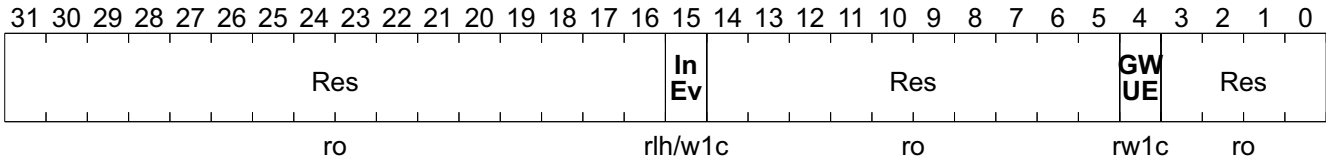
OMR	Offset	Reset Value
Operation Mode Register	FC_H	$0000\ 0007_H$



Field	Bits	Type	Description
SPEED	31	ro	**Network Speed Status** 0_B , 10M 1_B , 100M
FD	30	ro	**Full/Half Duplex Status** 0_B , Half duplex 1_B , Full duplex
LINK	29	ro	**Network Link Status** 0_B , Link off 1_B , Link OK
Res	28	ro	**Reserved**
ET	27	rw	**ET** 0_B , 9346 1_B , 9366
E2SL	26	rw	**E2prom_Soft_Load** Write 1 to reload e2prom
Res	25:3	ro	**Reserved**
CMode	2:0	rw	**Chip Mode** These three bits are used to configure AN985B/BX's chip mode: 111_B , normal mode 110_B , monitor mode 100_B , HOME PNA mode 001_B , phy only mode 101_B , HP94000tester mode(vaux, vcc_detect will be internal forced to 1_B, and muxed with poweron_reset input and ssram_rdy)

Function Event Register

FER	Offset	Reset Value
Function Event Register	**100_H**	**$0000\ 0000_H$**

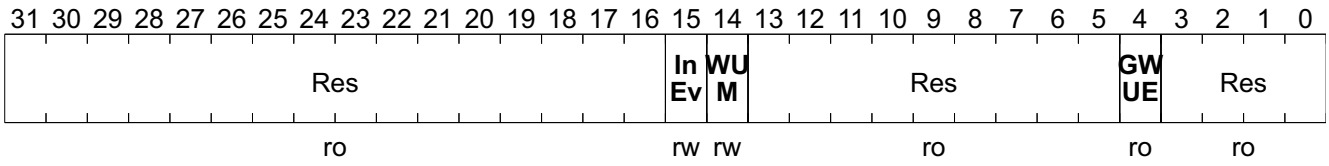


Field	Bits	Type	Description
Res	31:16	ro	**Bits[31:16] are reserved in the CARDBUS Specification**

Field	Bits	Type	Description
InEv	15	rlh/w1c	**Interrupt Event** This bit is used for as the interrupt bit. It is set when the Ethernet interrupt source is set,regardless of the mask value. It is cleared when the OS writes 1_B to the field and the interrupt source has been serviced. Writing 0_B to the field has no effect.
Res	14:5	ro	**Bits[14:5] are reserved in the CARDBUS Specification**
GWUE	4	rw1c	**General Wake-up Event** This bit is used for general wake-up. It is set when the Ethernet wake-up source is set, regardless of the mask value. Writing 1_B to the field clears this bit and the PME status bit in the PMCSR. Writing 0_B to the field has no effect. Note that writing 1_B to the PME status bit in the PMCSR has the same effect. *Note: rw1c: Read only and Write one cleared.*
Res	3:0	ro	**Bits[3:0] are reserved in the CARDBUS Specification**

Function Event Mask Register

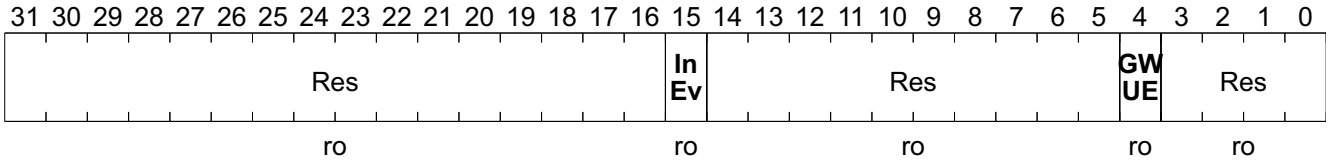
FEMR	Offset	Reset Value
Function Event Mask Register	**104_H**	**$0000\ 8000_H$**



Field	Bits	Type	Description
Res	31:16	ro	**Bits[31:16] are reserved in the CARDBUS Specification**
InEv	15	rw	**Interrupt Event** This bit is the interrupt mask. When the bit equals 0_B, it masks the Ethernet function CSTSCHG signal bit has no effect on the Function Event Register. This bit is dependent on bit 4 of this register.
WUM	14	rw	**Wake-Up Mask** When the bit equals 0_B, it masks the Ethernet function INTA# line bus has no effect on the Function Event Register. The interrupt mask
Res	13:5	ro	**Bits[14:5] are reserved in the CARDBUS Specification**
GWUE	4	ro	**General Wake-up Event** This bit is the general wake-up mask. When the bit equals 0_B, it masks Ethernet function wake-up events towards the CSTSCHG signal. It has no effect on the Function Event register. The AN985B/BX can assert the CSTSCHG signal in the following configuration of masked bits:wake-up bit AND general wake-up bit, or PME Enable bit in the PMCSR register only.
Res	3:0	ro	**Bits[3:0] are reserved in the CARDBUS Specification**

Function Present State Register

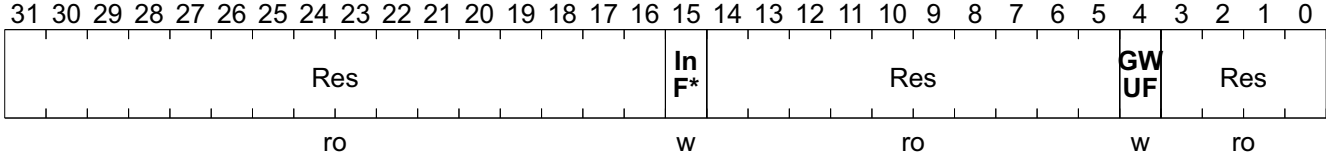
FPSR	Offset	Reset Value
Function Present State Register	108_H	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:16	ro	**Bits[31:16] are reserved in the CARDBUS Specification**
InEv	15	ro	**Interrupt Event** This bit is used for interrupts. It reflects the current state of the Ethernet source of the interrupt regardless of the mask value. It is set when the Ethernet function hasa pending interrupt and cleared when the software driver acknowledges all active interrups through the SCB Command Word.
Res	14:5	ro	**Bits[14:5] are reserved in the CARDBUS Specification**
GWUE	4	ro	**General Wake-up Event** This bit is used for general wake-up. It reflects the current state of the Ethernet source of CSTSCHG. It is a logical OR reseult of the gated three most significant bits in the PMDR: Link Status change bit is gated by the Link Status Change Wake Enable bit in the Configuration command. The Magic Packet bit is gated by the Magic Packet Wake-up disable bit in the Configuration command. The Interesting Packet bit is gated by the programmable filter command.
Res	3:0	ro	**Bits[3:0] are reserved in the CARDBUS Specification**

Function Force Event Register

FFER	Offset	Reset Value
Function Force Event Register	$10C_H$	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:16	ro	**Bits[31:16] are reserved in the CARDBUS Specification**

Field	Bits	Type	Description
InFor	15	w	**Interrupt Force** This bit is used for interrupts. Writing 1_B in the field will set the interrupt bit in the Function Event register. If the INTA# pin is not masked, then it will also be actived. Writing 0_B to the field has no effect.
Res	14:5	ro	**Bits[14:5] are reserved in the CARDBUS Specification**
GWUF	4	w	**General Wake-up Force** This bit is used for general wake-up. Writing 1_B in the field will set the CSTSCHG bit in the Function Event register. If the CSTSCHG pin is not masked, then it will also be actived. Writing 0_B to the field has no effect
Res	3:0	ro	**Bits[3:0] are reserved in the CARDBUS Specification**

8.3 PHY Registers

Table 14 Registers Address Space

Module	Base Address	End Address	Note
PHY	0000 0000_H	0000 0006_H	

Table 15 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
R0	Register 0(MII Control)	0_H	83
R1	Register 1(Status)	1_H	85
R2	Register 2	2_H	87
R3	Register 3	3_H	87
R4	Register 4	4_H	88
R5	Register 5	5_H	89
R6	Register 6	6_H	90

The register is addressed wordwise.

Standard abbreviations:

Table 16 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)

Table 16 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

8.3.1 PHY Transceiver Registers Descriptions

Register 0

MII Control

R0	Offset	Reset Value
Register 0(MII Control)	0_H	1000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	**LOOP**	**SPEED**	**ANE**	**PD**	**IS**	**RAN**	**DM**	**CT**	Res						
rwsc	rw	rw	rw	rw	rw	rwsc	rw	ro	ro						

Field	Bits	Type	Description
RESET	15	rwsc	**Reset** 0_B , normal operation 1_B , PHY Reset
LOOP	14	rw	**Loopback** 0_B , disable loopback 1_B , enable loopback

Field	Bits	Type	Description
SPEED	13	rw	**Speed Selection** 0_B , 10 Mbit/s 1_B , 100 Mbit/s
ANE	12	rw	**Autonegotiation Enable** 0_B , disable autoneg 1_B , enable autoneg
PD	11	rw	**Power Down** 0_B , normal operation 1_B , Power Down
IS	10	rw	**Isolate** 0_B , normal operation 1_B , isolate PHY from MII
RAN	9	rwsc	**Restart Autonegotiation** 1_B , Restart Autoneg
DM	8	rw	**Duplex Mode** 0_B , half duplex 1_B , full duplex
CT	7	ro	**Collision Test** Not implemented
Res	6:0	ro	**Reserved**

SC: Self Clearing

Reset: Reset this port only. This will cause the following:

1. Restart the autonegotiation process.
2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesizers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

Loopback: Loop back of transmit data to receive via a path as close to the wire as possible. When set inhibits actual transmission on the wire.

Speed selection: Forces speed of Phy only when autonegotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of autoneg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence.

Restart Negotiation: only has effect when autonegotiating. Restarts state machine.

Power down: Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate: Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode: When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision test: Always 0 because collision signal is not implemented.

Register 1

Status

R1	Offset	Reset Value
Register 1(Status)	1_H	7849_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100B T4	**100B FD**	**100B HD**	**10FD**	**10HD**	**100B T2FD**	**100B T2HD**	Res		**MFPS**	**AC**	**RF**	**AA**	**LS**	**JD**	**EC**
ro	ro	ro	ro	ro	ro	ro	ro		ro	ro	ro, lh	ro	ro, ll	ro, lh	ro

Field	Bits	Type	Description
100BT4	15	ro	**100 BASE T4** Not supported
100BFD	14	ro	**100 BASE-X Full Duplex** 0_B , PHY is not 100BASE-X full duplex capable 1_B , PHY is 100BASE-X full duplex capable
100BHD	13	ro	**100BASE-X Half Duplex** 0_B , PHY is not 100BASE-X half duplex capable 1_B , PHY is 100BASE-X half duplex capable
10FD	12	ro	**10 Mbit/s Full Duplex** 0_B , PHY is not 10 Mbit/s/s Full duplex capable 1_B , PHY is 10 Mbit/s/s Full duplex capable
10HD	11	ro	**10 Mbit/s Half Duplex** 0_B , PHY is not 10 Mbit/s/s Half duplex capable 1_B , PHY is 10 Mbit/s/s Half duplex capable
100BT2FD	10	ro	**100BASE-T2 Full Duplex** Not supported
100BT2HD	9	ro	**100BASE-T2 Half Duplex** Not supported
Res	8:7	ro	**Reserved**
MFPS	6	ro	**MF Preamble Suppression** 0_B , PHY cannot accept management frames with preamble suppression 1_B , PHY can accept management frames with preamble suppression
AC	5	ro	**Autoneg Complete** 0_B , autoneg incomplete 1_B , autoneg completed
RF	4	ro, lh	**Remote Fault** *Note: lh: Latch High* 0_B , no remote fault detected 1_B , remote fault detected

Field	Bits	Type	Description
AA	3	ro	**Autoneg Ability** 0_B , PHY cannot auto-negotiate 1_B , PHY can auto-negotiate
LS	2	ro, ll	**Link Status** *Note: lh: Latch Low* 0_B , link is down 1_B , link is up
JD	1	ro, lh	**Jabber Detect** Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode. *Note: lh: Latch High* 1_B , jabber condition detected
EC	0	ro	**Extended Capability** 0_B , basic register set capabilities only 1_B , extended register capabilities

Register 2 and 3

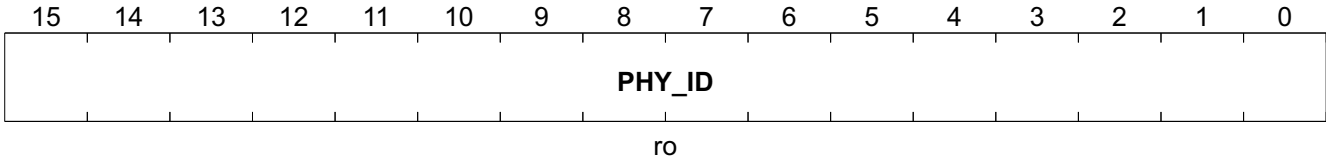
Each PHY has an unique identifier, which is assigned to the device.

The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organizationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1.

There is physically only one of each of these registers for all six network(MDI) ports. When reading this register the port number is ignored.

Register 2

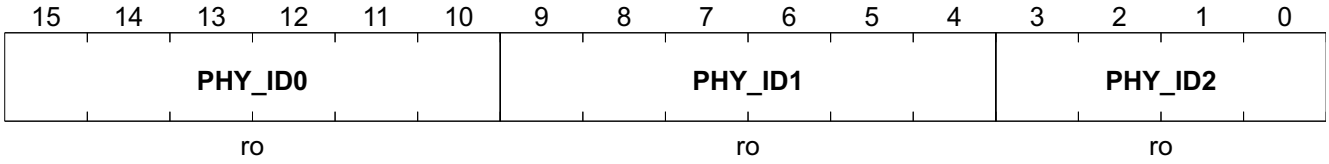
R2	Offset	Reset Value
Register 2	**2_H**	**$001D_H$**



Field	Bits	Type	Description
PHY_ID	15:0	ro	**PHY_ID[31-16]** 3Com OUI (bits 3-18)

Register 3

R3	Offset	Reset Value
Register 3	**3_H**	**2411_H**



Field	Bits	Type	Description
PHY_ID0	15:10	ro	**PHY_ID[15-10]** 3Com OUI (bits 19-24)
PHY_ID1	9:4	ro	**PHY_ID[9-4]** Manufacturer's Model Number (bits 5-0)
PHY_ID2	3:0	ro	**PHY_ID[3-0]** Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier

This uses the OUI of Infineon-ADMtek, device type of 1 and rev 0

Register 4

R4	Offset	Reset Value
Register 4	**4_H**	**0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	**RF**	**NI1**		**PAUSE**	**NI2**	**100BFD**	**100BHD**	**10BFD**	**10BHD**	**SF**				
rw	ro	rw	ro		rw	ro	rw	rw	rw	rw	ro				

Field	Bits	Type	Description
NP	15	rw	**Next Page** 0_B , Device not set to use Next Page 1_B , Device set to use Next Page
Res	14	ro	**Reserved**
RF	13	rw	**Remote Fault** 0_B , no fault detected 1_B , Local remote fault sent to link partner
NI1	12:11	ro	**Not Implemented** Technology ability bits A7-A6
PAUSE	10	rw	**Pause** Technology ability bit A5
NI2	9	ro	**Not Implemented** Technology ability bit A4
100BFD	8	rw	**100BASE-TX Full Duplex** Technology ability bit A3 0_B , Unit is not capable of Full Duplex 1_B , Unit is capable of Full Duplex
100BHD	7	rw	**100BASE-TX Half Duplex** Technology ability bit A2 0_B , Unit is not capable of Half Duplex 100BASE-TX 1_B , Unit is capable of Half Duplex
10BFD	6	rw	**10BASE-T Full Duplex** Technology ability bit A1 0_B , Unit is not capable of Full Duplex 10BASE-T 1_B , Unit is capable of Full Duplex 10BASE-T
10BHD	5	rw	**10BASE-T Half Duplex** Technology ability bit A0 0_B , Unit is not capable of Half Duplex 10BASE-T 1_B , Unit is capable of Half Duplex 10BASE-T
SF	4:0	ro	**Selector Field** Identifies type of message being sent. Currently only one value is defined.

Register 5

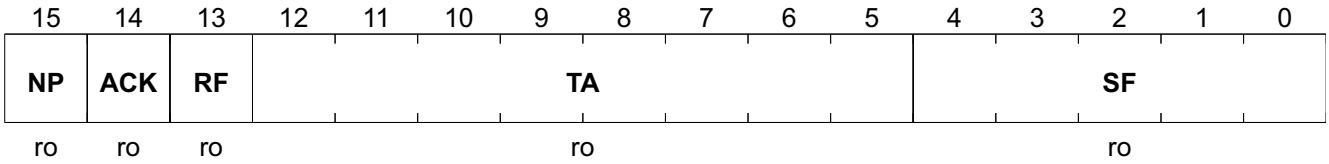
The register is used to view the advertised capabilities of the link partner once autonegotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (autoneg complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.

All bits are read only.

This register is used for Base Page code word only.

Base Page Register Format

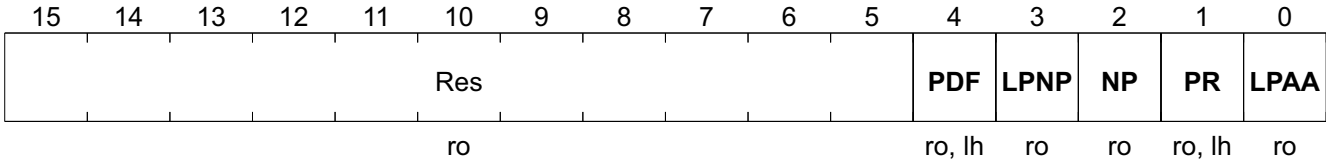
R5	Offset	Reset Value
Register 5	5_H	$0000\ 0000_H$



Field	Bits	Type	Description
NP	15	ro	**Next Page** 0_B , Base Page is requested 1_B , Link Partner is requesting Next Page function
ACK	14	ro	**Acknowledge** Link Partner acknowledgement bit
RF	13	ro	**Remote Fault** Link Partner is indicating a fault
TA	12:5	ro	**Technology Ability** Link Partner technology ability field.
SF	4:0	ro	**Selector Field** Link Partner selector field

Register 6

R6	Offset	Reset Value
Register 6	**6_H**	**0004_H**



Field	Bits	Type	Description
Res	15:5	ro	**Reserved**
PDF	4	ro, lh	**Parallel Detection Fault** *Note: lh: Latch Hight* 0_B , No fault detected 1_B , Local Device Parallel Detection Fault
LPNP	3	ro	**Link Partner Next Page Able** 0_B , Link Partner is not Next Page Able 1_B , Link Partner is Next Page Able
NP	2	ro	**Next Page Able** 0_B , Local device is not Next Page Able 1_B , Local device is Next Page Able
PR	1	ro, lh	**Page Received** *Note: lh: Latch Hight* 0_B , A New Page has not been received 1_B , A New Page has been received
LPAA	0	ro	**Link Partner Autonegotiation Able** 0_B , Link Partner is not Autonegotiation able 1_B , Link Partner is Autonegotiation able

LH: Latch High

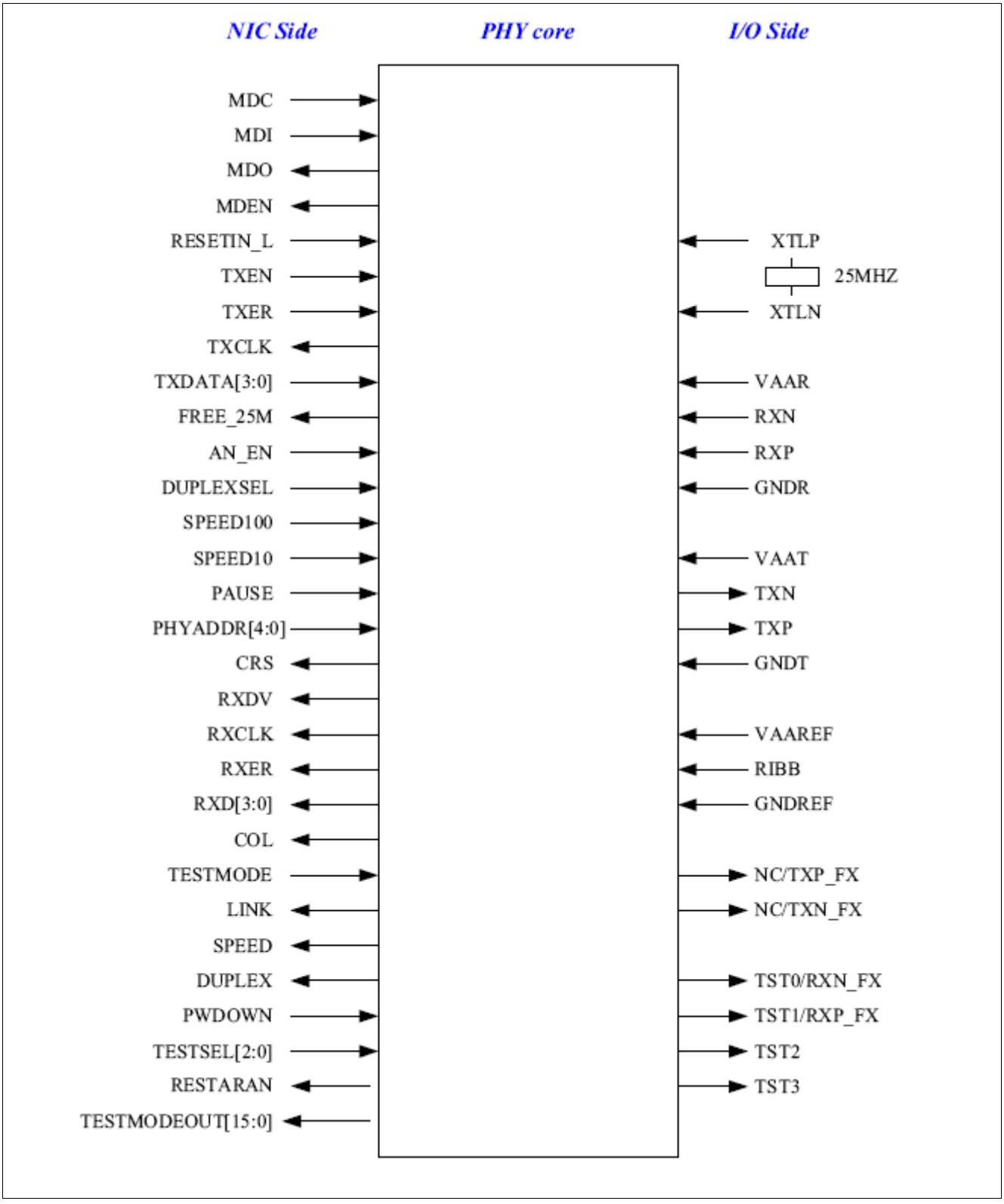


Figure 15 NIC, PHY, and I/O interconnection

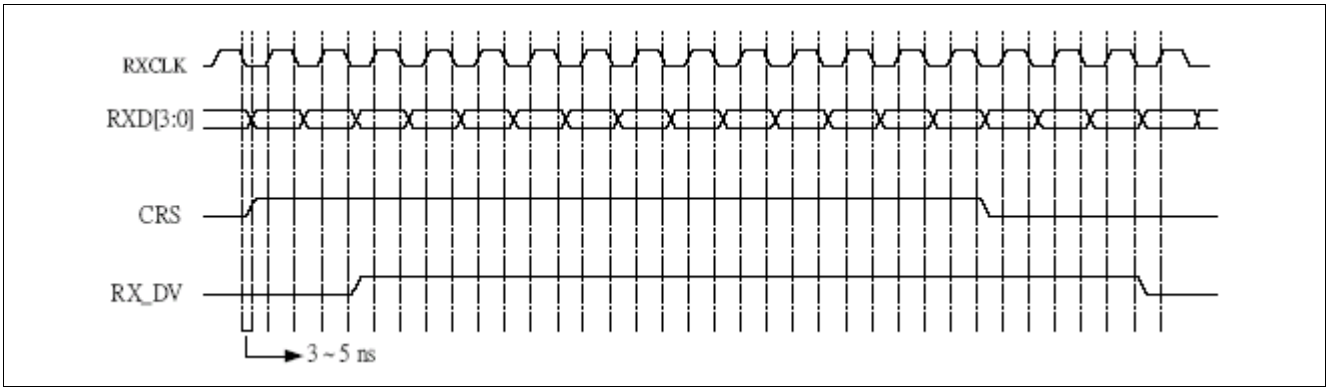


Figure 16 Timing

8.4 Descriptors and Buffer Management

Table 17 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
RDES0	RDES0	00_H	94
RDES1	RDES1	04_H	97
RDES2	RDES2	08_H	97
RDES3	RDES3	$0Ch_H$	97
TDES0	TDES0	00_H	98
TDES1	TDES1	04_H	99
TDES2	TDES2	08_H	100
TDES3	TDES3	$0Ch_H$	100

The register is addressed wordwise.

Standard abbreviations:

Table 18 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)

Table 18 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

8.4.1 Receive Descriptor Descriptions

The AN985B/BX provides receive and transmit descriptors for packet buffering and management.

Descriptors and receive buffers addresses must be longword alignment

Table 19 Receive Descriptor Table

	31 ---------- 0				
RDES0	Own	Status			
RDES1		---	Control	Buffer2 byte-count	Buffer1 byte-count
RDES2	Buffer1 address (DW boundary)				
RDES3	Buffer2 address (DW boundary)				

RDES0

RDES0	**Offset**	**Reset Value**
RDES0	**00_H**	**xxxx xxxx$_H$**

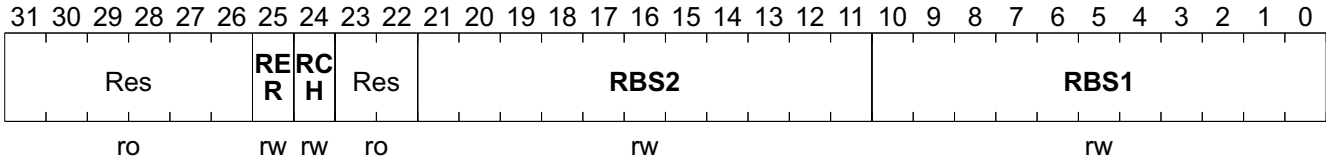
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OWN								FL								ES	DE	DT		RF	MF	FS	LS	TL	CS	FT	RW	Res	DB	CE	OF
rw								rw								rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw

Field	Bits	Type	Description
OWN	31	rw	**Own Bit** 0_B , Host does not move the receiving data out yet 1_B , indicate the new receiving data can be put into this descriptor
FL	30:16	rw	**Frame Length, Including CRC** This field is valid only in last descriptor
ES	15	rw	**Error Summary, OR of the Following Bit** This field is valid only in last descriptor. 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error
DE	14	rw	**Descriptor Error** This bit is valid only in last descriptor 1_B , the current receiving packet is not able to put into the current valid descriptor. This packet is truncated
DT	13:12	rw	**Data Type** These bits are valid only in last descriptor 00_B , normal 01_B , MAC loop-back 10_B , Transceiver loop-back 11_B , remote loop-back
RF	11	rw	**Runt Frame (packet length < 64 bytes)** This bit is valid only in last descriptor.
MF	10	rw	**Multicast Frame** This bit is valid only in last descriptor.
FS	9	rw	**First Descriptor**
LS	8	rw	**Last Descriptor**
TL	7	rw	**Too Long Packet (packet length > 1518 bytes)** This bit is valid only in last descriptor.
CS	6	rw	**Late Collision** Set when collision is active after 64 bytes. This bit is valid only in last descriptor.
FT	5	rw	**Frame Type** This bit is valid only in last descriptor. 0_B , 802.3 type 1_B , Ethernet type
RW	4	rw	**Receive Watchdog (refer to CSR15, bit 4)** This bit is valid only in last descriptor.
Res	3	ro	**Reserved**
DB	2	rw	**Dribble Bit** This bit is valid only in last descriptor. ECPacket length is not integer multiple of 8-bit.
CE	1	rw	**CRC Error** This bit is valid only in last descriptor.

Field	Bits	Type	Description
OF	0	rw	**Overflow** This bit is valid only in last descriptor.

RDES1

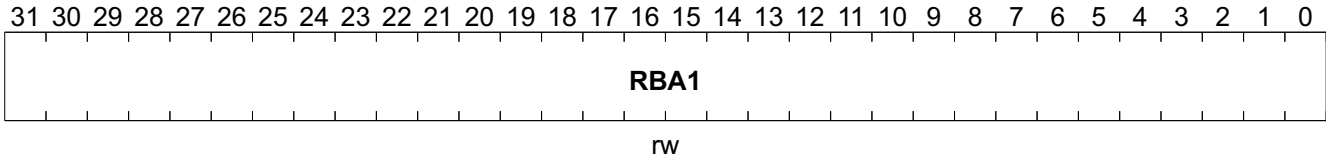
RDES1	Offset	Reset Value
RDES1	04_H	xxxx xxxx$_H$



Field	Bits	Type	Description
Res	31:26	ro	**Reserved**
RER	25	rw	**Receive End of Ring** Indicates this descriptor is last, return to base address of descriptor.
RCH	24	rw	**Second Address Chain** Use for chain structure. Indicates the buffer2 address is the next descriptor address.Ring mode takes precedence over chained mode
Res	23:22	ro	**Reserved**
RBS2	21:11	rw	**Buffer 2 Size** DW boundary
RBS1	10:0	rw	**Buffer 1 Size** DW boundary

RDES2

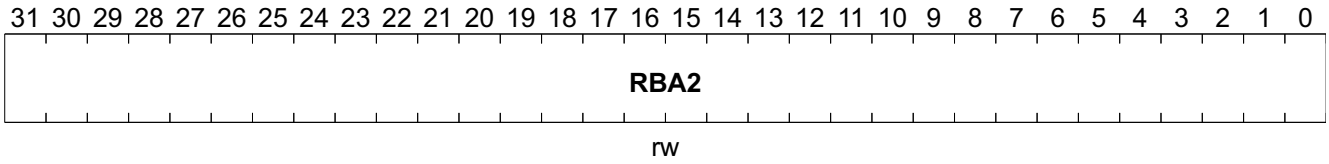
RDES2	Offset	Reset Value
RDES2	08_H	xxxx xxxx$_H$



Field	Bits	Type	Description
RBA1	31:0	rw	**Receive Buffer Address 1** This buffer address should be double word aligned.

RDES3

RDES3	Offset	Reset Value
RDES3	$0Ch_H$	xxxx xxxx$_H$



Field	Bits	Type	Description
RBA2	31:0	rw	**Receive Buffer Address 2** This buffer address should be double word aligned.

8.4.2 Transmit Descriptor Descriptions

The AN985B/BX provides receive and transmit descriptors for packet buffering and management.

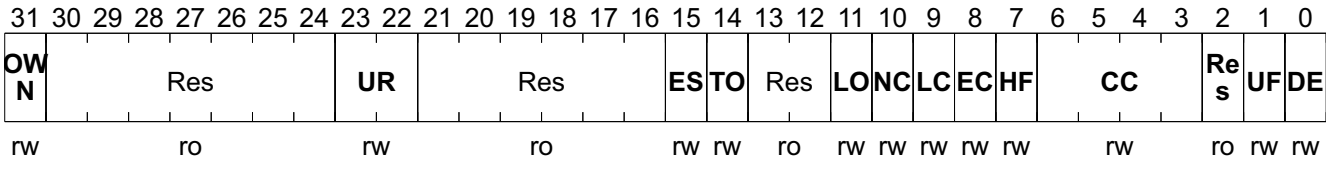
Descriptor addresses must be longword alignment

Table 20 Transmit Descriptor Table

	31 ---------- 0			
TDES0	Own	Status		
TDES1	Control		Buffer2 byte-count	Buffer1 byte-count
TDES2	Buffer1 address			
TDES3	Buffer2 address			

TDES0

TDES0	Offset	Reset Value
TDES0	00_H	xxxx xxxx$_H$



Field	Bits	Type	Description
OWN	31	rw	**Own Bit** 0_B , No transmit data in this descriptor for transmission 1_B , Indicate this descriptor is ready to transmit
Res	30:24	ro	**Reserved**
UR	23:22	rw	**Under-run Count**
Res	21:16	ro	**Reserved**

Field	Bits	Type	Description
ES	15	rw	**Error Summary, OR of the Following Bit** 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out
TO	14	rw	**Transmit Jabber Time-out**
Res	13:12	ro	**Reserved**
LO	11	rw	**Loss Carrier**
NC	10	rw	**No Carrier**
LC	9	rw	**Late Collision**
EC	8	rw	**Excessive Collision**
HF	7	rw	**Heartbeat Fail**
CC	6:3	rw	**Collision Count**
Res	2	ro	**Reserved**
UF	1	rw	**Under-run Error**
DE	0	rw	**Deferred**

TDES1

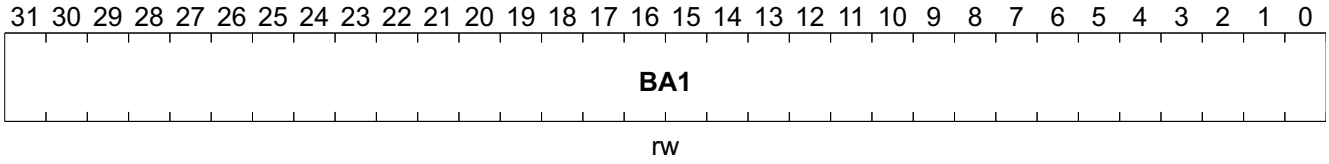
TDES1	Offset	Reset Value
TDES1	04_H	xxxx xxxx$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC	LS	FS	Res		AC	TER	TCH	DPD	Res	TBS2											TBS1										
rw	rw	rw	ro		rw	rw	rw	rw	ro	rw											rw										

Field	Bits	Type	Description
IC	31	rw	**Interrupt Completed**
LS	30	rw	**Last Descriptor**
FS	29	rw	**First Descriptor**
Res	28:27	ro	**Reserved**
AC	26	rw	**Disable add CRC Function**
TER	25	rw	**End of Ring**
TCH	24	rw	**2nd Address Chain** Indicate the buffer2 address is the next descriptor address
DPD	23	rw	**Disable Padding Function**
Res	22	ro	**Reserved**
TBS2	21:11	rw	**Buffer 2 Size**
TBS1	10:0	rw	**Buffer 1 Size**

TDES2

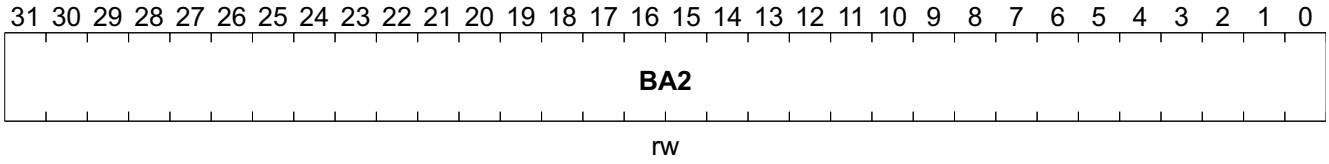
TDES2	Offset	Reset Value
TDES2	08_H	xxxx xxxx$_H$



Field	Bits	Type	Description
BA1	31:0	rw	**Buffer Address 1** Without any limitation on the transmission buffer address.

TDES3

TDES3	Offset	Reset Value
TDES3	$0Ch_H$	xxxx xxxx$_H$



Field	Bits	Type	Description
BA2	31:0	rw	**Buffer Address 2** Without any limitation on the transmission buffer address.

9 Electrical Specifications and Timings

9.1 Absolute Maximum Ratings

Table 21 Min-Max Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	-0.5	–	3.6	V	–
Input Voltage	V_{CC}	-0.5	–	V_{CC} + 0.5	V	
Output Voltage	V_{CC}	-0.5	–	V_{CC} + 0.5	V	
Storage Temperature	°C	- 65		150	°C	
Ambient Temperature	°C	0		70	°C	
ESD Protection				2000	V	

9.2 DC Specifications

Table 22 General DC Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3.0	–	3.6	V	–
Power Supply	I_{CC}	–	–	1	A	–

Table 23 PCI Interface DC Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input LOW Voltage	V_{ilp}	-0.5	–	0.325 V_{CC}	V	–
Input HIGH Voltage	V_{ihp}	0.475 V_{CC}	–	V_{CC} + 0.5	V	–
Input Leakage Current	I_{ilp}	-10	–	10	µA	$0 < V_{in} < V_{CC}$
Output LOW Voltage	V_{olp}	–	–	0.1 V_{CC}	V	I_{out} = 700 µA
Output HIGH Voltage	V_{ohp}	0.9 V_{CC}	–	–	V	I_{out} = -150 µA
Input Pin Capacitance	C_{inp}	5	–	17	pF	–
CLK Pin Capacitance	C_{clkp}	10	–	22	pF	–

Table 24 Flash/EEPROM Interface DC Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input LOW Voltage	V_{ilf}	0	–	0.3 V_{CC}	V	–
Input HIGH Voltage	V_{ihf}	0.7 V_{CC}	–	V_{CC} + 1	V	–
Input Leakage Current	I_{if}	?	–	?	µA	–
Output LOW Voltage	V_{olf}	–	–	0.2	V	–

Table 24 Flash/EEPROM Interface DC Specifications (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output HIGH Voltage	V_{ohf}	V_{CC} - 0.2	–	–	V	–
Input Pin Capacitance	C_{inf}	?	–	?	pF	–

9.3 AC Specifications

Table 25 PCI Signaling AC Specifications for 3.3 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Current High	I_{oh} (AC)	–	4	–	mA	–
Switching Current Low	I_{ol} (AC)	–	6	–	mA	–
Slew Rate	–	0.25	–	1	V/ns	–
Unloaded Output Rise Time	T_r	1	–	4	V/ns	0.2 V_{CC} ~ 0.6 V_{CC}
Unloaded Output Fall Time	T_f	1	–	4	V/ns	0.6 V_{CC} ~ 0.2 V_{CC}

9.4 Timing Specifications

Table 26 PCI Clock Specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock Cycle Time	T_{cyc}	30	–	–	ns	–
Clock High Time	T_{high}	12	–	–	ns	–
Clock Low Time	T_{low}	12	–	–	ns	–
Clock Slew Rate	–	1	–	4	V/ns	–

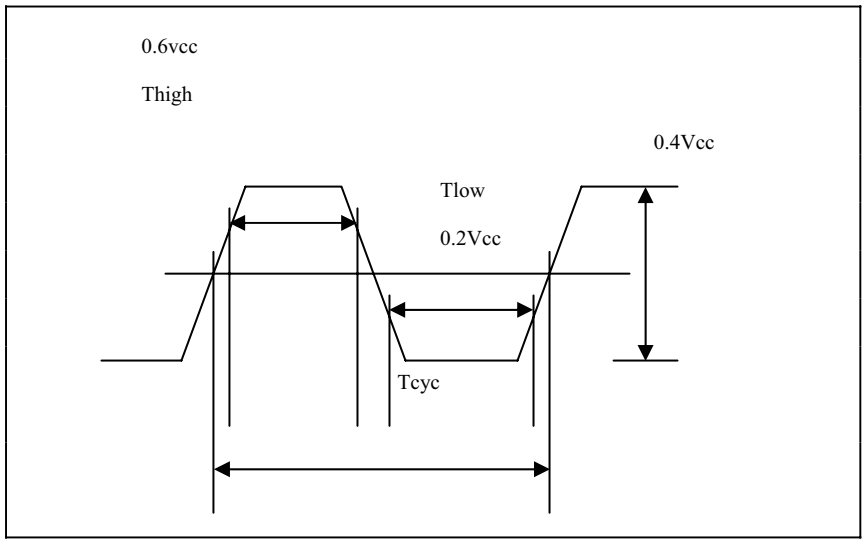


Figure 17 PCI Clock Waveform

Table 27 PCI Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Access time – bused signals	T_{val}	2	–	11	ns	–
Access time – point to point	T_{val} (ptp)	2	–	12	ns	–
Float to Active Delay	T_{on}	2	–	–	ns	–
Active to Float Delay	T_{off}	–	–	28	ns	–
Input Set up Time to Clock – bused signals	T_{su}	7	–	–	ns	–
Input Set up Time to Clock – point to point	T_{su} (ptp)	10, 12	–	–	ns	–
Input Hold Time from Clock	T_h	0	–	–	ns	–
Reset Active Time after Power Stable	T_{rst}	1	–	–	ms	–
Reset Active Time after CLK Stable	$T_{rst\text{-}clk}$	100	–	–	µs	–
Reset Active to Output Float delay	$T_{rst\text{-}off}$	–	–	40	ns	–

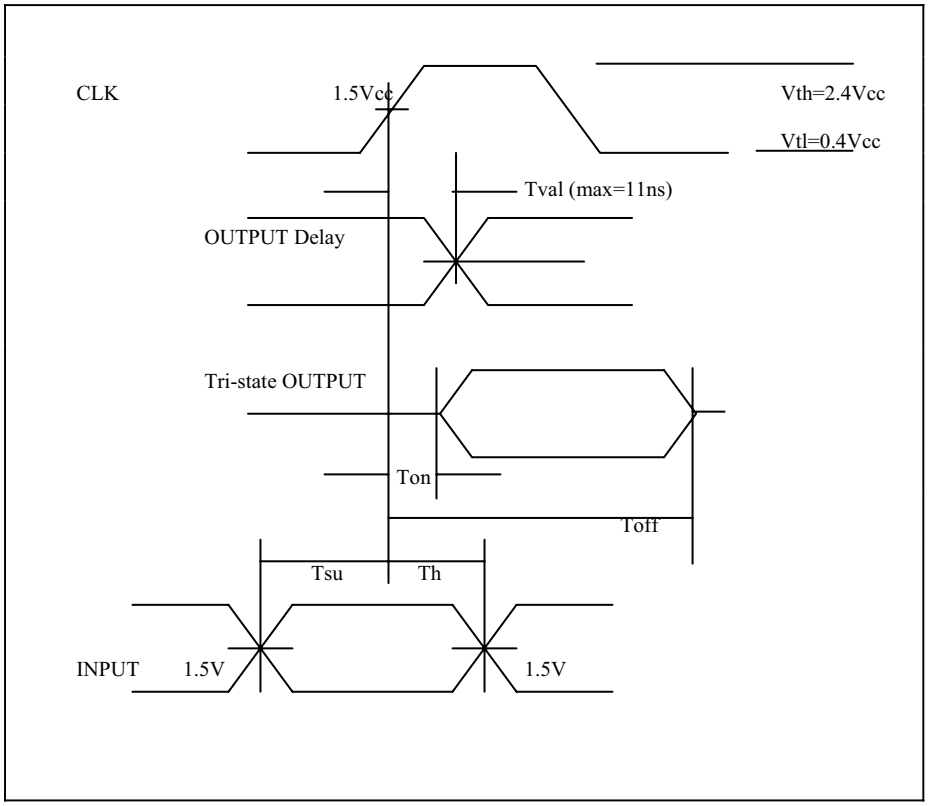


Figure 18 PCI Timings

Table 28 Flash Interface Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Read cycle time	T_{rc}	90	–	–	ns	–
Chip enable access time	T_{ce}	–	–	90	ns	–
Address access time	T_{aa}	–	–	90	ns	–
Output enable access time	T_{oe}	–	–	45	ns	–
$\overline{CE}$ low to active output	T_{clz}	0	–	–	ns	–
$\overline{OE}$ low to active output	T_{olz}	0	–	–	ns	–
$\overline{CE}$ high to active output	T_{chz}	–	–	45	ns	–
$\overline{OE}$ high to active output	T_{ohz}	–	–	45	ns	–
Output hold from address change	T_{oh}	0	–	–	ns	–
Write cycle time	T_{wc}	–	–	10	ms	–
Address setup time	T_{as}	0	–	–	ns	–
Address hold time	T_{ah}	50	–	–	ns	–
$\overline{WE}$ and $\overline{CE}$ setup time	T_{cs}	0	–	–	ns	–
$\overline{WE}$ and $\overline{CE}$ hold time	T_{ch}	0	–	–	ns	–
$\overline{OE}$ high setup time	T_{oes}	10	–	–	ns	–
$\overline{OE}$ high hold time	T_{oeh}	10	–	–	ns	–

Table 28 Flash Interface Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{CE}$ pulse width	T_{cp}	70	–	–	ns	–
$\overline{WE}$ pulse width	T_{wp}	70	–	–	ns	–
$\overline{WE}$ high width	T_{wph}	150	–	–	ns	–
Data setup time	T_{ds}	50	–	–	ns	–
Data hold time	T_{dh}	10	–	–	ns	–
Byte load cycle time	T_{blc}	0.22	–	200	µs	–
Byte load cycle time out	T_{blco}	300	–	–	µs	–

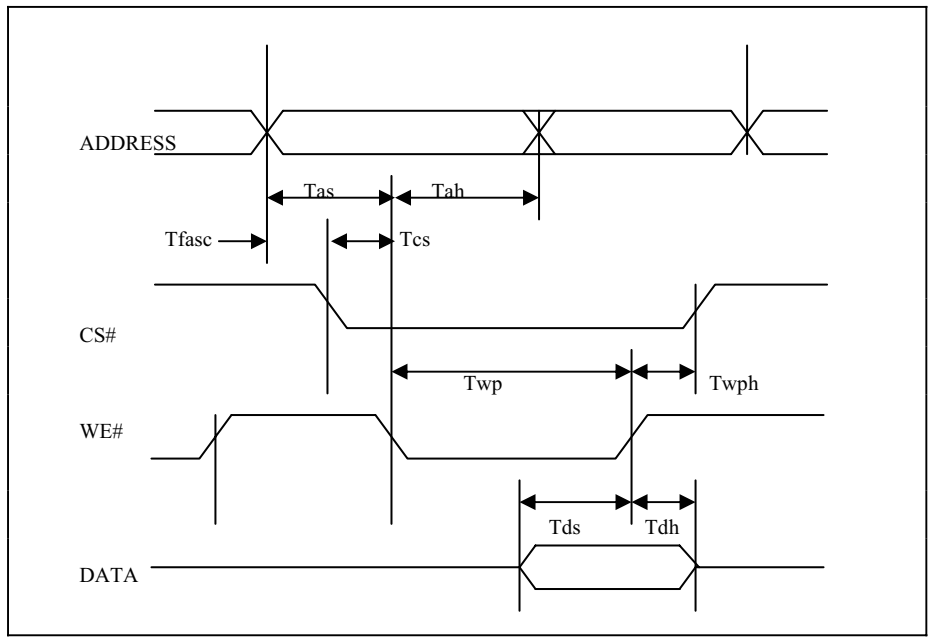


Figure 19 Flash Write Timings

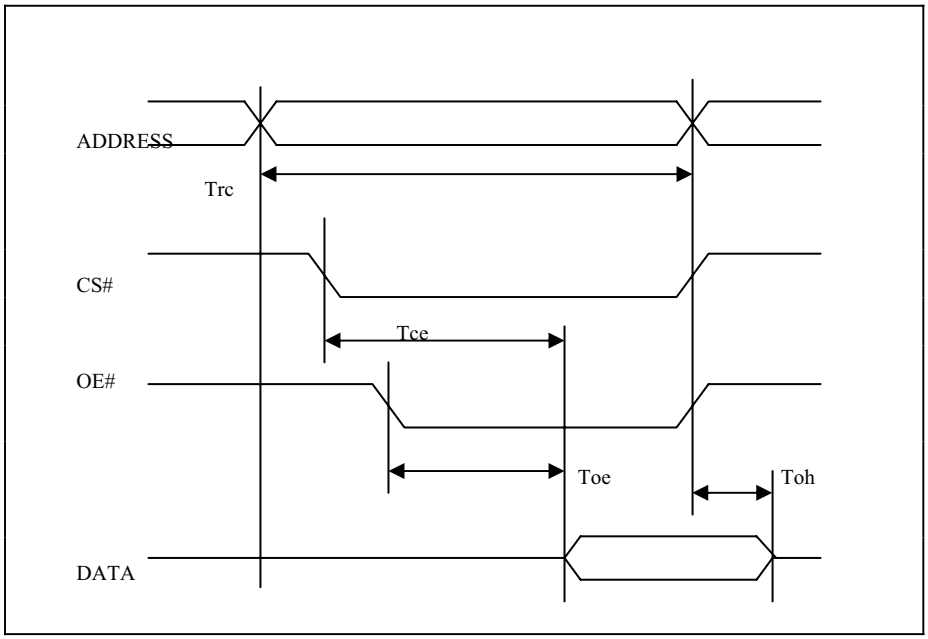


Figure 20 Flash Read Timings

Table 29 EEPROM Interface Timings (AC/AD)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Serial Clock Frequency	T_{scf}	–	–	0.4M/ 0.1M	Hz	2.7 V < V_{CC} < 5.5 V
Delay from CS High to SK High	T_{ecss}	160/640	–	–	ns	2.7 V < V_{CC} < 5.5 V
Delay from SK Low to CS Low	T_{ecsh}	1120/ 4480	–	–	ns	2.7 V < V_{CC} < 5.5 V
Setup Time of DI to SK	T_{edts}	160/640	–	–	ns	2.7 V < V_{CC} < 5.5 V
Hold Time of DI after SK	T_{edth}	2320/ 9280	–	–	ns	2.7 V < V_{CC} < 5.5 V
CS Low Time	T_{ecsl}	7400/ 29600	–	–	ns	2.7 V < V_{CC} < 5.5 V

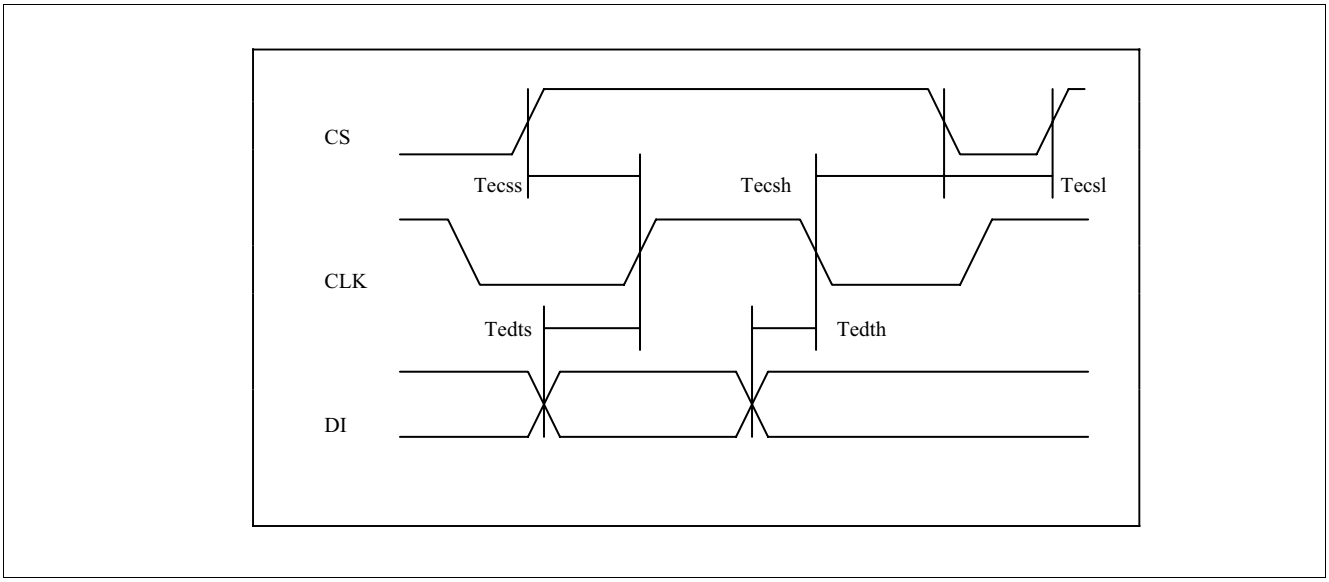


Figure 21 Serial EEPROM Timing

10 Package Outlines

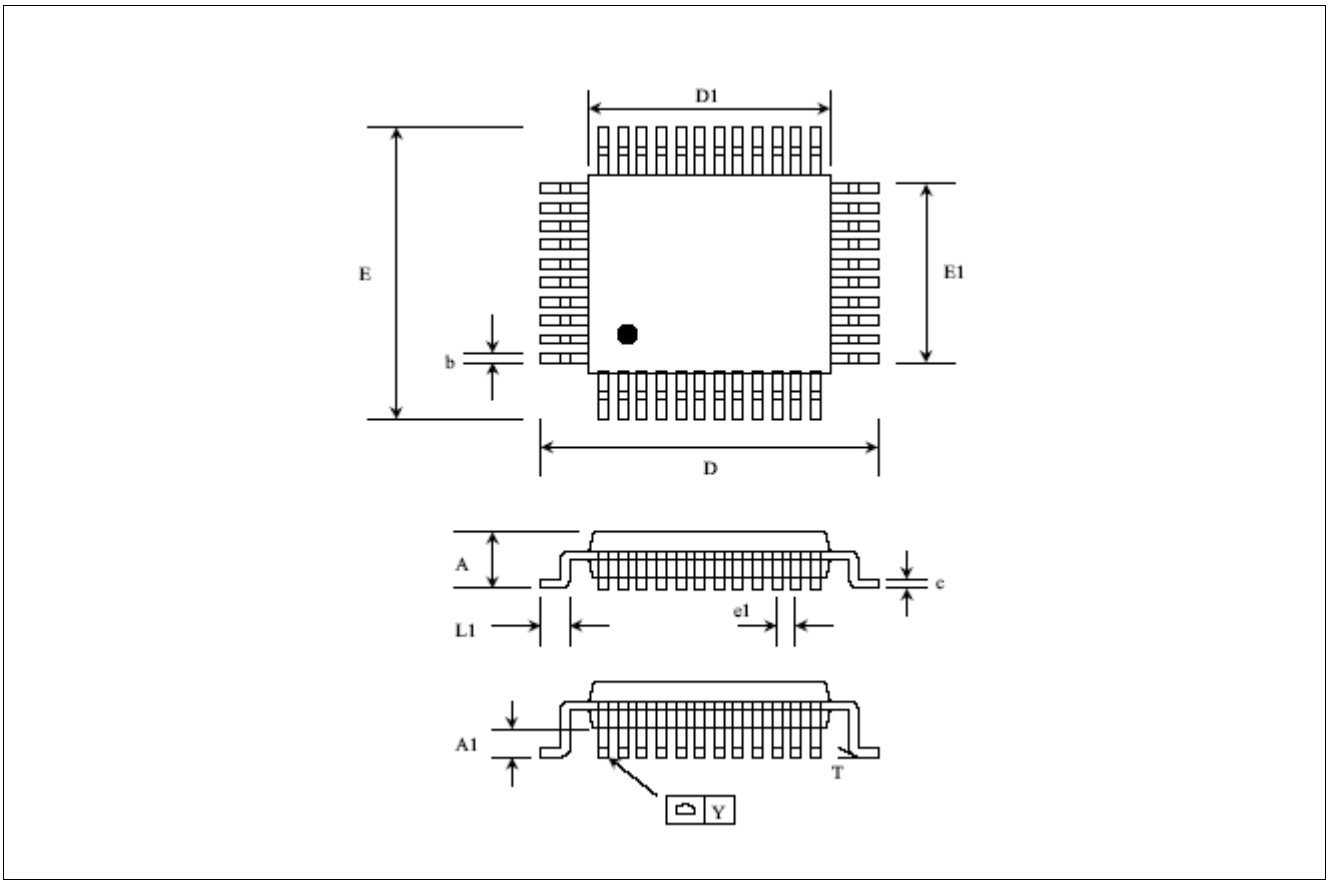


Figure 22 Package Outline for the AN985B/BX

Table 30 Dimensions for 128 -pin LQFP Package (AN985B/BX)

Symbol	Description	Minimum	Maximum
A	Overall Height	-	1.6 mm
A1	Stand Off	0.05 mm	0.15 mm
b	Lead Width	0.17 mm	0.27 mm
c	Lead Thickness	0.13 mm	0.23 mm
D	Terminal Dimension 1	21.9.0 mm	22.1 mm
D1	Package Body 1	19.9 mm	20.1 mm
E	Terminal Dimension 2	15.9 mm	16.1 mm
E1	Package Body 2	13.9 mm	14.1 mm
e1	Lead Pitch	0.50 mm	-
L1	Foot Length	0.45 mm	0.75 mm
T	Lead Angle	0°	7°
Y	Coplanarity		0.076 mm

11 Appendix

11.1 MII Management Access Procedure

Read Management Data From Phyter

1. Write CSR9[18]=1 to let Mdio become input mode.
2. Write CSR9[16] according to the IEEE802.3u spec to generate the MII management clock.
3. Read CSR9[19] with reference the MII management clock.

Write Management Data From Phyter

1. Write CSR9[18]=1 to let Mdio become output mode.
2. Write CSR9[16] according to the IEEE802.3u spec to generate the MII management clock.
3. Write CSR9[19] with reference the MII management clock.

11.2 Debugging Purpose Registers: Offset FCH

MAC(HOME/PNA), MODE/SET FCH[2:0]=100_B

MDC:bra11

TXEN:bra10

TXD[3:0]:bra[9:6]

TXER:bra5

MDIO:bra3

RXDV:brd4

CRS:bra2

RXD[2:0]:brd[3:0]

COL:bra1

RXER:bra0

RXCLK:brwe_

RXCLK:broe_

PHY MINITOR MODE/SET FCH[2:0]=110_B

bra[16:0]=rxd[3:0], crs, col, rx_clk, rx_dv, rx_er, rx_clk,txd[3:0], tx_er, tx_en, mdi

brd[7:6]=mdo, mdc

PHY ONLY MODE/SET FCH[2:0]=001_B

bra[16:9]=rxd[3:0], csr, col,rx_er, rx_dv

brd[7:0]=mdc, mdio, tx_er, tx_en, txd[3:0]

broez=rx_clk

brwez=tx_clk

11.3 EEPROM DATA TABLE

Table 31 EEPROM DATA TABLE

Offset	b15----------b8	b7----------b0
08_H	PHY ADDR 00	
$0A_H$	PHY ADDR 01	
$0C_H$	PHY ADDR 10	
16_H	[b15~b4]=csr_MISC_control(offset $f8_H$[15:4]) [b3~b0]=CSR15[31:28]	
20_H	Device ID	
22_H	Vendor ID	
24_H	Subsystem ID	
26_H	Subsystem Vendor ID	
28_H	MaxLat	MinGnt
$2A_H$	LAN CISL	
$2C_H$	LAN CISH	
$2E_H$	CSR18_REG	
30_H~$3F_H$		
40_H	PWRDATA1HB(LAN D0)	PWRDATA1LB(LAN D321)
42_H~51_H		
52_H	CARDBUS CIS word count(<128)	
54_H~$7F_H$		
80_H~$13F_H$		
140_H~$1FF_H$	CARDBUS CIS DATA(192 Words)	

References

[1]

[2]

[3]

[4]

[5]

[6]

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