Dual and Quad Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Op Amp

ISL28278, ISL28478

The ISL28278 and ISL28478 are dual and quad channel micropower operational amplifiers optimized for single supply operation over the 2.4V to 5.5V range. They can be operated from one lithium cell or two Ni-Cd batteries.

These devices feature an Input Range Enhancement Circuit (IREC) that enables them to maintain CMRR performance for input voltages 10% above the positive supply rail and to 100mV below the negative supply. The output operation is rail-to-rail.

The ISL28278 and ISL28478 draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise, and output drive specifications. The ISL28278 contains a power-down enable pin that reduces the power supply current typically to 4µA in the disabled state.

Related Literature

- AN1345: ISL2827xEVAL1Z Evaluation Board User Guide

Features

- Low-power 120µA Typical Supply Current (ISL28278)
- 225µV Max Offset Voltage
- 30pA Max Input Bias Current
- 250kHz Typical Gain-bandwidth Product
- 105dB Typical PSRR
- 100dB Typical CMRR
- Single Supply Operation Down to 2.4V
- Input Capable of Swinging Above V+ and Below V- (Ground Sensing)
- Rail-to-rail Input and Output (RRIO)
- Enable Pin (ISL28278 Only)
- Pb-free (RoHS-compliant)

Applications

- Battery- or Solar-powered Systems
- 4mA to 25mA Current Loops
- Handheld Consumer Products
- Medical Devices
- Thermocouple Amplifiers
- Photodiode Pre-amps
- pH Probe Amplifiers

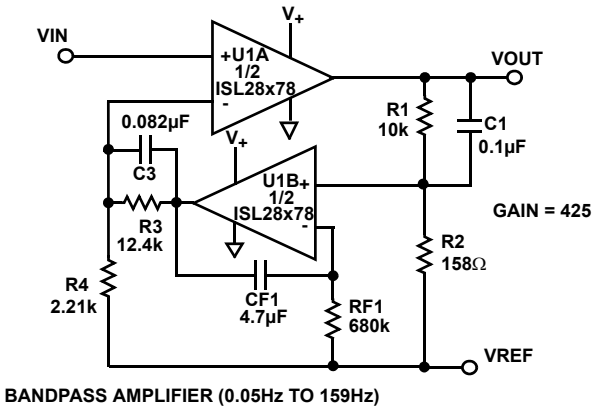
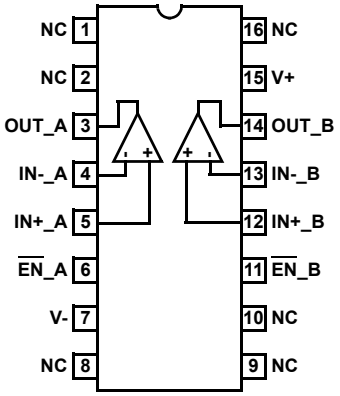


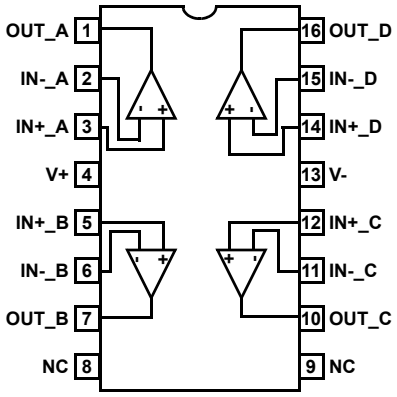
FIGURE 1. TYPICAL APPLICATION CIRCUIT

Pin Configurations

ISL28278
(16 LD QSOP)
TOP VIEW

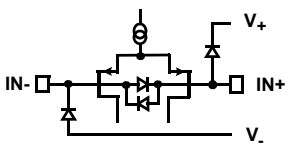


ISL28478
(16 LD QSOP)
TOP VIEW

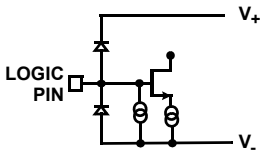


Pin Descriptions

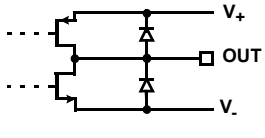
ISL28278 (16 LD QSOP)	ISL28478 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	1	OUT_A	Circuit 3	Amplifier A output
4	2	IN-_A	Circuit 1	Amplifier A inverting input
5	3	IN+_A	Circuit 1	Amplifier A non-inverting input
15	4	V+	Circuit 4	Positive power supply
12	5	IN+_B	Circuit 1	Amplifier B non-inverting input
13	6	IN-_B	Circuit 1	Amplifier B inverting input
14	7	OUT_B	Circuit 3	Amplifier B output
1, 2, 8, 9, 10, 16	8, 9	NC		No internal connection
	10	OUT_C	Circuit 3	Amplifier C output
	11	IN-_C	Circuit 1	Amplifier C inverting input
	12	IN+_C	Circuit 1	Amplifier B non-inverting input
7	13	V-	Circuit 4	Negative power supply
	14	IN+_D	Circuit 1	Amplifier D non-inverting input
	15	IN-_D	Circuit 1	Amplifier D inverting input
	16	OUT_D	Circuit 3	Amplifier D output
6		$\overline{EN}$_A	Circuit 2	Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
11		$\overline{EN}$_B	Circuit 2	Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.



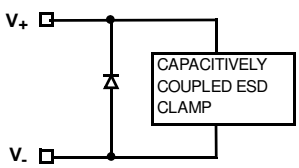
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Ordering Information

PART NUMBER (Notes 1, 2, 3, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28278FAZ	28278 FAZ	-40 to +125	16 Ld QSOP	MDP0040
ISL28478FAZ	28478 FAZ	-40 to +125	16 Ld QSOP	MDP0040

NOTES:

1. Add “-T7” suffix is for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28278 and ISL28478. For more information on MSL please see Tech Brief TB363.
4. Not recommended for new designs. For a possible substitute product, contact Intersil Technical Support Center at 1-888-INTERSIL or www.intersil.com/tsc.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage, V_- to V_+ 5.75V
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage ..... V_- - 0.5V to V_+ + 0.5V
ESD Tolerance
- Human Body Model 3kV
- Machine Model 300V
- Charged Device Model 1200V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
16 Ld QSOP Package	112

Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Pb-free reflow profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range ..... -40°C to +125°C
Maximum Operating Junction Temperature ..... +125°C
Supply Voltage ..... 2.4V (±1.2V) to 5.5V (±2.75V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-225 **-450**	±0.20	225 **450**	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			1.0		µV/°C
I_{OS}	Input Offset Current	 -40°C to +85°C	-30 -80	±5	30 80	pA
I_B	Input Bias Current	 -40°C to +85°C	-30 -80	±10	30 80	pA
CMIR	Common-Mode Voltage Range	Guaranteed by CMRR	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	V+ = 2.4V to 5.5V	85 **80**	105		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	103 **102**	109		dB
		V_O = 0.5V to 4.5V, R_L = 1kΩ		95		dB
V_{OL}	Output Voltage Swing, Low V_{OUT} - V_-	R_L = 100kΩ		3	6 **30**	mV
		R_L = 1kΩ		130	175 **225**	mV
V_{OH}	Output Voltage Swing, High V_+ - V_{OUT}	R_L = 100kΩ		4	10 **30**	mV
		R_L = 1kΩ		120	200 **250**	mV
$I_{S,ON}$	Quiescent Supply Current, Enabled	ISL28278, all channels enabled.		120	156 **175**	µA
		ISL28478, all channels enabled.		240	315 **350**	µA

Electrical Specifications V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
$I_{S,OFF}$	Quiescent Supply Current, Disabled	All channels disabled. ISL28278		4	7 **9**	µA
I_O+	Short Circuit Sourcing Capability	R_L = 10Ω	24 **20**	31		mA
I_O-	Short Circuit Sinking Capability	R_L = 10Ω		-26	-24 **-20**	mA
V_{SUPPLY}	Supply Operating Range	V_- to V_+	**2.4**		**5.5**	V
$V_{\overline{EN}H}$	$\overline{EN}$ Pin High Level	ISL28278	**2**			V
$V_{\overline{EN}L}$	$\overline{EN}$ Pin Low Level	ISL28278			**0.8**	V
$I_{\overline{EN}H}$	$\overline{EN}$ Pin Input High Current	$V\overline{EN} = V_+$ ISL28278		0.8	1 **1.5**	µA
$I_{\overline{EN}L}$	$\overline{EN}$ Pin Input Low Current	$V\overline{EN} = V_-$ ISL28278		0	**0.1**	µA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		250		kHz
e_n	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		3		μV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		48		nV/√Hz
i_n	Input Noise Current Density	f_O = 1kHz		9		fA/√Hz
CMRR @ 60Hz	Input Common Mode Rejection Ratio	V_{CM} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-70		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio, +V	V_+,V_- = ±1.2V and ±2.5V, V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-80		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio, -V	V_+,V_- = ±1.2V and ±2.5V V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-60		dB
TRANSIENT RESPONSE						
SR	Slew Rate			±0.15		V/µs
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% Vout	$V\overline{EN}$ = 5V to 0V, A_V = -1, R_G = R_F = R_L = 1k to V_{CM}, ISL28278		2		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% Vout	$V\overline{EN}$ = 0V to 5V, A_V = -1, R_G = R_F = R_L = 1k to V_{CM}, ISL28278		0.1		µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified.

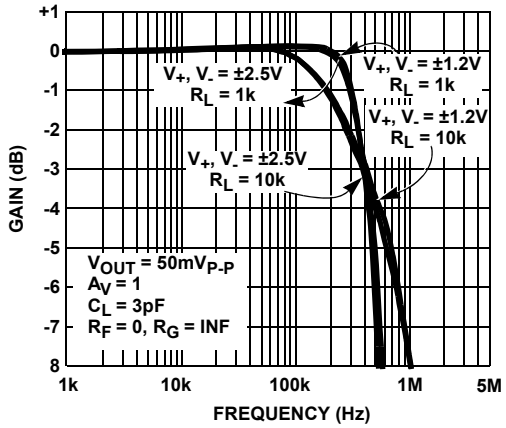


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

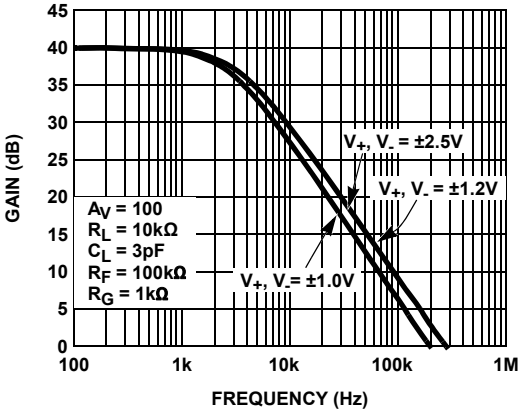


FIGURE 3. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

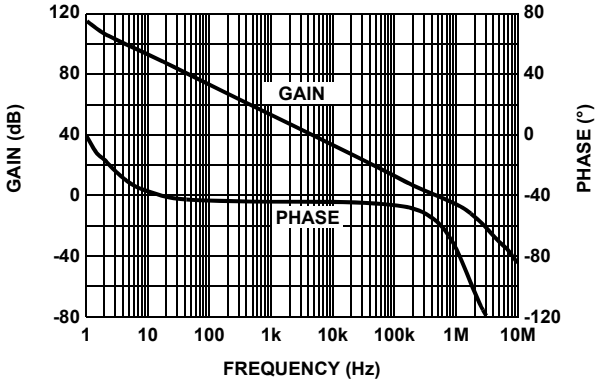


FIGURE 4. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

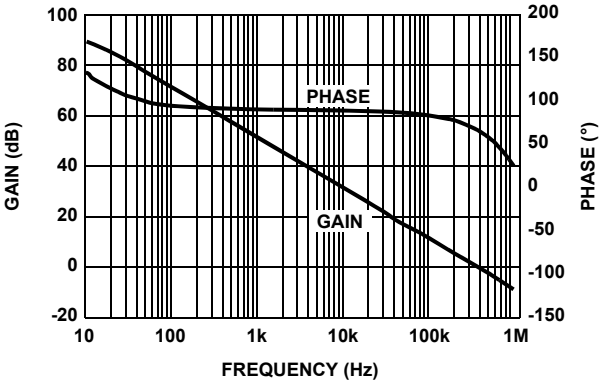


FIGURE 5. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

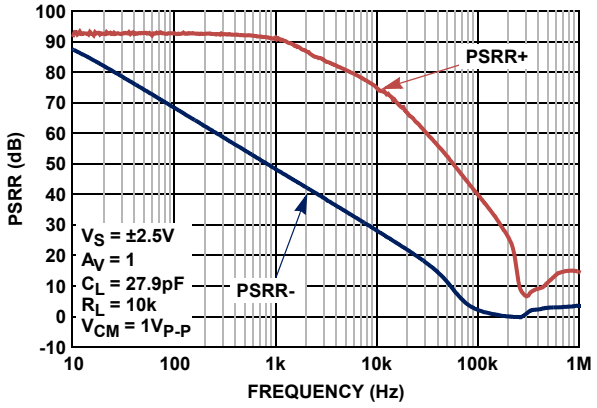


FIGURE 6. PSRR vs FREQUENCY

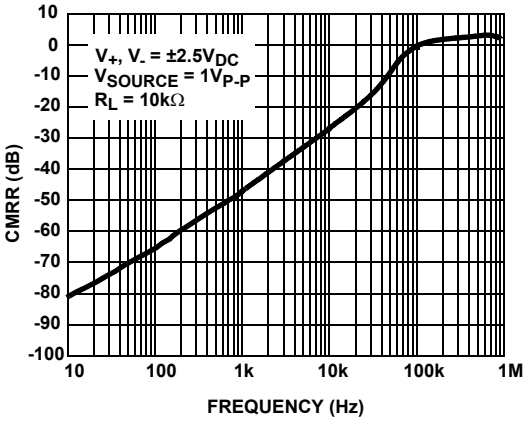


FIGURE 7. CMRR vs FREQUENCY

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

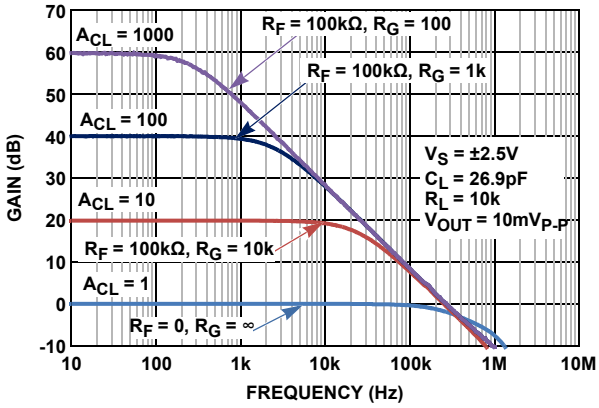


FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

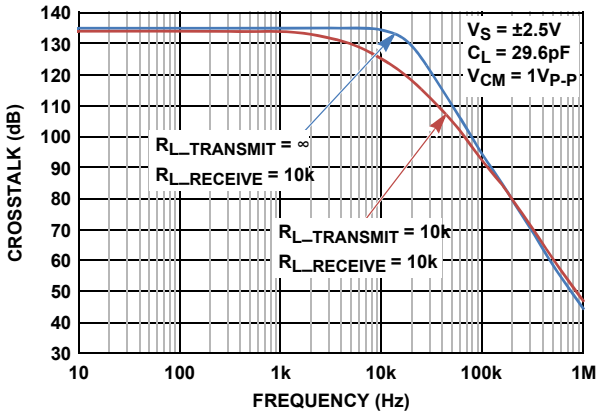


FIGURE 9. CROSSTALK vs FREQUENCY

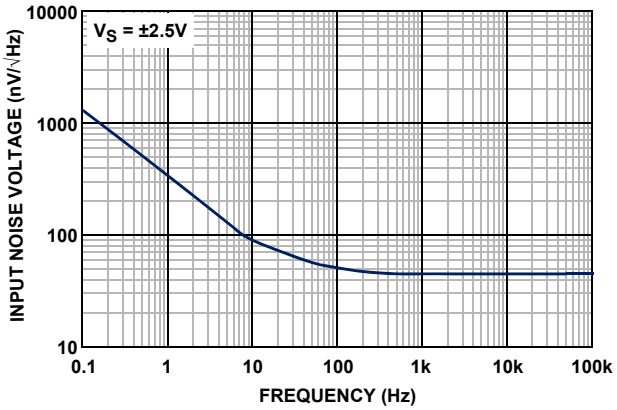


FIGURE 10. VOLTAGE NOISE vs FREQUENCY

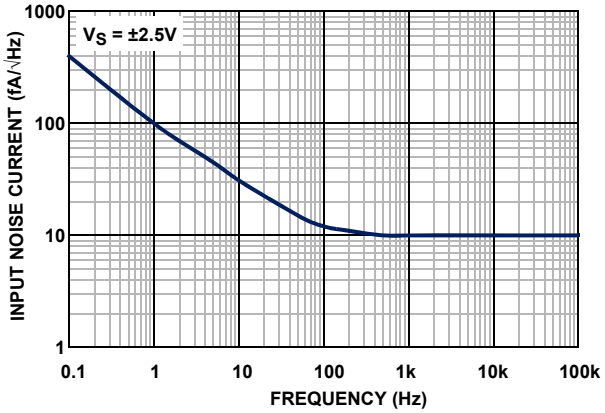


FIGURE 11. CURRENT NOISE vs FREQUENCY

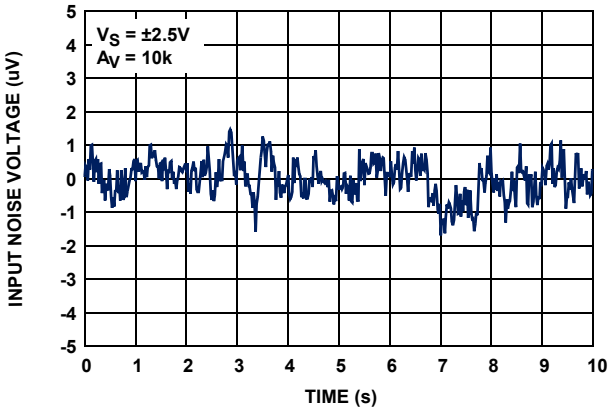


FIGURE 12. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

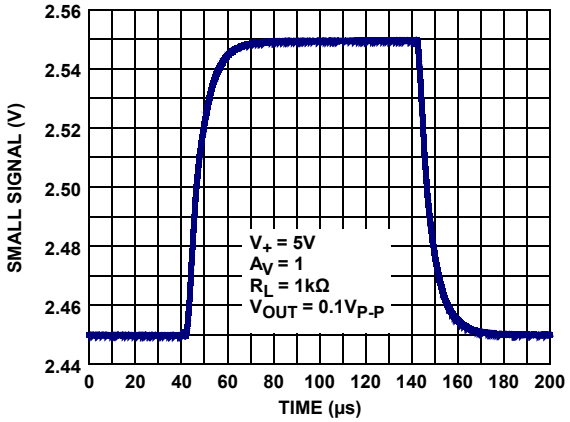


FIGURE 13. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves v_+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

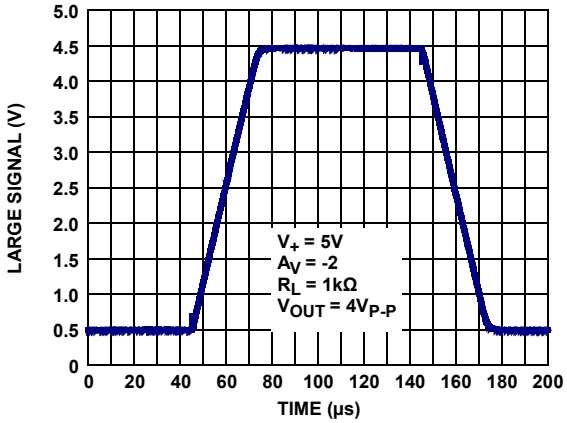


FIGURE 14. LARGE SIGNAL TRANSIENT RESPONSE

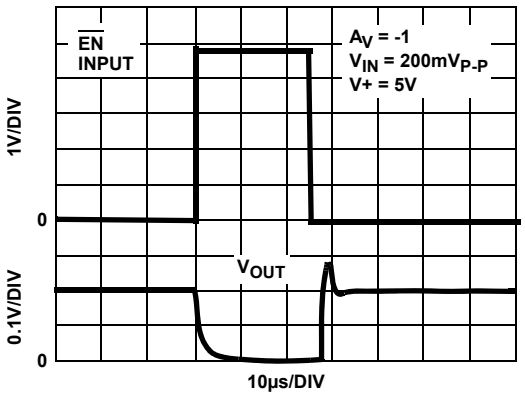


FIGURE 15. ISL28278 ENABLE TO OUTPUT DELAY TIME

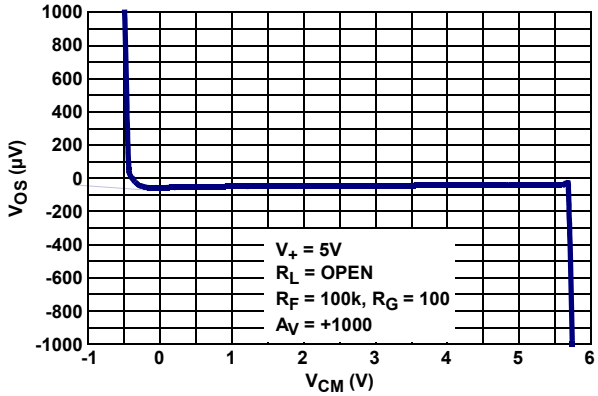


FIGURE 16. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

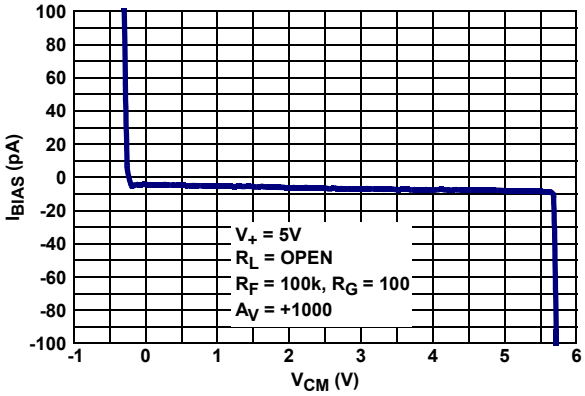


FIGURE 17. INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

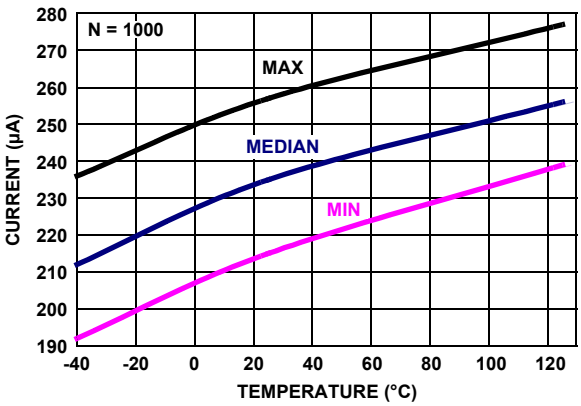


FIGURE 18. ISL28478 SUPPLY CURRENT vs TEMPERATURE, V_+, V- = ±2.5V, R_L = INF

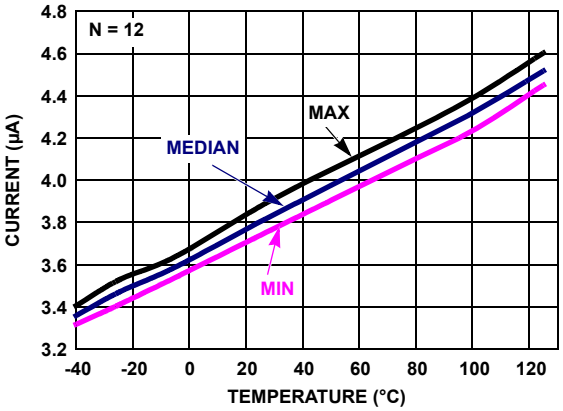


FIGURE 19. ISL28278 DISABLED SUPPLY CURRENT vs TEMPERATURE, V_+, V- = ±2.5V R_L = INF

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

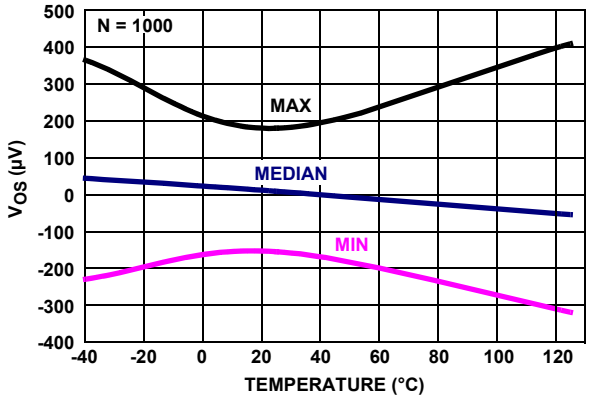


FIGURE 20. V_{OS} vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

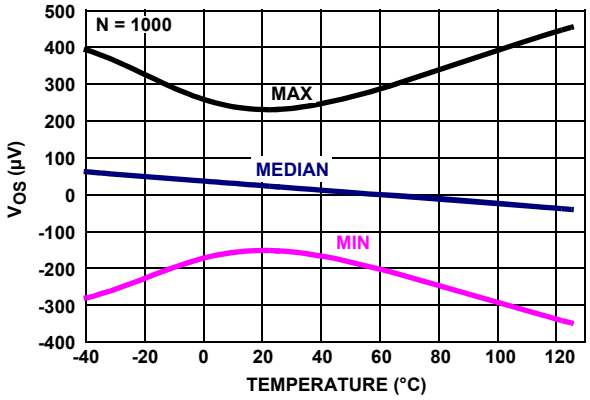


FIGURE 21. V_{OS} vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±1.2V

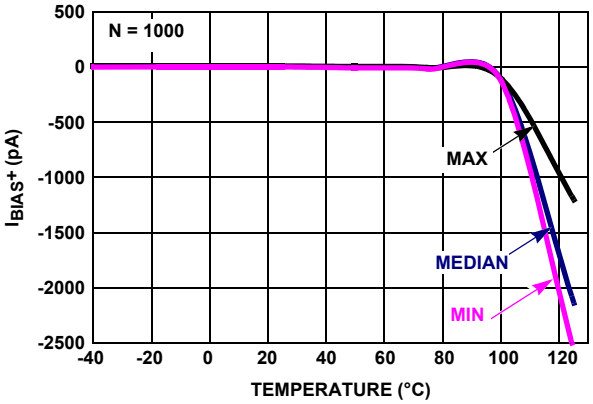


FIGURE 22. I_{BIAS}+ vs TEMPERATURE, V_+,V_- = ±2.5V

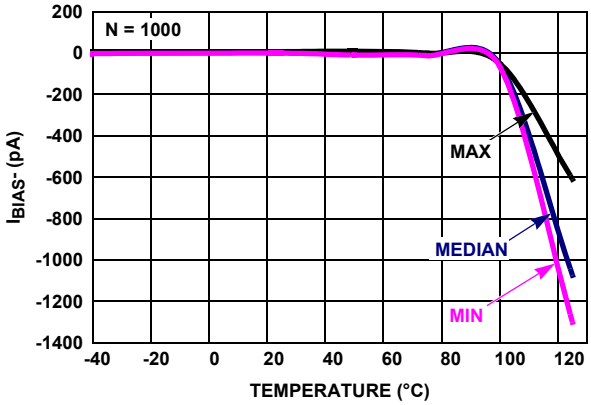


FIGURE 23. I_{BIAS}- vs TEMPERATURE, V_+,V_- = ±2.5V

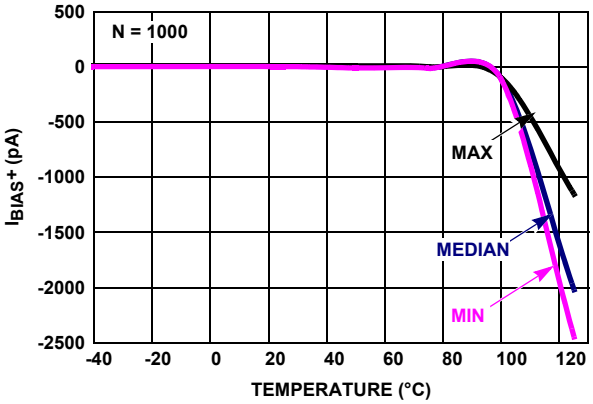


FIGURE 24. I_{BIAS}+ vs TEMPERATURE, V_+, V_- = ±1.2V

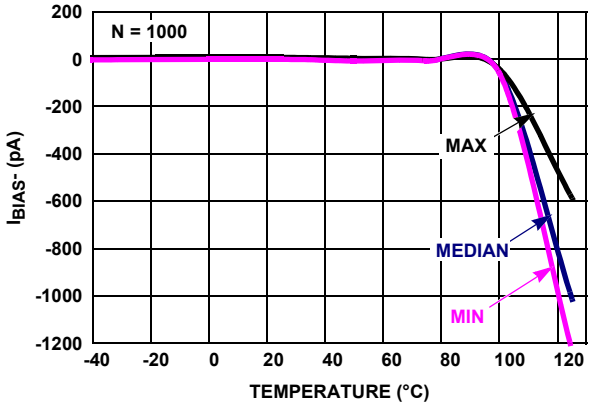


FIGURE 25. I_{BIAS}- vs TEMPERATURE, V_+, V_- = ±1.2V

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

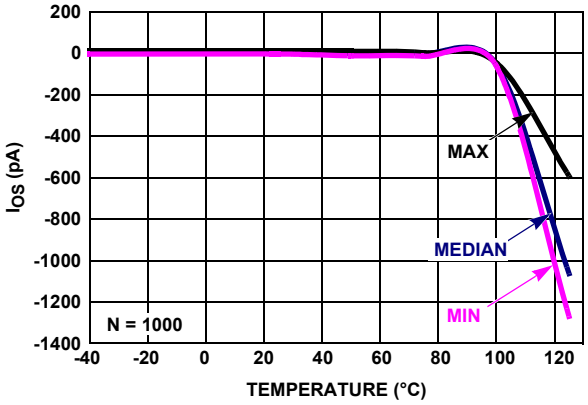


FIGURE 26. I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V

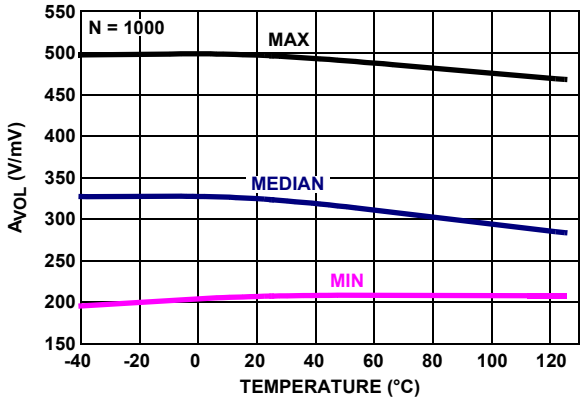


FIGURE 27. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

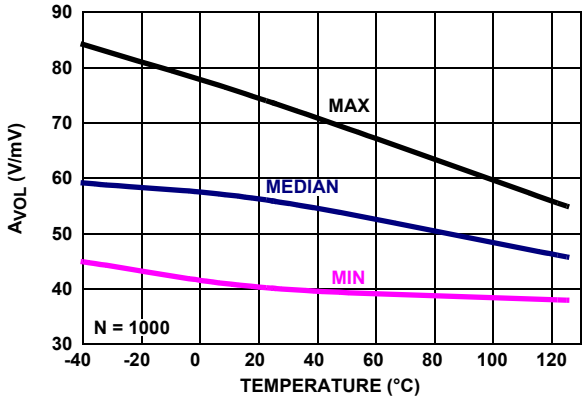


FIGURE 28. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

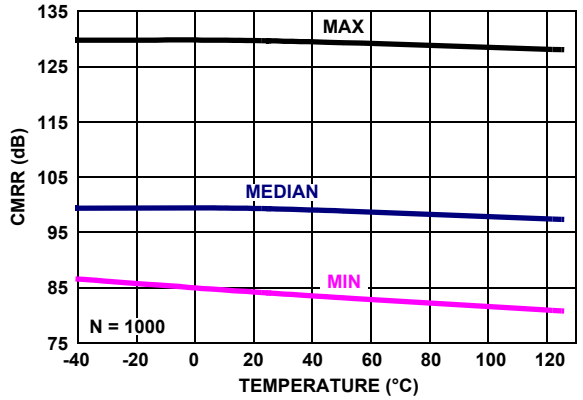


FIGURE 29. CMRR vs TEMPERATURE, V_{CM} = +2.5V TO -2.5V V_+, V_- = ±2.5V

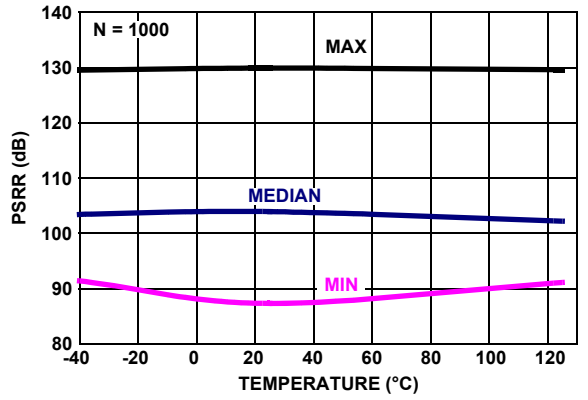


FIGURE 30. PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.5V

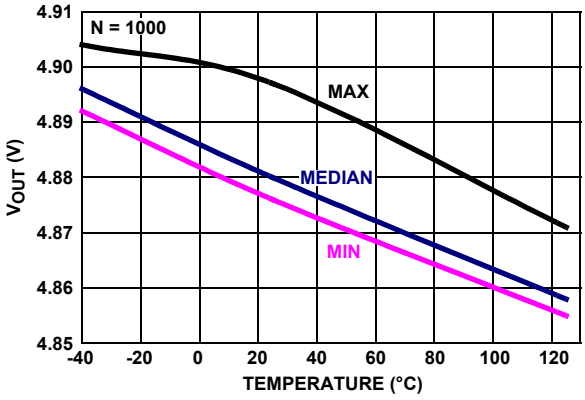


FIGURE 31. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 1k

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

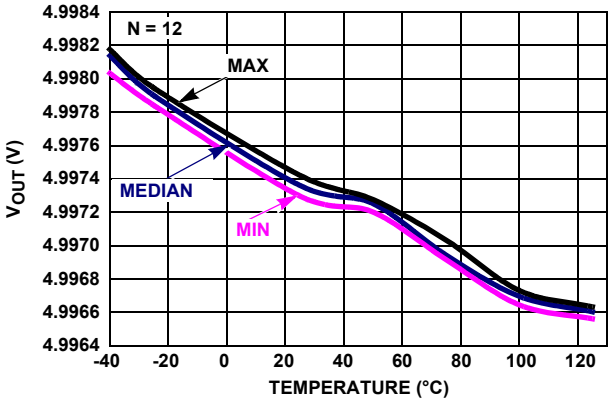


FIGURE 32. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 100k

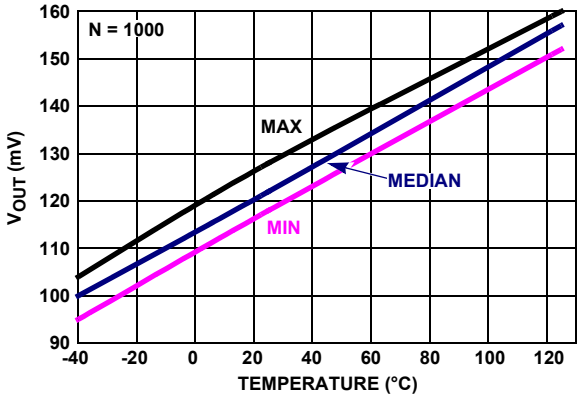


FIGURE 33. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 1k

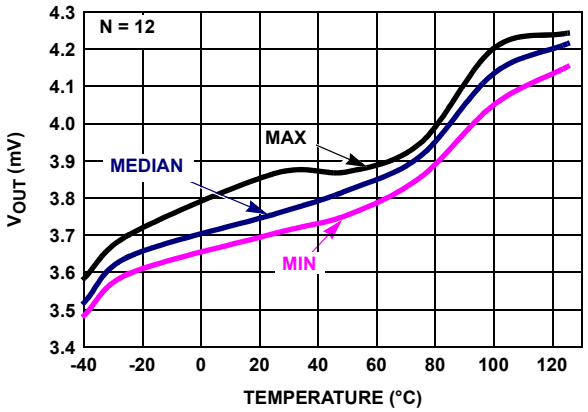


FIGURE 34. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 100k

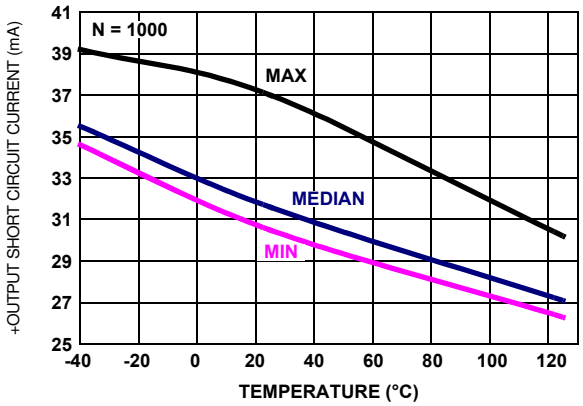


FIGURE 35. +OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE, V_{IN} = -2.55V, R_L = 10, V_+, V_- = ±2.5V

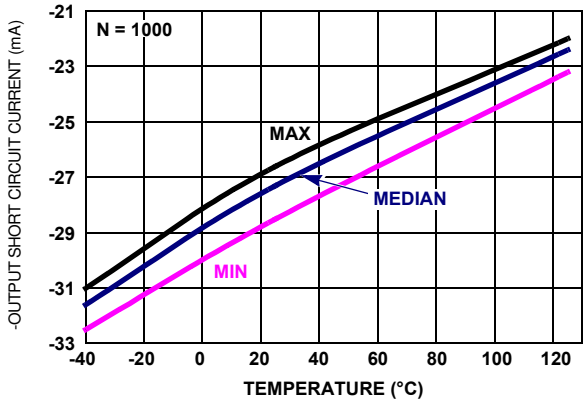


FIGURE 36. -OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE, V_{IN} = +2.55V, R_L = 10, V_+, V_- = ±2.5V

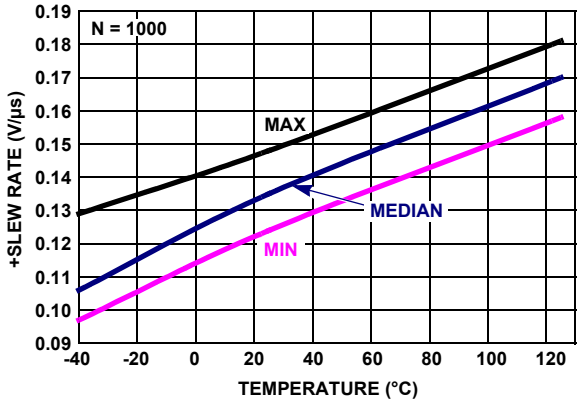


FIGURE 37. +SLEW RATE vs TEMPERATURE, V_{OUT} = ±1.5V, A_V = +2

Typical Performance Curves v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, unless otherwise specified. (Continued)

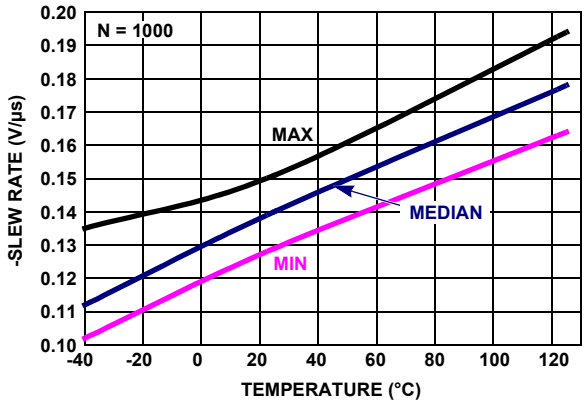


FIGURE 38. -SLEW RATE vs TEMPERATURE, V_{OUT} = ±1.5V, A_V = +2

Applications Information

The ISL28278 and ISL28478 are dual and quad CMOS rail-to-rail input, output (RRIO) micropower operational amplifiers. These devices are designed to operate from a single supply (2.4V to 5.5V) or dual supplies (±1.2V to ±2.75V) while drawing only 120µA (ISL28278) of supply current. This combination of low power and precision performance makes these devices suitable for solar and battery power applications.

Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs: a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other, causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28278 achieves input rail-to-rail without sacrificing important precision specifications and degrading distortion performance. The input offset voltage exhibits smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range has undistorted behavior typically from 100mV below the negative rail and 10% higher than the V_+ rail (0.5V higher than V_+ when V_+ equals 5V).

Input Protection

All input terminals have internal ESD protection diodes to the positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. There is an additional pair of back-to-back diodes across the input terminals. For applications in which the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA (as shown in Figure 39).

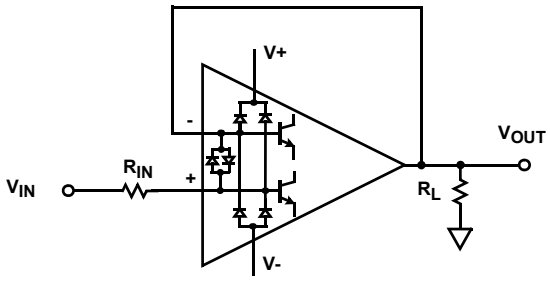


FIGURE 39. INPUT ESD DIODE CURRENT LIMITING - UNITY GAIN

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. Both parts, with a 100kΩ load, typically swing to within 4mV of the positive supply rail and within 3mV of the negative supply rail.

Enable/Disable Feature

The ISL28278 offers two $\overline{EN}$ pins ($\overline{EN}$_A and $\overline{EN}$_B) which disable the op amp when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part typically consumes 4µA. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel, and a channel can be selected by the $\overline{EN}$ pins. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin pulls to the negative rail, and the device is enabled by default.

Using Only One Channel

The ISL28278 and ISL28478 are dual and quad channel op amps. If the application requires only one channel when using the ISL28278 or fewer than four channels when using the ISL28478, the user must configure any unused channels to prevent them from oscillating. Unused channels oscillate if the input and output pins are floating, resulting in higher than

expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input, and ground the positive input (as shown in Figure 40).

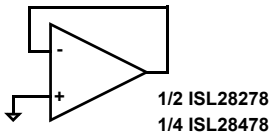


FIGURE 40. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve maximum performance from the high input impedance and low offset voltage of the ISL28278 and ISL28478, care should be taken in circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

Current Limiting

The ISL28278 and ISL28478 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the absolute maximum rating for output current or power dissipation, potentially resulting in destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications, to determine whether power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

PD_{MAX} for each amplifier is calculated in Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Supply voltage (magnitude of V_+ and V_-)
- I_{SMAX} = Maximum supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Application Circuits

THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28x78 (see Figure 41) is used to convert the differential thermocouple voltage into a single-ended signal with 10x gain. The amplifier's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the amplifier to run from a single 5V supply.

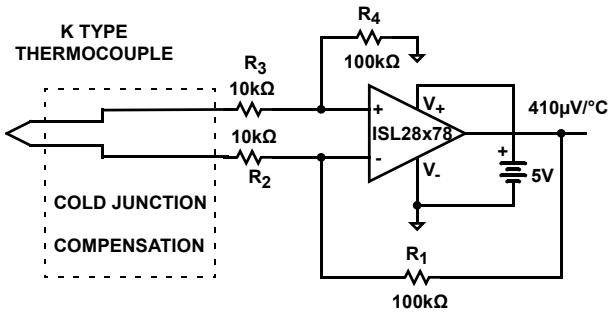


FIGURE 41. THERMOCOUPLE AMPLIFIER

ECG AMPLIFIER

In medical applications, ECG amplifiers must extract millivolt low frequency AC signals from the skin of the patient while rejecting AC common mode interference and static DC potentials created at the electrode-to-skin interface. In Figure 42, the ISL28278 (U1) forms one of the multiple high gain AC band-pass amplifiers using active feedback. Amplifier U1B and RC RF1, CF1 form a high gain LP filtered amplifier with the corner frequency given by Equation 3:

$$f\text{-}HPF_{-3dB} = \frac{1}{2 \times Pi \times RF1 \times CF1} \quad \text{(EQ. 3)}$$

Inserting the low pass amplifier, U1B, in the U1A feedback loop results in an overall high-pass frequency response. Voltage divider pairs R_1-R_2 and R_3-R_4 set the overall amplifier pass-band gain. The DC input offset is canceled by U1B at the U1A inverting input. Resistor divider pair R_3-R_4 defines the maximum input DC level that is canceled, and is given by Equation 4:

$$V_{IN}DC = V_+ \times \left(\frac{R_4}{R_3 + R_4}\right) \quad \text{(EQ. 4)}$$

In the passband range, U1B gain is +1, and the total signal gain is defined by the divider ratios according to Equation 5:

$$V_{OUT}U1\ GAIN = \frac{V_{OUT}}{V_{IN}} = \left(\frac{R_1 + R_2}{R_2}\right) \times \left(\frac{R_3 + R_4}{R_4}\right) \quad \text{(EQ. 5)}$$

At frequencies greater than the LPF corner, the R_1-C_1 and R_3-C_3 networks work to roll-off the U1A gain to unity. Setting both R-C time constants to the same value simplifies to Equation 6:

$$f\text{-}LPF_{-3dB} = \frac{1}{2 \times Pi \times R_1 \times C_1} \quad \text{(EQ. 6)}$$

Right leg drive and reference amplifiers U2A and U2B form a DC feedback loop that applies a correction voltage at the right leg

electrode to cancel out DC and low frequency body interference. The voltage at the V_{CM} sense electrode is maintained at the reference voltage set by RF1-RF2.

With the values shown in Figure 42, the ECG circuit performance parameters are:

1. Supply Voltage Range = +2.4V to +5.5V
2. Total Supply Current Draw @ +5V = 500µA (typ)
3. Common-Mode Reference Voltage (V_{CM}) = $V_+/2$
4. Max DC Input Offset Voltage = V_{CM} ±0.18V to ±0.41V
5. Passband Gain = 425V/V
6. Lower -3dB Frequency = 0.05Hz
7. Upper -3dB Frequency = 159Hz

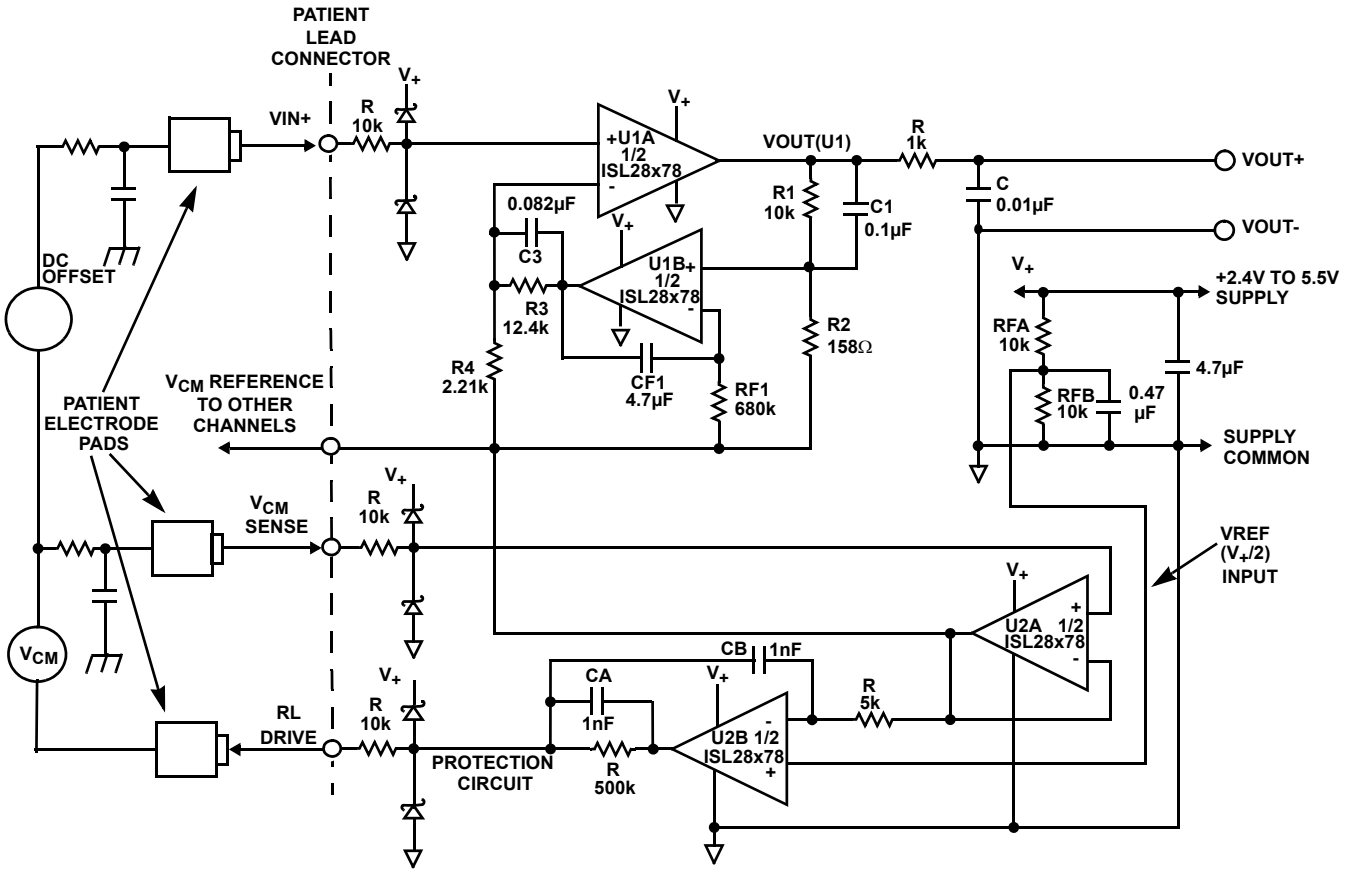


FIGURE 42. ECG AMPLIFIER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 16, 2011	FN6145.4	On page 1, Features: changed "300kHz typical gain-bandwidth product" to "250kHz typical gain-bandwidth product" Added Related Literature section with link to "AN1345: ISL2827xEVAL1Z Evaluation Board User Guide." On page 1: added Figure 1, Typical Application Circuit diagram. On page 4, Absolute Maximum Ratings: removed "Supply Turn On Voltage Slew Rate . . . 1V/µs". Under "Operating Conditions," added "Supply Voltage . . . 2.4V (±1.2V) to 5.5V (±2.75V)" and changed "Operating Junction Temperature" to "Maximum Operating Junction Temperature". On page 4, Electrical Specifications: - Changed A_{VOL} room temperature MIN from 200V/mV to 103dB; changed over-temp MIN from 190V/mV to 102dB; changed TYP from 300V/mV to 109dB. For R_L = 1kΩ, changed TYP from 60V/mV to 95dB. - Split V_{OUT} into two parameters: V_{OL} and V_{OH}. For Output Voltage Swing, High, removed MIN limits, changed TYP from 4.996V and 4.880V to 4mV and 120mV; added MAX limits. - For Gain Band Width, changed TYP from 300kHz to 250kHz. - For Slew Rate, removed MIN/MAX limits; changed TYP from ±0.14V/µs to ±0.15V/µs. On page 6: replaced FIGURE 6. PSRR vs FREQUENCY. On page 7: Typical Performance Curves: Added Figure 8 “FREQUENCY RESPONSE vs CLOSED LOOP GAIN”, Figure 9 “CROSSTALK vs FREQUENCY”, Figure 10 “VOLTAGE NOISE vs FREQUENCY” and Figure 11 “CURRENT NOISE vs FREQUENCY” On page 13: under “Proper Layout Maximizes Performance” removed discussion of guard ring for unity gain amplifier, and removed Figure 37. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER.
	FN6145.3	- Changed I_O+, I_O- specs. - Updated Supply Voltage in Electrical Specifications table; added CDM ESD spec. - Changed Noise Current TYP from 0.04pA to 9fA - Updated noise plots (Fig.7, 8, 9) - Updated transient response plots (Fig 10, 11) - Added ECG circuit to Applications section
	FN6145.2	Added ISL28476 Quad to the ISL28276 Dual data sheet.
	FN6145.1	Pg 10: revised Pin Description to include ISL28478 pin numbers.
9/18/2006	FN6145.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28278, ISL28478

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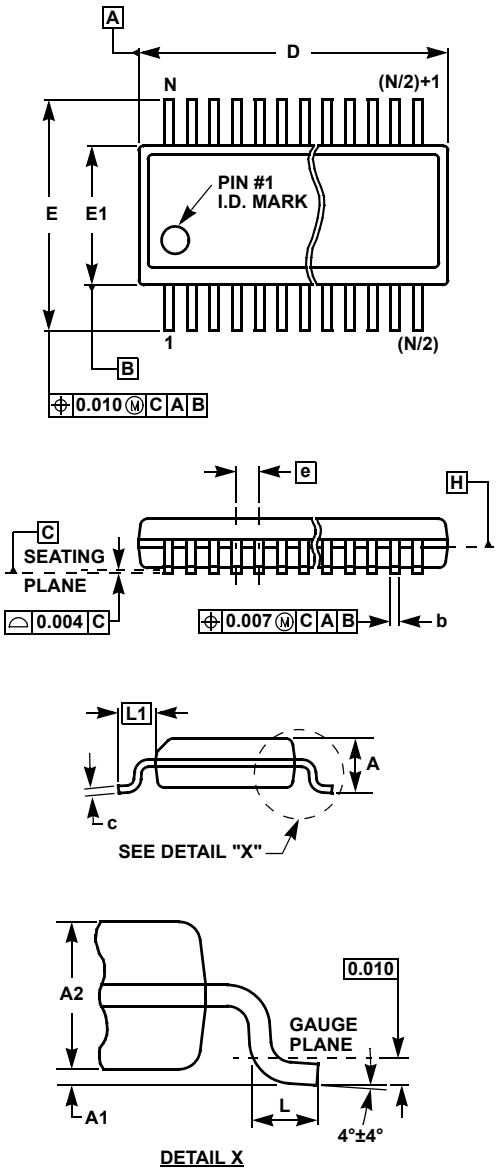
FITs are available from our website at: http://rel.intersil.com/reports/sear

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.