



AK9223

Dual 1-Bit, 10MHz, 2nd-Order, $\Delta\Sigma$ Modulator

General Description

The AK9223 is a 2ch delta-sigma modulator that achieves 86dB dynamic range. It operates of a 5V power supply. The AK9223 is available in a space-saving 24-pin TSSOP package.

Features

- Resolution: 16-bit
- Linearity: 13-bit
- Input Voltage Range: $\pm 2.3V$
- High Accurate Reference Voltage: $\pm 1\%$ ($2.5V \pm 0.025V$), $\pm 20ppm/^{\circ}C$ (typ.)
- Gain Error: 0.5% (max.)
- 2ch $\Delta\Sigma$ Modulator
- 2ch Input Reference
- 20MHz OSC
- Selectable External Clocks
- Power Consumption: 67.5 mW (SEL=1, AVDD = DVDD = 5V)
- Power Supply: AVDD = 4.5 to 5.5V、DVDD = 2.7 to 5.5V
- Ta = -40 to 105°C
- Small Package: 24-pin TSSOP (0.65mm pitch)

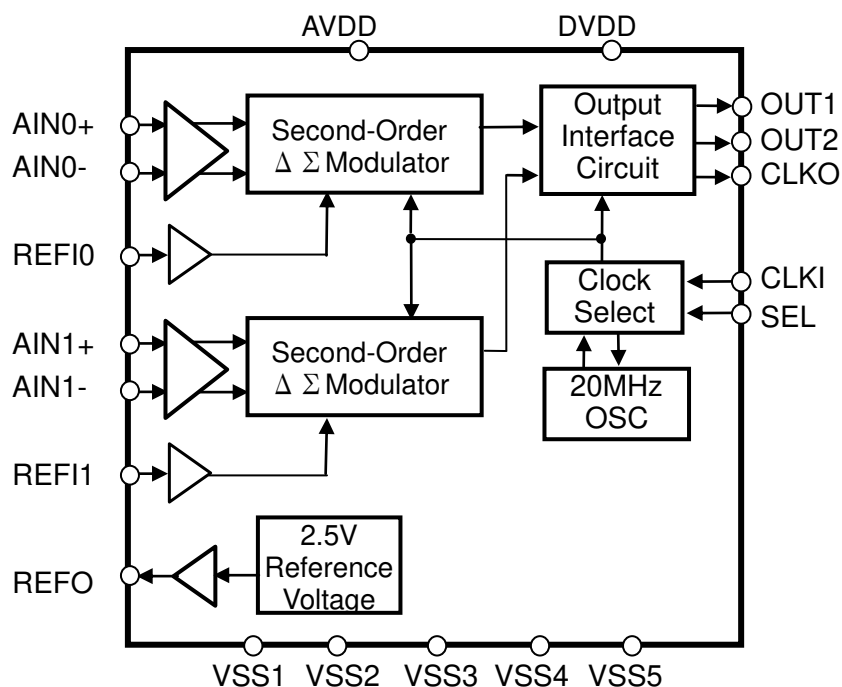
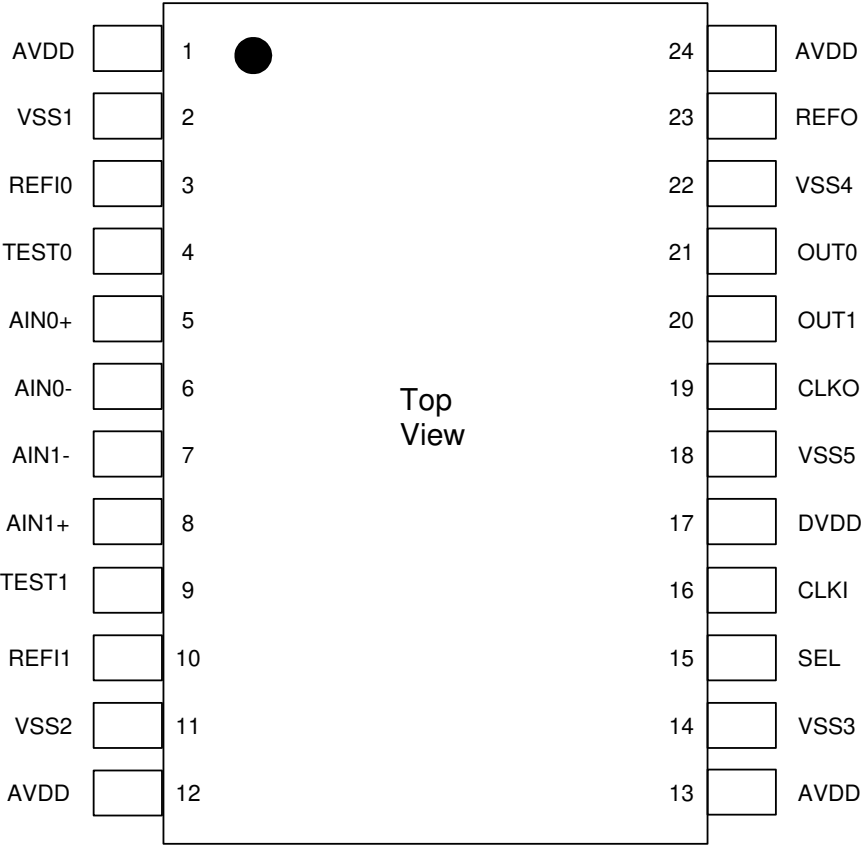


Figure 1. Block Diagram

■ Pin Configurations



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| Pin Functions |
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| Pin No. | Pin Name | I/O | Function |
|---------|----------|-----|--|
| 1 | AVDD | - | Analog Power Supply: 4.5V to 5.5V Connect to VSS1~VSS4 with a 0.1μF ceramic capacitor. |
| 2 | VSS1 | - | Ground |
| 3 | REFI0 | I | Reference Voltage input for Channel 0 |
| 4 | TEST0 | - | TEST Pin. This pin must be open. |
| 5 | AIN0+ | I | Channel 0 Analog input+ |
| 6 | AIN0- | I | Channel 0 Analog input- |
| 7 | AIN1- | I | Channel 1 Analog input- |
| 8 | AIN1+ | I | Channel 1 Analog input+ |
| 9 | TEST1 | - | TEST Pin. This pin must be open. |
| 10 | REFI1 | I | Reference Voltage input for Channel 1 |
| 11 | VSS2 | - | Ground |
| 12 | AVDD | - | Analog Power Supply: 4.5V to 5.5V Connect to VSS1~VSS4 with a 0.1μF ceramic capacitor. |
| 13 | AVDD | - | Analog Power Supply: 4.5V to 5.5V Connect to VSS1~VSS4 with a 0.1μF ceramic capacitor. |
| 14 | VSS3 | - | Ground |
| 15 | SEL | I | Clock select input “H”: internal oscillator, “L”: external clock source |
| 16 | CLKI | I | External clock input If not used, must be tied to DVDD or VSS5 |
| 17 | DVDD | - | Digital Power Supply: 2.7 V to 3.6V (or 4.5V to 5.5V) Connect to VSS5 with a 0.1μF ceramic capacitor. |
| 18 | VSS5 | - | Ground |
| 19 | CLKO | O | Clock output |
| 20 | OUT1 | O | Data output of Channel 1 modulator |
| 21 | OUT0 | O | Data output of Channel 0 modulator |
| 22 | VSS4 | - | Ground |
| 23 | REFO | O | Reference Voltage output for Channel 0 and Channel 1 |
| 24 | AVDD | - | Analog Power Supply: 4.5V to 5.5V Connect to VSS1~VSS4 with a 0.1μF ceramic capacitor. |

Note 1. Digital input pins (SEL, CLKI) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

| Classification | Pin Name | Setting |
|----------------|--|---------|
| Analog | AIN0+, AIN0-, AIN1+, AIN1-, REFI0, REFI1 | VSS |

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| Absolute Maximum Ratings |
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(VSS1~VSS5 = 0V; Note 2, Note 3)

| Parameter | Symbol | Min. | Max. | Unit |
|--|--------|------|----------|------|
| Power Supply | VDD | -0.3 | +6.0 | V |
| Analog Input Current (AIN0+, AIN0-, AIN1+, AIN1-, REF10, REF11) | AIIN | - | ±10 | mA |
| Analog Input Voltage (AIN0+, AIN0-, AIN1+, AIN1-, REF10, REF11) | AVIN | -0.3 | AVDD+0.3 | V |
| Digital Input Current (CLKI, SEL) | DIIN | - | ±10 | mA |
| Digital Input Voltage (CLKI, SEL) | DVIN | -0.3 | DVDD+0.3 | V |
| Storage Temperature | Tstg | -65 | 150 | °C |

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

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| Recommended Operating Conditions |
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(VSS1~VSS5 = 0V; Note 2, Note 3)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------|----------------------|----------------|------|--------------|------|
| Analog Power Supply | AVDD | 4.5 | 5.0 | 5.5 | V |
| Digital Power Supply | DVDD | 3V logic level | 2.7 | 3.0 | V |
| | | 5V logic level | 4.5 | 5 | V |
| Input Reference Voltage | REFI | 0.5 | 2.5 | 2.6 | V |
| Analog Input | Vin= (AIN+) - (AIN-) | -0.92 x VREF | | +0.92 x VREF | V |
| External clock | | 16 | 20 | 24 | MHz |
| Ambient Operating Temperature | Ta | -40 | | 105 | °C |

Note 2. All voltages are with respect to ground.

Note 3. VSS1, VSS2, VSS3, VSS4 and VSS5 must be connected to the same analog ground plane.

Note 4. The power supply sequence between AVDD and DVDD is not critical upon power-up.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

Analog Characteristics

(Ta = -40°C to 105°C; AVDD=5V, DVDD=3V, AIN+=0.2V to 4.8V, AIN-=2.5V, REFI=REFO=2.5V (internal), CLKI= 20MHz, and 16bit Sinc³ filter with OSR =256; unless otherwise specified)

| Parameter | | Min. | Typ. | Max. | Unit |
|--|---------------------------------|--------------|------------|--------------|-------------------|
| Resolution | | 16 | - | - | Bits |
| Integral Nonlinearity (INL) Error (Note 5) | VIN = $\pm 2.3V_{pp}$ | -8 | ± 3.8 | +8 | LSB |
| | VIN = $\pm 2.0V_{pp}$ | -4 | ± 1.8 | +4 | LSB |
| Integral Nonlinearity Match | | - | 1 | 4 | LSB |
| Differential Nonlinearity (DNL) Error | | -1 | - | +1 | LSB |
| Offset Error REFI=2.5V | | -3 | ± 1.5 | +3 | mV |
| Offset Error Match | | - | 0.2 | 2 | mV |
| Offset Error Drift (Note 6) | | -8 | 1 | +8 | $\mu V/^{\circ}C$ |
| Gain Error (Note 7) | Referenced REFI = 2.5V | -0.5 | ± 0.02 | +0.5 | %FSR |
| Gain Error Match | | - | 0.1 | 0.5 | %FSR |
| Gain Error Drift (Note 8) | | - | ± 1.3 | - | ppm/ $^{\circ}C$ |
| PSRR | | - | 82 | - | dB |
| Analog Input | | | | | |
| Full scale Differential Input Voltage Range: | (AIN+)-(AIN-) AIN- =2.5V | -REFI | - | +REFI | V |
| Specified Differential Input Voltage Range | (AIN+)-(AIN-) AIN- =2.5V | -0.92 x REFI | - | +0.92 x REFI | V |
| Absolute Input Voltage Range | | 0 | - | AVDD | V |
| Input Capacitance | AIN to VSS | - | 1 | - | pF |
| Input Leakage Current | Clock turned off (Note 9) | -1 | - | +1 | μA |
| Differential Input Resistance | | 80 | 100 | 120 | k Ω |
| Differential Input Capacitance | | - | 2.5 | - | pF |
| CMRR AIN- =2.5V | at dc | - | 108 | - | dB |
| | Vin = $\pm 1.25V_{pp}$ at 40kHz | - | 117 | - | dB |
| Sampling Dynamics | | | | | |
| Internal Clock Frequency | SEL=1, -40°C to +105°C | 9 | 10 | 11 | MHz |
| External Clock Frequency | SEL=0 (Note 10) | 1 | 20 | 24 | MHz |
| Dynamic Characteristics | | | | | |
| THD | Vin = $\pm 2.3V_{pp}$ at 5kHz | - | -85 | -80 | dB |
| SFDR | Vin = $\pm 2.3V_{pp}$ at 5kHz | 82 | 86 | - | dB |
| S/N | Vin = $\pm 2.3V_{pp}$ at 5kHz | 88 | 92 | - | dB |
| | Vin = $\pm 2.0V_{pp}$ at 5kHz | 87 | 91 | - | dB |
| S/(N+D) | Vin = $\pm 2.3V_{pp}$ at 5kHz | 80 | 84 | - | dB |
| Channel to Channel Isolation | Vin = $\pm 2.3V_{pp}$ at 5kHz | - | 100 | - | dB |

Note 5. Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range.

Note 6. This is the maximum variation referring the offset of Ta = 25°C when the temperature range is from -40 to 105°C.

Note 7. Referring the REFI pin (It does not include internal VREF variation)

Note 8. This value does not include temperature drift of the internal VREF.

Note 9. Outgoing current from the AK9223 is defined as “-” polarity.

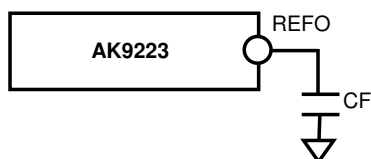
Note 10. Recommended input range of the external clock is from 16MHz to 24MHz. The range of 1MHz~16MHz and 24MHz~32MHz can also be available with reduced accuracy.

Analog Characteristics

(Ta = -40°C to 105°C; AVDD=5V, DVDD=3V, AIN+=0.2V to 4.8V, AIN-=2.5V, REFIx=REFO=2.5V (internal), CLKI= 20MHz, and 16bit Sinc³ filter with OSR =256; unless otherwise specified)

| Parameter | | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------------|-------|------|-------|--------|
| Reference Voltage Output | | | | | |
| Reference output voltage | | 2.475 | 2.5 | 2.525 | V |
| Reference output voltage drift | | | ±20 | | ppm/°C |
| Output current | | | 10 | | μA |
| Short-circuit current | | | 0.5 | | mA |
| Turn-on settling time | CF = 0.1μF (Note 11) | | 500 | | μs |
| Reference Voltage Input | | | | | |
| Reference input voltage | | 0.5 | 2.5 | 2.6 | V |
| Input resistance | | | 100 | | MΩ |
| Input capacitance | | | 5 | | pF |
| Input current | | | | 1 | μA |
| Power Supplies | | | | | |
| AIDD | SEL=1 | | 12.2 | 17 | mA |
| | SEL=0 | | 11.8 | 16 | mA |
| DIDD | DVDD=3V, CLKO = 10MHz | | 0.9 | 2 | mA |
| | DVDD=5V, CLKO = 10MHz | | 1.3 | 3 | mA |

Note 11. To accuracy level of 0.1%. This value will be 40μs (typ) when no load.



DC Characteristics

(Ta = -40°C to 105°C, AVDD=4.5V to 5.5V, DVDD=2.7V to 5.5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|------------|------|------------|------|
| High-Level Input Voltage1, DVDD=2.7V to 3.6V | VIH1 | 2 | | - | V |
| Low-Level Input Voltage1, DVDD=2.7V to 3.6V | VIL1 | - | | 0.8 | V |
| High-Level Input Voltage2, DVDD=4.5V to 5.5V | VIH2 | 0.7 x DVDD | - | - | V |
| Low-Level Input Voltage2, DVDD=4.5V to 5.5V | VIL2 | - | - | 0.3 x DVDD | V |
| Input capacitance | Ic | - | 5 | - | pF |
| Input Leakage Current | Iin | - | - | ±1 | uA |
| High-Level Output Voltage , DVDD=4.5V (Iout = -100μA) | VOH2 | 4.44 | - | - | V |
| Low-Level Output Voltage , DVDD=4.5V (Iout = 100μA) | VOL2 | - | - | 0.5 | V |
| High-Level Output Voltage , DVDD=2.7V (Iout = -100μA) | VOH1 | DVDD-0.2 | - | - | V |
| Low-Level Output Voltage , DVDD=2.7V (Iout = 100μA) | VOL1 | - | - | 0.2 | V |
| Output Capacitance | CO | - | 5 | - | pF |
| Load Capacitance | CL | - | - | 30 | pF |

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| Switching Characteristics |
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(Ta = -40°C to 105°C, AVDD=5V, DVDD=2.7V to 5.5V, CL=30pF)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|-------|--------|-------------|------|-------------|------|
| CLKI period | | tCKI | 41.6 | | 1000 | ns |
| CLKI High Pulse Width | | tCKH | 10 | | tCKI-10 | ns |
| CLKO period | SEL=0 | tCKO1 | 2 x tCKI | | 111 | ns |
| | SEL=1 | tCKO2 | 91 | | | ns |
| CLKO High Pulse Width | | tCKOH | (tCKO/2) -5 | | (tCKO/2)+ 5 | ns |
| CLKI "↑" to CLKO "↓" Delay | SEL=0 | tPD1 | | | 10 | ns |
| CLKI "↑" to CLKO "↑" Delay | SEL=0 | tPD2 | | | 10 | ns |
| CLKO "↑" to OUT data Delay | SEL=0 | tPD3 | tCKH-3 | | tCKH+7 | ns |
| | SEL=1 | tPD4 | (tCKO/4)-8 | | (tCKO/4)+8 | ns |

■ Timing Diagram

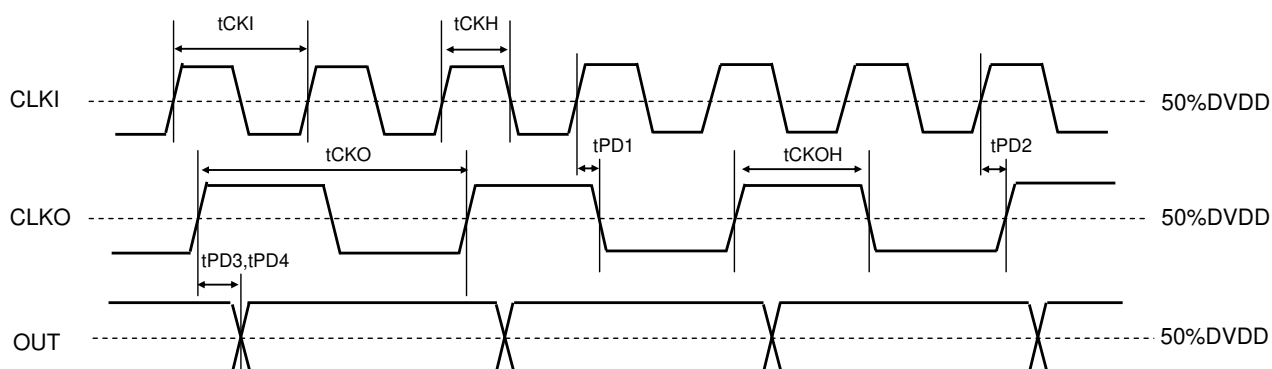


Figure 2. Data Output Timing

Functional Descriptions

The AK9223 is a 2ch delta-sigma modulator. “0” and “1” data is output from its OUT pins and the level of analog input signal is expressed by the density of this digital output.

A delta-sigma modulator shifts quantized noise to high band. A low-pass filter is needed at the output of the AK9223. High band noise is filtered and the 1-bit data stream at a high sampling rate is converted into a higher-bit data word at a lower rate by this low-pass filter (decimation). This digital filter can be composed by a FPGA and etc. [Figure 3](#) shows external circuit example. Recommended parts shown below should be connected as close as possible to the device.

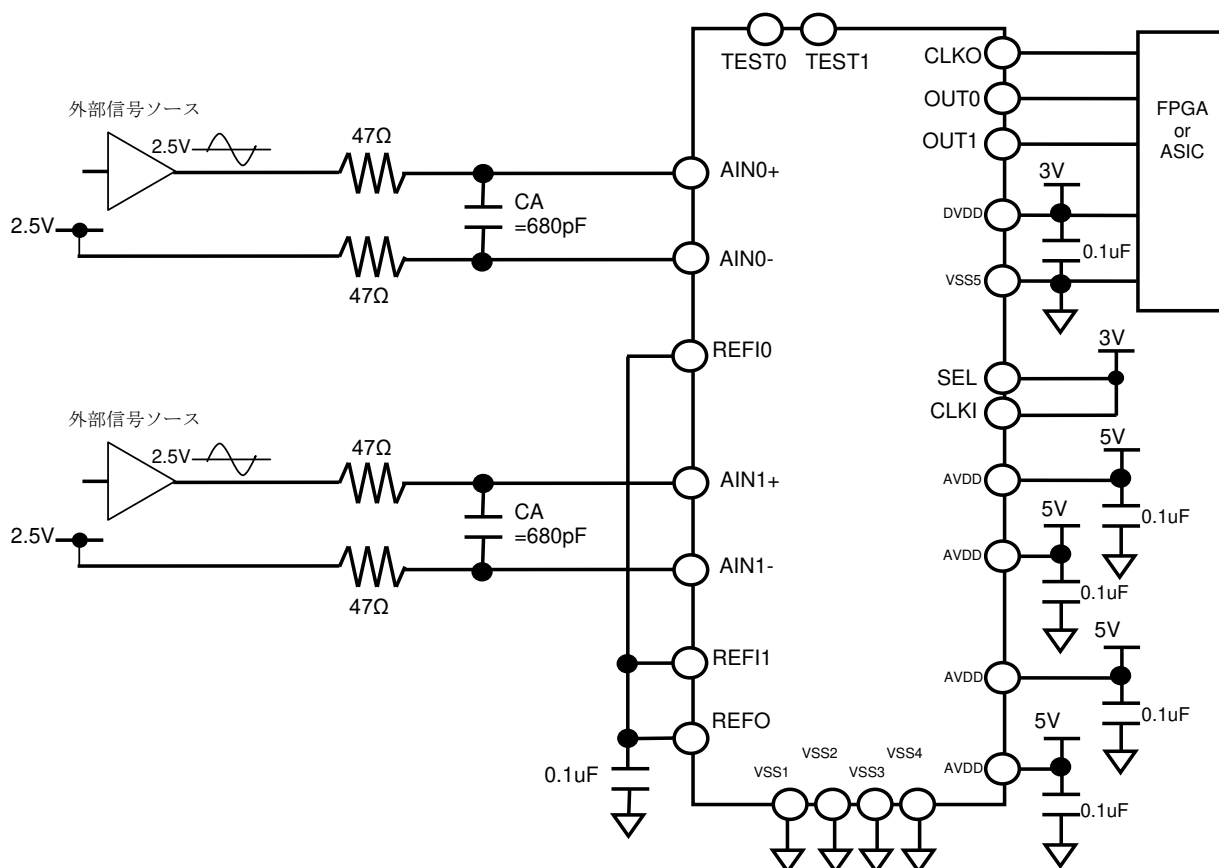


Figure 3. AK9223 Recommended External Circuits

AD conversion characteristics (speed and accuracy) are dependent on OSR (over sampling ratio) and digital filter type. When the conversion rate is low, greater output accuracy can be achieved by increasing the OSR. When the OSR is low, output accuracy is low but high speed conversion is available. With an appropriate digital filter, the AK9223 is capable of AD conversion results that have a dynamic range exceeding 86dB with an OSR = 256.

■ Internal Operation

The analog input of the AK9223 is composed by SC (switched-capacitor) circuits and this modulator block digitizes analog inputs to 1-bit data stream. The clock source can be external or internal oscillator output. Analog input is sampled by the modulator and compared with the reference voltage of the REFI pin. A digital stream that represents the analog input voltage over time appears at the output of the corresponding converter.

■ Modulator

The AK9223 can be operated in two modes. Internal oscillation is used for the operation clock of the modulator by setting the SEL pin = "H". In this case, the internal clock is fixed to 20MHz. When the SEL pin is set to "L", modulator clock is externally input to the CLKI pin. In both of modes, the clock is internally divided by two and functions as the modulator clock. When using an external clock, available input clock range is from 1MHz to 24MHz. In this case, the modulator operates of a clock from 500kHz to 12MHz.

■ Digital I/F

Analog input signals are converted with the modulator input clock. The OUT pin outputs the result of AD conversion. The common clock that is used for two modulators is output from the CLKO pin. When the SEL pin = "H", the CLKI pin must not be allowed to float but should be connected to DVDD or VSS5.

■ Digital Filter

Digital data stream is output from the modulator. This data stream should be processed by a digital filter to obtain an equivalent digital data to the analog input. Transfer function of the simple Sinc³ filter is shown below.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3$$

This filter provides the best output performance with a relatively low number of gates required for implementation. All the characterizations in this datasheet are done using a Sinc³ filter (OSR = 256, Output Word Width: 16 bits).

Figure 4 and Figure 5 show the filter characteristics. The location of the first notch is fDATA (=fMOD / OSR). The -3dB point is located at half the Nyquist frequency or fDATA/4.

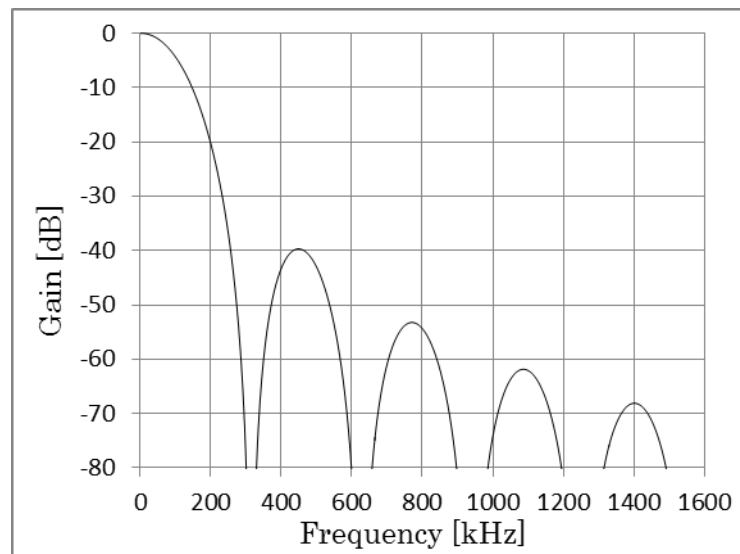


Figure 4. Sinc³ Frequency Characteristics (OSR=32)

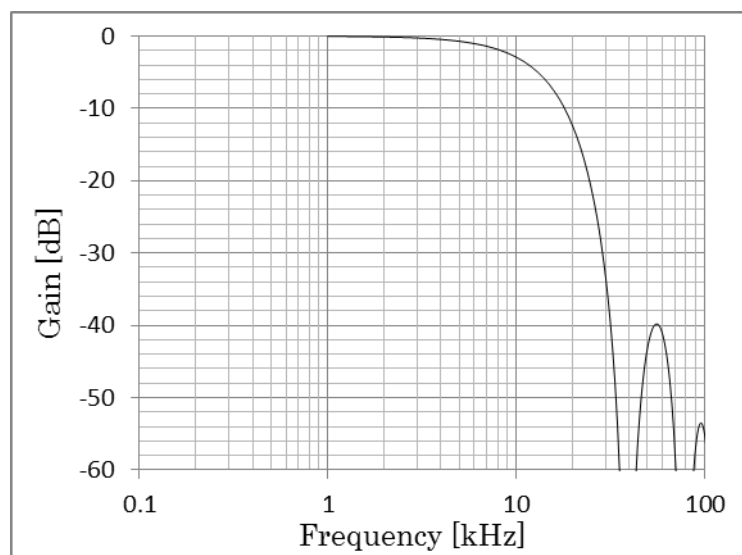


Figure 5. Sinc³ Frequency Characteristics (OSR=256)

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| System Design |
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■ Power Supply

Digital power supply determines the I/O interface voltage. It ranges from 2.7V to 5.5V. Inputs to the AK9223, such as AIN+, AIN- and CLKI pins should not be present before the power supply is on.

■ Decoupling

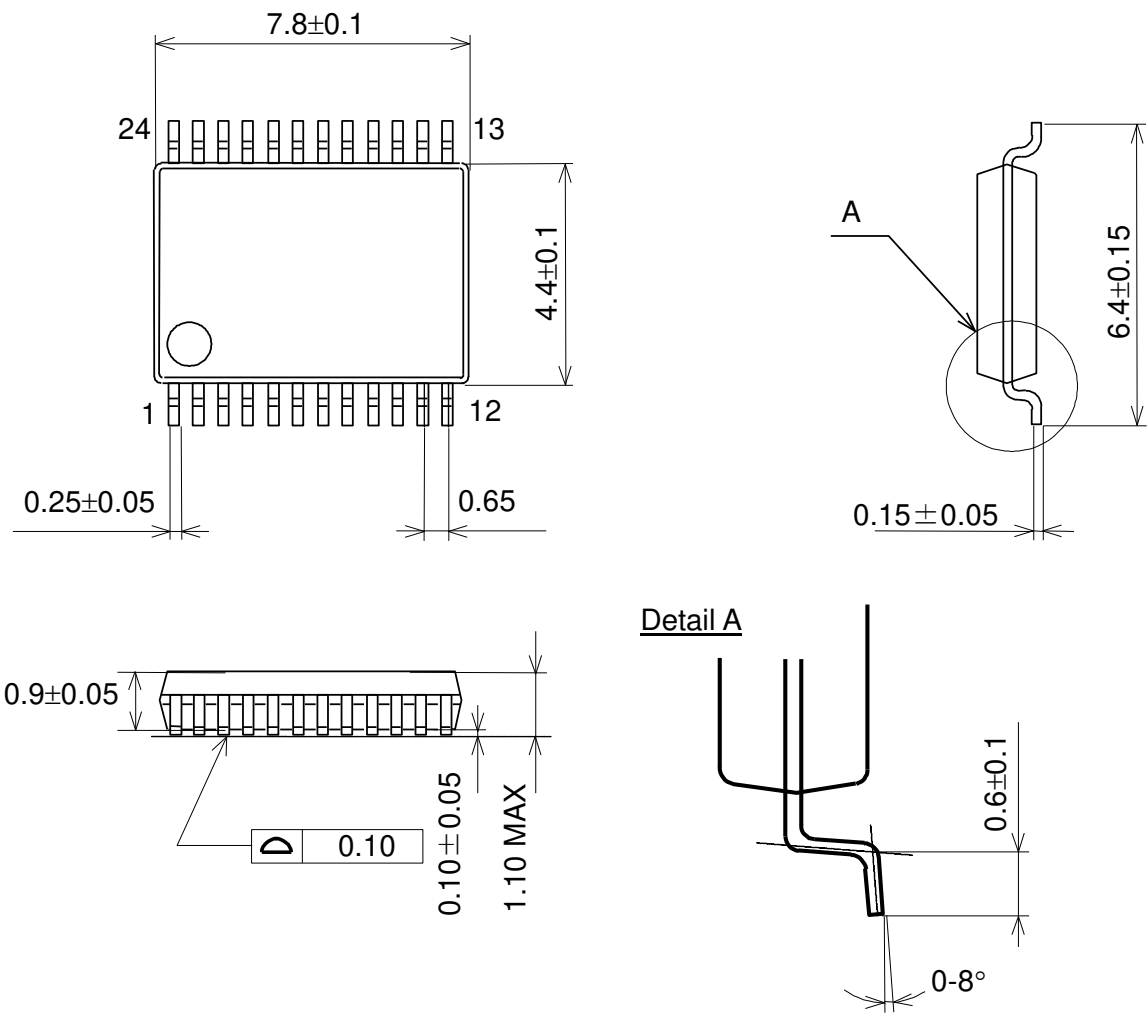
A decoupling capacitor should be connected to the pin as close as possible. A 0.1 μ F ceramic capacitor should be connected between AVDD (Pin #1) and VSS1, AVDD (Pin #12) and VSS2, AVDD (Pin #13) and VSS3, AVDD (Pin #24) and VSS4, and DVDD and VSS5.

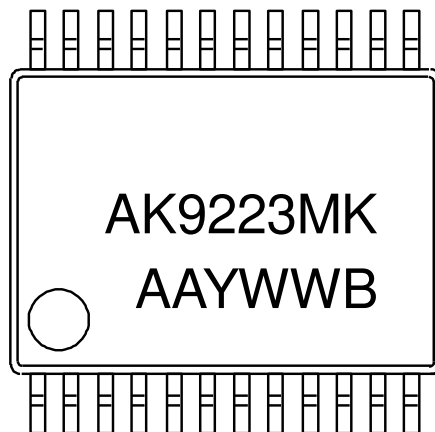
If the analog and digital I/O powers are drawn from the same source, connect a 10 Ω resistor between the analog and digital power supply pins, and connect the power source to the analog power supply pin. An RC filter should be composed by this 10 Ω resistor and a 0.1 μ F capacitor to reduce noises in the analog supply.

Package

■ Outline Dimensions

24-pin TSSOP (Unit: mm)



■ Marking

- a. Pin #1 Indication
- b. Product Name: AK9223MK
- c. Date Code: AAYWWB

| | | |
|----|---|-----------------------------|
| AA | : | Administration Code 2digits |
| Y | : | Year 1digit |
| WW | : | Week 2digits |
| B | : | Administration Code 1digit |

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| Ordering Guide |
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■ Ordering Guide

AK9223MK

-40 ~ +105°C

24-pin TSSOP (0.65mm pitch)

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| Revision History |
|-------------------------|

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|--------------|----------|---------------|------|--|
| 15/01/15 | 00 | First Edition | | |
| 15/07/29 | 01 | | p.3 | (Pin No.7) Pin Name : AIN1+ Function : Channel 1 Analog input+ ↓ Pin Name : AIN1- Function : Channel 1 Analog input- (Pin No.8) Pin Name : AIN1- Function : Channel 1 Analog input- ↓ Pin Name : AIN1+ Function : Channel 1 Analog input+ |
| 19/02/01 | 02 | | p.3 | (Pin No.23) Pin Name : REF0 I/O: I ↓ Pin Name : REFO I/O: O (Pin No.23) Function : Reference Voltage input for Channel 0 ↓ Function : Reference Voltage output for Channel 0 and Channel 1 |

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