Si5323

Pin-Programmable Precision Clock Multiplier/Jitter Attenuator

Features

- Pin-selectable output frequencies ranging from 8 kHz–708 MHz
- Ultra-low jitter clock outputs as low as 250 fs rms (12 kHz–20 MHz) 270 fs rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz–8.4 kHz)
- Meets ITU-T G.8251 and Telcordia OC-192 GR-253-CORE jitter specifications
- Hitless input clock switching with phase build-out and digital hold
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOL, LOS alarm outputs
- Pin-controlled output phase adjust
- Single supply 1.8 ±5%, 2.5 or 3.3 V ±10% operation with high PSRR
- On-chip voltage regulator
- Small size: 6 x 6 mm 36-lead QFN

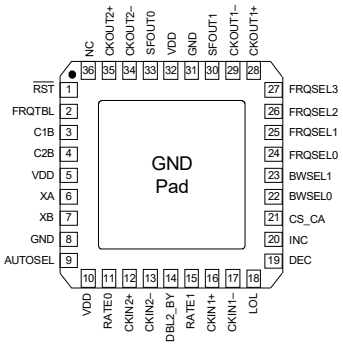
Ordering Information:

See page 33.

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement
- Synchronous Ethernet

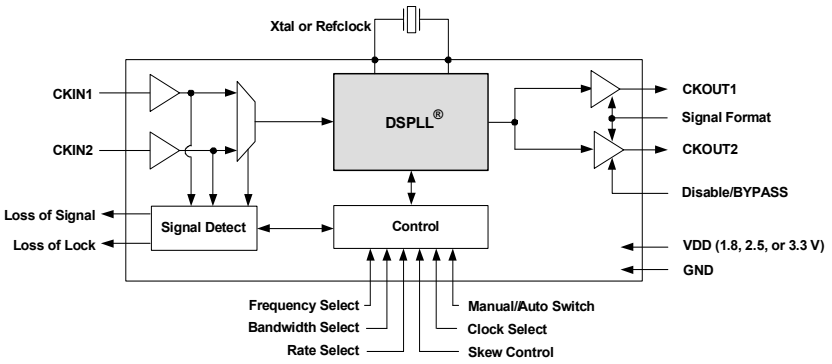
Pin Assignments



Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two equal frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5323 is based on Skyworks Solutions' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5323 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}	3.3 V nominal	2.97	3.3	3.63	V
		2.5 V nominal	2.25	2.5	2.75	V
		1.8 V nominal	1.71	1.8	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current (Supply current is independent of V_{DD})	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled[1]	—	251	279	mA
		LVPECL Format 622.08 MHz Out Only 1 CKOUT Enabled[1]	—	217	243	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	204	234	mA
		CMOS Format 19.44 MHz Out Only CKOUT1 Enabled	—	194	220	mA
CKIN Input Pins						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Input Voltage Level Limits	CKN_{VIN}	See note [2]	0	—	V_{DD}	V
Single-ended Input Voltage Swing	V_{ISE}	$f_{CKIN} \leq$ 212.5 MHz See Figure 2.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 2.	0.25	—	—	V_{PP}

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential Input Voltage Swing	V_{ID}	$f_{CKIN} \leq$ 212.5 MHz See Figure 2.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 2.	0.25	—	—	V_{PP}
Output Clocks (CKOUTn)[1]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single-ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD} – 0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVDS, LVPECL	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current	CKO_{IO}	CMOS Driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally.				
		V_{DD} = 1.8 V	—	7.5	—	mA
		V_{DD} = 3.3 V	—	32	—	mA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V
Input Low Current	I_{IL}		—	—	50	µA
Input High Current	I_{IH}		—	—	50	µA
Weak Internal Input Pull-up Resistor	R_{PUP}		—	75	—	kΩ
Weak Internal Input Pull-down Resistor	R_{PDN}		—	75	—	kΩ
3-Level Input Pins						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}[3]		–20	—	—	µA
Input Mid Current	I_{IMM}[3]		–2	—	2	µA
Input High Current	I_{IHH}[3]		—	—	20	µA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	I_O = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
		I_O = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	I_O = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
		I_O = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V
Disabled Leakage Current	I_{OZ}	$\overline{RST}$ = 0	–100	—	100	µA
Single-Ended Reference Clock Input Pin XA (XB with cap to gnd)						
Input Resistance	XA_{RIN}	XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM	—	12	—	kΩ
Input Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Input Voltage Swing	XA_{VPP}		0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Resistance	XA/XB_{RIN}	XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM	—	12	—	kΩ
Differential Input Voltage Level Limits	XA/XB_{VIN}		0	—	1.2	V
Input Voltage Swing	XA_{VPP}/XB_{VPP}		0.5	—	1.2	$V_{PP, each}$

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

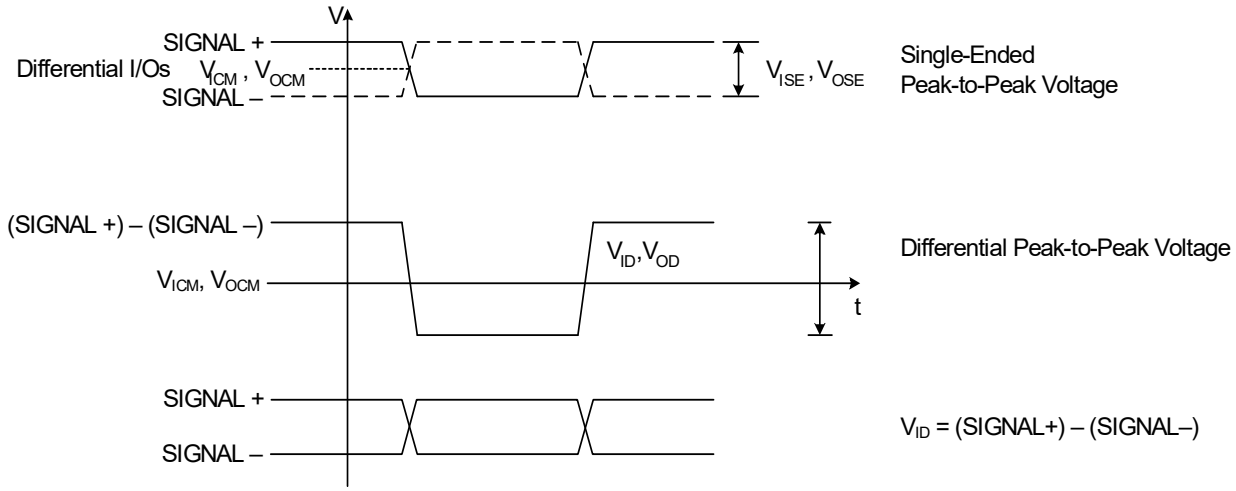


Figure 1. Voltage Characteristics

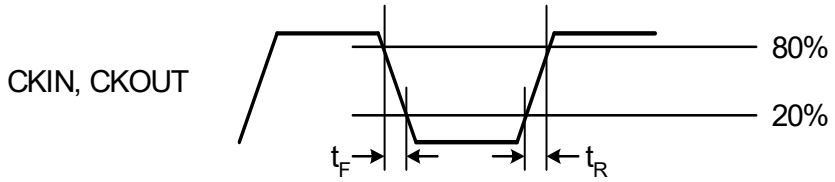


Figure 2. Rise/Fall Time Characteristics

1.1. Three-Level (3L) Input Pins (No External Resistors)

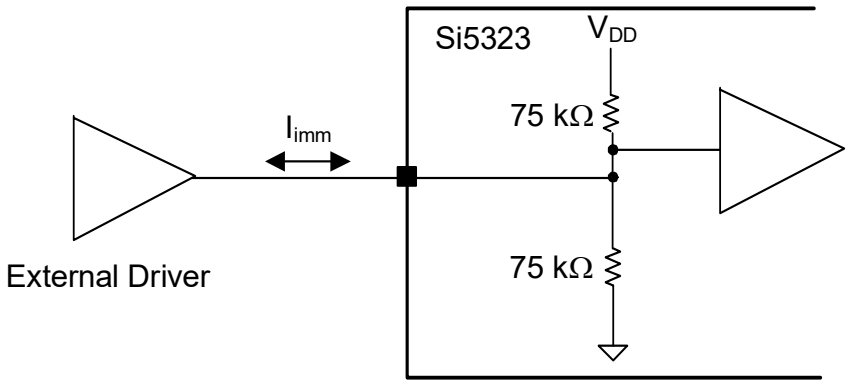
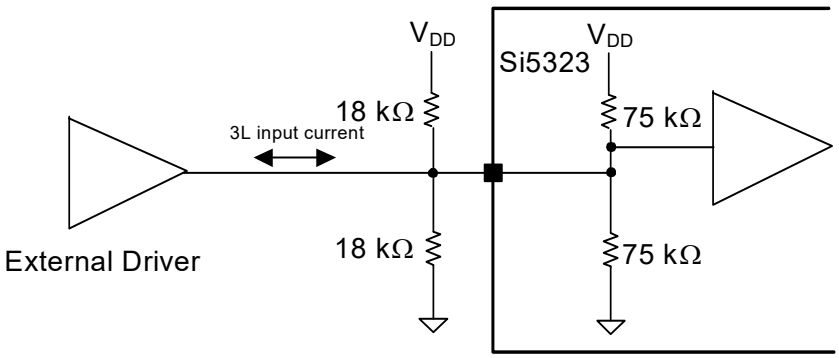


Figure 3. Three-Level Input Pins

1.2. Three-Level Input Pins (Example with External Resistors)



One of eight resistors from a Panasonic EXB-D10C183J (or similar) resistor pack

Figure 4. Three-Level Input Pins

Table 3. Three-Level Input Pins[1,2,3,4]

Parameter	Min	Max
Input Low Current	–30 µA	—
Input Mid Current	–11 µA	–11 µA
Input High Current	—	–30 µA

Notes:
1. The current parameters are the amount of leakage that the 3L inputs can tolerate from an external driver using the external resistor values indicated in this example. In most designs, an external resistor voltage divider is recommended.
2. Resistor packs are only needed if the leakage current of the external driver exceeds the current specified in Table 2, Iimm. Any resistor pack may be used (e.g., Panasonic EXB-D10C183J). PCB layout is not critical.
3. If a pin is tied to ground or V_{DD}, no resistors are needed.
4. If a pin is left open (no connect), no resistors are needed.

Table 4. AC Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CKIN Input Pins						
Input Frequency	CKN_F		.008	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40%/60% limitation applies only to high clock frequencies)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins						
Output Frequency (Output not configured for CMOS or disable)	CK_{OF}		.008	—	710	MHz
Maximum Output Frequency in CMOS Format	CKO_{FMC}		—	—	212.5	MHz
Single-ended Output Rise/Fall (20–80%)	CKO_{TRF}	CMOS Output V_{DD} = 1.71 Cload = 5 pF	—	—	8	ns
		CMOS Output V_{DD} = 2.97 Cload = 5 pF	—	—	2	ns
Differential Output Rise/Fall Time	CKO_{TRF}	20 to 80 %, f_{OUT} = 622.08	—	230	350	ps
Output Duty Cycle Differential Uncertainty	CKO_{DC}	100 Ω Load Line to Line Measured at 50% Point (not for CMOS)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMIN}		1	—	—	µs
Input Capacitance	C_{IN}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20 pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKIN↑ to LOS↑		—	750	µs
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	f_{in} unchanged and XA/XB stable. ↓ LOS to ↓ LOL	—	10	—	ms

Table 4. AC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PLL Performance						
Lock Time	t_{LOCKHW}	Whenever $\overline{RST}$, FRQTBL, RATE, BWSEL, or FRQSEL are changed, with valid CKIN to ↓ LOL; BW = 100 Hz	—		1.2	sec
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	BW determined by BWSEL[1:0]	5000/ BW	—	—	ns pk-pk
Spurious Noise	SP_{SPUR}	Max spur @ n x f3 (n ≥ 1, n x f3 < 100 MHz)	—	–93	–70	dBc
Phase Change due to Temperature Variation	t_{TEMP}	Max phase changes from –40 to +85 ºC	—	300	500	ps

Table 5. Performance Specifications[1, 2, 3, 4, 5]
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Generation f_{IN} = f_{OUT} = 622.08 MHz, LVPECL Output Format BW = 120 Hz	J_{GEN}	50 kHz–80 MHz	—	0.27	0.42	ps rms
		12 kHz–20 MHz	—	0.25	0.41	ps rms
		800 Hz–80 MHz	—	0.28	0.45	ps rms
Phase Noise f_{IN} = f_{OUT} = 622.08 MHz LVPECL Output Format	CKO_{PN}	1 kHz offset	—	–106	–87	dBc/Hz
		10 kHz offset	—	–121	–100	dBc/Hz
		100 kHz offset	—	–122	–104	dBc/Hz
		1 MHz offset	—	–132	–119	dBc/Hz

Notes:
1. BWSEL [1:0] loop bandwidth settings provided in Table 11 on page 27.
2. 114.285 MHz 3rd OT crystal used as XA/XB input.
3. V_{DD} = 2.5 V
4. T_A = 85 °C
5. Test condition: f_{IN} = 622.08 MHz, f_{OUT} = 622.08 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20-80%), LVPECL clock output.

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	32	—	ºC/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	14	—	ºC/W

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CKINn Voltage Level Limits	CKN_{VIN}	0 to V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}	0 to 1.2	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		150	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		750	V
ESD MM Tolerance; CKIN+/CKIN–		100	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Phase Noise Plots

The following is the typical phase noise performance of the Si5323. The clock input source was a Rohde and Schwarz model SML03 RF Generator. The phase noise analyzer was an Agilent model E5052B. The Si5323 operates at 3.3 V with an ac coupled differential PECL output and an ac coupled differential sine wave input from the RF generator at 0 dBm. Note that, as with any PLL, the output jitter that is below the loop BW is caused by the jitter at the input clock. The loop BW was 120 Hz.

2.1. Example: SONET OC-192

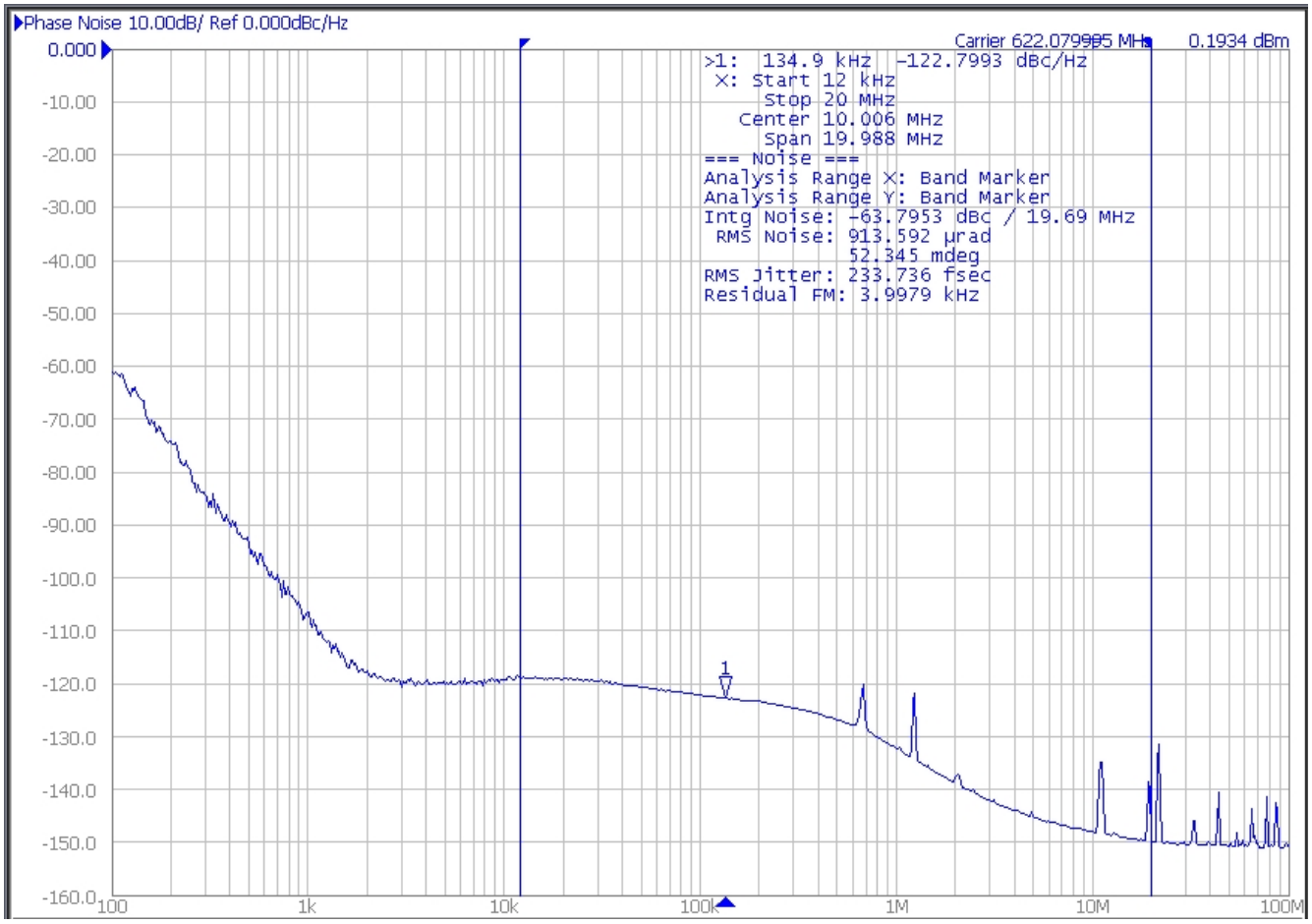
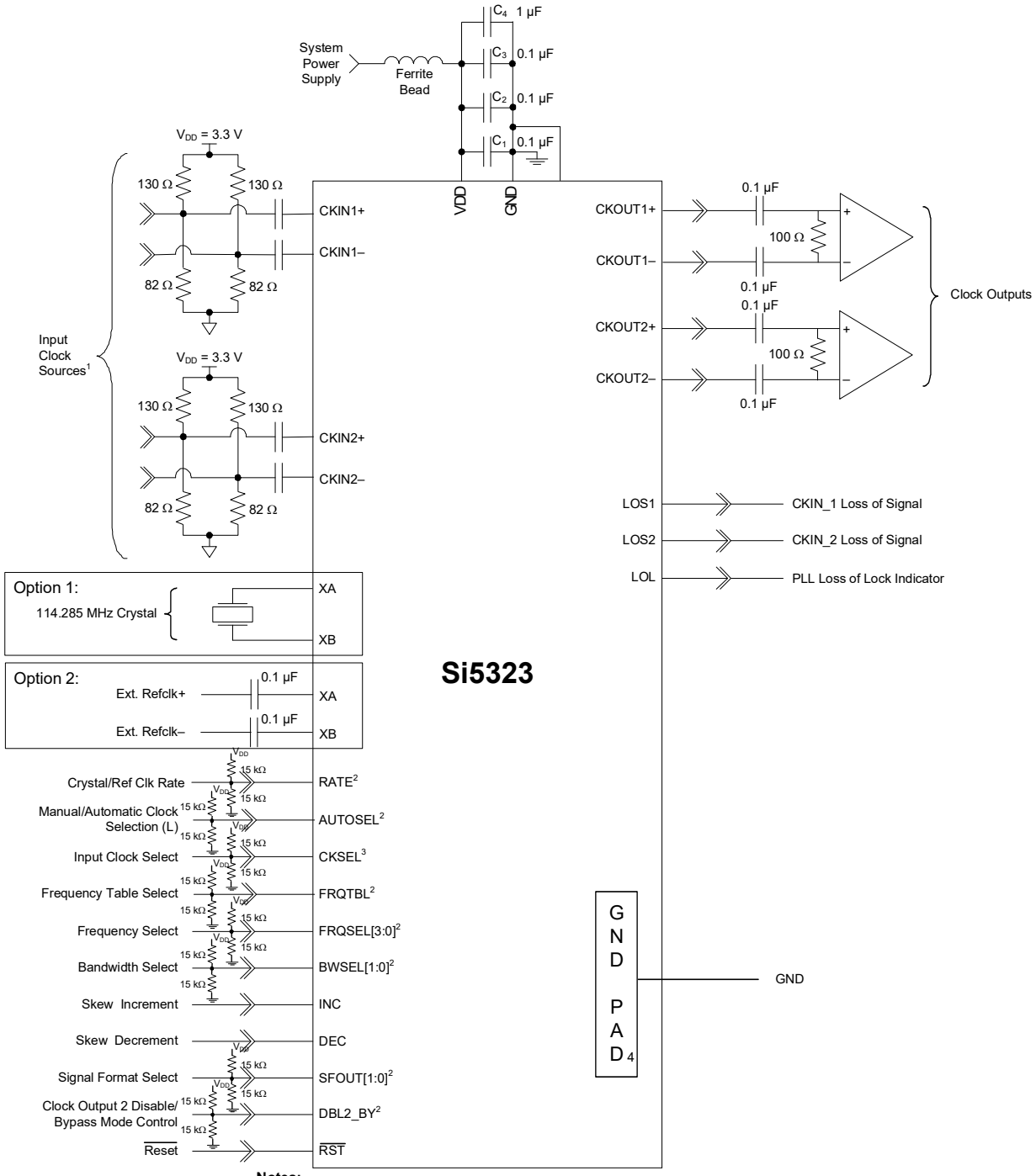


Figure 5. Typical Phase Noise Plot

Jitter Band	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	250 fs
SONET_OC192_A, 20 kHz to 80 MHz	274 fs
SONET_OC192_B, 4 to 80 MHz	166 fs
SONET_OC192_C, 50 kHz to 80 MHz	267 fs
Brick Wall, 800 Hz to 80 MHz	274 fs

Note: SONET jitter bands include the SONET skirts. The phase noise plot is brick wall integration.



Notes:
1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.
4. GND pad must be connected for normal operation.

Figure 6. Si5323 Typical Application Circuit

3. Functional Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5323 supports SONET-to-datacom frequency translations. Skyworks Solutions offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5323 frequency translations.

This utility can be downloaded from https://www.skyworksinc.com/en/Products/Timing.

The Si5323 is based on Skyworks Solutions' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5323 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 60 Hz to 8.4 kHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5323 supports hitless switching between the two input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual and automatic revertive and non-revertive input clock switching options are available via the AUTOSEL input pin. The Si5323 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5323 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5323 has two differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

3.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Skyworks Solutions recommends using a high-quality crystal. Specific recommendations may be found in the Any-Frequency Precision Clock Family Reference Manual. An external clock from a high quality OCXO or TCXO can also be used as a reference for the device.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

3.2. Further Documentation

Consult the Skyworks Solutions Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5323. Additional design support is available from Skyworks Solutions through your distributor.

Skyworks Solutions has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection.

The FRM and this utility can be downloaded from https://www.skyworksinc.com/en/Products/Timing.

3.3. Frequency Plan Tables

The Si5323 provides flexible frequency plans for SONET, Datacom, and interworking between the two (Table 8, Table 9, and Table 10 respectively). Both CKINn inputs must be the same Fin frequency and CKOUTn outputs as specified in the tables.

The following notes apply to Tables 8, 9, and 10:

1. All multiplication ratios are exact, but the frequency values are rounded.
2. For loop bandwidth settings, BWSEL[1:0], f3 values, and frequency operating ranges, consult the DSPLL*sim* software configuration utility.

Table 8. SONET Clock Multiplication Settings (FRQTBL=L)

Plan #	FRQSEL [3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
0	LLLL	0.008	1	0.008
1	LLLM		2430	19.44
2	LLLH		4860	38.88
3	LLML		9720	77.76
4	LLMM		19440	155.52
5	LLMH		38880	311.04
6	LLHL		77760	622.08
7	LLHM	19.44	1	19.44
8	LLHH		2	38.88
9	LMLL		4	77.76
10	LMLM		8	155.52
11	LMLH		8 x (255/238)	166.63
12	LMML		8 x (255/237)	167.33
13	LMMM		8 x (255/236)	168.04
14	LMMH		16	311.04
15	LMHL		32	622.08
16	LMHM		32 x (255/238)	666.51
17	LMHH		32 x (255/237)	669.33
18	LHLL		32 x (255/236)	672.16
19	LHLM		48	933.12
20	LHLH		54	1049.76

Table 8. SONET Clock Multiplication Settings (FRQTBL=L) (Continued)

Plan #	FRQSEL [3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
21	LHML	38.88	1	38.88
22	LHMM		2	77.76
23	LHMH		4	155.52
24	LHHL		16	622.08
25	LHHM		16 x (255/238)	666.51
26	LHHH		16 x (255/237)	669.33
27	MLLL		16 x (255/236)	672.16
28	MLLM	77.76	1/4	19.44
29	MLLH		1/2	38.88
30	MLML		1	77.76
31	MLMM		2	155.52
32	MLMH		2 x (255/238)	166.63
33	MLHL		2 x (255/237)	167.33
34	MLHM		2 x (255/236)	168.04
35	MLHH		4	311.04
36	MMLL		8	622.08
37	MMLM		8 x (255/238)	666.51
38	MMLH		8 x (255/237)	669.33
39	MMML		8 x (255/236)	672.16
40	MMMM	155.52	1/8	19.44
41	MMMH		1/4	38.88
42	MMHL		1/2	77.76
43	MMHM		1	155.52
44	MMHH		255/238	166.63
45	MHLL		255/237	167.33
46	MHLM		255/236	168.04
47	MHLH		2	311.04
48	MHML		4	622.08
49	MHMM		4 x (255/238)	666.51
50	MHMH		4 x (255/237)	669.33
51	MHHL		4 x (255/236)	672.16

Table 8. SONET Clock Multiplication Settings (FRQTBL=L) (Continued)

Plan #	FRQSEL [3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
52	MHHM	166.63	238/255	155.52
53	MMHM		1	166.63
54	MHHH		4 x (238/255)	622.08
55	MHML		4	666.51
56	HLLL	167.33	237/255	155.52
57	MMHM		1	167.33
58	HLLM		4 x (237/255)	622.08
59	MHML		4	669.33
60	HLLH	168.04	236/255	155.52
61	MMHM		1	168.04
62	HLML		4 x (236/255)	622.08
63	MHML		4	672.16
64	HLMM	311.04	1	311.04
65	HLMH		2	622.08
66	HLHL		2 x (255/238)	666.51
67	HLHM		2 x (255/237)	669.33
68	HLHH		2 x (255/236)	672.16
69	HMLL	622.08	1/32	19.44
70	HMLM		1/16	38.88
71	HMLH		1/8	77.76
72	HMML		1/4	155.52
73	HMMM		1/2	311.04
74	HMMH		1	622.08
75	HMHL		255/238	666.51
76	HMHM		255/237	669.33
77	HMHH		255/236	672.16
78	HHLL	666.51	1/4 x 238/255	155.52
79	HMML		1/4	166.63
80	HHLM		238/255	622.08
81	HMMH		1	666.51

Table 8. SONET Clock Multiplication Settings (FRQTBL=L) (Continued)

Plan #	FRQSEL [3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
82	HHLH	669.33	1/4 x 237/255	155.52
83	HMML		1/4	167.33
84	HHML		237/255	622.08
85	HMMH		1	669.33
86	HHMM	672.16	1/4 x 236/255	155.52
87	HMML		1/4	168.04
88	HHMH		236/255	622.08
89	HMMH		1	672.16

Table 9. Datacom Clock Multiplication Settings (FRQTBL = M)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
0	LLLL	15.625	2	31.25
1	LLLM		4	62.5
2	LLLH		8	125
3	LLML		16	250
4	LLMM	25	17/4	106.25
5	LLMH		5	125
6	LLHL		25/4 x 66/64	161.13
7	LLHM		51/8 x 66/64	164.36
8	LLHH		25/4 x 66/64 x 255/238	172.64
9	LMLL		25/4 x 66/64 x 255/237	173.37
10	LMLM		51/8 x 66/64 x 255/238	176.1
11	LMLH		51/8 x 66/64 x 255/237	176.84
12	LMML		17/2	212.5
13	LMMM		17	425
14	LMMH		25 x 66/64	644.53
15	LMHL		51/2 x 66/64	657.42
16	LMHM		25 x 66/64 x 255/238	690.57
17	LMHH		25 x 66/64 x 255/237	693.48
18	LHLL		51/2 x 66/64 x 255/238	704.38
19	LHLM		51/2 x 66/64 x 255/237	707.35
20	LHLH	31.25	2	62.5
21	LHML		4	125
22	LHMM		8	250

Table 9. Datacom Clock Multiplication Settings (FRQTBL = M) (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
23	LHMH	53.125	2	106.25
24	LHHL		4	212.5
25	LHHM		8	425
26	LHHH	106.25	3/2 x 66/64	164.36
27	MLLL		3/2 x 66/64 x 255/238	176.1
28	MLLM		3/2 x 66/64 x 255/237	176.84
29	MLLH		2	212.5
30	MLML		4	425
31	MLMM		6 x 66/64	657.42
32	MLMH		6 x 66/64 x 255/238	704.38
33	MLHL		6 x 66/64 x 255/237	707.35
34	MLHM	125	10/8 x 66/64	161.13
35	MLHH		10/8 x 66/64 x 255/238	172.64
36	MMLL		10/8 x 66/64 x 255/237	173.37
37	MMLM		5 x 66/64	644.53
38	MMLH		5 x 66/64 x 255/238	690.57
39	MMML		5 x 66/64 x 255/237	693.48
40	MMMM	156.25	66/64	161.13
41	MMMH		66/64 x 255/238	172.64
42	MMHL		66/64 x 255/237	173.37
43	MMHM		4 x 66/64	644.53
44	MMHH		4 x 66/64 x 255/238	690.57
45	MHLL		4 x 66/64 x 255/237	693.48
46	MMMM	159.375	66/64	164.36
47	MMMH		66/64 x 255/238	176.1
48	MMHL		66/64 x 255/237	176.84
49	MMHM		4 x 66/64	657.4
50	MMHH		4 x 66/64 x 255/238	704.38
51	MHLL		4 x 66/64 x 255/237	707.35
52	MHLM	161.13	4/5 x 64/66	125
53	MHLH		255/238	172.64
54	MHML		255/237	173.37
55	MHMM		4	644.53
56	MHMH		4 x 255/238	690.57
57	MHHL		4 x 255/237	693.48

Table 9. Datacom Clock Multiplication Settings (FRQTBL = M) (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
58	MHHM	164.36	2/3 x 64/66	106.25
59	MHLH		255/238	176.1
60	MHML		255/237	176.84
61	MHMM		4	657.42
62	MHMH		4 x 255/238	704.38
63	MHHL		4 x 255/237	707.35
64	MHHH	172.64	4/5 x 64/66 x 238/255	125
65	HLLL		64/66 x 238/255	156.25
66	HLLM		238/255	161.13
67	HLLH		4 x 238/255	644.53
68	MHMM		4	690.57
69	HLML	173.37	4/5 x 64/66 x 237/255	125
70	HLMM		64/66 x 237/255	156.25
71	HLMH		237/255	161.13
72	HLHL		4 x 237/255	644.53
73	MHMM		4	693.48
74	HLHM	176.1	2/3 x 64/66 x 238/255	106.25
75	HLLL		64/66 x 238/255	159.375
76	HLLM		238/255	164.36
77	HLLH		4 x 238/255	657.42
78	MHMM		4	704.38
79	HLHH	176.84	2/3 x 64/66 x 237/255	106.25
80	HLMM		64/66 x 237/255	159.375
81	HLMH		237/255	164.36
82	HLHL		4 x 237/255	657.42
83	MHMM		4	707.35
84	HMLL	212.5	2	425
85	HMLM	425	1	425
86	HMLH	644.53	1/5 x 64/66	125
87	HMML		1/4	161.13
88	HMMM		1	644.53
89	HMMH		255/238	690.57
90	HMHL		255/237	693.48
91	HMHM	657.42	1/6 x 64/66	106.25
92	HMML		1/4	164.36
93	HMMM		1	657.42
94	HMMH		255/238	704.38
95	HMHL		255/237	707.35

Table 9. Datacom Clock Multiplication Settings (FRQTBL = M) (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
96	HMHH	690.57	1/5 x 64/66 x 238/255	125
97	HHLL		1/4 x 64/66 x 238/255	156.25
98	HHLM		1/4 x 238/255	161.13
99	HMML		1/4	172.64
100	HHLH		238/255	644.53
101	HMMM		1	690.57
102	HHML	693.48	1/5 x 64/66 x 237/255	125
103	HHMM		1/4 x 64/66 x 237/255	156.25
104	HHMH		1/4 x 237/255	161.13
105	HMML		1/4	173.37
106	HHHL		237/255	644.53
107	HMMM		1	693.48
108	HHHM	704.38	1/6 x 64/66 x 238/255	106.25
109	HHLL		1/4 x 64/66 x 238/255	159.375
110	HHLM		1/4 x (238/255)	164.36
111	HMML		1/4	176.1
112	HHLH		238/255	657.42
113	HMMM		1	704.38
114	HHHH	707.35	1/6 x 64/66 x 237/255	106.25
115	HHMM		1/4 x 64/66 x 237/255	159.375
116	HHMH		1/4 x (237/255)	164.36
117	HMML		1/4	176.84
118	HHHL		237/255	657.42
119	HMMM		1	707.35

Table 10. SONET to Datacom Clock Multiplication Settings

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
0	LLLL	0.008	3125	25
1	LLLM		6480	51.84
2	LLLH		53125/8	53.125
3	LLML		15625/2	62.5
4	LLMM		53125/4	106.25
5	LLMH		15625	125
6	LLHL		78125/4	156.25
7	LLHM		159375/8	159.375
8	LLHH		53125/2	212.5
9	LMLL		53125	425

Table 10. SONET to Datacom Clock Multiplication Settings (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
10	LMLM	19.440	625/486	25
11	LMLH		10625/3888	53.125
12	LMML		3125/972	62.5
13	LMMM		10625/1944	106.25
14	LMMH		3125/486	125
15	LMHL		15625/1944	156.25
16	LMHM		31875/3888	159.375
17	LMHH		15625/1944 x 66/64	161.13
18	LHLL		31875/3888 x 66/64	164.36
19	LHLM		15625/1944 x 66/64 x 255/238	172.64
20	LHLH		31875/3888 x 66/64 x 255/238	176.1
21	LHML		10625/972	212.5
22	LHMM		10625/486	425
23	LHMH		15625/486 x 66/64	644.53
24	LHHL		31875/972 x 66/64	657.42
25	LHHM		15625/486 x 66/64 x 255/238	690.57
26	LHHH		31875/972 x 66/64 x 255/238	704.38
27	MLLL	27.000	1	27
28	MLLM		250/91	74.17582
29	MLLH		11/4	74.25
30	MLML	62.500	2	125
31	MLMM		4	250
32	MLMH	74.176	91/250	27
33	MLHL		1	74.17582
34	MLHM		91 x 11/250 x 4	74.25

Table 10. SONET to Datacom Clock Multiplication Settings (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
35	MLHH	74.250	4/11	27
36	MMLL		4 x 250/11 x 9 1	74.17582
37	MMLM		1	74.25
38	MMLH	77.760	10625/7776	106.25
39	MMML		3125/1944	125
40	MMMM		15625/7776	156.25
41	MMMH		31875/15552	159.375
42	MMHL		15625/7776 x 66/64	161.13
43	MMHM		31875/15552 x 66/64	164.36
44	MMHH		15625/7776 x 66/64 x 255/23 8	172.64
45	MHLL		31875/15552 x 66/64 x 255/2 38	176.1
46	MHLM		10625/3888	212.5
47	MHLH		10625/1944	425
48	MHML		15625/1944 x 66/64	644.53
49	MHMM		31875/3888 x 66/64	657.42
50	MHMH		15625/1944 x 66/64 x 255/23 8	690.57
51	MHHL		31875/3888 x 66/64 x 255/23 8	704.38

Table 10. SONET to Datacom Clock Multiplication Settings (Continued)

Plan #	FRQSEL[3:0]	f_{IN} (MHz)	Mult Factor	f_{OUT}* (MHz)
52	MHHM	155.520	15625/15552	156.25
53	MHHH		31875/31104	159.375
54	HLLL		15625/15552 x 66/64	161.13
55	HLLM		31875/31104 x 66/64	164.36
56	HLLH		15625/15552 x 66/64 x 255/238	172.64
57	HLML		31875/31104 x 66/64 x 255/238	176.1
58	HLMM		10625/7776	212.5
59	HLMH		10625/3888	425
60	HLHL		15625/3888 x 66/64	644.53
61	HLHM		31875/7776 x 66/64	657.42
62	HLHH		15625/3888 x 66/64 x 255/238	690.57
63	HMLL		31875/7776 x 66/64 x 255/238	704.38
64	HMLM	622.080	15625/15552 x 66/64	644.53
65	HMLH		31875/31104 x 66/64	657.42
66	HMML		15625/15552 x 66/64 x 255/238	690.57
67	HMMM		31875/31104 x 66/64 x 255/238	704.38

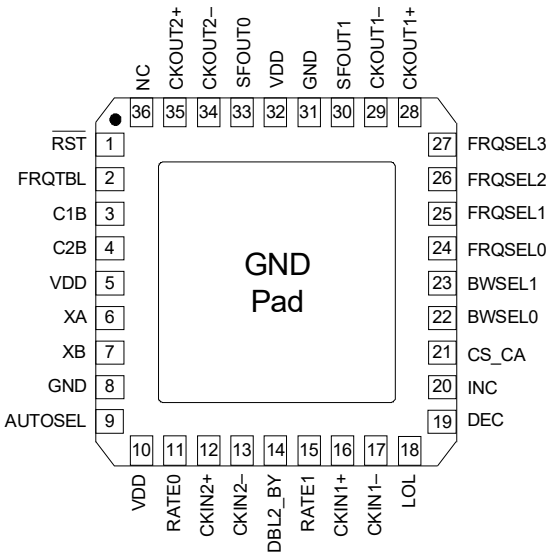
3.3.1. Recommended Reset Guidelines

Follow the recommended RESET guidelines in Table 11 when reset should be applied to the device.

Table 11. Si5323 Pins and Reset

Pin #	Si5323 Pin Name	Must Reset after Changing
2	FRQTBL	Yes
11	RATE0	Yes
14	DBL2_BY	No
15	RATE1	Yes
19	DEC	No
20	INC	No
22	BWSEL0	Yes
23	BWSEL1	Yes
24	FRQSEL0	Yes
25	FRQSEL1	Yes
26	FRQSEL2	Yes
27	FRQSEL3	Yes
30	SFOUT1	No, but skew not guaranteed without Reset
33	SFOUT0	No, but skew not guaranteed without Reset

4. Pin Descriptions: Si5323



Pin assignments are preliminary and subject to change.

Table 12. Si5323 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5323 will perform an internal self-calibration when a valid input signal is present. This pin has a weak pull-up.
2	FRQTBL	I	3-Level	**Frequency Table Select.** Selects SONET/SDH, datacom, or SONET/SDH to datacom frequency table. L = SONET/SDH M = Datacom H = SONET/SDH to Datacom This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tristate.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present 1 = LOS on CKIN1

Table 12. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present 1 = LOS on CKIN2
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to device as is practical.
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. Refer to Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.
8, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
9	AUTOSEL	I	3-Level	**Manual/Automatic Clock Selection.** Three level input that selects the method of input clock selection to be used. L = Manual M = Automatic non-revertive H = Automatic revertive This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
11 15	RATE0 RATE1	I	3-Level	**External Crystal or Reference Clock Rate.** Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
12 13	CKIN2+ CKIN2–	I		**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.

Table 12. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
14	DBL2_BY	I	3-Level	**Output 2 Disable/Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 enabled M = CKOUT2 disabled H = Bypass mode with CKOUT2 enabled This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked
19	DEC	I	LVCMOS	**Skew Decrement.** A pulse on this pin decreases the input to output device skew by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. This pin has a weak pull-down.
20	INC	I	LVCMOS	**Skew Increment.** A pulse on this pin increases the input to output device skew by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. **Note:** If NI_HS = 4, increment is not available. This pin has a weak pull-down.

Table 12. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
21	CS_CA	I/O	LVCMOS	**Input Clock Select/Active Clock Indicator.** **Input**: If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state. 0 = Select CKIN1 1 = Select CKIN2 If configured as an input, this pin must be set high or low. **Output**: If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the digital hold state has been entered, CA will indicate the last active clock that was used before entering the hold state. 0 = CKIN1 active input clock 1 = CKIN2 active input clock
23 22	BWSEL1 BWSEL0	I	3-Level	**Bandwidth Select.** Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
27 26 25 24	FRQSEL3 FRQSEL2 FRQSEL1 FRQSEL0	I	3-Level	**Multiplier Select.** Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting. Consult the Any-Frequency Precision Clock Family Reference Manual or DSPLLsim configuration software for settings, both available for download at https://www.skyworksinc.com/en/Products/Timing. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
29 28	CKOUT1– CKOUT1+	O	Multi	**Clock Output 1.** Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 12. Si5323 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>33
30</td><td>SFOUT0
SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disable</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
These pins have both weak pull-ups and weak pull-downs and default to M.
Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. CMOS outputs do not support bypass mode. LVPECL outputs are not available when V_{DD} = 1.8 V.</td></tr>
<tr><td>34
35</td><td>CKOUT2–
CKOUT2+</td><td>O</td><td>Multi</td><td>Clock Output 2.
Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>36</td><td>NC</td><td>—</td><td>—</td><td>No Connect.
These pins must be left unconnected for normal operation.</td></tr>
<tr><td>GND
PAD</td><td>GND</td><td>GND</td><td>Supply</td><td>Ground Pad.
The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

5. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5323-C-GM	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5322/23-EVB	Evaluation Board		
Note: Add an “R” at the end of the device to denote tape and reel option (i.e., Si5323-C-GMR).			

6. Package Outline: 36-Pin QFN

Figure 7 illustrates the package details for the Si5323. Table 13 lists the values for the dimensions shown in the illustration.

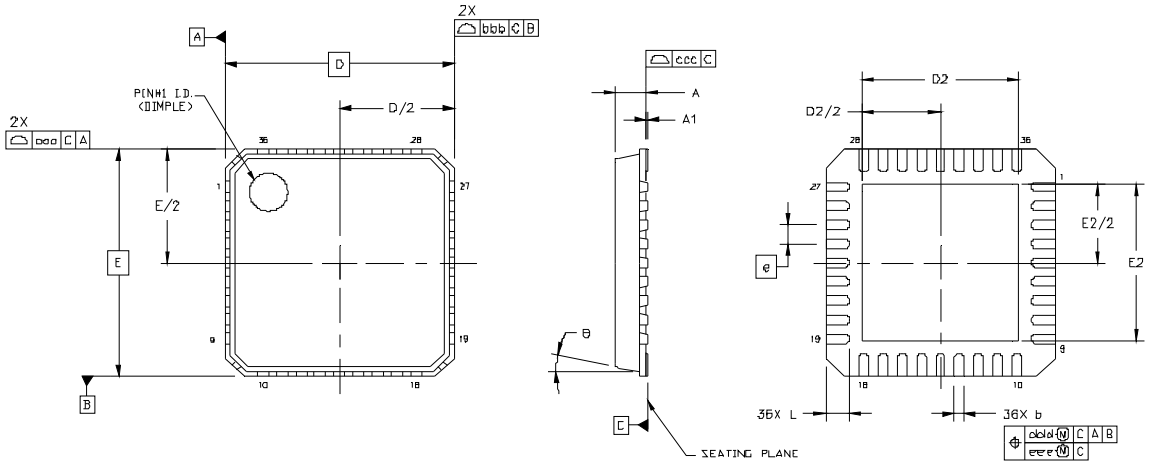


Figure 7. 36-Pin Quad Flat No-Lead (QFN)

Table 13. Package Dimensions

Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.80	0.85	0.90	L	0.50	0.60	0.70
A1	0.00	0.02	0.05	θ	—	—	12º
b	0.18	0.25	0.30	aaa	—	—	0.10
D	6.00 BSC			bbb	—	—	0.10
D2	3.95	4.10	4.25	ccc	—	—	0.08
e	0.50 BSC			ddd	—	—	0.10
E	6.00 BSC			eee	—	—	0.05
E2	3.95	4.10	4.25				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Recommended PCB Layout

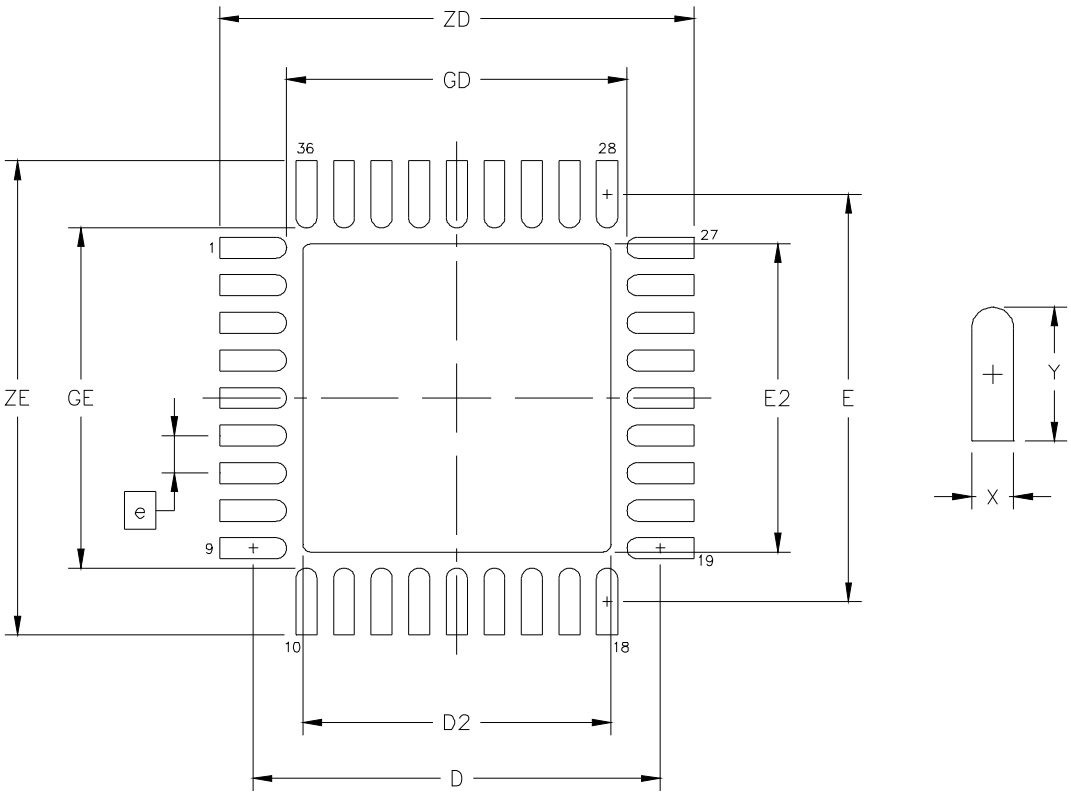


Figure 8. PCB Land Pattern Diagram

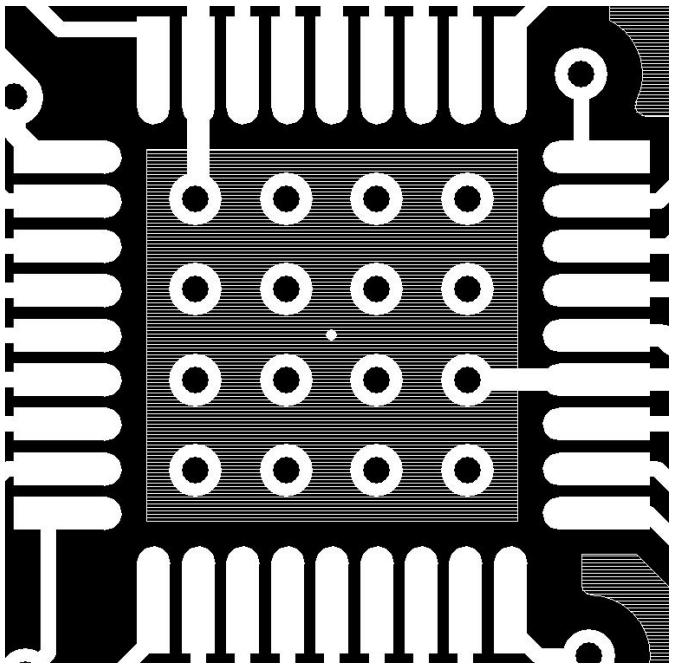


Figure 9. Ground Pad Recommended Layout

Table 14. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

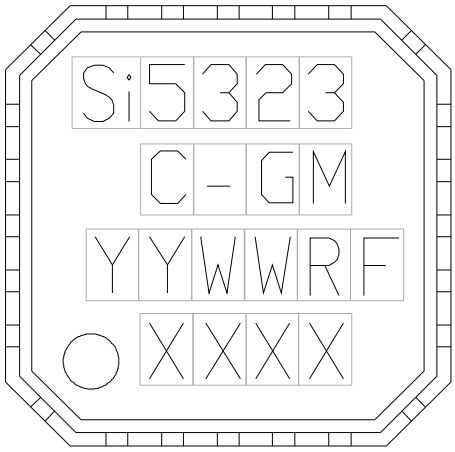
Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Si5323 Device Top Mark



Mark Method:	Laser	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Si5323	Customer Part Number See Ordering Guide for options
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

NOTES:

Document Change List

Revision 0.1 to Revision 0.2

- Changed LVTTL to LVCMOS in Table 7, “Absolute Maximum Ratings,” on page 12.
- Added Figure 5, “Typical Phase Noise Plot,” on page 13.
- Updated Figure 6, “Si5323 Typical Application Circuit,” on page 14 to show external reference interface.
- Added RATE0 and expanded the RATE[1:0] description in 4. "Pin Descriptions: Si5323”.
- Updated 5. "Ordering Guide" on page 33.
- Added 7. "Recommended PCB Layout”.

Revision 0.2 to Revision 0.3

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 4.
- Updated Table 7 on page 12.
- Added table under Figure 5 on page 13.
- Updated 3. "Functional Description" on page 15.
- Clarified 4. "Pin Descriptions: Si5323" on page 28 including pull-up/pull-down.
- Updated SFOUT values.

Revision 0.3 to Rev 1.0

- Updated feature list on page 1.
- Updated all Electrical Specification tables.
- Updated Typical phase noise performance plot and table values.
- Added Section 3.3. "Frequency Plan Tables" on page 16.
- Updated package outline drawing.
- Added ground pad layout drawing.
- Added Top Device Mark section.
- Updated Section 5. "Ordering Guide” table
- Added product selection guide

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