

IS31FL3731C

AUDIO MODULATED MATRIX LED DRIVER

April 2014

GENERAL DESCRIPTION

The IS31FL3731C is a compact LED driver for 144 single LEDs. The device can be programmed via an I2C compatible interface. The high logic ($0.77V_{CC}$) and low logic ($0.2V_{CC}$) control threshold are specially designed for white goods and industry application to minimize the impact by the EMC noise. The IS31FL3731C offers two blocks each driving 72 LEDs with 1/9 cycle rate. The required lines to drive all 144 LEDs are reduced to 18 by using the cross-plexing feature optimizing space on the PCB. Additionally each of the 144 LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming.

To reduce CPU usage up to 8 frames can be stored with individual time delays between frames to play small animations automatically. LED frames can be modulated with audio signal.

IS31FL3731C is available in QFN-28 (4mm × 4mm) and SSOP-28 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to $+85^{\circ}\text{C}$.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 400kHz I2C-compatible interface
- $0.77V_{CC}$ threshold logic high control
- 144 LEDs in dot matrix
- Individual blink control
- 8 frames memory for animations
- Picture mode and animation mode
- Auto intensity breathing during the switching of different frames
- LED frames displayed can be modulated with audio signal intensity
- LED light intensity can be modulated with audio signal intensity
- QFN-28 (4mm × 4mm) and SSOP-28 package

APPLICATIONS

- White goods LED application
- Home, medical, industrial LED appliances

TYPICAL APPLICATION CIRCUIT

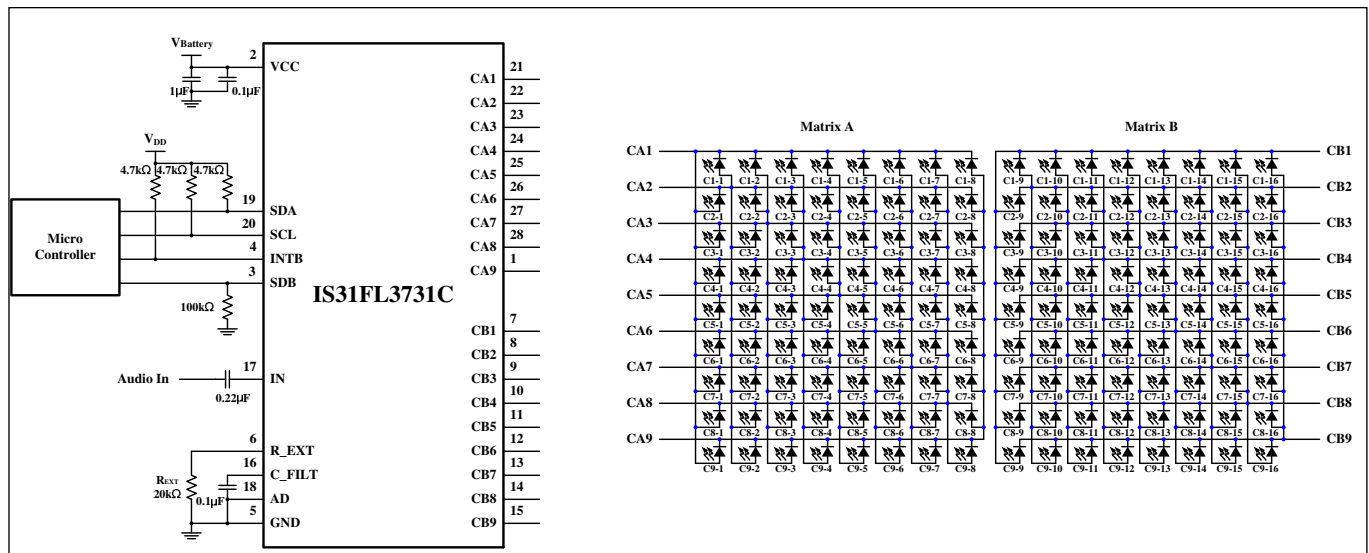


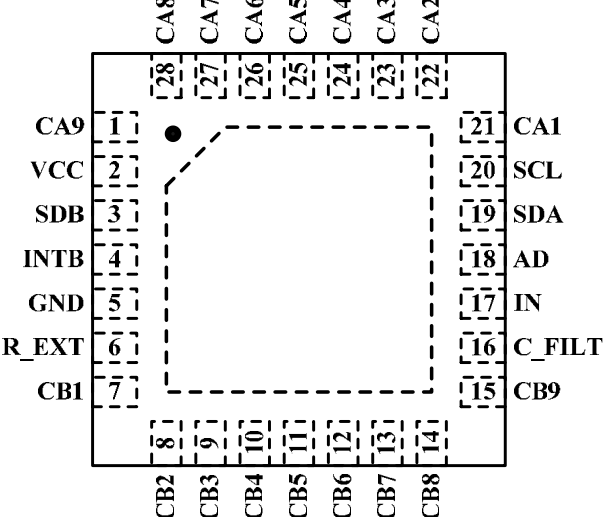
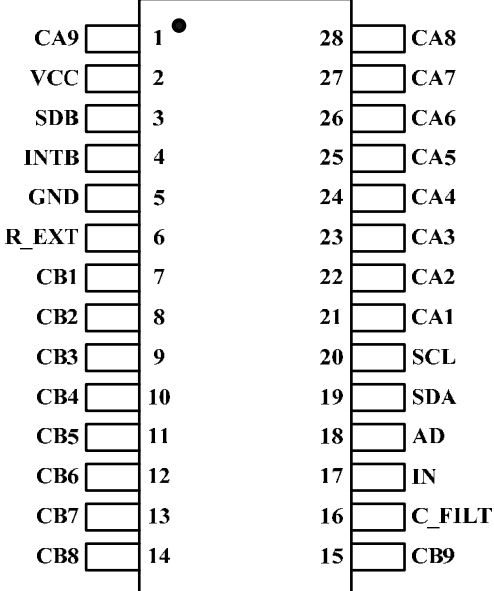
Figure 1 Typical Application Circuit

Note 1: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

Note 2: The average current of each LED is 3.2mA when $R_{EXT} = 20k\Omega$. The LED current can be modulated by the R_{EXT} . Please refer to the detail information in Page 18.

IS31FL3731C

PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFN-28 |  <p>Top view pin configuration for QFN-28 package. The chip is square with pins 1-14 on the left and 15-28 on the right. Pin 1 is the top-left corner. Pin 28 is the top-right corner. Pin 15 is the bottom-right corner. Pin 14 is the bottom-left corner. A dashed line indicates the chip's footprint. Pin 1 has a dot indicating the notch.</p> |
| SSOP-28 |  <p>Side view pin configuration for SSOP-28 package. The chip is rectangular with pins 1-14 on the left and 15-28 on the right. Pin 1 is the top-left corner. Pin 28 is the top-right corner. Pin 15 is the bottom-right corner. Pin 14 is the bottom-left corner. A dot indicates the notch on pin 1.</p> |

IS31FL3731C

PIN DESCRIPTION

| No. | Pin | Description |
|---------|-------------|---------------------------------------------|
| 1 | CA9 | LED matrix A current output/input port. |
| 2 | VCC | Power supply. |
| 3 | SDB | Shutdown the chip when pull to low. |
| 4 | INTB | Interrupt output. Active low. |
| 5 | GND | Ground. |
| 6 | R_EXT | 20kΩ resistance to confirm the LED current. |
| 7 ~ 15 | CB1 ~ CB9 | LED matrix B current output/input port. |
| 16 | C_FILT | Capacitor used for audio. |
| 17 | IN | Audio input. |
| 18 | AD | I2C address setting. |
| 19 | SDA | I2C compatible serial data. |
| 20 | SCL | I2C compatible serial clock. |
| 21 ~ 28 | CA1 ~ CA8 | LED matrix A current output/input port. |
| | Thermal Pad | Connect to GND. |



IS31FL3731C

ORDERING INFORMATION

INDUSTRIAL RANGE: -40°C TO +85°C

| Order Part No. | Package | QTY/Reel |
|----------------------|--------------------|-----------|
| IS31FL3731C-QFLS2-TR | QFN-28, Lead-free | 2500/Reel |
| IS31FL3731C-SALS2 | SSOP-28, Lead-free | 48/Tube |

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IS31FL3731C

ABSOLUTE MAXIMUM RATINGS

| | |
|------------------------------------------|-----------------------|
| Supply voltage, V_{CC} | -0.3V ~ +5.5V |
| Voltage at any input pin | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | 150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, T_A | -40°C ~ +85°C |
| ESD(HBM) | 8kV |
| ESD(CDM) | 1kV |

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$, $V_{CC} = 2.7V \sim 5.5V$, unless otherwise noted. Typical value is $T_A = 25^\circ\text{C}$, $V_{CC} = 3.6V$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------|--------------------------------------------------|---------------------------------------------------------|------|----------------|------|---------------|
| V_{CC} | Supply voltage | | 2.7 | | 5.5 | V |
| I_{CC} | Quiescent power supply current | $V_{IN} = 0V$, without audio input, all LEDs off | | 2.17 | | mA |
| I_{SD} | Shutdown current | $V_{SDB} = 0V$ | | 0.5 | 5 | μA |
| | | $V_{SDB} = V_{CC}$, software shutdown | | 230 | | |
| I_{OUT} | Output current of C1~C9 | Matrix display mode without audio modulation | | 34 (Note 1) | | mA |
| V_{HR} | Current sink headroom voltage C1~C9 | $I_{sink} = 270\text{mA}$ (Note 2) | | 400 | | mV |
| | Current source headroom voltage C1~C9 | $I_{source} = 34\text{mA}$ | | 400 | | |
| t_{SCAN} | Period of scanning (Figure 2) | | | 106 | | μs |
| t_{SCANOL} | Non-overlap blanking time during scan (Figure 2) | | | 15 | | μs |
| I_{LED} | Average current of each LED | $R_{EXT} = 20\text{k}\Omega$, PWM in 255 step (Note 3) | | 3.2 | | mA |

Logic Electrical Characteristics (SDA, SCL, AD, SDB)

| | | | | | | |
|----------|--------------------------------------|--------------------------------------------|--------------|---------------|--------------|----|
| V_{IL} | Logic "0" input voltage for SDB, AD | $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ | GND | | $0.2V_{CC}$ | V |
| | Logic "0" input voltage for SDA, SCL | | GND | | $0.16V_{CC}$ | |
| V_{IH} | Logic "1" input voltage for SDB, AD | $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ | $0.77V_{CC}$ | | V_{CC} | V |
| | Logic "1" input voltage for SDA, SCL | | $0.84V_{CC}$ | | V_{CC} | |
| I_{IL} | Logic "0" input current | $V_{INPUT} = 0V$ | | 5 (Note 4) | | nA |
| I_{IH} | Logic "1" input current | $V_{INPUT} = V_{CC}$ | | 5 (Note 4) | | nA |

IS31FL3731C

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---------------|----------------------------------------------------|-----------|------|----------|------|---------|
| f_{SCL} | Serial-Clock frequency | | | | 400 | kHz |
| t_{BUF} | Bus free time between a STOP and a START condition | | 1.3 | | | μs |
| $t_{HD, STA}$ | Hold time (repeated) START condition | | 0.6 | | | μs |
| $t_{SU, STA}$ | Repeated START condition setup time | | 0.6 | | | μs |
| $t_{SU, STO}$ | STOP condition setup time | | 0.6 | | | μs |
| $t_{HD, DAT}$ | Data hold time | | | | 0.9 | μs |
| $t_{SU, DAT}$ | Data setup time | | 100 | | | ns |
| t_{LOW} | SCL clock low period | | 1.3 | | | μs |
| t_{HIGH} | SCL clock high period | | 0.7 | | | μs |
| t_R | Rise time of both SDA and SCL signals, receiving | (Note 5) | | 20+0.1Cb | 300 | ns |
| t_F | Fall time of both SDA and SCL signals, receiving | (Note 5) | | 20+0.1Cb | 300 | ns |

Note 1: The average current of each LED is $I_{OUT}/10.5$.

Note 2: All LEDs are on.

Note 3: $I_{LED} = 64.7/R_{EXT}$, $R_{EXT} = 20k\Omega$ is recommended. The recommended minimum value of R_{EXT} is $18k\Omega$, or it may cause a large current.

Note 4: Guaranteed by design.

Note 5: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

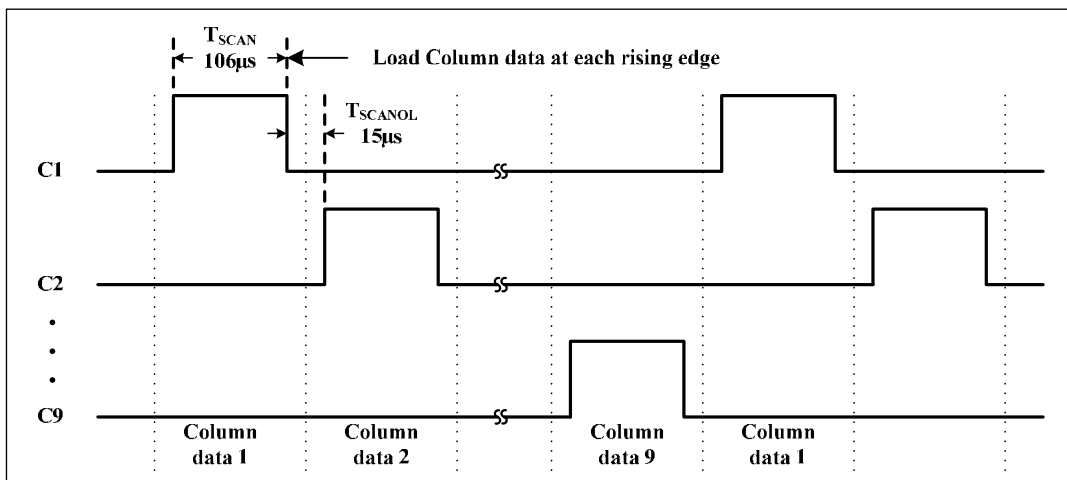


Figure 2 Scanning timing

IS31FL3731C

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3731C uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3731C has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write only):

| Bit | A7:A3 | A2:A1 | A0 |
|-------|-------|-------|-----|
| Value | 11101 | AD | 0/1 |

- AD connected to GND, AD=00;
- AD connected to VCC, AD=11;
- AD connected to SCL, AD=01;
- AD connected to SDA, AD=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3731C.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3731C's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3731C has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3731C, the register address byte is sent, most significant bit first. IS31FL3731C must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3731C must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3731C, load the address of the data register that the first data byte is intended for. During the IS31FL3731C acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3731C will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3731C (Figure 6).

READING PORT REGISTERS

All of registers in IS31FL3731C can be read. But Frame Registers can only be read in software shutdown mode as SDB pin is high. The Function Register can be read in software shutdown mode or operating mode.

To read the device data, the bus master must first send the IS31FL3731C address with the R/W bit set to "0", followed by the Command Register address, FDh, then send command data which determines which response register is accessed. After a restart, the bus master must send the IS31FL3731C address with the R/W bit set to "0" again, followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3731C address with the R/W bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3731C to the master (Figure 7).

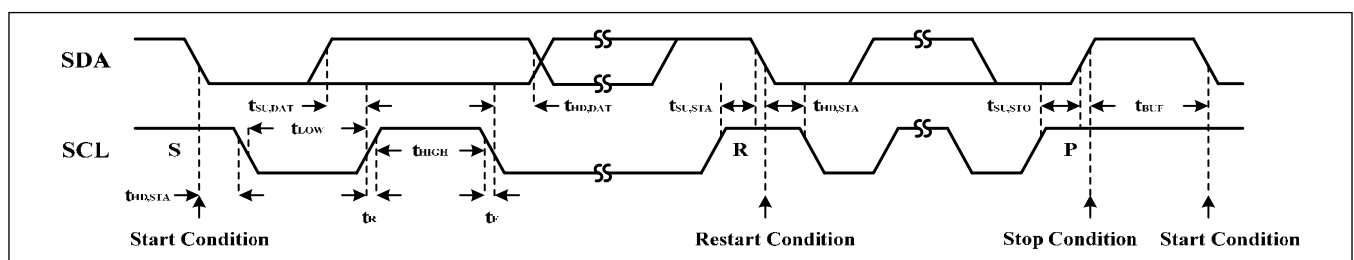


Figure 3 Interface timing

IS31FL3731C

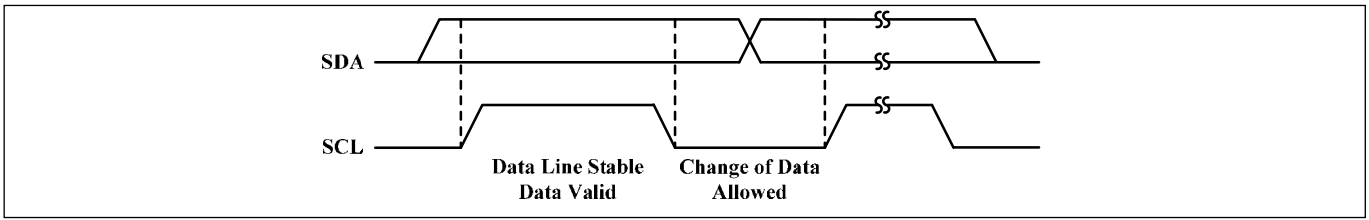


Figure 4 Bit transfer

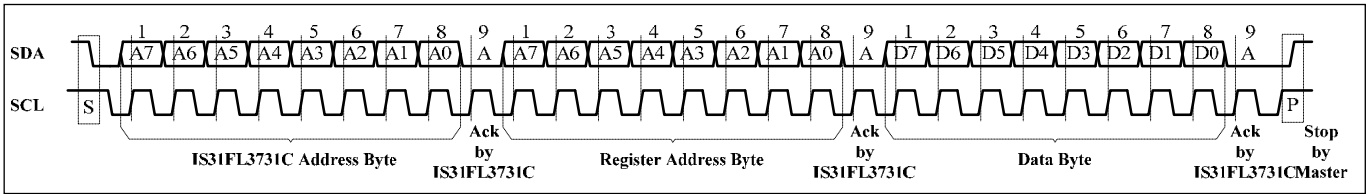


Figure 5 Writing to IS31FL3731C(Typical)

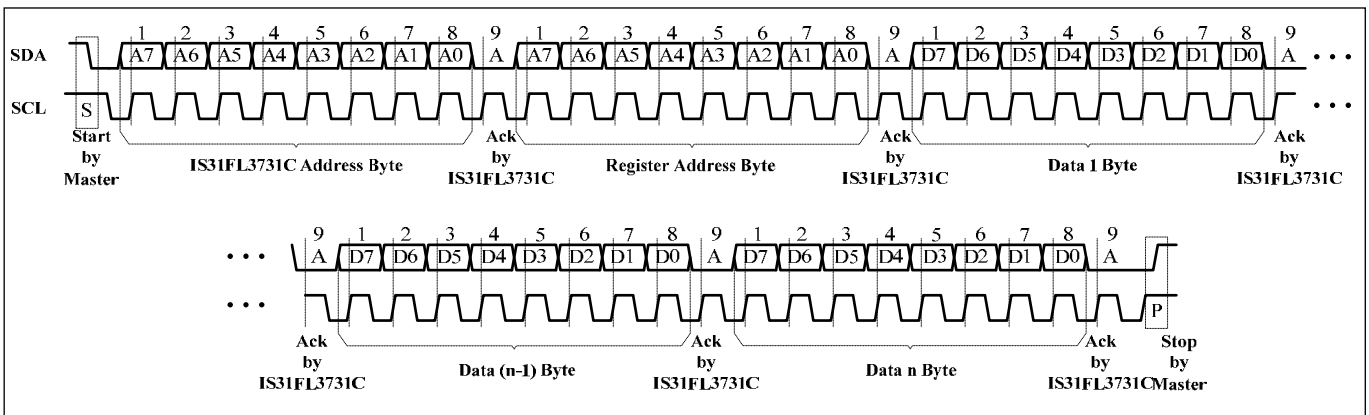


Figure 6 Writing to IS31FL3731C(Automatic address increment)

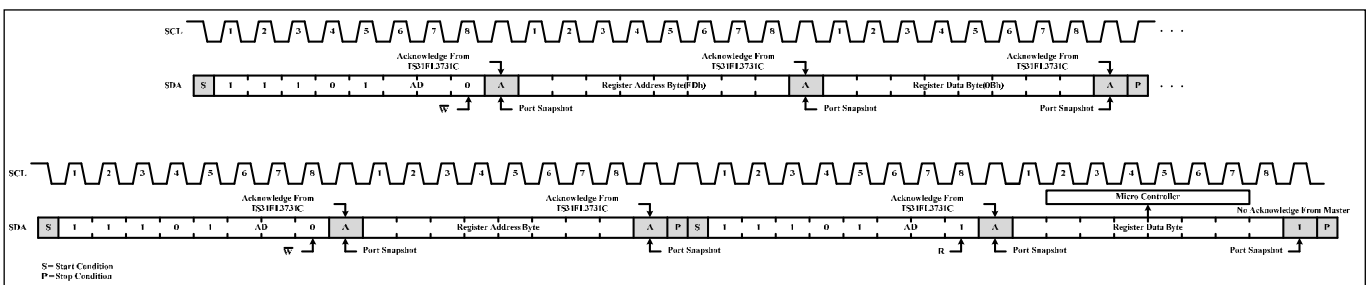


Figure 7 Reading from IS31FL3731C

IS31FL3731C

REGISTER DEFINITION

Table 2 FDh Command Register

| Data | Function | Data | Function |
|-----------|----------------------------------------------------|-----------|----------------------------------------------------|
| 0000 0000 | Point to Page One(Frame 1 Register is available) | 0000 0001 | Point to Page Two(Frame 2 Register is available) |
| 0000 0010 | Point to Page Three(Frame 3 Register is available) | 0000 0011 | Point to Page Four(Frame 4 Register is available) |
| 0000 0100 | Point to Page Five(Frame 5 Register is available) | 0000 0101 | Point to Page Six(Frame 6 Register is available) |
| 0000 0110 | Point to Page Seven(Frame 7 Register is available) | 0000 0111 | Point to Page Eight(Frame 8 Register is available) |
| 0000 1011 | Point to Page Nine(Function Register is available) | Others | Reserved |

Note: The Command Register should be configured first after writing in the slave address to choose the available register (Frame Registers and Function Registers). Then write data in the choosing register.

For example, when write "0000 0011" in the Command Register (FDh), the data which writing after will be stored in the Frame 4 Register. Write new data can configure other registers.

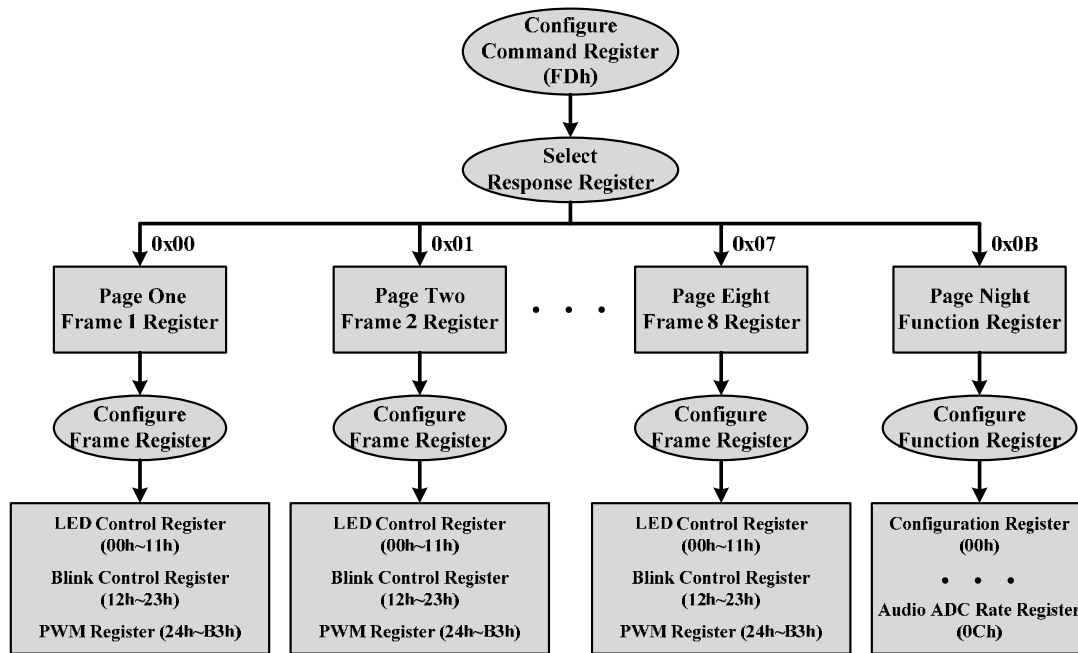
Table 3 Response Register Function

(The address of each Page is starting from 00h. Frame Registers have the same format.)

| Address | Name | Function | Table | R/W | Default |
|---------------------------------------------------------|--------------------------------|---------------------------------------------------|-------|-----|--------------|
| Frame Register (Page One to Page Eight) (Note 6) | | | | | |
| 00h ~ 11h | LED Control Register | Store on or off state for each LED | 4 | R/W | xxxx xxxx |
| 12h ~ 23h | Blink Control Register | Control the blink function for each LED | 5 | R/W | |
| 24h ~ B3h | PWM Register | 144 LEDs PWM duty cycle data register | 6 | R/W | |
| Function Register (Page Night) | | | | | |
| 00h | Configuration Register | Configure the operation mode | 8 | R/W | 0000 0000 |
| 01h | Picture Display Register | Set the display frame in Picture Mode | 9 | R/W | |
| 02h | Auto Play Control Register 1 | Set the way of display in Auto Frame Play Mode | 10 | R/W | |
| 03h | Auto Play Control Register 2 | Set the delay time in Auto Frame Play Mode | 11 | R/W | |
| 04h | Reserved (Note 7) | Reserved | - | R/W | |
| 05h | Display Option Register | Set the display option | 12 | R/W | |
| 06h | Audio Synchronization Register | Set audio synchronization function | 13 | R/W | |
| 07h | Frame State Register | Store the frame display information | 14 | R | |
| 08h | Breath Control Register 1 | Set fade in and fade out time for breath function | 15 | R/W | |
| 09h | Breath Control Register 2 | Set the breath function | 16 | R/W | |
| 0Ah | Shutdown Register | Set software shutdown mode | 17 | R/W | |
| 0Bh | AGC Control Register | Set the AGC function and the audio gain. | 18 | R/W | |
| 0Ch | Audio ADC Rate Register | Set the ADC sample rate of the input signal | 19 | R/W | |

Note 6: The data of Frame Registers is not assured when power on. Please initialize the Frame Registers first to ensure operate normally.

Note 7: The 04h register has no function although it can be written. It also can be read but the data is not assured.



FRAME REGISTER

Table 4 00h ~ 11h LED Control Register

| Bit | D7:D0 |
|---------|-----------------------------------------------------------------------------|
| Name | C _{X-8} : C _{X-1} or C _{X-16} : C _{X-9} |
| Default | xxxx xxxx |

The LED Control Registers store the on or off state of each LED in the Matrix A and B. Please refer to the detail information in Table 7.

| | |
|------------------------|---------------|
| C_{X-Y} | LED State Bit |
| 0 | LED off |
| 1 | LED on |

Figure 8 in Page 11 shows the ordering of C_{X-Y}.

Table 5 12h ~ 23h Blink Control Register

| Bit | D7:D0 |
|---------|-----------------------------------------------------------------------------|
| Name | C _{X-8} : C _{X-1} or C _{X-16} : C _{X-9} |
| Default | xxxx xxxx |

The Blink Control Registers configure the blink function of each LED in the Matrix A and B. Please refer to the detail information in Table 7.

| | |
|------------------------|-------------------|
| C_{X-Y} | Blink Control Bit |
| 0 | Disable |
| 1 | Enable |

Figure 8 in Page 11 shows the ordering of C_{X-Y}.

Table 6 24h ~ B3h PWM Register

| Bit | D7:D0 |
|---------|-----------|
| Name | PWM |
| Default | xxxx xxxx |

PWM Registers modulate the 144 LEDs in 256 steps. The value of the PWM Registers decides the output current of each LED. The output current may be computed using the Formula (1):

$$I_{PWM} = \frac{I_{LED}}{256} \cdot \sum_{n=0}^7 D[n] \cdot 2^n \quad (1)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$$I_{PWM} = I_{LED} (2^0 + 2^2 + 2^4 + 2^5 + 2^7) / 256$$

I_{LED} is set by the external resistor, R_{EXT}, I_{LED} = 64.7/R_{EXT}.

For example, when R_{EXT} = 20kΩ, I_{LED} = 64.7/20 = 3.2mA.

IS31FL3731C

Table 7 Address of Frame Register

| LED Location | | LED Control Register | | Blink Control Register | | PWM Register | |
|------------------------------------------|-------------------------------------------|----------------------|----------|------------------------|----------|--------------|-----------|
| Matrix A | Matrix B | Matrix A | Matrix B | Matrix A | Matrix B | Matrix A | Matrix B |
| CA1(C ₁₋₁ ~C ₁₋₈) | CB1(C ₁₋₉ ~C ₁₋₁₆) | 00h | 01h | 12h | 13h | 24h ~ 2Bh | 2Ch ~ 33h |
| CA2(C ₂₋₁ ~C ₂₋₈) | CB2(C ₂₋₉ ~C ₂₋₁₆) | 02h | 03h | 14h | 15h | 34h ~ 3Bh | 3Ch ~ 43h |
| CA3(C ₃₋₁ ~C ₃₋₈) | CB3(C ₃₋₉ ~C ₃₋₁₆) | 04h | 05h | 16h | 17h | 44h ~ 4Bh | 4Ch ~ 53h |
| CA4(C ₄₋₁ ~C ₄₋₈) | CB4(C ₄₋₉ ~C ₄₋₁₆) | 06h | 07h | 18h | 19h | 54h ~ 5Bh | 5Ch ~ 63h |
| CA5(C ₅₋₁ ~C ₅₋₈) | CB5(C ₅₋₉ ~C ₅₋₁₆) | 08h | 09h | 1Ah | 1Bh | 64h ~ 6Bh | 6Ch ~ 73h |
| CA6(C ₆₋₁ ~C ₆₋₈) | CB6(C ₆₋₉ ~C ₆₋₁₆) | 0Ah | 0Bh | 1Ch | 1Dh | 74h ~ 7Bh | 7Ch ~ 83h |
| CA7(C ₇₋₁ ~C ₇₋₈) | CB7(C ₇₋₉ ~C ₇₋₁₆) | 0Ch | 0Dh | 1Eh | 1Fh | 84h ~ 8Bh | 8Ch ~ 93h |
| CA8(C ₈₋₁ ~C ₈₋₈) | CB8(C ₈₋₉ ~C ₈₋₁₆) | 0Eh | 0Fh | 20h | 21h | 94h ~ 9Bh | 9Ch ~ A3h |
| CA9(C ₉₋₁ ~C ₉₋₈) | CB9(C ₉₋₉ ~C ₉₋₁₆) | 10h | 11h | 22h | 23h | A4h ~ ABh | ACh ~ B3h |

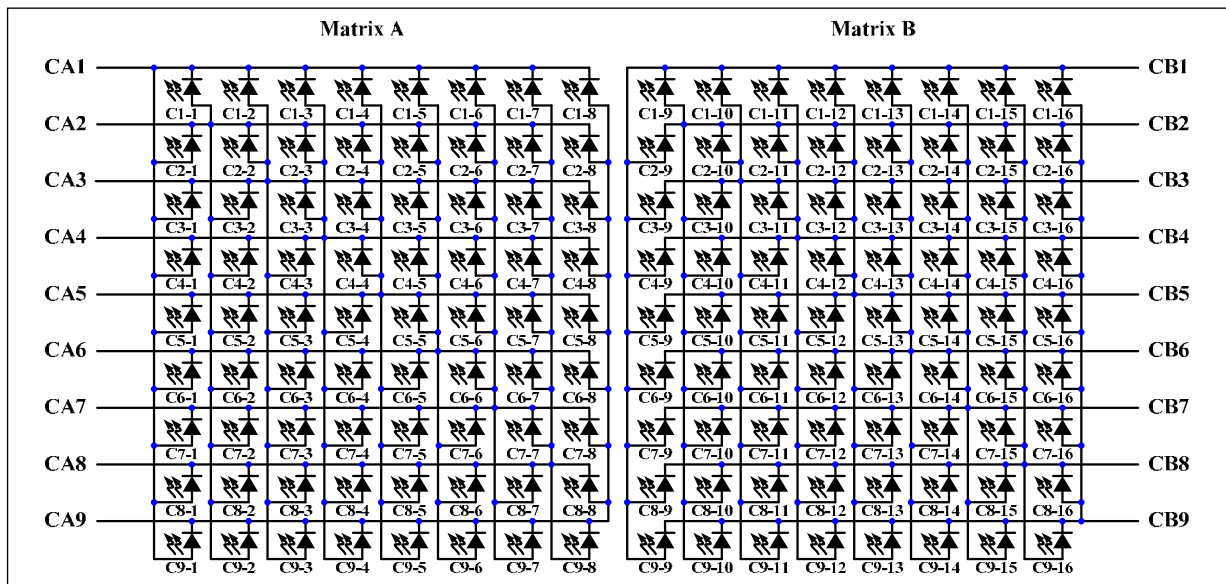


Figure 8 LED array

IS31FL3731C

FUNCTION REGISTER

Table 8 00h Configuration Register

| Bit | D7:D5 | D4:D3 | D2:D0 |
|---------|-------|-------|-------|
| Name | - | MODE | FS |
| Default | 000 | 00 | 000 |

The Configuration Register sets operating mode of IS31FL3731C.

MODE Display Mode
 00 Picture Mode
 01 Auto Frame Play Mode
 1x Audio Frame Play Mode

FS Frame Start
 (Available in Auto Frame Play Mode)
 000 Frame 1
 001 Frame 2
 010 Frame 3
 011 Frame 4
 100 Frame 5
 101 Frame 6
 110 Frame 7
 111 Frame 8

FS bit sets the start frame in Auto Frame Play Mode. Movie starts from Frame 4 when the FS bit is set to "011". The FS bit is only available in Auto Frame Play Mode.

Table 9 01h Picture Display Register

| Bit | D7:D3 | D2:D0 |
|---------|-------|-------|
| Name | - | PFS |
| Default | 00000 | 000 |

The Picture Display Register sets display frame in Picture Mode.

PFS Picture Frame Selection
 (Available in Picture Mode)
 000 Frame 1
 001 Frame 2
 010 Frame 3
 011 Frame 4
 100 Frame 5
 101 Frame 6
 110 Frame 7
 111 Frame 8

Table 10 02h Auto Play Control Register 1

| Bit | D7 | D6:D4 | D3 | D2:D0 |
|---------|----|-------|----|-------|
| Name | - | CNS | - | FNS |
| Default | 0 | 000 | 0 | 000 |

The Auto Play Control Register 1 sets the way of display in Auto Frame Play Mode.

CNS Number of Loops Playing Selection
 (Available in Auto Frame Play Mode)
 000 Play endless
 001 1 loop
 010 2 loops
 011 3 loops
 100 4 loops
 101 5 loops
 110 6 loops
 111 7 loops

FNS Number of Frames Playing Selection
 (Available in Auto Frame Play Mode)
 000 All Frame
 001 1 frame
 010 2 frames
 011 3 frames
 100 4 frames
 101 5 frames
 110 6 frames
 111 7 frames

Movie will be stop in the next frame of the cycle. For example, FS bit is set to "011", CNS bit is set to "011" and FNS bit is set to "011". Then the movie will play from frame 4 to frame 6 and play three times it stops in frame 7.

Table 11 03h Auto Play Control Register 2

| Bit | D7:D6 | D5:D0 |
|---------|-------|--------|
| Name | - | A |
| Default | 00 | 000000 |

The Auto Play Control Register 2 sets the delay time in Auto Frame Play Mode (Figure 12).

FDT Frame Delay Time
 (Available in Auto Frame Play Mode)
 If A = 0, FDT = $\tau \times 64$;
 If A = 1~63, FDT = $\tau \times A$;
 A = 0~63 and $\tau = 11\text{ms}$ (Typ.);
 For example, when A = 23, FDT is $11\text{ms} \times 23 = 253\text{ms}$

IS31FL3731C

Table 12 05h Display Option Register

| Bit | D7:D6 | D5 | D4 | D3 | D2:D0 |
|---------|-------|----|----|----|-------|
| Name | - | IC | - | BE | A |
| Default | 00 | 0 | 0 | 0 | 000 |

The Display Option Register sets display option of IS31FL3731C.

IC Intensity Control
 0 Set the intensity of each frame independently
 1 Use intensity setting of frame 1 for all other frames

BE Blink Enable
 0 Disable
 1 Enable

BPT Blink Period Time
 $BPT = \tau \times A$;
 $A = 0 \sim 7, \tau = 0.27s$ (Typ.);
 For example, when $A = 5$, BPT is $0.27s \times 5 = 1.35s$.

The duty cycle for blink function is 50%.

Table 13 06h Audio Synchronization Register

| Bit | D7:D1 | D0 |
|---------|---------|----|
| Name | - | AE |
| Default | 0000000 | 0 |

The Audio Synchronization Register sets audio synchronization function.

AE Audio Synchronization Enable
 0 Audio synchronization disable
 1 Enable audio signal to modulate the intensity of the matrix

The intensity of matrix can be modulated by the audio input signal basing on each LED's current is set by PWM when the AE bit is set to "1".

Table 14 07h Frame State Register (Read Only)

| Bit | D7:D5 | D4 | D3 | D2:D0 |
|---------|-------|-----|----|-------|
| Name | - | INT | - | CFD |
| Default | - | | | |

The Frame State Register stores the frame display information.

INT Interrupt Bit
 (Available in Auto Frame Play Mode)
 0 Movie does not finish
 1 Movie has finished

CFD Current Frame Display
 000 Frame 1
 001 Frame 2
 010 Frame 3
 011 Frame 4
 100 Frame 5
 101 Frame 6
 110 Frame 7
 111 Frame 8

The INT bit will be set to "1" automatically when movie is end in Auto Frame Play Mode. The INT bit can be cleared up by reading the Frame State Register.

Table 15 08h Breath Control Register 1

| Bit | D7 | D6:D4 | D3 | D2:D0 |
|---------|----|-------|----|-------|
| Name | - | A | - | B |
| Default | 0 | 000 | 0 | 000 |

The Breath Control Register 1 sets fade in and fade out time for breath function.

FOT Fade Out Time
 $FOT = \tau \times 2^A$
 $A = 0 \sim 7, \tau = 26ms$ (Typ.)
 For example, when $A = 4$, FOT is $26ms \times 2^4 = 416ms$

FIT Fade In Time
 $FIT = \tau \times 2^B$
 $B = 0 \sim 7, \tau = 26ms$ (Typ.)
 For example, when $A = 4$, FIT is $26ms \times 2^4 = 416ms$

IS31FL3731C

Table 16 09h Breath Control Register 2

| Bit | D7:D5 | D4 | D3 | D2:D0 |
|---------|-------|------|----|-------|
| Name | - | B_EN | - | A |
| Default | 000 | 0 | 0 | 000 |

The Breath Control Register 2 sets the breath function.

B_EN Breath Enable
(Available in Picture Mode and Auto Frame Play Mode)
0 Disable
1 Enable

ET Extinguish Time
 $ET = \tau \times 2^A$
A = 0~7, $\tau = 3.5\text{ms}$ (Typ.)
For example, when A = 4, ET is $3.5\text{ms} \times 2^4 = 56\text{ms}$

Table 17 0Ah Shutdown Register

| Bit | D7:D1 | D0 |
|---------|---------|-----|
| Name | - | SSD |
| Default | 0000000 | 0 |

The Shutdown Register sets software shutdown mode.

SSD Shutdown Control
0 Shutdown Mode
1 Normal Operation

Table 18 0Bh AGC Control Register

| Bit | D7:D5 | D4 | D3 | D2:D0 |
|---------|-------|------|-----|-------|
| Name | - | AGCM | AGC | AGS |
| Default | 000 | 0 | 0 | 000 |

The AGC Control Register sets the AGC function and the audio gain.

AGCM AGC Mode
0 Slow Mode
1 Fast Mode

AGC AGC Enable
0 Disable
1 Enable

AGS Audio Gain Selection
000 0dB
001 3dB
010 6dB
011 9dB
100 12dB
101 15dB
110 18dB
111 21dB

The AGS bit is available in Audio Frame Play Mode and audio synchronization mode.

Table 19 0Ch Audio ADC Rate Register

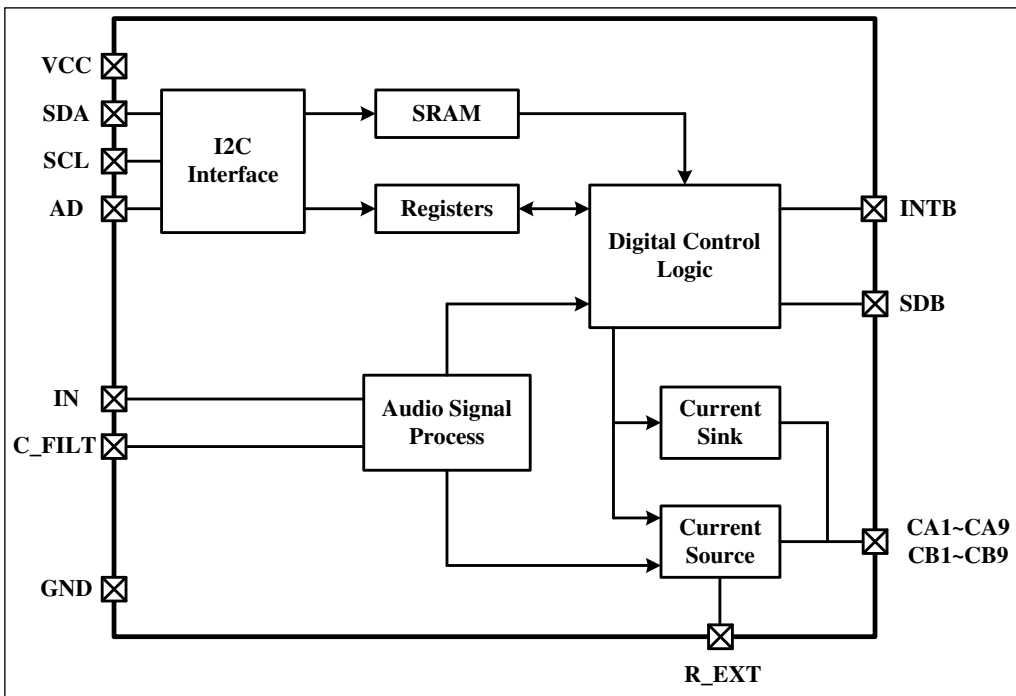
| Bit | D7:D0 |
|---------|-----------|
| Name | A |
| Default | 0000 0000 |

The Audio ADC Rate Register sets the ADC sample rate of the input signal in Audio Frame Play Mode.

AAR Audio ADC Rate
(Available in Audio Frame Play Mode)
If A = 0, $AAR = \tau \times 256$
If A = 1~255, $AAR = \tau \times A$
 $\tau = 46\mu\text{s}$ (Typ.)
For example, when A = 14, AAR is $46\mu\text{s} \times 14 = 644\mu\text{s}$

IS31FL3731C

FUNCTIONAL BLOCK DIAGRAM



IS31FL3731C

APPLICATION INFORMATION (The description below is for the Function Register unless otherwise noted.)

PWM CONTROL

The brightness of 144 LEDs can be modulated with 256 steps by PWM Register. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3731C can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 17 32 gamma steps with 256 PWM steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 4 | 6 | 10 | 13 | 18 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 22 | 28 | 33 | 39 | 46 | 53 | 61 | 69 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 78 | 86 | 96 | 106 | 116 | 126 | 138 | 149 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 161 | 173 | 186 | 199 | 212 | 226 | 240 | 255 |

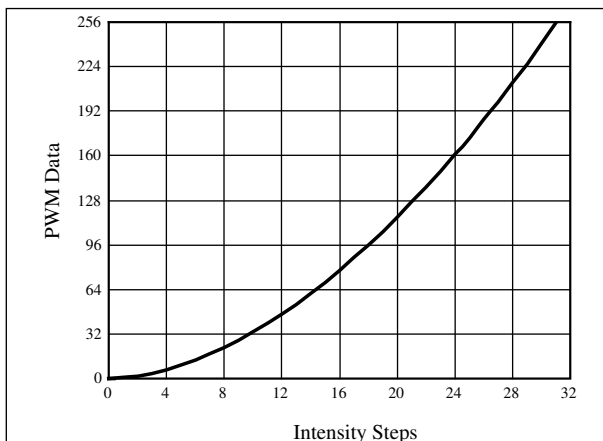


Figure 9 Gamma Correction(32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended

configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 18 64 gamma steps with 256 PWM steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 24 | 26 | 29 | 32 | 35 | 38 | 41 | 44 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 47 | 50 | 53 | 57 | 61 | 65 | 69 | 73 |
| C(32) | C(33) | C(34) | C(35) | C(36) | C(37) | C(38) | C(39) |
| 77 | 81 | 85 | 89 | 94 | 99 | 104 | 109 |
| C(40) | C(41) | C(42) | C(43) | C(44) | C(45) | C(46) | C(47) |
| 114 | 119 | 124 | 129 | 134 | 140 | 146 | 152 |
| C(48) | C(49) | C(50) | C(51) | C(52) | C(53) | C(54) | C(55) |
| 158 | 164 | 170 | 176 | 182 | 188 | 195 | 202 |
| C(56) | C(57) | C(58) | C(59) | C(60) | C(61) | C(62) | C(63) |
| 209 | 216 | 223 | 230 | 237 | 244 | 251 | 255 |

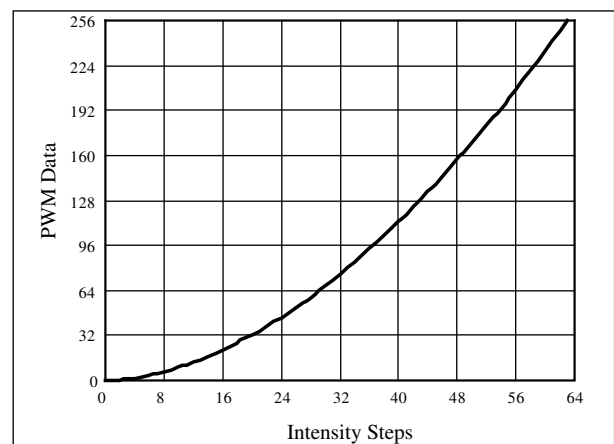


Figure 10 Gamma Correction(64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3731C has three operating modes, Picture Mode, Auto Frame Play Mode and Audio Frame Play Mode.

PICTURE MODE

By setting the MODE bit of the Configuration Register (00h) to "00", the IS31FL3731C operates in Picture Mode. Set the PFS bit of Picture Display Register (01h) to choose the display frame. The Picture Mode

IS31FL3731C

can be operating with breath function by configuring Breath Control Register 2 (09h).

AUTO FRAME PLAY MODE

By setting the MODE bit of the Configuration Register (00h) to "01", the IS31FL3731C operates in Auto Frame Play Mode. It stores data of 8 frames and automatically plays in order. Customers can configure the delay time between each two frames and the first playing frame by setting the FS bit of Configuration Register (00h). The Auto Play Control Register 1 (02h) can configure the display cycle and display frames.

Configure the Auto Play Control Register 2 (03h), Breath Control Register 1 (08h) and Breath Control Register 2 (09h) can set the breath time between two frames switching.

AUDIO FRAME PLAY MODE

By setting the MODE bit of the Configuration Register (00h) to "1x", the IS31FL3731C operates in Audio Frame Play Mode. It stores data of 8 frames and the 8 frames playing follow the input signal. 0Ch register is used to set the ADC sample rate for the input signal to control frames playing. It plays the first frame when the value is the smallest and plays the eighth frame when the value is the biggest.

AUDIO MODULATED AND GAIN SETTING

By setting the AE bit of the Audio Synchronization Register (06h) to "1", IS31FL3731C operates with audio synchronization. The intensity of LEDs is adjusted by the input signal. The audio input gain can be set by the AGC Control Register (0Bh).

BLINK FUNCTION SETTING

By setting the BE bit of the Display Option Register (05h) to "1", blink function enable. If the BE bit is set to "1", each LED can be controlled by the Blink Control Registers (12h~23h in Page One to Page Eight). The Display Option Register (05h) is used to set the blink period time, BPT, and the duty cycle is 50% (Figure 11).

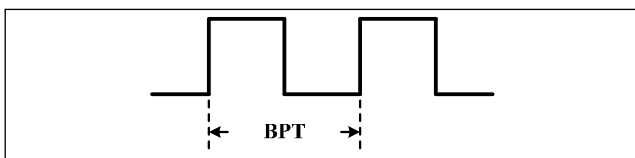


Figure 11 Blink function

BREATHING FUNCTION SETTING

When IS31FL3731C switches playing frame, breath function is available. By setting the B_EN bit of the Breath Control Register 2 (09h) to "1", breath function enable. When set the B_EN bit to "0", breath function disable.

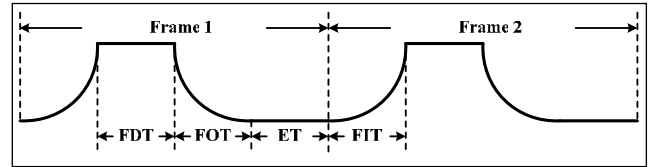


Figure 12 Breathing function

INTERRUPT CONTROL

When IS31FL3731C is playing frame in the Auto Frame Play Mode, the INTB pin is high and the INT bit of Frame State Register (07h) is "0". It will be pulled low as movie end and the INT bit will be set to "1" at the same time.

The INTB pin will come back to high level automatically if it stays low at least 7ms. The INT bit will reset to "0" only when reading the Frame State Register (07h).

LED MATRIX CIRCUIT

The IS31FL3731C can drive 144 LEDs totally. Part of LEDs can if there is no need to use all 144 LEDs (Figure 13). But the LEDs which are no connected must be off by LED Control Register (Frame Registers) or it will affect other LEDs.

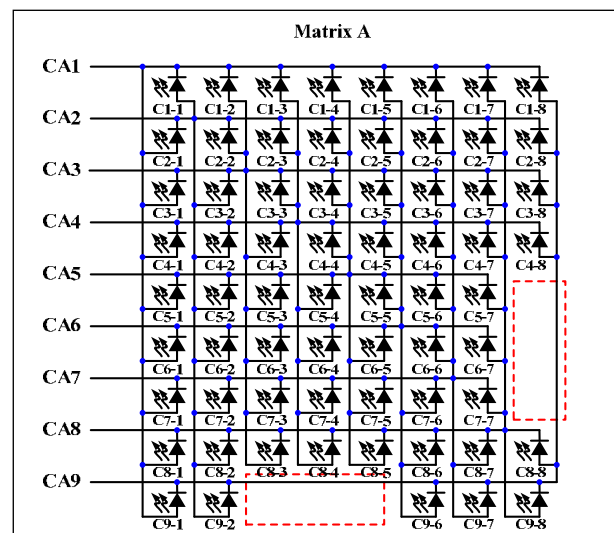


Figure 13 No C9-3~C9-5, C5-8~C9-8

IS31FL3731C

MORE FRAMES DISPLAY

The IS31FL3731C can store 8 frames data at best. Each 4 frames writing in Frame Registers is recommended if there are more frames to play (Figure 14). First, store 8 frames data and play 4 frames in front. Then play last 4 frames and writing new data in the Frame Registers (1~4) at the same time. Play the new 4 frames (1~4) and write new data in the Frame Registers (5~8).

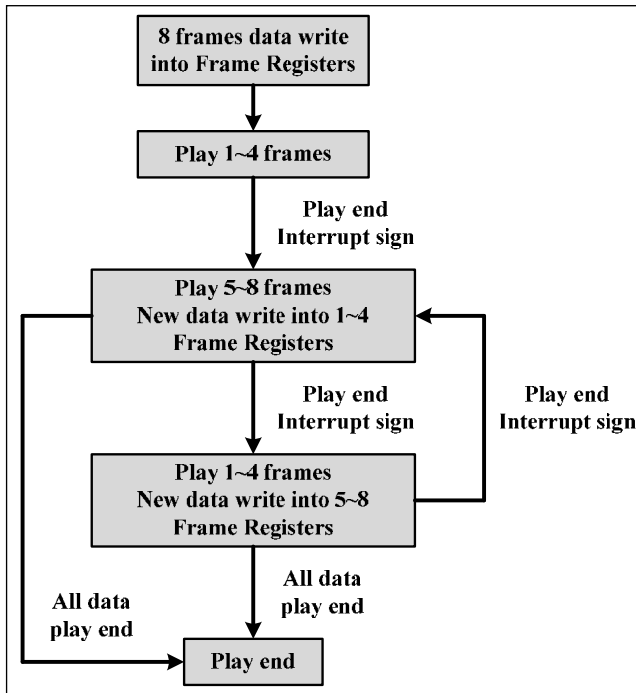


Figure 14 More frame data writing in

R_{EXT}

The average output current of each LED can be adjusted by the external resistor, R_{EXT}, as described in Formula (2).

$$I_{LED} = 64.7 / R_{EXT} \quad (2)$$

For example, in Figure 1, R_{EXT} = 20kΩ,

$$\text{So } I_{LED} = 64.7 / 20 = 3.2mA$$

The recommended minimum value of R_{EXT} is 18kΩ, or it may cause a large current.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

SOFTWARE SHUTDOWN

By setting SSD bit of the Shutdown Register (0Ah) to "0", the IS31FL3731C will operate in software shutdown mode. When the IS31FL3731C is in software shutdown mode, all current sources and digital drivers are switched off, so that the matrix is blanked. All registers can be writing or read when the SDB pin is pulled high in software shutdown mode.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low. All registers are forbidden writing and reading.

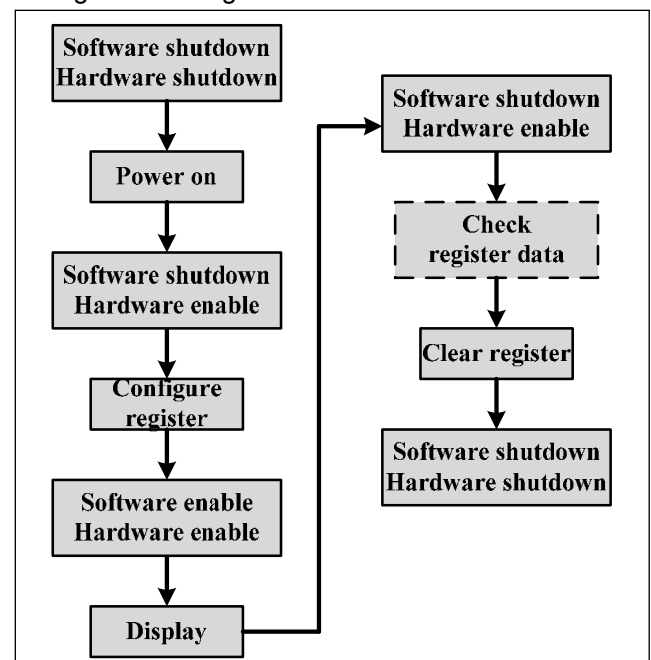
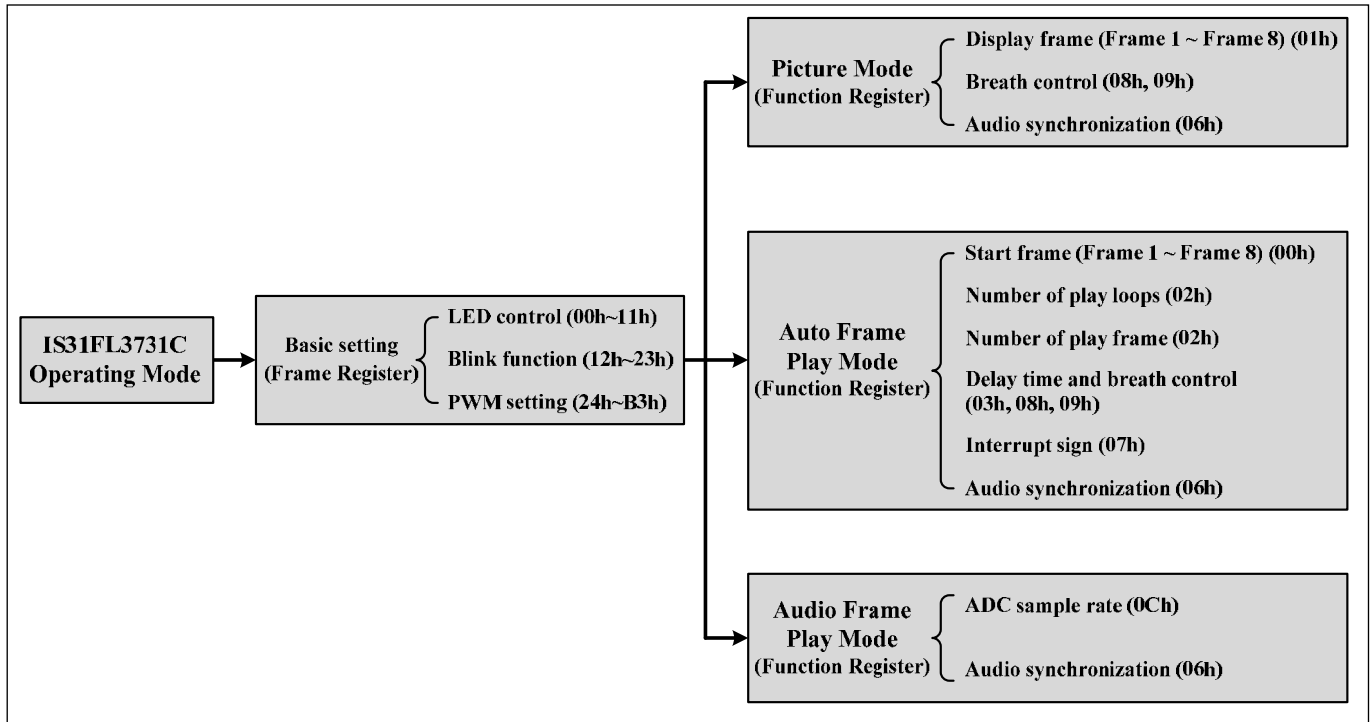


Figure 15 Shutdown Control

IS31FL3731C

APPLICATION DESIGN



IS31FL3731C

CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---------------------------------------------------------------------------------------------------|------------------|
| Preheat & Soak | |
| Temperature min (T _{smin}) | 150°C |
| Temperature max (T _{smax}) | 200°C |
| Time (T _{smin} to T _{smax}) (t _s) | 60-120 seconds |
| Average ramp-up rate (T _{smax} to T _p) | 3°C/second max. |
| Liquidous temperature (T _L) | 217°C |
| Time at liquidous (t _L) | 60-150 seconds |
| Peak package body temperature (T _p)* | Max 260°C |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | Max 30 seconds |
| Average ramp-down rate (T _p to T _{smax}) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

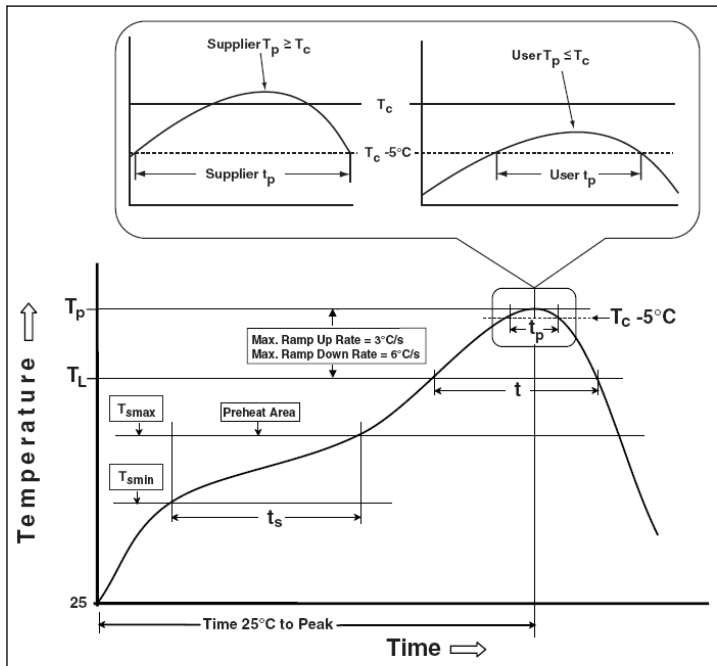
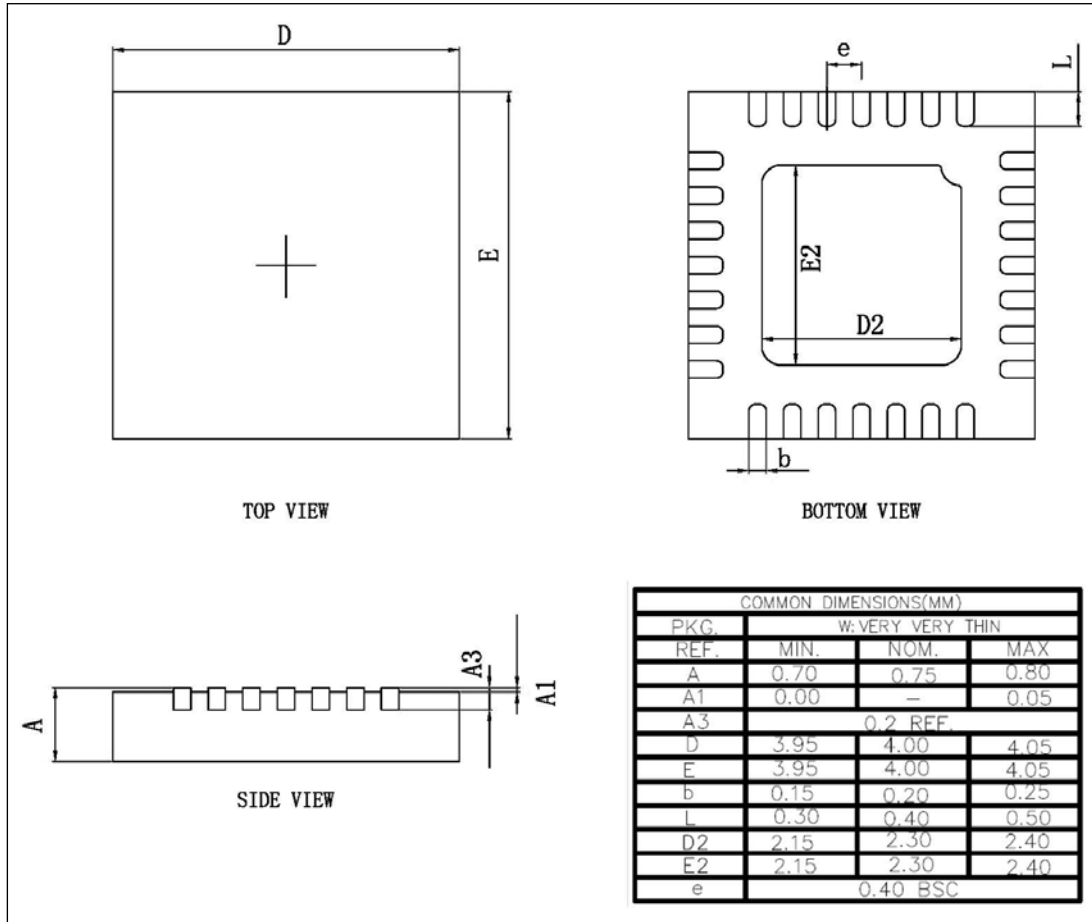


Figure 16 Classification Profile

IS31FL3731C

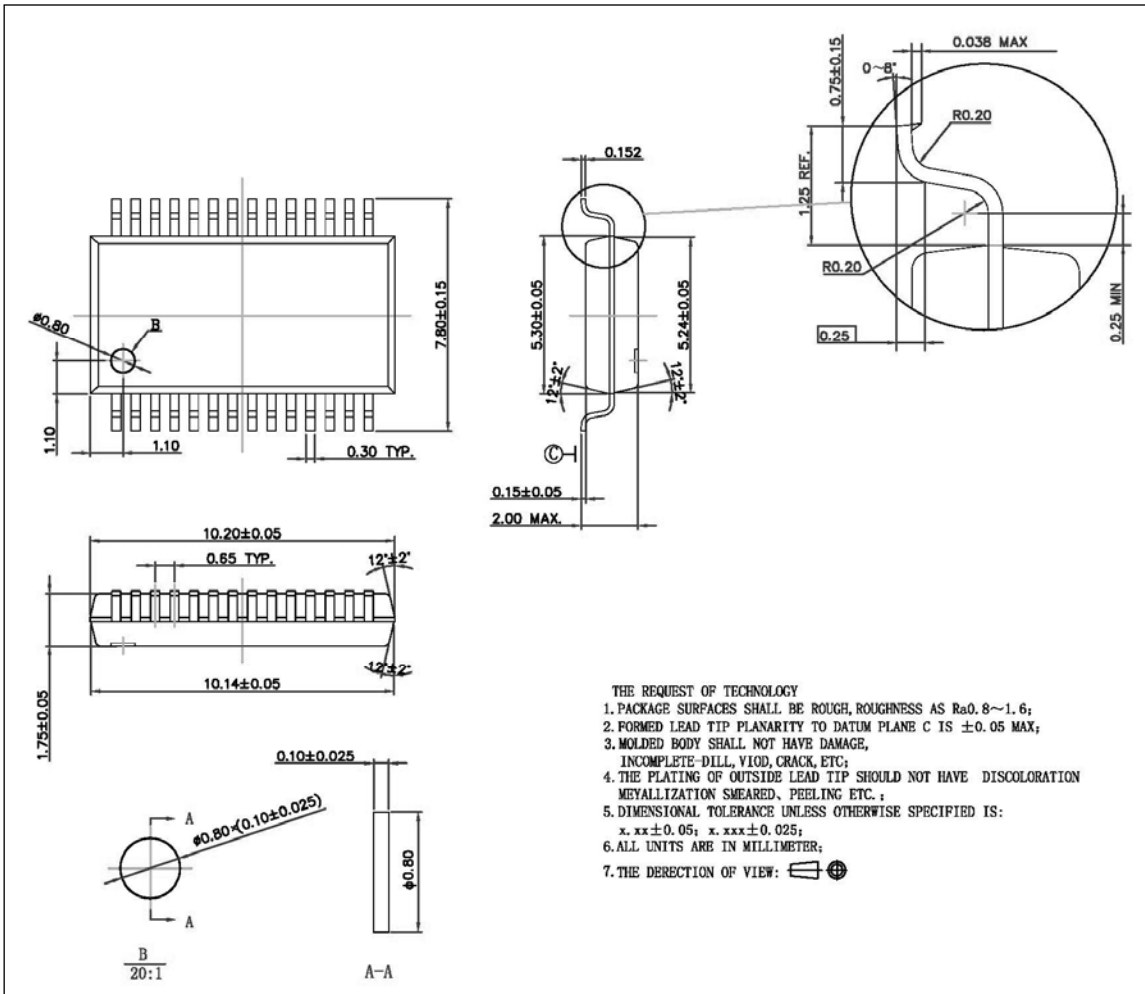
PACKAGE INFORMATION

QFN-28



IS31FL3731C

SSOP-28



Note: All dimensions in millimeters unless otherwise stated.