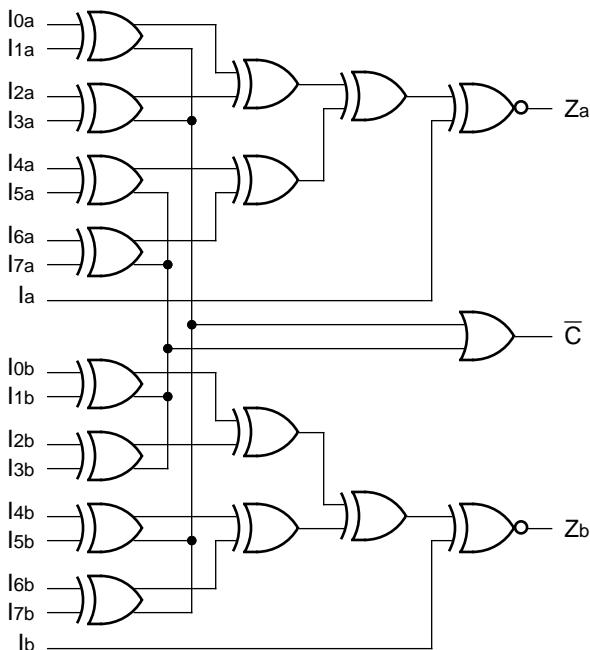
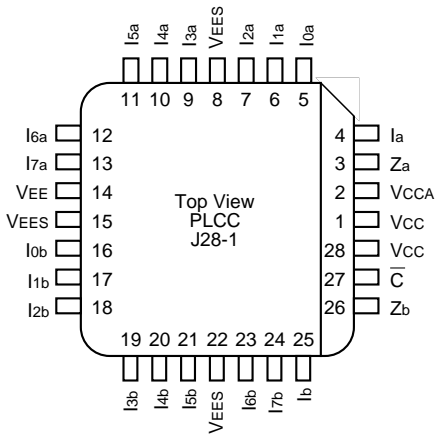


- Max. propagation delay of 2200ps
- IEE min. of -70mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 15% faster than Fairchild 300K
- Approximately 30% lower power than Fairchild 300K
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

The SY100S360 is a dual parity checker/generator and is designed for use in high-performance ECL systems. The inputs are segmented into two groups of nine inputs each and the parity output is at a logic LOW when an even number of inputs are at a logic HIGH. In each group, one of the nine inputs (Ia, Ib) has a shorter propagation delay and, therefore, is ideal as the expansion input for parity generation of wider data.

A Compare output (\bar{C}) is also provided which allows comparison of two 8-bit words. A logic LOW on the C output indicates a match. The inputs on this device have 75kΩ pull-down resistors.





28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S360JC	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JCTR ⁽¹⁾	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JZ ⁽²⁾	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S360JZTR ^(1, 2)	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

Pin	Function
Ia, Ib, I _{na} , I _{nb}	Data Inputs (n = 1...7)
Z _a – Z _b	Parity Odd Outputs
C̄	Compare Output
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

Sum of High Inputs	Output Z
Even	HIGH
Odd	LOW

Note:

1. Comparator Function:

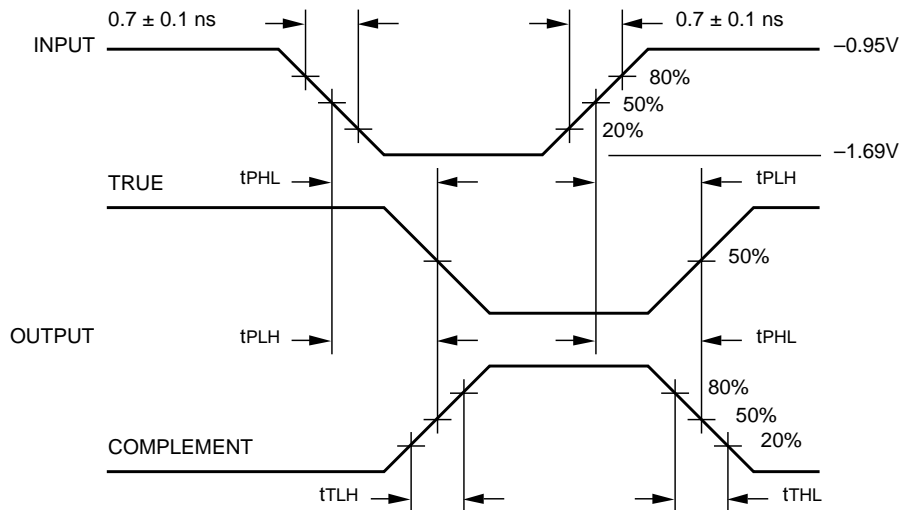
$$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current	—	—	300	μA	V _{IN} = V _{IH} (Max.)
	I _a , I _b I _{na} , I _{nb}	—	—	200		
I _{EE}	Power Supply Current	-70	-45	-30	mA	Inputs Open

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

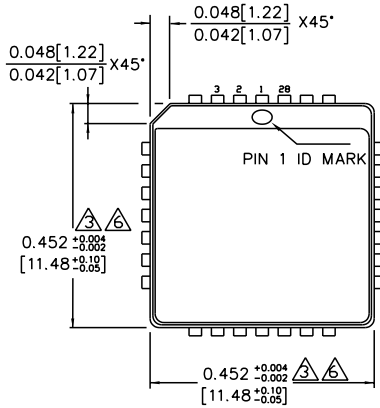
Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay I _{na} , I _{nb} to Z _a , Z _b	500	2200	500	2200	500	2200	ps	
t _{PLH} t _{PHL}	Propagation Delay I _{na} , I _{nb} to C	500	1700	500	1700	500	1700	ps	
t _{PLH} t _{PHL}	Propagation Delay I _a , I _b to Z _a , Z _b	300	900	300	900	300	900	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	



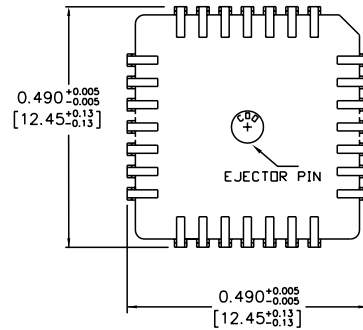
Propagation Delay and Transition Times

NOTE:

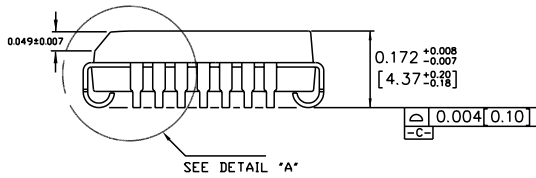
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$



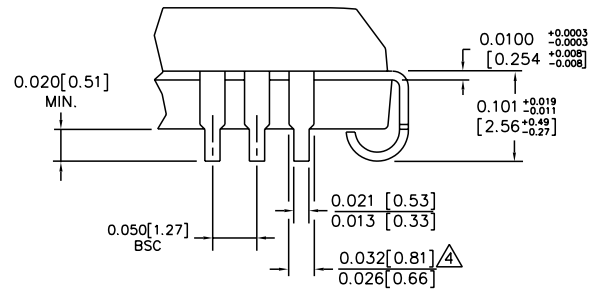
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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