

# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCAS280I – JANUARY 1993 – REVISED OCTOBER 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W), Chip Carriers (FK), and DIPs (J)**

## description

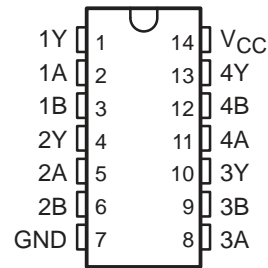
The SN54LVC02A quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation and the SN74LVC02A quadruple 2-input positive-NOR gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The 'LVC02A devices perform the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

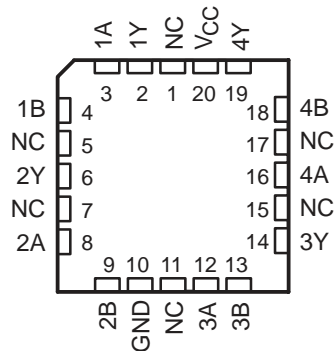
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC02A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVC02A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LVC02A . . . J OR W PACKAGE  
SN74LVC02A . . . D, DB, OR PW PACKAGE  
(TOP VIEW)



SN54LVC02A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H



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 **TEXAS  
INSTRUMENTS**

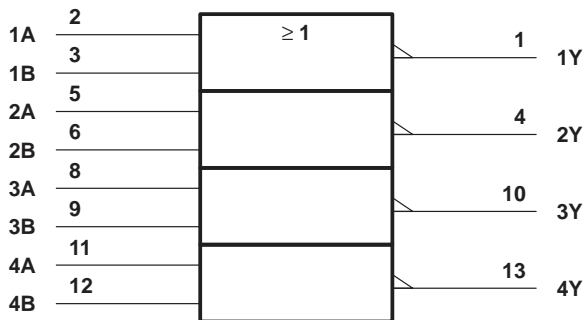
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# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, PW, and W packages.

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply-voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input-voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Output-voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package .....	127°C/W
DB package .....	158°C/W
PW package .....	170°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51.

# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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## recommended operating conditions (see Note 4)

		SN54LVC02A		SN74LVC02A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5	1.5	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V			1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V		2	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V			-4	mA
		V <sub>CC</sub> = 2.3 V			-8	
		V <sub>CC</sub> = 2.7 V		-12	-12	
		V <sub>CC</sub> = 3 V		-24	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V			4	mA
		V <sub>CC</sub> = 2.3 V			8	
		V <sub>CC</sub> = 2.7 V		12	12	
		V <sub>CC</sub> = 3 V		24	24	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC02A			SN74LVC02A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V			V <sub>CC</sub> -0.2			V	
		2.7 V to 3.6 V	V <sub>CC</sub> -0.2						
	I <sub>OH</sub> = -4 mA	1.65 V			1.2				
	I <sub>OH</sub> = -8 mA	2.3 V			1.7				
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		2.2				
		3 V	2.4		2.4				
I <sub>OH</sub> = -24 mA	3 V	2.2		2.2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2			V	
		2.7 V to 3.6 V	0.2						
	I <sub>OL</sub> = 4 mA	1.65 V			0.45				
	I <sub>OL</sub> = 8 mA	2.3 V			0.7				
	I <sub>OL</sub> = 12 mA	2.7 V		0.4	0.4				
3 V			0.55	0.55					
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V		±5		±5	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		10		10	μA		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500		500	μA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5		5	pF		

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC02A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	5.4		1	4.4	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC02A						UNIT	
			V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			TYP	MIN	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	13.4	1	7.4	5.4	1	4.4	ns	
t <sub>sk(o)†</sub>							1		ns	

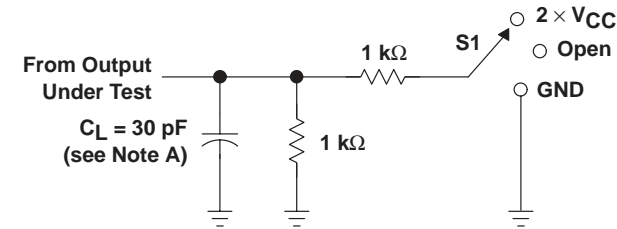
† Skew between any two outputs of the same package switching in the same direction

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
		TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	7.5	8.5	9.5	pF

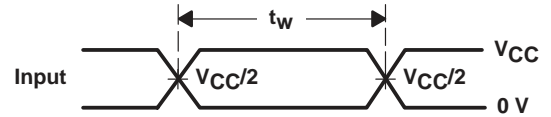


PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

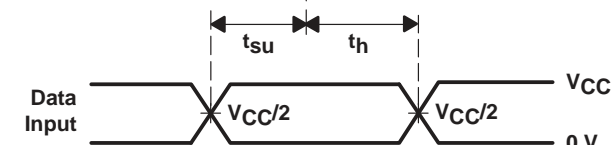


LOAD CIRCUIT

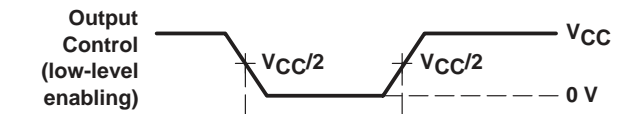
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



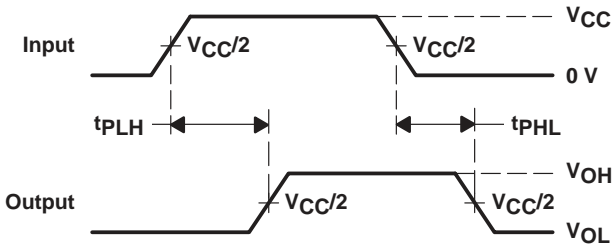
VOLTAGE WAVEFORMS  
 PULSE DURATION



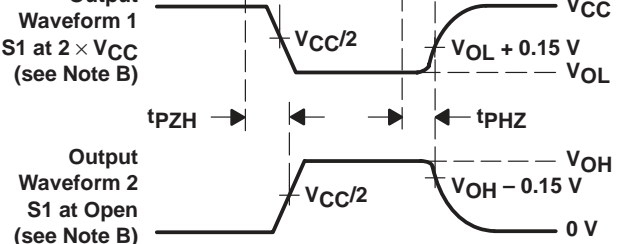
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

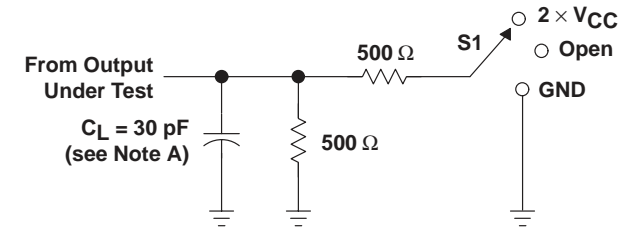
Figure 1. Load Circuit and Voltage Waveforms

# SN54LVC02A, SN74LVC02A QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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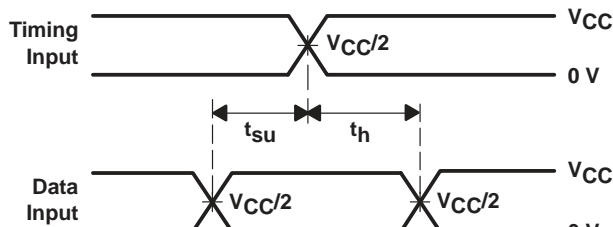
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

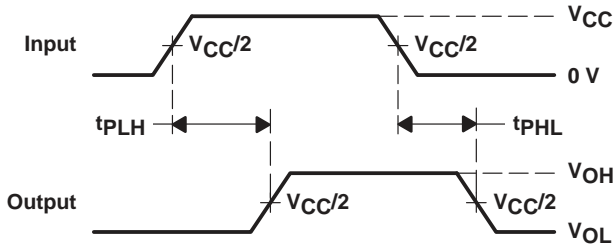


LOAD CIRCUIT

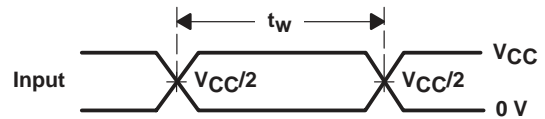
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



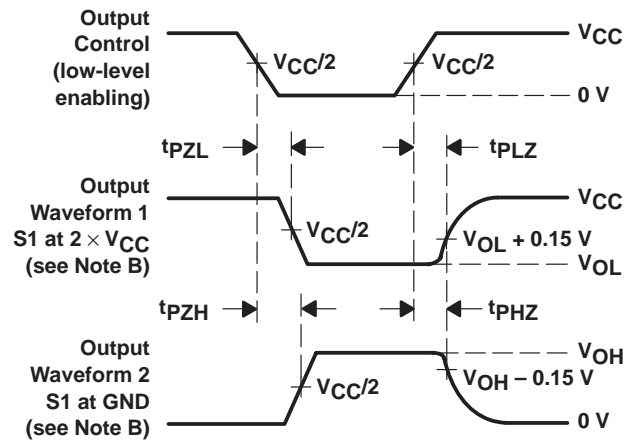
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION

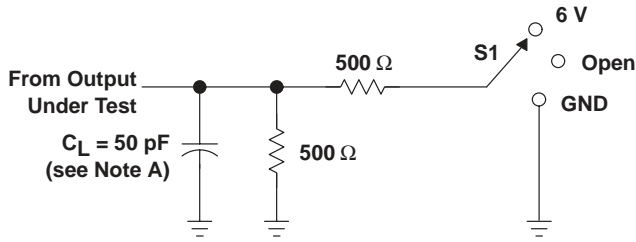


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

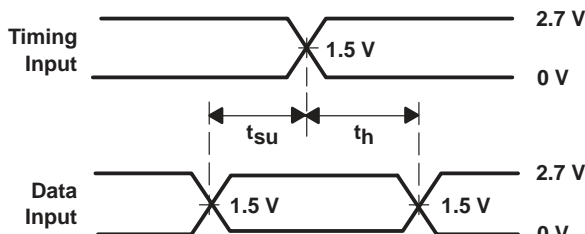
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

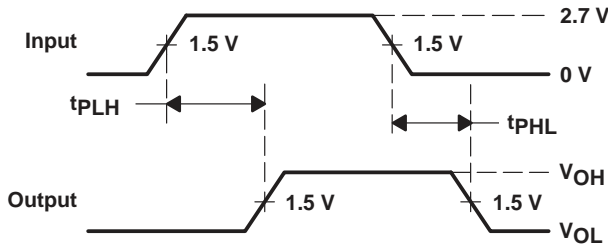


TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

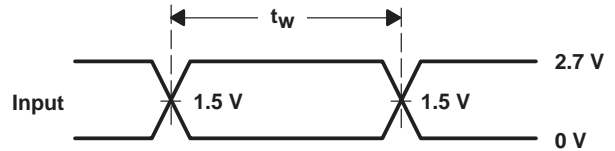
LOAD CIRCUIT



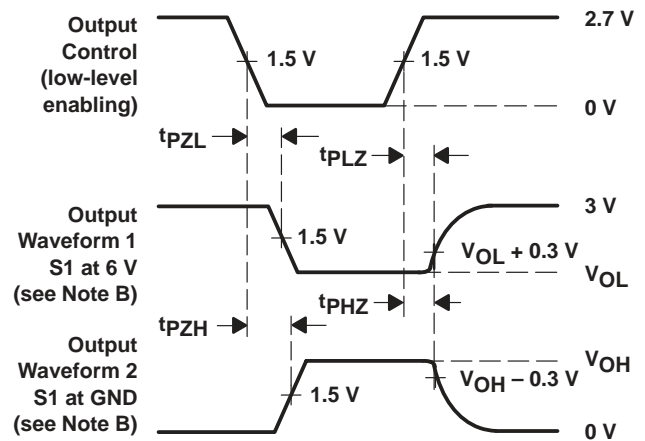
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

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