

PI2127-EVAL1 60V/12A Full-Function High Side Active ORing Evaluation Board User Guide

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Cool-ORing® Series



*PI2127-EVAL1 Evaluation Board
featuring the Cool-ORing PI2127
Full-Function Active ORing Solution.*

The PI2127-EVAL1 Evaluation Board is intended to acquaint the user with the benefits and features of the *Cool-ORing®* PI2127 full-function Active ORing solution. It is not designed to be installed in end-use equipment.

Please read this document before setting up the PI2127-EVAL1 Evaluation Board and refer to the PI2127 product datasheet for device specifications, functional description and characteristics. During operation, the

power devices and surrounding structures can be operated safely at high temperatures.

Remove power and use caution when connecting and disconnecting test probes and interface lines to avoid inadvertent short circuits and contact with hot surfaces.

When testing electronic products always use approved safety glasses. Follow good laboratory practice and procedures.

Introduction

The PI2127-EVAL1 allows the user to test the basic principles and operational characteristics of an Active ORing function in a redundant power architecture, while also experiencing the benefits and value of the PI2127 solution versus conventional Active ORing solutions. The PI2127-EVAL1 evaluation board is configured to receive two independent power source inputs, per a typical redundant power architecture, through two Active ORing channels that are combined to form a redundant power output. Each channel is capable of up to 12A, and is suitable redundant bus voltages up to 48V.

The PI2127-EVAL1 evaluation board is designed with optimized PCB layout and component placement to represent a realistic high density final design for an embedded Active ORing solution for 48V BUS applications

requiring up to 12A. This evaluation board is intended as an easy and simple way to test the electrical and thermal performance of the PI2127 Full-Function Active ORing solution.

Both dynamic and steady state testing of the PI2127 can be completed on the PI2127-EVAL1 evaluation board, in addition to using the key features of the product. Dynamic testing can be completed under a variety of system level fault conditions to check for response time to faults.

This document provides basic instructions for initial start-up and configuration of the evaluation board. Further information on the functionality of the PI2127 can be found in the PI2127 product datasheet.

Cool-ORing® PI2127 Product Description

The PI2127 *Cool-ORing*® is a complete full-function Active ORing solution with a high-speed ORing MOSFET controller and a very low on-state resistance MOSFET designed for use in redundant power system architectures. The PI2127 *Cool-ORing*® solution is offered in an extremely small, thermally enhanced 7mm x 8mm LGA package and can be used in high side, medium voltage Active ORing applications. The PI2127 enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems.

The PI2127, with its 60V/8.5mΩ internal MOSFET provides very high efficiency and low power loss during steady state operation, while achieving high-speed turn-off of the internal MOSFET during input power source fault conditions that cause reverse current flow. The PI2127 provides an active low fault flag output to the system during reverse current, excessive forward over-current and UVLO fault conditions.

Figure 1 shows a photo of the PI2127-EVAL1 evaluation board, with two PI2127 SiPs used to form the two Active ORing channels. The board is built with two identical Active ORing circuits with options and features that enable the user to fully explore the capabilities of the PI2127 *Cool-ORing*® solution.



Figure 1: PI2127-EVAL1 Evaluation Board (1.8" x 1.8")

Terminals Maximum Rating.

Vin1+, Vin2+,	60V/12A
Vout+	60V/24A
$\overline{FT1}$, $\overline{FT2}$	20V / 10mA
VL1, VL2 (R5=R6=1.5kΩ)*	5.5V
* VL1, VL2 voltage can be raised , but R5 and R6 values have to be increased to accommodate the LEDs	

Terminal	Description
Vin1+	Power source Input #1: or bus input designed to accommodate up to 60V and 12A continuous current.
Vin1-	Vin1+ return connection
Vin2+	Power source Input #2: or bus input designed to accommodate up to 60V and 12A continuous current.
Vin2-	Vin2+ return connection
$\overline{FT1}$	PI2127 (U1) Fault pin: referenced to the Gnd terminal (Vin1-)
$\overline{FT2}$	PI2127 (U2) Fault pin: referenced to the Gnd terminal (Vin2-)
EN1	PI2127 (U1) Enable: leave open to enable the U1 and connect to return (Vin1-) to disable U1
EN2	PI2127 (U2) Enable: leave open to enable the U2 and connect to return (Vin2-) to disable U2
Vout+	Output: U1 and U2 D pins connection, connect to the load high side.
Vout-	Vout+ return connection
Note: Vin1-, Vin2- and Vout- are connected to the same point at the PCB bottom layer	

Table 1: PI2127-EVAL1 Evaluation Board Terminals Description

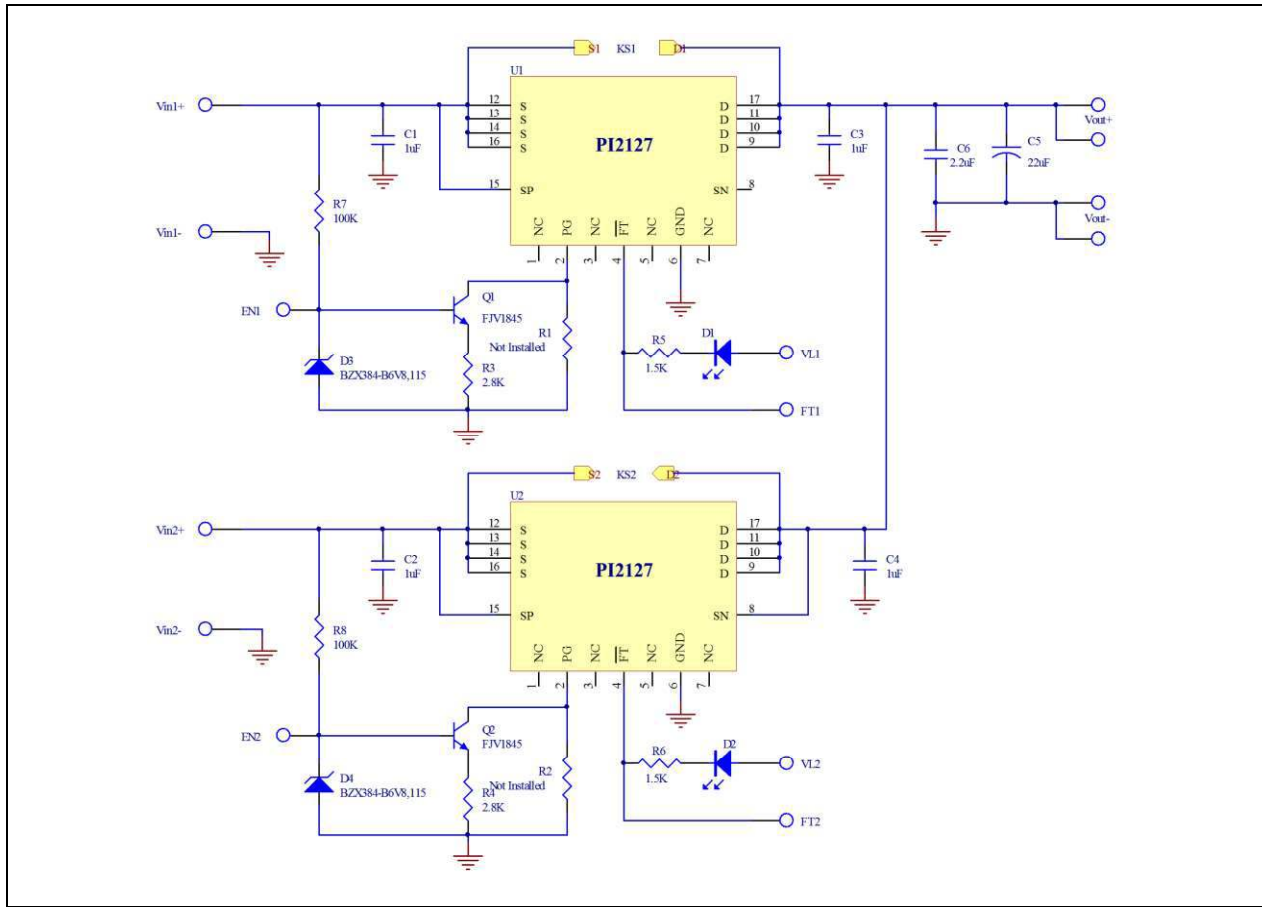


Figure 2: PI2127-EVAL1 Evaluation Board schematic.

Item	Reference Designator	Value	Description	Footprint	Manufacturer
1	C1, C2, C3, C4	Not Installed	MLCC, X7R,1uF,50V	1206	
2	C5	22uF	Electrolytic 22uF,100V	Panasonic_E/F	Panasonic
3	C6	2.2uF	MLCC 2.2uF,100V	1812	
4	D1, D2	LTST-C191CKT	LED, Red	0603 LED	Lite-On
5	D3, D4	BZX384-B6V8	Zener, 6.8V,300mW	SOD-323	NXP
6	EN1, EN2, FT1, FT2, VL1, VL2	1528	Turret Test point	TURRET - 1528	Keystone Electronics
7	Vin1+, Vin1-, Vin2+, Vin2-, Vout+, Vout-	1502	Turret Test point	TURRET - 1502	Keystone Electronics
8	Q1, Q2	FJV1845	NPN,120V,50mA	SOT-23	Fairchild
9	R1, R2	Not Installed		1206	
10	R3, R4	2.8K	Resistor,2.8K,1%	0603	
11	R5, R6	1.5K	Resistor,1.5K,1%	0603	
12	R7, R8	100K	Resistor,100K,1%	0805	
13	U1, U2	PI2127-01-LGIZ	12A 60V Full-Function Cool-ORing® Solution	7mm x 8mm 17 pin	PICOR

Table 2: Complete PI2127-EVAL1 Evaluation Board Bill of Material

Reference Designator	Value	Functional Description
C1, C2, C3, C4	Not installed	Snubber to reduce voltage ringing when the device turns off
C3	22 μ F	Output (Load) Capacitor
C6	2.2 μ F	Output (Load) Capacitor
D1, D2	LED	To indicate a fault exists when it is on
Q1, Q2	FJV1845	Constant Current bias circuit
R1, R2	Not Installed	Bias Circuit R _{PG} , replaces constant current circuit
R3, R4	2.8K	Constant Current bias circuit, sets the current limiting
R5, R6,	1.5K Ω	LED current limit resistor, selected to operate at 3.3V and 5.0V logic voltage. Replace R5 and R6 with the proper resistor value for different logic voltage.
R7, R8	100K	Constant Current bias circuit
U1, U2	PI2127-01-LGIZ	Cool-ORing® SiP.

Table 3: Component functional description

Test Procedure:

Initial Test Set Up

PI2127-EVAL1 designed with two bias circuit options, bias resistor R_{PG} (R1 and R2) and constant current circuit. The constant current circuits are installed; where R1 and R2 were not installed.

Leave enable inputs (EN1 and EN2) unconnected (open).

Baseline Test Procedure – PI2127 (Refer to Figure 3)

1. Recommended Material

1.1. Material Needed-Picor supplied

- 1.1.1. PI2127-EVAL1
- 1.1.2. PI2127 Product Datasheet

1.2. Recommended Users Supplied Equipment

- 1.2.1. Two DC power supplies: 0-60V; 15A each.
- 1.2.2. One low power logic voltage power supply
- 1.2.3. Load: electronic Load, Power resistors or actual load.
- 1.2.4. Multimeter.
- 1.2.5. Oscilloscope.
- 1.2.6. Appropriately sized interconnect cables.
- 1.2.7. Safety glasses.

Before initial power-up follow these steps to configure the evaluation board for specific end application requirements:

2. EN inputs:

- 2.1. Enable inputs (EN1 and EN2) were left unconnected (open). PI2127 devices will be enabled while enable pins are open. To disable PI2127, connecting the enable input to return (Vin-) with a hard wire or with an active device (Transistor or MOSFET). **Leave EN1 and EN2 unconnected for the initial test.**

3. Control Circuitry Bias:

- 3.1. The PI2127 control circuitry and the gate driver for the internal MOSFET are biased through the S pin. An internal regulator clamps the S pin voltage with respect to PG pin (V_{S-PG}) to 11.7V typically. A bias resistor (R_{PG}) or a Constant Current bias circuit is required if the voltage at the S pin is higher than the minimum Voltage Clamp (V_{S-CLM}, 11V). PI2127-EVAL1 has both circuits laid out, but the constant current bias circuit components are installed while R_{PG} is not installed.

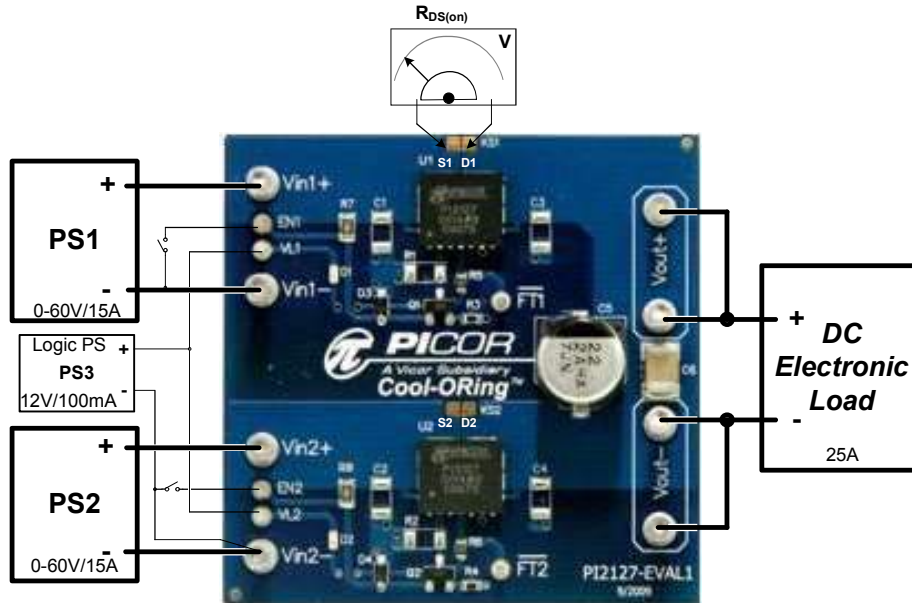


Figure 3: Layout configuration for typical redundant power application, using PI2127-01-LG1Z

3.2. If R_{PG} is desired instead of the Constant Current bias circuit, remove the Constant Current bias circuit components from the evaluation board. The upper ORing (U1) constant current bias circuit components are Q1, R3, R7 and D3. The lower ORing (U2) constant current bias circuit components are Q2, R4, R8 and D4. R_{PG} value can using the following equations:

$$R_{PG} = \frac{V_{in_{min}} - V_{VC-SGND_{Max}}}{I_{VC_{max}} + 0.1mA}$$

And R_{PG} maximum power dissipation is:

$$Pd_{RPG} = \frac{(V_{in_{max}} - V_{VC-SGND_{Min}})^2}{R_{PG}}$$

Where:

- $V_{in_{min}}$: Minimum applied input voltage (Vin to Rtn)
- $V_{in_{max}}$: Maximum applied input voltage (Vin to Rtn)
- $V_{VC-SGND_{Max}}$: Controller maximum clamp voltage, 12.5V
- $V_{VC-SGND_{Min}}$: Controller minimum clamp voltage, 11V
- $I_{VC_{max}}$: Controller maximum bias current, use 2.0mA

R_{PG} calculation example

V_{in} (minimum) = 40V and V_{in} (maximum) = 50V

$$R_{PG} = \frac{40V - 12.5V}{2.1mA} = 13.1K\Omega$$

$$Pd_{RPG} = \frac{(50V - 11V)^2}{13.1K\Omega} = 116mW$$

4. Hook Up of the Evaluation Board

- 4.1. Connect the positive terminal of PS1 power supply to Vin1+. Connect the ground terminal of PS1 to Vin1-. Set the power supply to 48V. **Keep PS1 output disabled, off.**
- 4.2. Connect the positive terminal of PS2 power supply to Vin2+. Connect the ground terminal of PS2 to Vin2-. Set the power supply to 48V. **Keep PS2 output disabled, off.**
- 4.3. Connect the logic power supply PS3 positive terminal to VL1 and VL2. Connect the ground terminal of this power supply to either Vin1- or Vin2-. Set the power supply to the desired logic voltage level, 3.3V or 5V. **Keep PS3 output disabled, off.**
- 4.4. Connect the electronic load to the output between Vout+ and Vout-. Set the load current to 5A.
- 4.5. Enable (turn on) PS3 power supply output.
- 4.6. Enable (turn on) PS1 power supply output.
- 4.7. Turn on the electronic load.
- 4.8. Verify that Vout+ voltage is a few millivolts below 48V. This verifies that the PI2127 (U1) internal MOSFET is in conduction mode.
- 4.9. Verify that Vin2+ is low. This verifies that the PI2127 (U2) internal MOSFET is off.

- 4.10. D2 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin2+).
- 4.11. Enable (turn on) PS2 output.
- 4.12. Verify that both PS1 and PS2 are sharing load current evenly by looking at the supply current. *Power supplies output may need adjustment to set current sharing between the supplies.*
- 4.13. Disable (turn off) PS1, PS2, and PS3 outputs.
- 4.14. Enable (turn on) PS2 output then Enable and PS3 outputs.
- 4.15. Verify that the electronic load voltage reading is few millivolts below 48V. This verifies that the PI2127-01-LGIZ internal MOSFET is in conduction mode.
- 4.16. D2 should be off. This verifies that there is no fault condition.
- 4.17. Verify that Vin1+ is low. This verifies that the PI2127 (U1) internal FET is off.
- 4.18. D1 should be on. This is due to a reverse voltage fault condition caused by the bus voltage being high with respect to the input voltage (Vin1+).

Note: *When the PI2127 internal MOSFET is in the on state, it will not turn off unless a reverse current greater than 0.75A is sensed in the MOSFET.*

When both power supplies are enabled and both PI2127 MOSFETs are in $R_{DS(on)}$, if one of the sources (Power supplies) removed or disabled both PI2127 stay on unless the disabled power supply sources current greater than 0.75A when turned off.

5. Internal MOSFET $R_{DS(on)}$ Measurement:

- 5.1. The internal MOSFET $R_{DS(on)}$ can be measured with a voltmeter between the S1 and D1 Kelvin connection for U1 and between the S2 and D2 Kelvin connection for U2. The potential between S1 and D1 is the voltage drop across the internal MOSFET and:

$$R_{DS(on)} = \frac{V_{S1} - V_{D1}}{I_{in}}$$

Where:

$V_{S1} - V_{D1}$: Voltage drop across the internal MOSFET

I_{in} : Input current.

Note: The $R_{DS(on)}$ value is temperature dependent and the junction temperature increases directly proportional to power dissipation.

6. Input short circuit test:

PI2127 has a very fast response (80ns) to a reverse current (Input short) fault condition. Measuring a short period event requires attention to the test set-up. Before proceeding, consider the following:

- 6.1. To emulate a real application, the BUS supplies for this test should have a solid output source such as a DC-DC converter that supplies high current and can be connected very close to the evaluation board to reduce stray parasitic inductance. Or use the prospective supply sources of the end application where the PI2127 will be used. Typical bench power supplies have slow response to output load change. In this test when the power supply output is shorted and then released, the bench power supply may produce high output voltage with high current capability that may damage the device under test.
- 6.2. Do not install Input capacitors (C1 and/or C2) in this test.
- 6.3. Output capacitor (C5) should be installed.
- 6.4. Place the scope probes very close to the PI2127 S and D pins to measure Vin and Vout, and make sure that the scope ground leads are very short. You may use a close by ground pad for the scope probe return, such as C1, C2, C3 and C4 return pads.
- 6.5. Apply a short at one of the inputs (Vin1+ or Vin2+) when both SIP's (U1 and U2) are on, PS1 and PS2 are enabled. The short can be applied electronically using a MOSFET connected between Vin+ and Vin- or simply by connecting Vin+ to Vin-. Then measure the response time between when the short is applied and the PI2127 internal MOSFET is disconnected (or turned off). An example for the PI2127 response time to an input short circuit is shown in Figure 4.

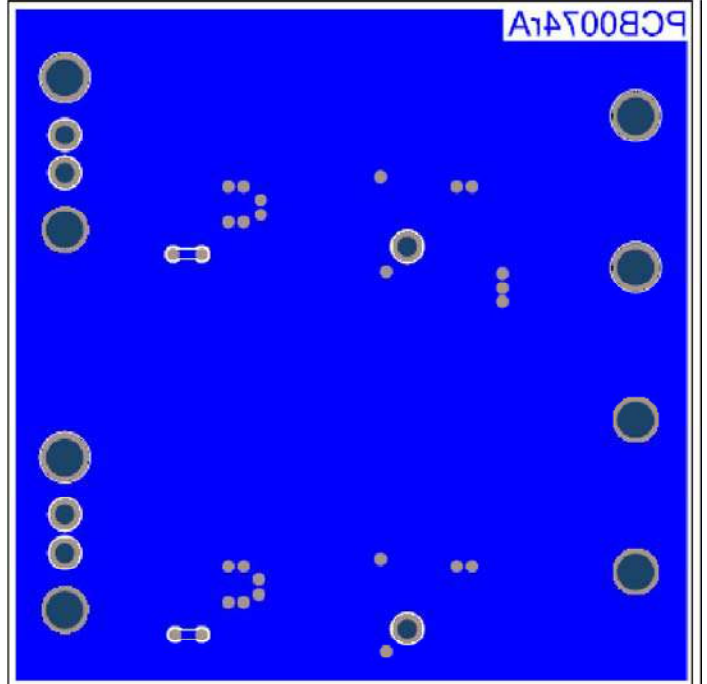
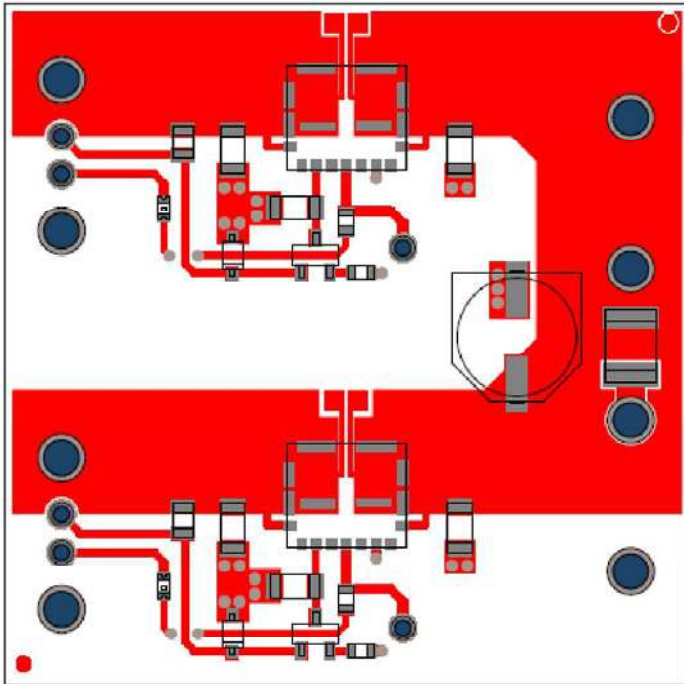


Figure 7: PI2127-EVAL1 layout top layer. Scale 2.0:1

Figure 8: PI2127-EVAL1 layout bottom layer 2. Scale 2.0:1

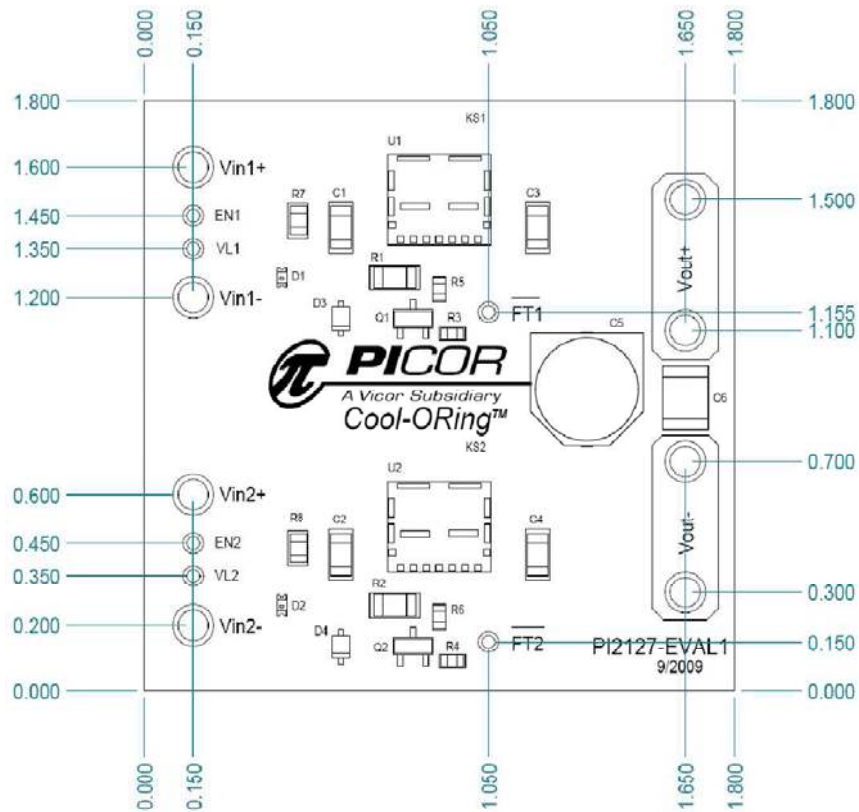


Figure 9: PI2127-EVAL1 evaluation board mechanical drawing.

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