# nanoSmart® Battery Management Under-Voltage Load Switch

POWER PRODUCTS

## Features

- Off-Active™ feature with ultra-low pico-amp current
- Best-in-class Off-active™ quiescent current of 100pA
- Ultra-low on-active quiescent current of 70nA
- Accurate on to Off-active™ voltage threshold
- Threshold voltage options of 1.2V - 4.2V in 100mV steps (programmed at manufacturing)
- Supervisory over-current limit shutdown
- Low Rds(on): 175mΩ typical @ 5V
- Low drop out disconnect from VBAT to loads
- Turn-on slew rate controlled
- 500mV off to on-active hysteresis

## Description

The TS12001 Off-Active™ battery management load switch is used to protect a battery from excessive discharge. It consists of an internally generated threshold voltage (VTHRESH), comparator with hysteresis, slew rate control for the load switch, a P-Channel load switch, and an open-drain indicator pin. When the input battery voltage is above VTHRESH, the load switch is on-active. When the input battery voltage falls to VTHRESH, the load switch is Off-Active™ and the quiescent current draw is approximately 100pA.

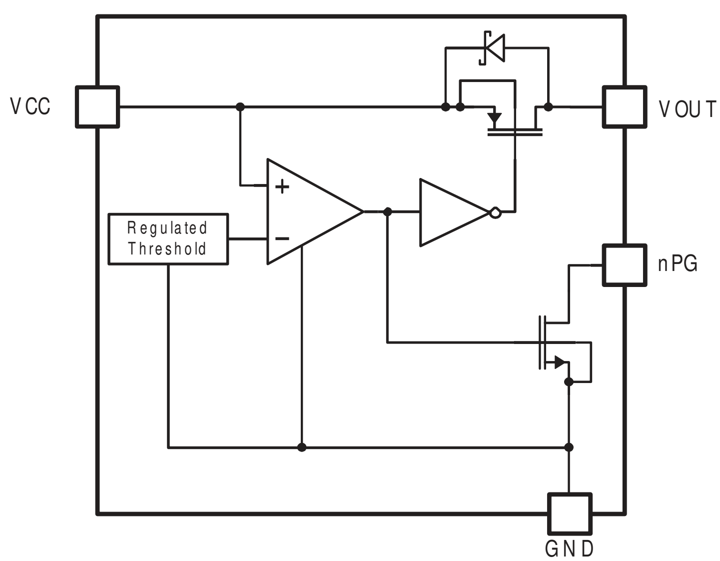
## Summary

- Wide input voltage range: 1.2V – 5.5V
- Packaged in a 8pin DFN (2x2)
- Product is lead-free, Halogen Free, RoHS / WEEE compliant

## Applications

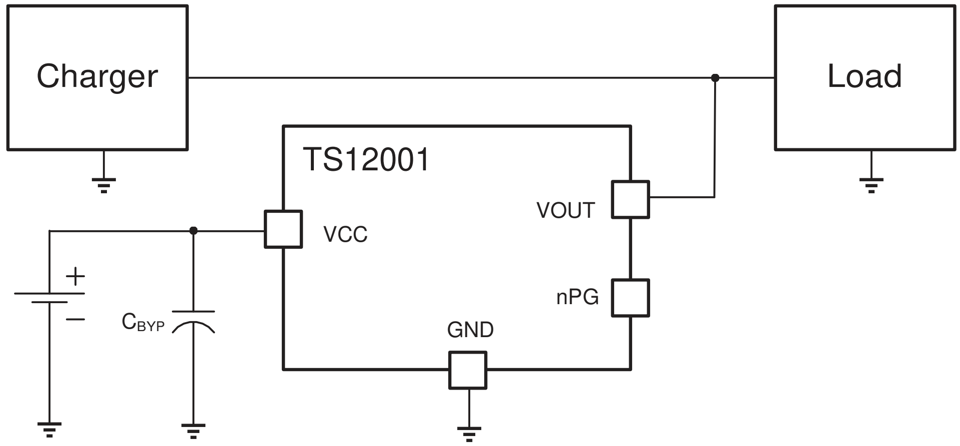
- Portable Battery
- Industrial
- Medical
- SmartCard
- RFID
- Energy Harvesting Systems

## Block Diagram



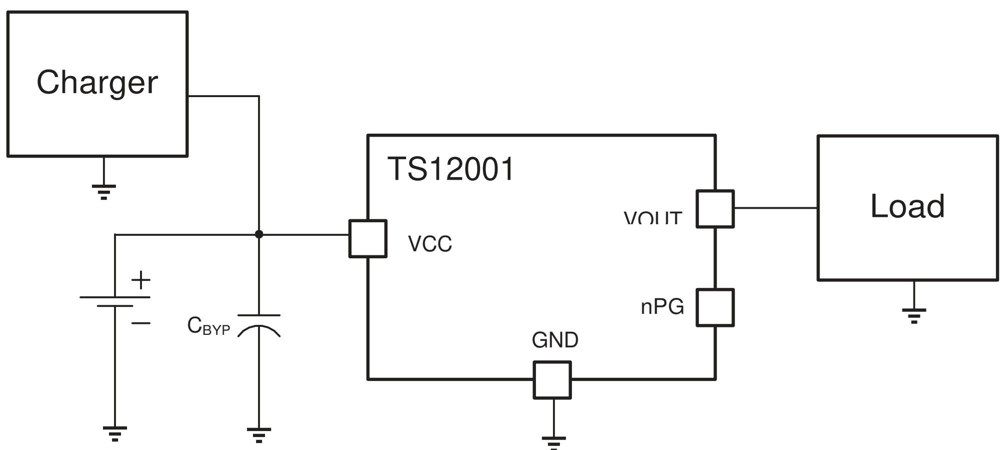
## Typical Applications

### Disconnect the Battery




Note: When the TS12001 is Off-Active™, the battery will continue to charge through the body diode between VOUT and VCC.

### Disconnect the Load



# Pin Description

| Pin # | Pin Name | Pin Type (1) | Description |
|---|---|---|---|
| 1 | GND | P | GND |
| 2 | $V_{OUT}$ | O | Output to System Load |
| 3 | NC | | No Connect (connect to GND or float) |
| 4 | NC | | No Connect (connect to GND or float) |
| 5 | NC | | No Connect (connect to GND or float) |
| 6 | $V_{CC}$ | I/P | Supply Input |
| 7 | $V_{CC}$ | I/P | Supply Input |
| 8 | nPG | O | Open-Drain N-Channel Output (low indicates Power Good) |

(1) I = Input, O = Output, P = Power

# Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted(2, 3, 4)

| Parameter | Value | Unit |
|---|---|---|
| VCC, VOUT, nPG | -0.3 to 6.0 | V |
| Electrostatic Discharge – Human Body Model | 2 | kV |
| Operating Junction Temperature Range, $T_J$ | -40 to 85 | °C |
| Storage Temperature Range, $T_{STG}$ | -65 to 150 | °C |
| Lead Temperature (soldering, 10 seconds) | 260 | °C |

(2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(3) All voltage values are with respect to network ground terminal.

(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

# Thermal Characteristics

| Package DFN | θJA (°C/W) (See Note 5) | θJC (°C/W) (See Note 6) |
|---|---|---|
| 8 pin | 73.1 | 10.7 |

(5) This assumes a FR4 board only.

(6) This assumes a 1 Oz. Copper JEDEC standard board with thermal vias – See Exposed Pad section and application note for more information.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Unregulated Supply Input Voltage ($V_{CC}$) | 1.2 | | 5.5 | V |
| Operating Ambient Temperature, $T_A$ (Note 7) | -40 | | 55 | °C |
| Operating Junction Temperature, $T_J$ | -40 | | 85 | °C |
| Input Bypass Capacitor ($C_{BYP}$) | | 100 | | nF |

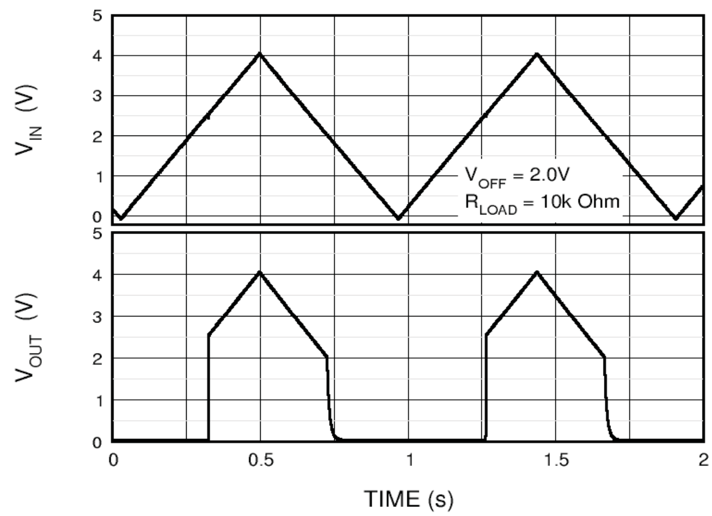
(7) TA Max shown here is a guideline. Higher $T_A$ can be tolerated if $T_J$ does not exceed the Absolute Maximum Rating.

## Characteristics

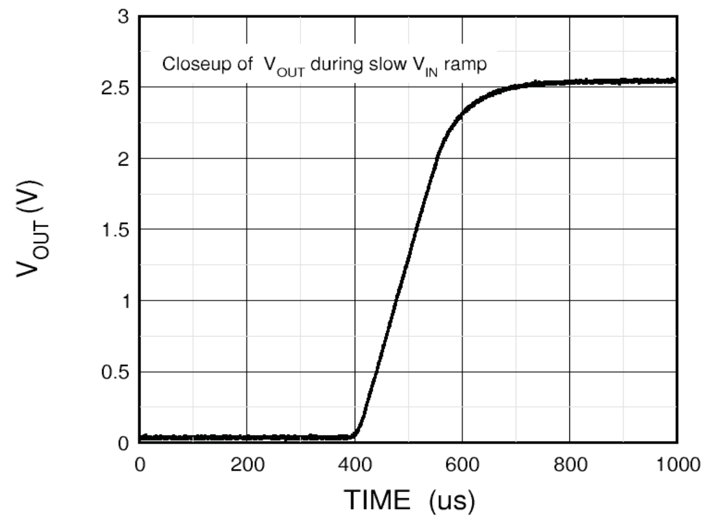
Electrical characteristics, $V_{CC}$ = 1.2V to 5.5V, TJ = 25C, unless otherwise noted

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input Supply** | | | | | | |
| $V_{CC}$ | Input Supply Voltage | | 1.2 | | 5.5 | V |
| $I_{q\text{-}ON}$ | Quiescent current: on-active Mode | $V_{CC}$ = 5V, No Load | | 70 | 150 | nA |
| $I_{q\text{-}OFF}$ | Quiescent current: Off-Active™ Mode | $V_{CC} < V_{THRESH}$, No Load | | 100 | | pA |
| **Load Switch** | | | | | | |
| $I_{OC}$ | Over Current Shutdown | $V_{CC}$ = 5.0V | | 3 | | A |
| $T_{OC}$ | Over Current Retry Period | $V_{CC}$ = 5.0V | | 1.7 | | ms |
| $I_{LEAK\text{-}SW}$ | Output Switch Leakage Current | $V_{CC} < V_{THRESH}$; $V_{OUT}$ Grounded | | 100 | | pA |
| Rds-on | Switch On Resistance | $V_{CC}$ = 5.0V | | 175 | | mΩ |
| | | $V_{CC}$ = 3.3V | | 200 | | mΩ |
| | | $V_{CC}$ = 1.8V | | 350 | | mΩ |
| **Transition Times** | | | | | | |
| $t_{d1}$ | Transition delay: on-active to Off-Active™ | $V_{OFF}$ = 2.0V, $V_{CC}$ = 3.0V → 1.5V | | 650 | | μs |
| $t_{d2}$ | Transition delay: Off-Active™ to on-active | $V_{OFF}$ = 2.0V, $V_{CC}$ = 1.5V → 3.0V | | 1.7 | | ms |
| $t_{ON}$ | Output turn-on rise time | $V_{CC}$ = 2.5V, $R_{LOAD}$ = 50Ω | | 200 | | μs |
| **nPG Output** | | | | | | |
| $I_{LEAK\text{-}nPG}$ | Output Leakage | $V_{CC}$ = 5.0V, $V_{nPG}$ = 5.5V | | | 100 | nA |
| $V_{OL\text{-}nPG}$ | Low-Level Output Voltage | $I_{nPG}$ = 5 mA | | | 0.4 | V |
| **Off-Active Thresholds** | | | | | | |
| $V_{OFF}$ | Off-Active™ Threshold | $V_{THRESH}$ = 1.2V to 3.3V | 0.95* $V_{THRESH}$ | $V_{THRESH}$ | 1.05* $V_{THRESH}$ | V |
| $V_{Hys}$ | Off-Active™ to on-active Hysteresis | Rising Transition: Off-Active™ to on-active | | 500 | | mV |

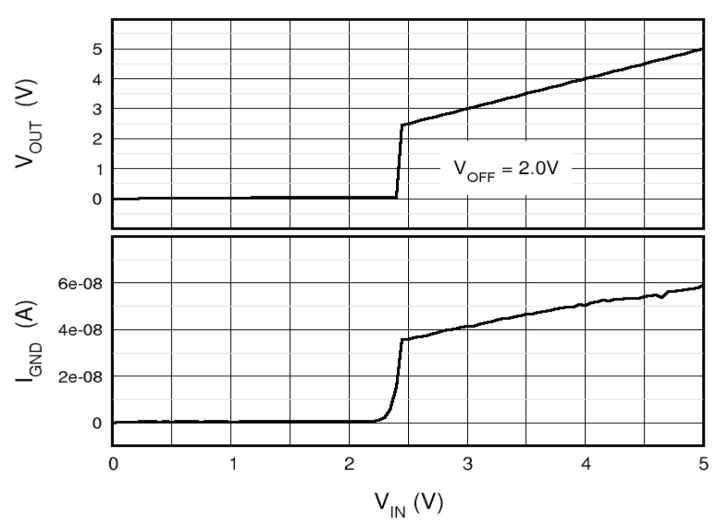
On-Active / Off-Active™ Characteristics



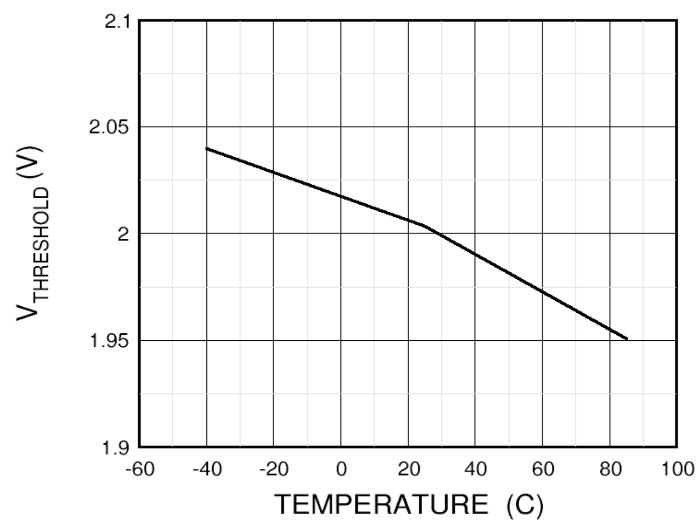

On-Active Switching Behavior



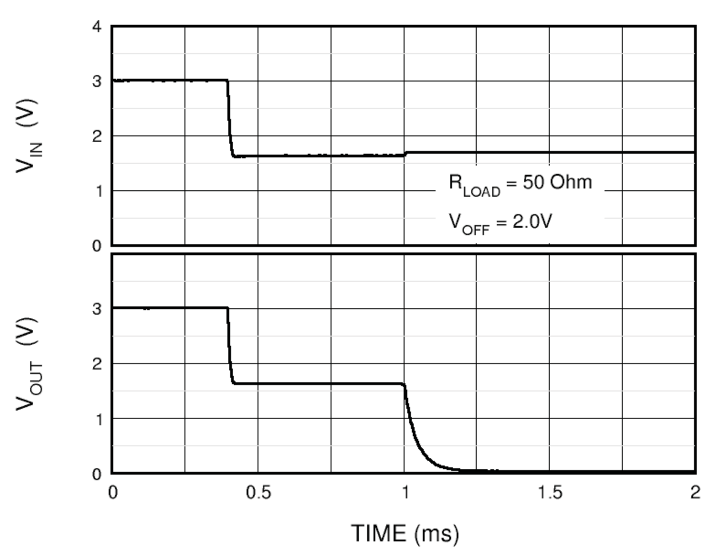

On-Active / Off-Active™ $I_q$



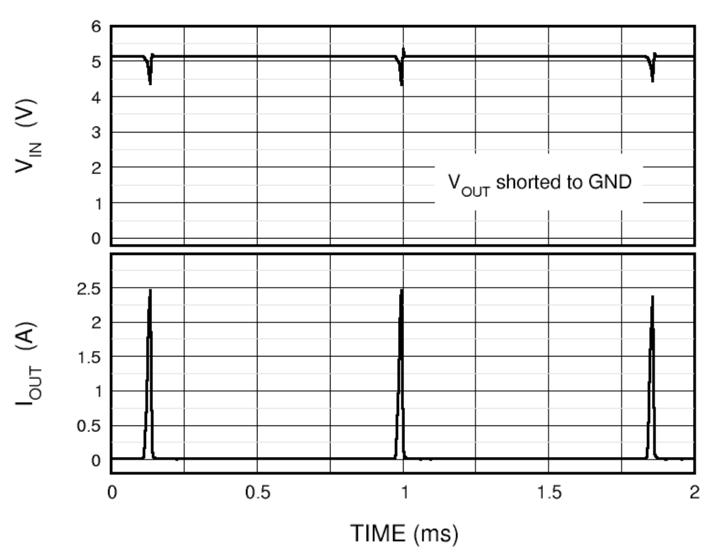

Off-Active™ $V_{THRESH}$ Temperature Performance



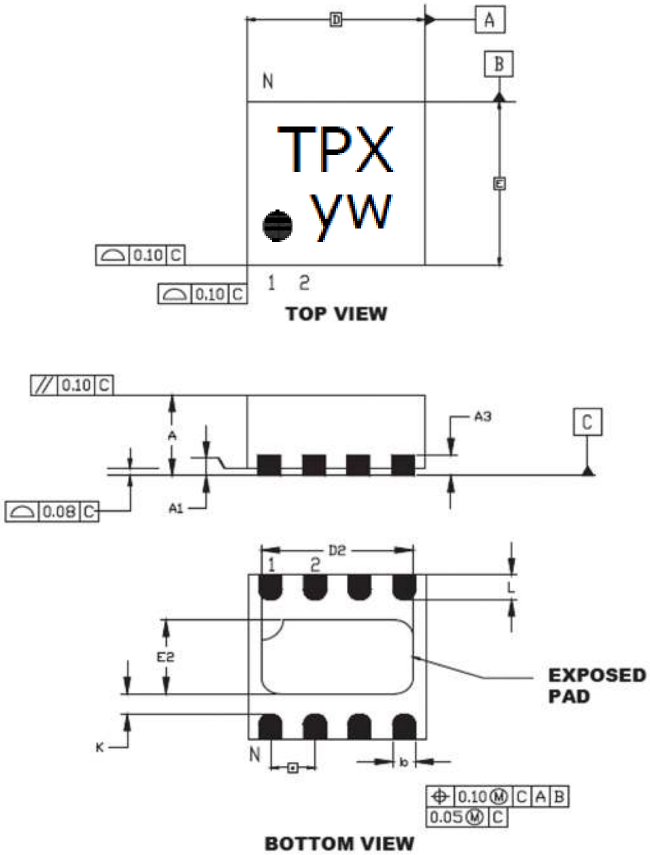

On-Active / Off-Active™ Transition Delay




Over Current Retry Performance



# Package Mechanical Drawings (all dimensions in mm)

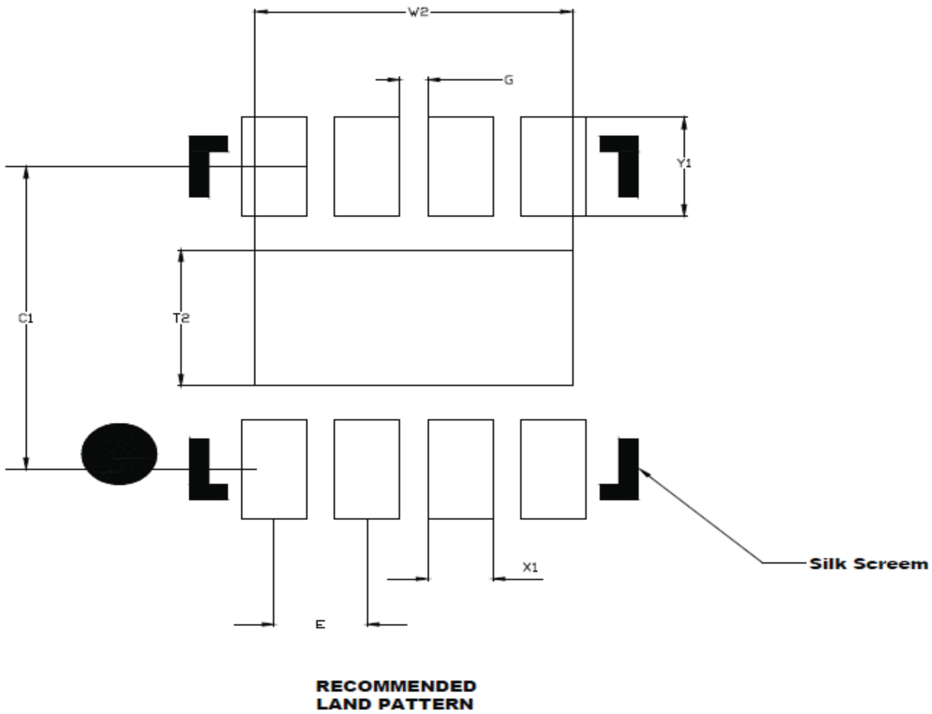



Refer to the Ordering Information table on page 10 for device marking codes

| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Width | E2 | 0.75 | 0.90 | 1.00 |
| Overall Width | E | | 2.00 BSC | |
| Exposed Pad Length | D2 | 1.55 | 1.70 | 1.80 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.30 | 0.40 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

# Recommended PCB Land Pattern



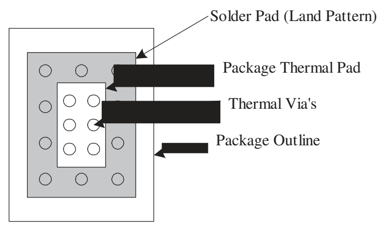

DIMENSIONS IN MILLIMETERS

| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | W2 | - | - | 1.70 |
| Optional Center Pad Length | T2 | - | - | 0.90 |
| Contact Pad Spacing | C1 | - | 2.00 | - |
| Contact Pad Spacing | C2 | - | - | - |
| Contact Pad Width (X8) | X1 | - | - | 0.35 |
| Contact Pad Length (X8) | Y1 | - | - | 0.65 |
| Distance Between Pads | G | 0.15 | - | - |

# Application Using a Multi-Layer PCB

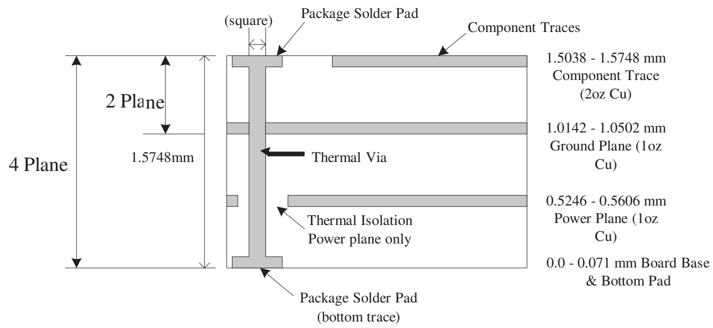
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

**The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with a ground plane.**



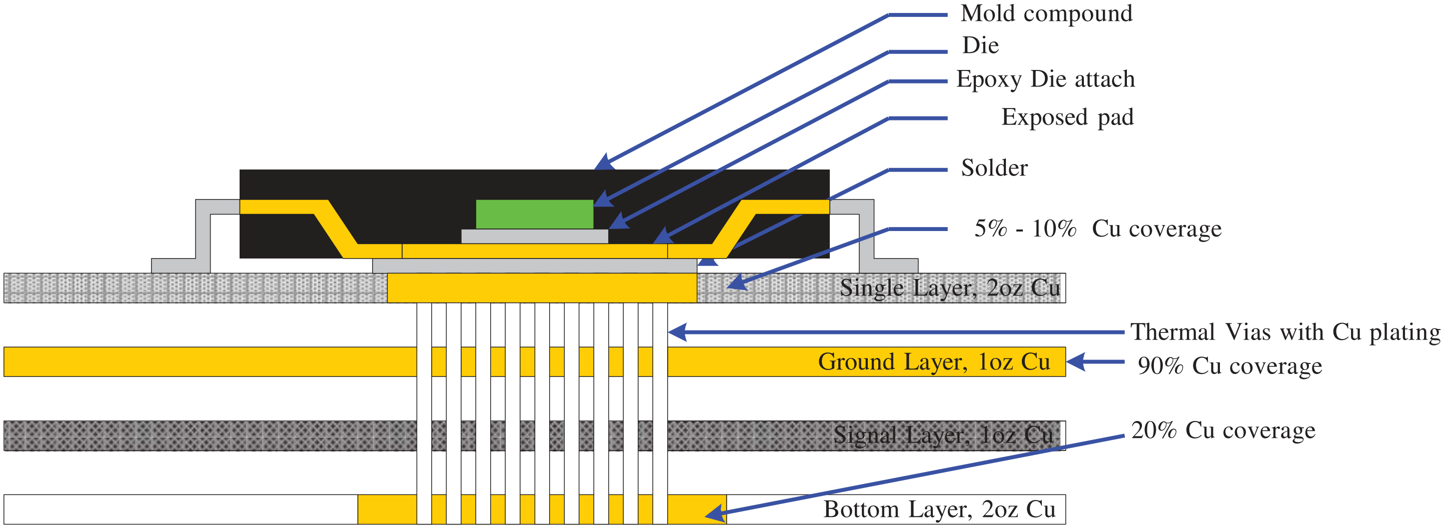

Package and PCB Land Configuration
For a Multi-Layer PCB

**JEDEC standard FR4 PCB Cross-section:**




Multi-Layer Board (Cross-sectional View)

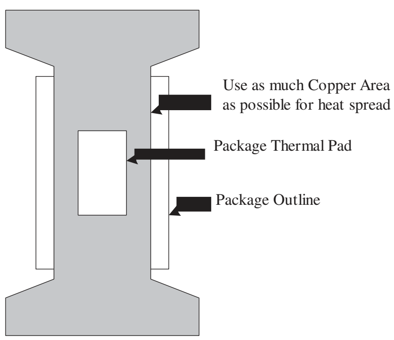
In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.




Note: NOT to Scale

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

# Application Using a Single Layer PCB




Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

**IMPORTANT:**

If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

# Ordering Information

**TS12001-CvvvDFNR**

| Part Number | Description | Marking Code |
|---|---|---|
| vvv | Threshold Voltage ($V_{THRESH}$)* | TPX |
| 017 | 1.7 V | T05 |
| 021 | 2.1 V | T09 |
| 023 | 2.3 V | T0B |
| 024 | 2.4 V | T0C |
| 025 | 2.5 V | T0D |
| 026 | 2.6 V | T0E |
| 028 | 2.8 V | T0F |
| 030 | 3.0 V | T0G |

* Custom values also available (1.2V - 4.2V typical in 100mV increments)

# RoHS and Reach Compliance

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- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons (Halogen free)
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg) Perfluorocarbons
- (PFCs) Polybrominated
- biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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