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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	40				
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.00112				
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00161				
I _D (A)	350				
Configuration	Single				
Package	PowerPAK SO-8L				

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



	O D
G O F	
N-Channel MOSFET	o _s

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V _{GS}	± 20		
Continuous drain current	T _C = 25 °C	1	350		
	T _C = 125 °C	I _D	261		
Continuous source current (diode conduction)		I _S	324	Α	
Pulsed drain current ^a		I _{DM}	600		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	42		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	84	mJ	
Maximum power dissipation ^a	T _C = 25 °C	D	500	W	
	T _C = 125 °C	P_{D}	166		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperat	-	260	C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount b	R _{thJA}	68	°C/W	
Junction-to-case (drain)		R _{th.IC}	0.3	C/VV	

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		40	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.2	1.7	2.2	V	
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1	μΑ	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50		
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250		
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α	
		V _{GS} = 10 V	I _D = 15 A	-	0.0009	0.00112		
Duein annua an atata unaistana 3		V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	1	-	0.00200		
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.00244	Ω	
		V _{GS} = 4.5 V	I _D = 15 A	-	0.00124	0.00161		
Forward transconductance b	9 _{fs}	V_{DS}	= 15 V, I _D = 10 A	1	30	-	S	
Dynamic ^b								
Input capacitance	C _{iss}			-	5725	8015		
Output capacitance	C _{oss}	V _{GS} = 0 V V _{DS} = 25 V, f = 1 MHz		-	1790	2505	pF	
Reverse transfer capacitance	C _{rss}			-	183	256	1	
Total gate charge ^c	Qg			-	107	150	nC	
Gate-source charge c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 40 \text{ A}$	-	17.5	-		
Gate-drain charge ^c	Q _{gd}			-	19	-		
Gate resistance	R_g	f = 1 MHz		0.67	1.48	2.40	Ω	
Turn-on delay time ^c	t _{d(on)}	$V_{DD} = 20 \text{ V}, R_L = 0.5 \Omega$ $I_D \cong 40 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		-	13	19	ns	
Rise time ^c	t _r			-	16	23		
Turn-off delay time ^c	t _{d(off)}			-	50	71		
Fall time ^c	t _f			-	14	20		
Source-Drain Diode Ratings and Cha	racteristics b							
Pulsed current ^a	I _{SM}			=	-	600	Α	
Forward voltage	V_{SD}	I _F = 15 A, V _{GS} = 0 V		-	-	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 40 A, di/dt = 100 A/μs		-	57	80	ns	
Body diode reverse recovery charge	Q _{rr}			-	62	86	nC	
Reverse recovery fall time	t _a			1	26	37		
Reverse recovery rise time	t _b			-	31	42	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	1.8	2.6	Α	

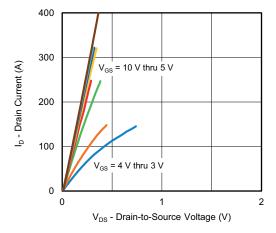
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

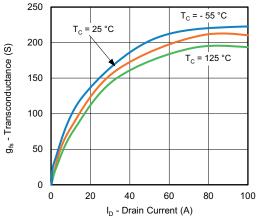
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



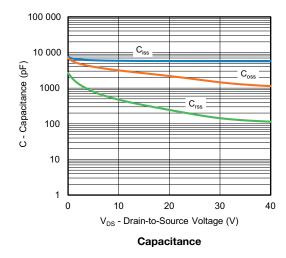
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

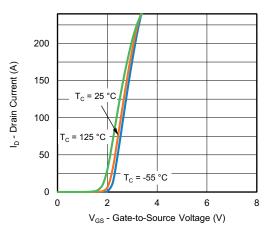


Output Characteristics

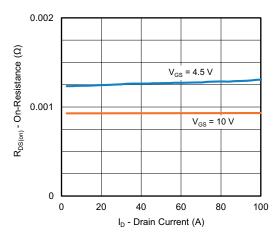


Transconductance

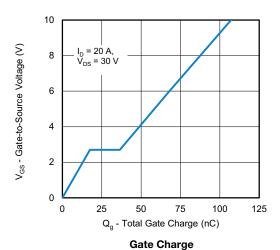




Transfer Characteristics

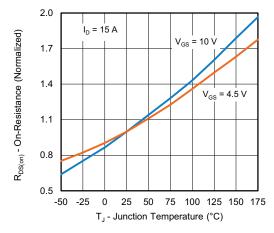


On-Resistance vs. Drain Current

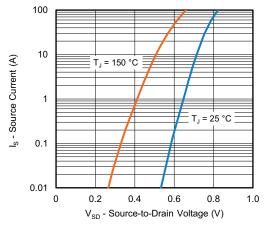




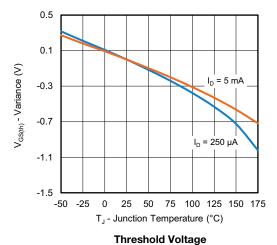
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature

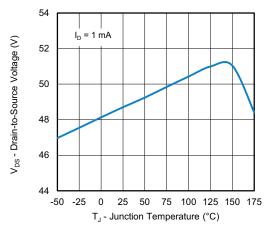


Source Drain Diode Forward Voltage

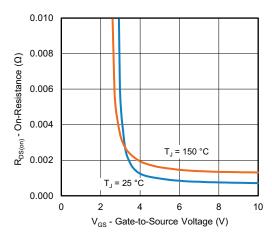


Note

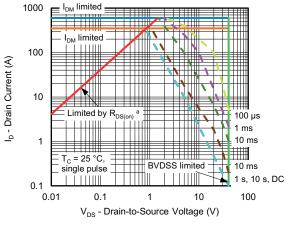
a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



Drain Source Breakdown vs. Junction Temperature



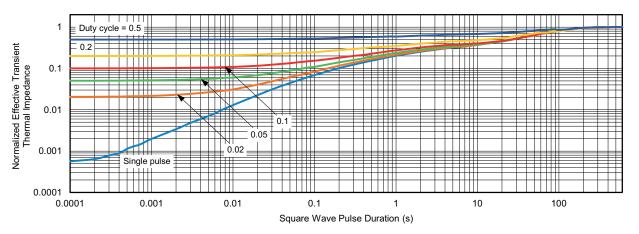
On-Resistance vs. Gate-to Source Voltage



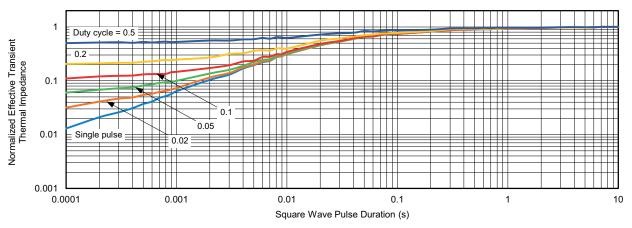
Safe Operating Area



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

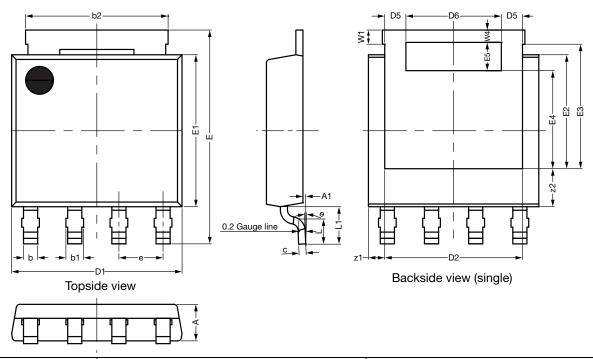
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg277510.



PowerPAK® SO-8L (PPKSO8LWLA) Case Outline 3



DIM		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.00	1.05	1.10	0.039	0.041	0.043	
A1	0.00		0.127	0.000		0.005	
b	0.33	0.41	0.49	0.013	0.016	0.019	
b1	0.43	0.51	0.59	0.017	0.020	0.023	
b2	4.00	4.10	4.20	0.157	0.161	0.165	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D5	0.51	0.61	0.71	0.020	0.024	0.028	
D6	2.64	2.74	2.84	0.104	0.108	0.112	
е		1.27 BSC		0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
E3	3.48	3.58	3.68	0.137	0.141	0.145	
E4	2.72	2.82	2.92	0.107	0.111	0.115	
E5	0.71	0.81	0.91	0.028	0.032	0.036	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
W1	0.31	0.41	0.51	0.012	0.016	0.020	
W4	0.31	0.36	0.41	0.012	0.014	0.016	
z1	0.37	0.47	0.57	0.015	0.019	0.022	
z2	0.99	1.09	1.19	0.039	0.043	0.047	
θ	0°		5°	0°		5°	

ECN: C22-1223-Rev. C, 19-Dec-2022

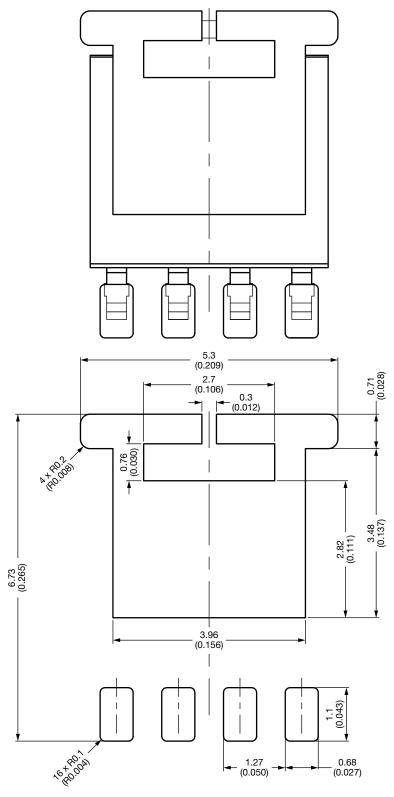
DWG: 6067 **Note**

Millimeter will govern

Revison: 19-Dec-2022 1 Document Number: 76666



Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)



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