TEXAS INSTRUMENTS

# DAC8534 Evaluation Module

# User's Guide

*June 2003* *Data Acqusition - Digital/Analog Converters*

*SLAU107*

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
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# Preface

# Read This First

### *About This Manual*

This user's guide describes the characteristics, operation, and the use of the DAC8534 Evaluation Module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

### *How to Use This Manual*

This document contains the following chapters:

Chapter 1 – EVM Overview

Chapter 2 – PCB Design and Performance

Chapter 3 – EVM Operation

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| **Data Sheets:** | **Literature Number:** |
|---|---|
| DAC8534 | SBAS254 |
| REF02 | SBVS-003A |
| OPA627 | PDS-998H |
| OPA2132 | PDS-1309B |

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Chapter 1

# EVM Overview

This chapter gives a general overview of the DAC8534 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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## 1.1 Features

This EVM features the DAC8534 digital-to-analog converter. The DAC8534 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the high resolution, quad-channel, and serial input DAC. This EVM features a serial interface to communicate with any host microprocessor or TI DSP-based system.

## 1.2 Power Requirements

The following sections describe the power requirements of this EVM.

### 1.2.1 Supply Voltage

The DC power supply requirement for the digital section ($V_{DD}$) of this EVM is typically 5 V connected to the J5-1, or via J6-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J5-2 and J6-5 terminal. The DC power supply requirements for the analog section of this EVM are as follows: the $V_{CC}$ and $V_{SS}$ ranges from 15.75 V to -15.75V maximum and connects through J1-3 and J1-1 respectively, or through J6-1 and J6-2 terminals. The 5 VA connects through J5-3 or J6-3 and the 3.3 VA connects through J6-8. All of the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The device under test (U1), can be powered by connecting an analog power supply at terminal 5 VA or 3.3 VA and selecting the proper position of jumper W1. This allows the DAC8534 analog section to operate from either supply power, while the I/O and digital section is powered by 5 V, $V_{DD}$.

The $V_{CC}$ supply source is mainly used to provide the positive rail of the external output op amp U2, the reference chip U3, and the reference buffer U8. The negative rail of the output op amp U2 can be selected between $V_{SS}$ and AGND via W5 jumper. The external op amp is installed as an option to provide output signal conditioning, or boost capacitive load drive and for other output mode requirement desired.

**CAUTION**

**To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.**

**Stresses above the maximum listed voltage ratings may cause permanent damage to the device.**

### 1.2.2 Reference Voltage

The 5 V precision voltage reference is provided to supply the external voltage reference for the DAC through U3 (REF02), via jumper W4 by shorting pins 1 and 2. The reference voltage goes through an adjustable 100-KΩ potentiometer R11, in series with 20-kΩ R10, to allow the user to adjust the reference voltage to its desired settings. The voltage reference is then

buffered through U8A as seen by the device under test. The test points TP1, TP2, and TP5 are also provided, as well as J4-18 and J4-20, to allow the user to connect an external reference source, if the onboard reference circuit is not desired. The external voltage reference should not exceed 5-V DC.

The REF02 precision reference is powered by $V_{CC}$ (15 V) through J1-3 or J6-1 terminal.

**CAUTION**

**When applying an external voltage reference through TP1 or J4-20, make sure that it does not exceed 5 V maximum. Otherwise, this can permanently damage the DAC8434, U1, device under test.**

## 1.3 EVM Basic Functions

The DAC8534 EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8534 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TI DSP or some sort of a waveform generator.

The headers J2 and P2 are the connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8534 EVM using a custom built cable.

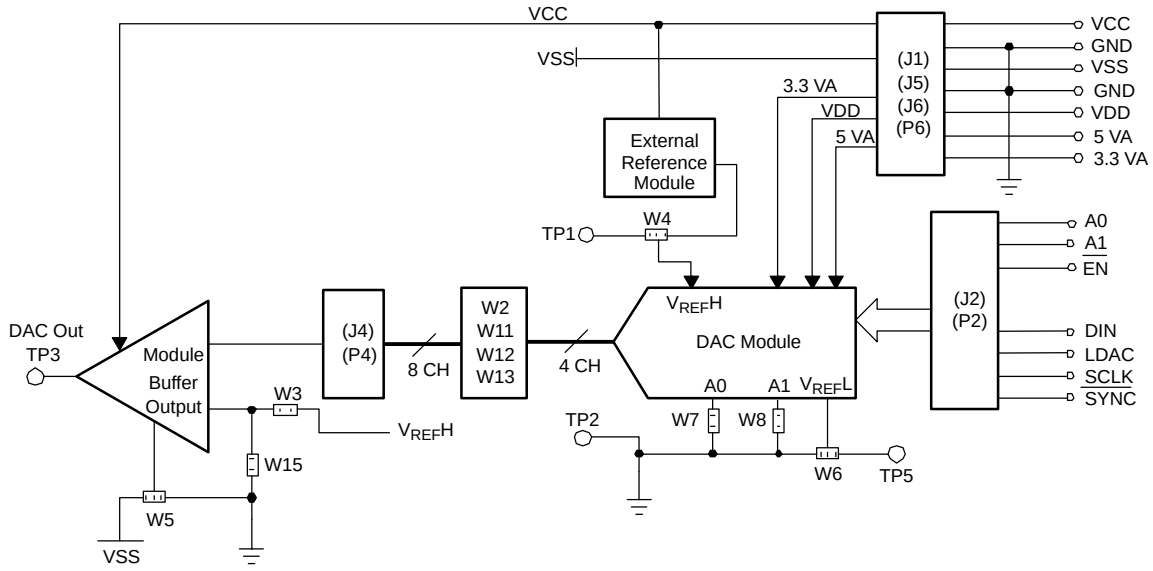
A specific adapter interface card is also available for most of TI's DSP starter kits (DSK)—card models depend on the type of TI DSP starter kit. Therefore, when requesting an adapter interface card be sure to specify the DSP in use. In addition, a motherboard platform that is MSP430-microprocessor-based can interface to this EVM, and is available. For more details or information regarding the adapter interface card, or the MSP430 motherboard platform, call Texas Instruments Inc. or e-mail us at dataconvapps@list.ti.com.

J4 allows for stacking EVMs and DAC output monitoring through selected header pins. Stacking allows a total of eight DAC channels to be used, provided the enable signals ($\overline{EN}$) are unique to each EVM board stacked. All outputs can be switched through their respective jumpers W2, W11, W12, and W13.

In addition, the option of selecting one DAC output to be fed to the noninverting side of the output op amp U2 is also possible by using a jumper across the selected pins of J4. U2 must be first configured correctly for the desired waveform characteristic—refer to Chapter 3 of this user's guide.

A block diagram of the EVM is shown in the Figure 1-1.

*Figure 1-1. EVM Block Diagram*



Chapter 2

# PCB Design and Performance

This chapter describes the layout design and mechanical characteristics of the PCB, as well as a brief description of the EVM test performance procedure. The EVM bill of materials is also included in this section.

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## 2.1 PCB Layout

The DAC8534EVM is designed to preserve the performance quality of the DAC device under test, as specified in the datasheet. Carefully analyzing the EVM's physical restrictions and the given or known elements that contribute to the EVM's performance degradation is the key to a successful design implementation. The obvious attributes, that diminish the performance of the EVM, can be taken care of during the schematic design phase by properly selecting the right components, and building the circuit correctly. The circuit design phase should include adequate bypassing, identifying and managing the analog and digital signals, and a knowedge or understanding of the mechanical attributes of individual components.

An obscure part of the design phase is the layout process, where lack of knowledge and inexperience can easily present a problem. The main concern here is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane does the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but using the largest possible trace width allowable in the design. Good design practice is seen in the layout figures in this chapter.

The DAC8534EVM board is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has a dimension of 43,180 mm (1.7 inch) $\times$ 82,550 mm (3.25 inch), and the board thickness is 1,5748 mm (0.062 inch). Figures 2 through 6 show the individual artwork layers.

*Figure 2-1. Top Silkscreen*

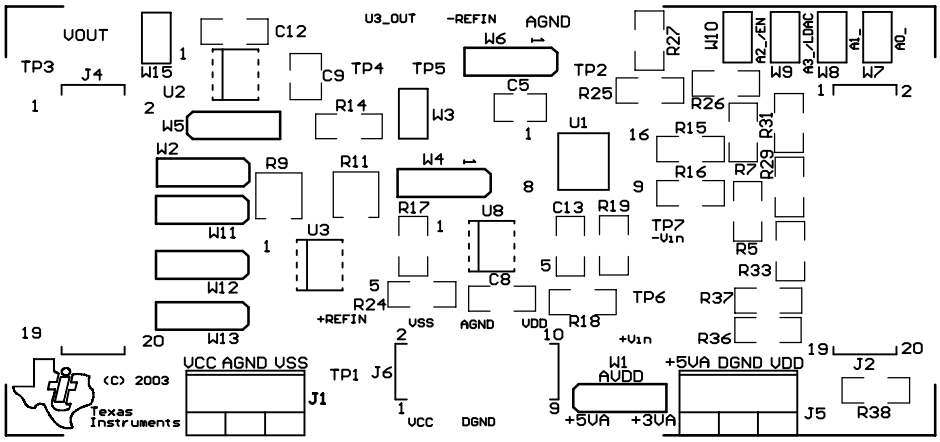



*Figure 2-2. Layer 1 (Top Signal Plane)*

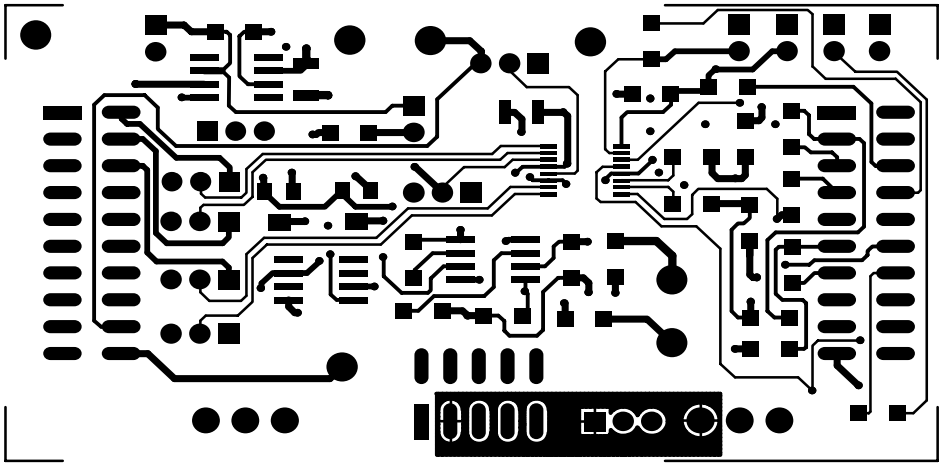


*Figure 2-3. Layer Two (Ground Plane)*

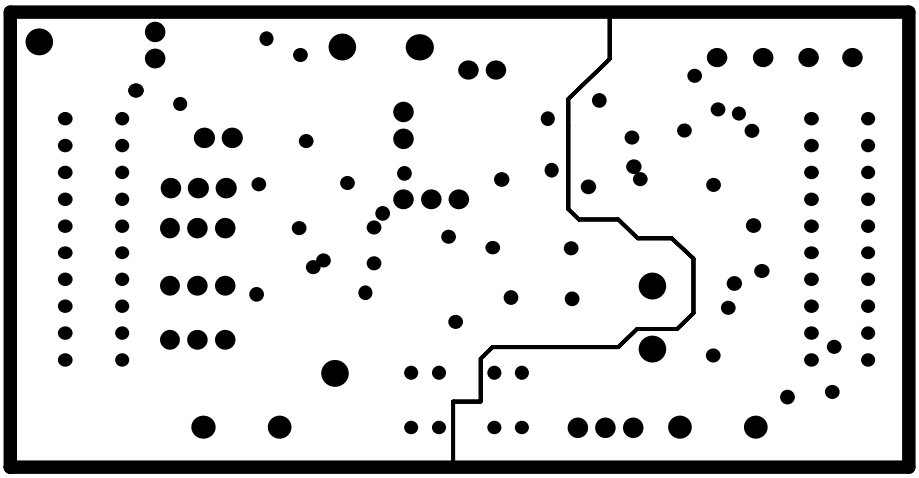


*Figure 2-4. Layer 3 (Power Plane)*

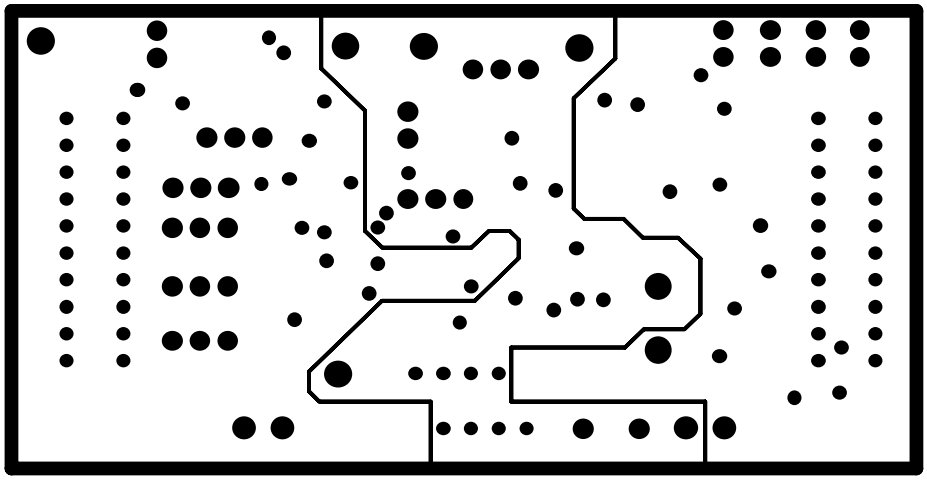


*Figure 2-5. Layer 4 (Bottom Signal Plane)*

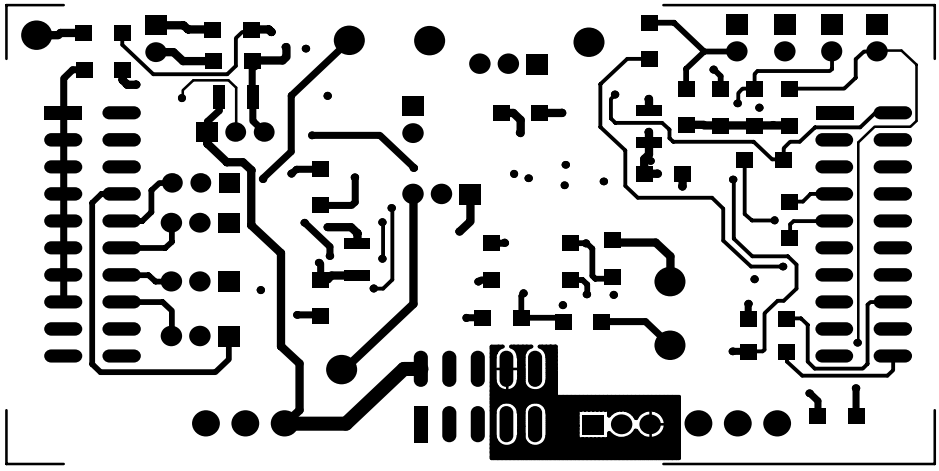


*Figure 2-6. Bottom Silkscreen*

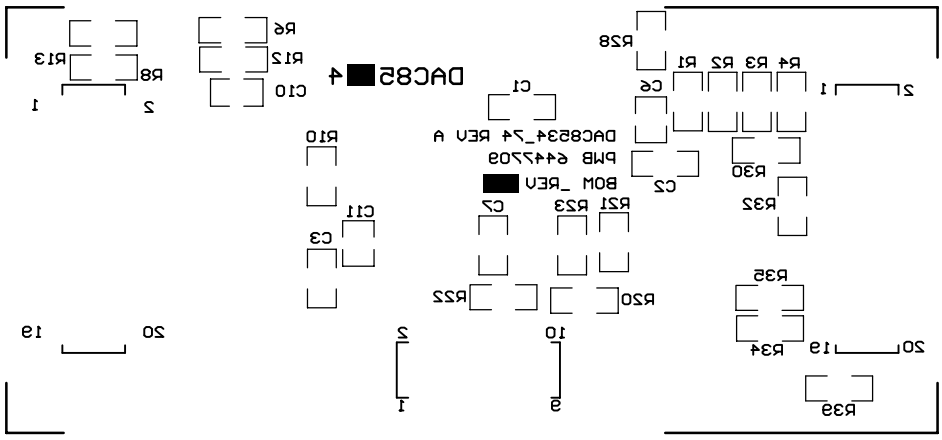
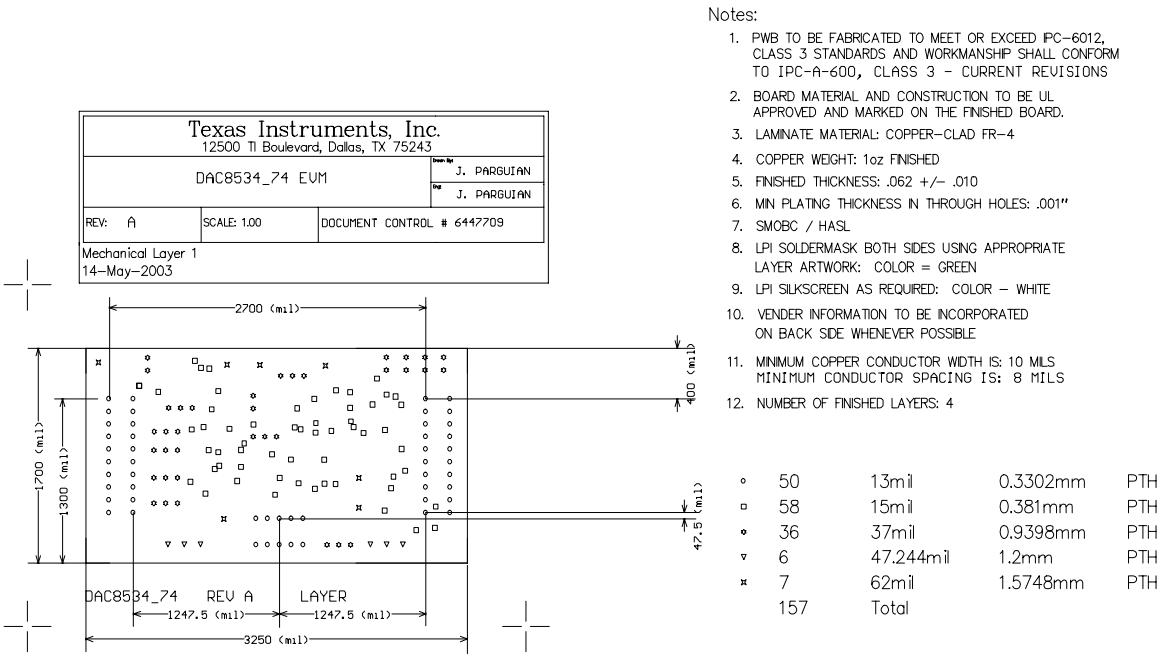


*Figure 2-7. Drill Drawing*




## 2.2 EVM Performance

The EVM performance test is conducted using a high density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LABVIEW software. The EVM board is tested for all codes of 65535, and the device under test (DUT) is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

## 2.3 Bill of Materials

*Table 2-1. Parts List*

| Item # | Qty | Designator | Manufacturer | Part Number | Description |
|---|---|---|---|---|---|
| 1 | 2 | C9, C10 | Panasonic | ECUV1H105JCH | 1 µF, 1206 Multilayer ceramic capacitor |
| 2 | 4 | C1, C2, C3, C7 | Panasonic | ECJ3VB1C104K | 0.1 µF, 1206 Multilayer ceramic capacitor |
| 3 | 1 | C12 | Panasonic | ECUV1H102JCH | 1 nF, 1206 Multilayer ceramic capacitor |
| 4 | 3 | C5, C6, C11 | Kemet | C1210C106K8PAC | 1 0µF, 1210 Multilayer ceramic X5R capacitor |
| 5 | 19 | R8, R15, R16, R17, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39 | Panasonic | ERJ-8GEY0R00V | 0 Ω, 1/4W 1206 Chip resistor |
| 6 | 1 | R13 | Panasonic | ERJ-8GEYJ101V | 100 Ω, 1/4W 1206 Chip resistor |
| 7 | 1 | R10 | Panasonic | ERJ-8ENF2002V | 20 kΩ, 1/4W 1206 Chip resistor |
| 8 | 7 | R1, R2, R3, R4, R6, R12, R14 | Panasonic | ERJ-8ENF1002V | 10 kΩ, 1/4W 1206 Chip resistor |
| 9 | 1 | R9 | Bourns | 3214W-203E | 20 kΩ, BOURNS_32X4W Series 5T Pot |
| 10 | 1 | R11 | Bourns | 3214W-104E | 100 kΩ, BOURNS_32X4W Series 5T Pot |
| 11 | 1 | R3 | Panasonic | ERJ-8GEYJ104V | 100 kΩ, 1/4W 1206 Chip resistor |
| 12 | 1 | J6 | Samtec | TSM-105-01-T-DV | 5X2X0.1 10-pin 3A isolated power socket |
| 13 | 2 | J2, J4 | Samtec | TSM-110-01-S-DV-M | 10X2X.1, 20 Pin 0.025”sq SMT socket |
| 14 | 2 | J1, J5 | On-Shore Technology | ED555/3DS | 3-Pin terminal connector |
| 15 | 1 | U1 | Texas Instruments | DAC8534IPW | 16-bit, Quad voltage output, serial input DAC, TSSOP-16 |
| 16 | 1 | U2 | Texas Instruments | OPA627AU | 8-SOP(D) Precision Op Amp |
| 17 | 1 | U3 | Texas Instruments | REF02AU | 5 V, 8-SOP(D) precision voltage reference |
| 18 | 1 | U8 | Texas Instruments | OPA2132UA | 8-SOP(D) Dual precision op amp |
| 19 | 7 | TP1, TP2, TP3, TP4, TP5, TP6 TP7 | Mill-max | 2348-2-01-00-00-07-0 | Turret terminal test point |
| 20 | 2 | P2, P4 (see Note) | Samtec | SSW-110-22-S-D-VS-P | 20PIN .025”sq SMT terminal strips |
| 21 | 1 | P6 (see Note) | Samtec | SSW-105-F-D-VS-K | 3A Isolated 10-pin power header |
| 22 | 6 | W3, W7, W8, W9, W10, W15 | Molex | 22-03-2021 | 2 Position Jumper_ 0.1” spacing |
| 23 | 8 | W1, W2, W4, W5, W6, W11, W12, W13 | Molex | 22-03-2031 | 3 Position Jumper_ 0.1” spacing |

**Note:** P2, P4 & P6 parts are not shown in the schematic diagram. All the P-designated parts are installed on the bottom side of the PC Board, opposite the J-designated counterpart. Example, J2 is installed on the topside while P2 is installed on the bottom side, opposite of J2.

Chapter 3

# EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC, and how to interface the EVM to a specific host processor.

Refer to the DAC8534 data sheet (SBAS254), for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

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## 3.1 Factory Default Setting

The EVM board is set to to operate in bipolar, ±10 V mode of operation, in its default configuration from the factory as described in Table 3-1 .

*Table 3-1. Factory Default Jumper Setting*

| Reference | Jumper Position | Function |
|---|---|---|
| W1 | 1-2 | Analog supply for the DAC8534 is +5 V, (labeled as +5 VA). |
| W2 | 1-2 | DAC output A ($V_{OUT}A$) is routed to J4-2. |
| W3 | OPEN | $V_{REF}H$ is not routed to the inverting input of the op amp for voltage offset with gain of 2 output. |
| W4 | 1-2 | Onboard external buffered reference U3 is routed to $V_{REF}H$. |
| W5 | 1-2 | Negative supply rail of U2 Op Amp is supplied with $V_{SS}$. |
| W6 | 1-2 | $V_{REF}L$ is tied to AGND. |
| W7 | CLOSED | A0 pin is tied to DGND. |
| W8 | CLOSED | A1 pin is tied to DGND. |
| W9 | CLOSED | LDAC pin is tied to DGND. Software LDAC is used. |
| W10 | CLOSED | $\overline{EN}$ pin is tied to DGND. |
| W11 | 1-2 | DAC output B ($V_{OUT}B$) is routed to J4-4. |
| W12 | 1-2 | DAC output C ($V_{OUT}C$) is routed to J4-6. |
| W13 | 1-2 | DAC output D ($V_{OUT}D$) is routed to J4-8. |
| W15 | CLOSED | Output op amp, U2, is configured for a gain of 2. |
| J4 | 2-1 | DAC output A ($V_{OUT}A$) is connected to the noninverting input of the output op amp, U2. |

## 3.2 Host Processor Interface

The host processor basically drives the DAC, so the proper operation of the DAC depends on successful configuration between the host processor and the EVM board. In addition, properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for specific TI DSP starter kits, as well as an MSP430-based microprocessor as mentioned in chapter 1 of this manual. Using the interface card alleviates the tedious task of building customized cables, and allows easy configuration of a simple evaluation system.

The DAC8534 interfaces with any host processor capable of handling SPI protocols, or the popular TI DSP. For more information regarding the DAC8534 data interface, refer to the data sheet (SBAS254).

## 3.3 EVM Stacking

EVM stacking is possible if there is a need to evaluate two DAC8534 devices in yielding a total of eight channel outputs. A maximum of two EVMs are allowed, since the output terminal J4 dictates the number of DAC channels that can be connected without colliding. Table 3-2 shows how the DAC output channels are mapped into the output terminal J4, with respect to the jumper position of W2, W11, W12, and W13.

*Table 3-2. DAC Output Channel Mapping*

| Reference | Jumper Position | Function |
|---|---|---|
| W2 | 1-2 | DAC output A ($V_{OUT}A$) is routed to J4-2. |
| | 2-3 | DAC output A ($V_{OUT}A$) is routed to J4-10. |
| W11 | 1-2 | DAC output B ($V_{OUT}B$) is routed to J4-4. |
| | 2-3 | DAC output B ($V_{OUT}B$) is routed to J4-12. |
| W12 | 1-2 | DAC output C ($V_{OUT}C$) is routed to J4-6. |
| | 2-3 | DAC output C ($V_{OUT}C$) is routed to J4-14. |
| W13 | 1-2 | DAC output D ($V_{OUT}D$) is routed to J4-8. |
| | 2-3 | DAC output D ($V_{OUT}D$) is routed to J4-16. |

In order to allow exclusive control of each stacked EVM, the DAC8534 must have separate enable signals, $\overline{EN}$. This is accomplished by routing the enable signal of the first EVM through GPIO2 (P2/J2 pin 8), populating R27, and disconnecting R28. The second EVM should use the GPIO3 (P2/J2 pin12) for enable signal routing. Also, populate R28 and disconnect R27.

The LDAC signal can be shared to have a synchronous DAC output update. If you prefer the LDAC signal be separated from each EVM, the same concept described above should be implemented. Use GPIO0 and R25 for the first EVM, and GPIO1 and R26 for the second EVM.

## 3.4 The Output Op Amp

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation since the odd-numbered pins (J4-1 to J4-15) are tied together. The output op amp is set to a gain of 2 configuration by default. Nevertheless, the raw outputs of the DAC can be probed through the even-numbered pins of J4, the output terminal. This header also provides mechanical stability when stacking, or plugging into any interface card. In addition, it provides easy access for monitoring up to eight DAC channels when stacking two EVMs together. See section 3.3.

The following sections describe the different configurations of the output amplifier, U2.

### 3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC8534, although it may present some slight distortion because of the feedback resistor and capacitor. Users can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R7 and C11, and replacing them with the desired values. If desired, you can also simply remove R7 and C11 altogether and just solder a 0-Ω resistor in place of R7.

Table 3-3 shows the jumper settings for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

*Table 3-3. Unity Gain Output Jumper Settings*

| Reference | Jumper Setting | | Function |
|---|---|---|---|
| | Unipolar | Bipolar | |
| W3 | OPEN | OPEN | Disconnects $V_{REF}H$ from the inverting input of the op amp. |
| W5 | 2-3 | 1-2 | Supplies $V_{SS}$ to the negative rail of op amp or ties it to AGND. |
| W15 | OPEN | OPEN | Disconnects negative input of op amp from AGND. |

### 3.4.2 Output Gain of Two

There are two types of configurations that yield a gain of two output depending on the setup of jumpers W3 and W15. These configurations allow the user to choose whether the DAC output has $V_{REF}H$ as an offset, or not.

Table 3-4 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

*Table 3-4. Gain of Two Output Jumper Settings*

| Reference | Jumper Setting | | Function |
|---|---|---|---|
| | Unipolar | Bipolar | |
| W3 | Close | Close | Inverting input of the output op amp, U2, is connected to $V_{REF}H$ for use as its offset voltage with a gain of 2. W15 jumper must be open. |
| | Open | Open | $V_{REF}H$ is disconnected from the inverting input of the output op amp, U2. W15 jumper must be close. |
| W5 | 2-3 | 1-2 | Supplies power, $V_{SS}$, to the negative rail of op amp, U2, for bipolar mode, or ties it to AGND for unipolar mode. |
| W15 | Close | Close | Configures op amp, U2, for a gain of 2 output without a voltage offset. W3 jumper must be open. |
| | Open | Open | Inverting input of the op amp, U2, is disconnected from AGND. W3 jumper must be close. |

### 3.4.3 Capacitive Load Drive

Another output configuration option may be a requirement to drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable depending on the op amp configuration, gain, and load value. These are just few factors that can affect op amp stability performance, and should be considered when implementing designs for capacitive loads.

In unity gain, the OPA627 op amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier's ability to drive

even more capacitance, and by adding a load resistor even improves the capacitive load drive capability.

*Table 3-5. Capacitive Load Drive Ouptut Jumper Settings*

| Reference | Jumper Setting | | Function |
|---|---|---|---|
| | Unipolar | Bipolar | |
| W3 | Open | Open | $V_{REF}H$ is disconnected from the inverting input of the output op amp, U2. |
| W5 | 2-3 | 1-2 | Supplies $V_{SS}$ power to the negative rail of op amp U2 for bipolar mode, or ties it to AGND for unipolar mode. |
| W15 | Open | Open | Capacitive load drive output of DAC is routed to pin 1 of W15 jumper, and may be used as the output terminal. |

## 3.5 Optional Signal Conditioning Op Amp (U8B)

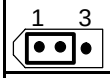
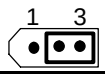
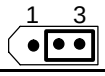
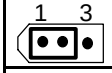
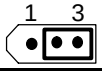
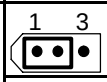
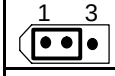
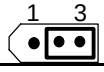
One part of the dual package op amp, OPA2132 (U8), is used for reference buffering (U8A) while the other is unused. This unused op amp (U8B) is available for whatever op amp circuit application the user desires to implement. The 1206 footprint for the resistors and capacitors surrounding the U8B op amp are not populated, but are available for easy configuration. TP6 and TP7 test points are also not installed, so it is up to the user as to how to connect the ± input signals to this op amp. No test point is available for the output due to space restriction, but a wire can be simply soldered to the output of the op amp via unused component pads connected to it.

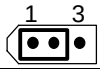
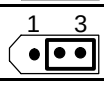
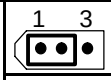
Once the op amp circuit design is realized, configuring the EVM becomes easy by simply populating the corresponding components that match the circuit design, and leaving all other unneeded component footprints unpopulated.

## 3.6 Jumper Setting

Table 3-6 shows the jumper setting configuration for a capacitive load drive.

*Table 3-6. Jumper Setting Function*

| Reference | Jumper Setting | Function |
|---|---|---|
| W1 |  | +5 V analog supply is selected for $AV_{DD}$. |
| |  | +3.3 V analog supply is selected for $AV_{DD}$. |
| W2 |  | Routes $V_{OUT}A$ to J4-2. |
| |  | Routes $V_{OUT}A$ to J4-10. |
| W3 |  | Disconnects $V_{REF}H$ to the inverting input of the output op amp, U2 |
| |  | Connects $V_{REF}H$ to the inverting input of the output op amp, U2 |
| W4 |  | Routes the adjustable, buffered, onboard +5 V reference to the $V_{REF}H$ input of the DAC8534. |
| |  | Routes the user supplied reference from TP1 or J4-20 to the $V_{REF}H$ input of the DAC8534. |
| W5 |  | Negative supply rail of the output op amp, U2, is powered by $V_{SS}$ for bipolar operation. |
| |  | Negative supply rail of the output op amp, U2, is tied to AGND for unipolar operation. |
| W6 |  | $V_{REF}L$ is tied to AGND. |
| |  | Routes the user supplied negative reference from TP2 or J4-18 to the $V_{REF}L$ input of the DAC8534. This voltage should be within the range of 0V to $V_{REF}H$. |
| W7 |  | A0 pin is set high through pull-up resistor, R4. A0 can be driven by GPIO5. |
| |  | A0 pin is set low. |
| W8 |  | A1 pin is set high through pull-up resistor, R3. A1 can be driven by GPIO4. |
| |  | A1 pin is set low. |
| W9 |  | LDAC pin is set high through pull-up resistor, R2. LDAC can be driven by GPIO0. |
| |  | LDAC pin is set low and DAC update is accomplished via software. |
| W10 |  | $\overline{EN}$ pin is set high through pull-up resistor, R1. /EN can be driven by GPIO2. |
| |  | $\overline{EN}$ pin is set low and DAC is enabled. |
| W11 |  | Routes $V_{OUT}B$ to J4-4. |
| |  | Routes $V_{OUT}B$ to J4-12. |

| Reference | Jumper Setting | Function |
|---|---|---|
| W12 |  | Routes $V_{OUT}C$ to J4-6. |
| |  | Routes $V_{OUT}C$ to J4-14. |
| W13 |  | Routes $V_{OUT}D$ to J4-8. |
| |  | Routes $V_{OUT}D$ to J4-16. |
| W15 |  | Disconnects the inverting input of the output op amp, U2, from AGND. |
| |  | Connects the inverting input of the output op amp, U2, to AGND for gain of 2. |

**Legend:**  Indicates the corresponding pins that are shorted or closed.

## 3.7 Schematic

A 17”X11” schematic diagram is an attachment to this document.

| Revision History | | |
|---|---|---|
| REV | ECN Number | Approved |
| | | |
| | | |
| | | |
| | | |

U1 DAC7574/8534/8574
AVDD IO_V/DVDD VrefH VrefL A3/LDAC A2/EN A1 A0 SDA/Din SCL/SCLK LDAC/SYNC GND VoutA VoutB VoutC VoutD
GPIO0 R25 0 (LDAC)
GPIO1 R26 0 (A3)
GPIO2 R27 0 (EN)
GPIO3 R28 0 (A2)
GPIO4 R38 0 (A1)
GPIO5 R39 0 (A0)
SDI R15 440/0
SCLK R16 440/0
FSX (SYNC) R29 0
GPIO0 (LDAC) R30 0
R1 10K R2 10K R3 10K R4 10K R5 3K R7 3K
W10 W9 W8 W7
W1 +5VA +3.3VA AVDD
C1 0.1µF C5 10µF C6 10µF C2 0.1µF
VDD
VrefH VrefL
OUT_A OUT_B OUT_C OUT_D
W2 W11 W12 W13
OUT_A1 OUT_A2 OUT_B1 OUT_B2 OUT_C1 OUT_C2 OUT_D1 OUT_D2
-REFin +REFin
J4 OUTPUT HEADER

U2_+IN R8 0 W3 U2_-IN R14 10K VrefH
U2 Op Amp U2_OUT R13 100 TP3 VOUT
VCC C9 1µF VSS W5 C10 1µF R6 10K C12 1nF W15 R12 10K

U3 REF02AU(8)
TRIM OUT V+ TEMP NC NC GND NC
Tantalum C11 10µF C3 0.1µF
R9 20K R11 100K R10 20K R17 0
TP4
U8A OPA2227UA
C7 0.1µF
W4 W6 VrefH VrefL
+REFin -REFin TP1 TP5 TP2
EXTERNAL REFERENCE
NOTE: Voltage range of -REFin input should not exceed 0 - VrefH.

TP6 +Vin TP7 -Vin
R18 NI R19 NI R20 NI R21 NI R22 NI R23 NI R24 NI
C8 NI C13 NI
U8B OPA2227UA

J2 Serial Header
R31 R32 R33 0 CLKX CLKR FSX FSR DX DR
GPIO0 (LDAC) GPIO1 (A3) GPIO2 (EN) GPIO3 (A2) GPIO4 (A1) SCL SDA
(A0) GPIO5
DX R36 0 SDI R34 0 SCLK R35 0 CLKX R37 0

J6 +3.3VD +1.8VD +5VA VCC VSS -5VA +3.3VA VDD
J1 VSS VCC
J5 VDD +5VA

VCC = +15V Analog
VDD = +2.7V to +5.0V Digital
VSS = 0V to -15V Analog

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

| | | | |
|---|---|---|---|
| Title: DAC8534_74 EVM | | | |
| Engineer: J. PARGUIAN | DOCUMENTCONTROL # 6447711 | | REV: A |
| Drawn By: | DATE: 13-Jun-2003 | SIZE: | SHEET: OF: 1 |
| FILE: DAC8534 RevA.Sch | | | |