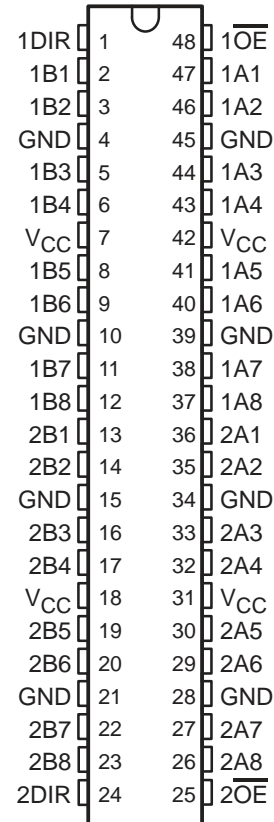


# SN54ABT16640, SN74ABT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS107C – APRIL 1992 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16640 . . . WD PACKAGE  
SN74ABT16640 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16640 are inverting 16-bit transceivers designed for asynchronous communication between data buses.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable ( $1\overline{OE}$  and  $2\overline{OE}$ ) inputs can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16640 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16640 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each 8-bit section)

| INPUTS          |     | OPERATION                    |
|-----------------|-----|------------------------------|
| $\overline{OE}$ | DIR |                              |
| L               | L   | $\overline{B}$ data to A bus |
| L               | H   | $\overline{A}$ data to B bus |
| H               | X   | Isolation                    |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

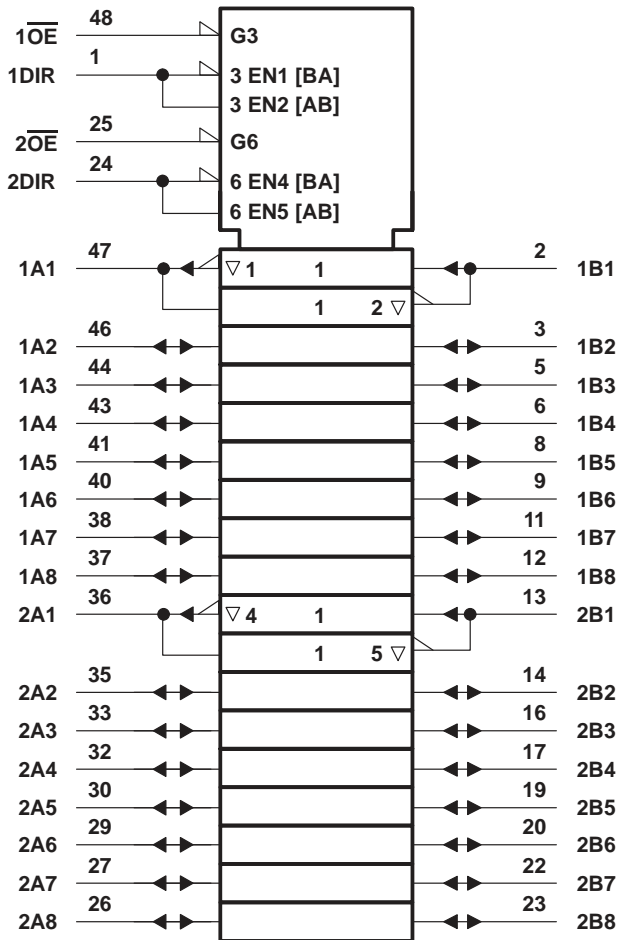
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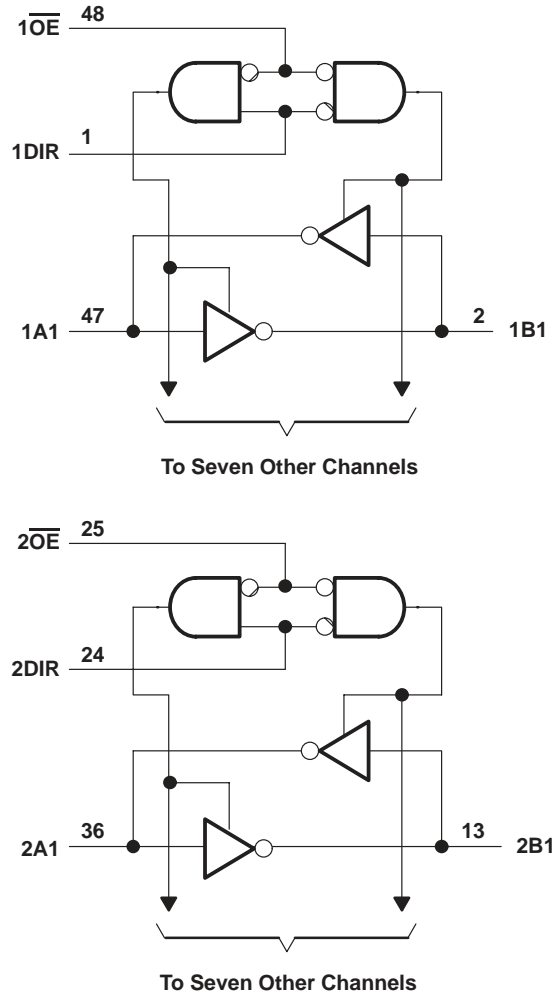
# SN54ABT16640, SN74ABT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$ .....  | -0.5 V to 7 V   |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....                | -0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ ..... | -0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT16640 .....            | 96 mA           |
| SN74ABT16640 .....  | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                               | -18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                              | -50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....        | 89°C/W          |
| DL package .....  | 94°C/W          |
| Storage temperature range, $T_{stg}$ .....                                      | -65°C to 150°C  |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



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**SN54ABT16640, SN74ABT16640**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

|                 |                                    | SN54ABT16640    |                 | SN74ABT16640 |                 | UNIT |
|-----------------|------------------------------------|-----------------|-----------------|--------------|-----------------|------|
|                 |                                    | MIN             | MAX             | MIN          | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5             | 5.5             | 4.5          | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2               |                 | 2            |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |                 | 0.8             |              | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      | 0               | V <sub>CC</sub> | 0            | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          |                 | -24             |              | -32             | mA   |
| I <sub>OL</sub> | Low-level output current           |                 | 48              |              | 64              | mA   |
| Δt/Δv           | Input transition rise or fall rate | Outputs enabled |                 | 10           | 10              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -55             | 125             | -40          | 85              | °C   |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



**SN54ABT16640, SN74ABT16640**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER          | TEST CONDITIONS   | T <sub>A</sub> = 25°C  |                  |               | SN54ABT16640 |          | SN74ABT16640 |          | UNIT |    |
|--------------------|---|--|------------------|---------------|--------------|----------|--------------|----------|------|----|
|                    |   | MIN  | TYP†             | MAX           | MIN          | MAX      | MIN          | MAX      |      |    |
| V <sub>IK</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA              |  |                  | -1.2          |              | -1.2     |              | -1.2     | V    |    |
| V <sub>OH</sub>    | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA              |  |                  | 2.5           |              | 2.5      |              | 2.5      | V    |    |
|                    | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                |  |                  | 3             |              | 3        |              | 3        |      |    |
|                    | V <sub>CC</sub> = 4.5 V                                       | I <sub>OH</sub> = -24 mA   |                  | 2             |              | 2        |              |          |      |    |
|                    |   | I <sub>OH</sub> = -32 mA   |                  | 2*            |              |          |              | 2        |      |    |
| V <sub>OL</sub>    | V <sub>CC</sub> = 4.5 V                                       | I <sub>OL</sub> = 48 mA  |                  |               |              | 0.55     |              | 0.55     | V    |    |
|                    |   | I <sub>OL</sub> = 64 mA  |                  |               |              | 0.55*    |              | 0.55     |      |    |
| V <sub>hys</sub>   |   |  |                  | 100           |              |          |              |          | mV   |    |
| I <sub>I</sub>     | Control inputs  | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                     |                  |               | ±1           |          | ±1           |          | ±1   | µA |
|                    | A or B ports  |  |                  |               | ±100         |          | ±100         |          | ±100 |    |
| I <sub>OZH</sub> ‡ | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V               |  |                  | 50            |              | 50       |              | 50       | µA   |    |
| I <sub>OZL</sub> ‡ | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V               |  |                  | -50           |              | -50      |              | -50      | µA   |    |
| I <sub>off</sub>   | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V |  |                  | ±100          |              |          |              | ±100     | µA   |    |
| I <sub>CEX</sub>   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V               | Outputs high   |                  |               | 50           | 50       |              | 50       | µA   |    |
| I <sub>O</sub> §   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V               |  |                  | -50 -100 -180 |              | -40 -180 |              | -50 -180 | mA   |    |
| I <sub>CC</sub>    | A or B ports  | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high     |               |              | 2        |              | 2        | 2    | mA |
|                    |   |  | Outputs low      |               |              | 32       |              | 32       | 32   |    |
|                    |   |  | Outputs disabled |               |              | 2        |              | 2        | 2    |    |
| ΔI <sub>CC</sub> ¶ | Data inputs   | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | Outputs enabled  |               |              | 1        |              | 1.5      | 1    | mA |
|                    |   |  | Outputs disabled |               |              | 0.05     |              | 0.05     | 0.05 |    |
|                    | Control inputs  | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                  |               | 1.5          |          | 1.5          |          | 1.5  |    |
| C <sub>i</sub>     | Control inputs  | V <sub>I</sub> = 2.5 V or 0.5 V  |                  |               | 3            |          |              |          | pF   |    |
| C <sub>io</sub>    | A or B ports  | V <sub>O</sub> = 2.5 V or 0.5 V  |                  |               | 8            |          |              |          | pF   |    |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT16640, SN74ABT16640**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | SN54ABT16640                          |     |     |     | UNIT |     |
|-----------|-----------------|-------------|---------------------------------------|-----|-----|-----|------|-----|
|           |                 |             | $V_{CC} = 5$ V,<br>$T_A = 25^\circ$ C |     |     | MIN |      | MAX |
|           |                 |             | MIN                                   | TYP | MAX |     |      |     |
| $t_{PLH}$ | A or B          | B or A      | 0.5                                   | 2.5 | 4.1 | 0.5 | 5.2  | ns  |
| $t_{PHL}$ |                 |             | 0.5                                   | 2.8 | 4   | 0.5 | 4.5  |     |
| $t_{PZH}$ | $\overline{OE}$ | A or B      | 0.5                                   | 3.5 | 5.2 | 0.5 | 6.2  | ns  |
| $t_{PZL}$ |                 |             | 0.5                                   | 3.9 | 6   | 0.5 | 7.4  |     |
| $t_{PHZ}$ | $\overline{OE}$ | A or B      | 0.5                                   | 3.8 | 6.8 | 0.5 | 7.9  | ns  |
| $t_{PLZ}$ |                 |             | 0.5                                   | 3   | 4.5 | 0.5 | 5    |     |

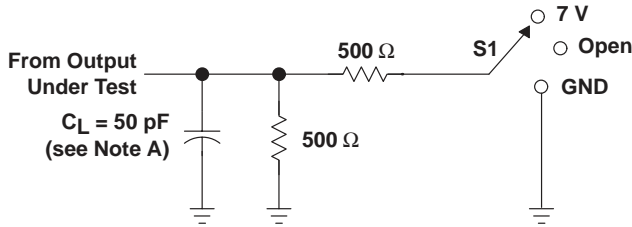
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | SN74ABT16640                          |     |     |     | UNIT |     |
|-----------|-----------------|-------------|---------------------------------------|-----|-----|-----|------|-----|
|           |                 |             | $V_{CC} = 5$ V,<br>$T_A = 25^\circ$ C |     |     | MIN |      | MAX |
|           |                 |             | MIN                                   | TYP | MAX |     |      |     |
| $t_{PLH}$ | A or B          | B or A      | 1                                     | 2.5 | 3.4 | 1   | 4.3  | ns  |
| $t_{PHL}$ |                 |             | 1.1                                   | 2.8 | 3.6 | 1.1 | 3.9  |     |
| $t_{PZH}$ | $\overline{OE}$ | A or B      | 1.2                                   | 3.5 | 4.5 | 1.2 | 5.5  | ns  |
| $t_{PZL}$ |                 |             | 1.5                                   | 3.9 | 5   | 1.5 | 6.3  |     |
| $t_{PHZ}$ | $\overline{OE}$ | A or B      | 1.8                                   | 3.8 | 4.8 | 1.8 | 6.3  | ns  |
| $t_{PLZ}$ |                 |             | 1.5                                   | 3   | 3.9 | 1.5 | 4.2  |     |

**SN54ABT16640, SN74ABT16640**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

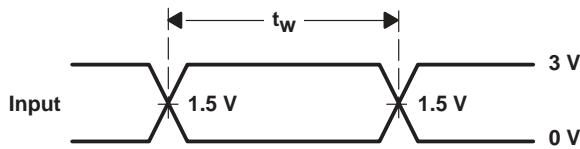
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**PARAMETER MEASUREMENT INFORMATION**

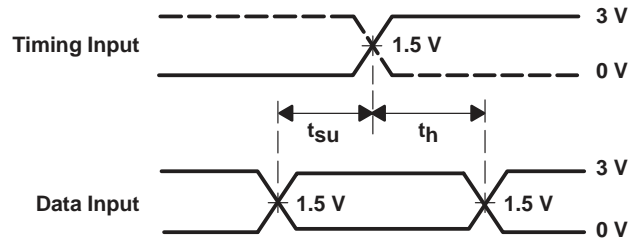


**LOAD CIRCUIT**

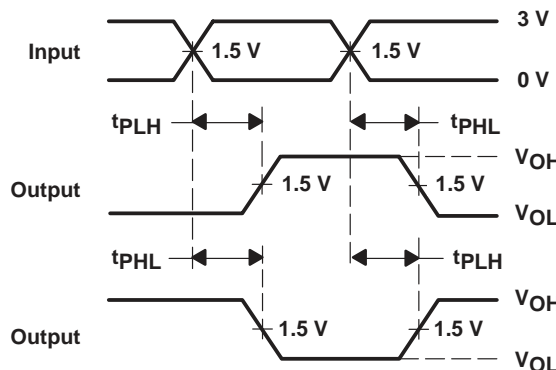
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



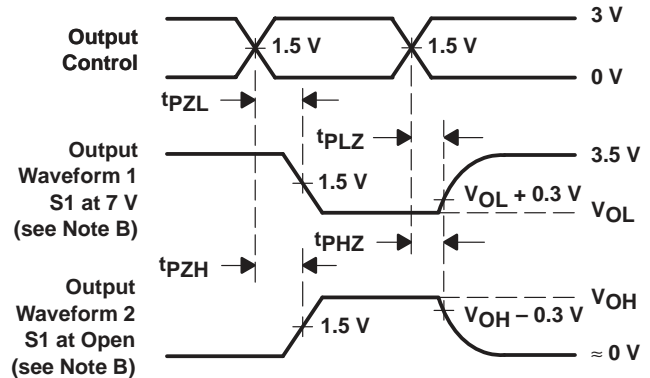
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ABT16640DGGR | ACTIVE        | TSSOP        | DGG             | 48   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16640                | <a href="#">Samples</a> |
| SN74ABT16640DL   | ACTIVE        | SSOP         | DL              | 48   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16640                | <a href="#">Samples</a> |
| SN74ABT16640DLR  | ACTIVE        | SSOP         | DL              | 48   | 1000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16640                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

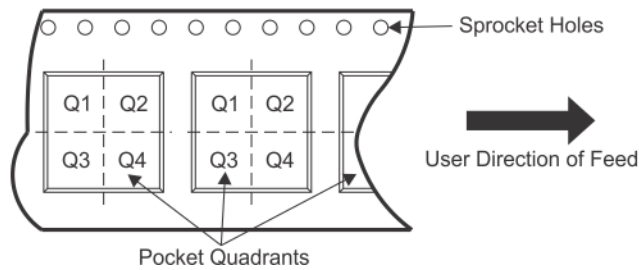
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16640DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74ABT16640DLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16640DGGR | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ABT16640DLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |

**TUBE**

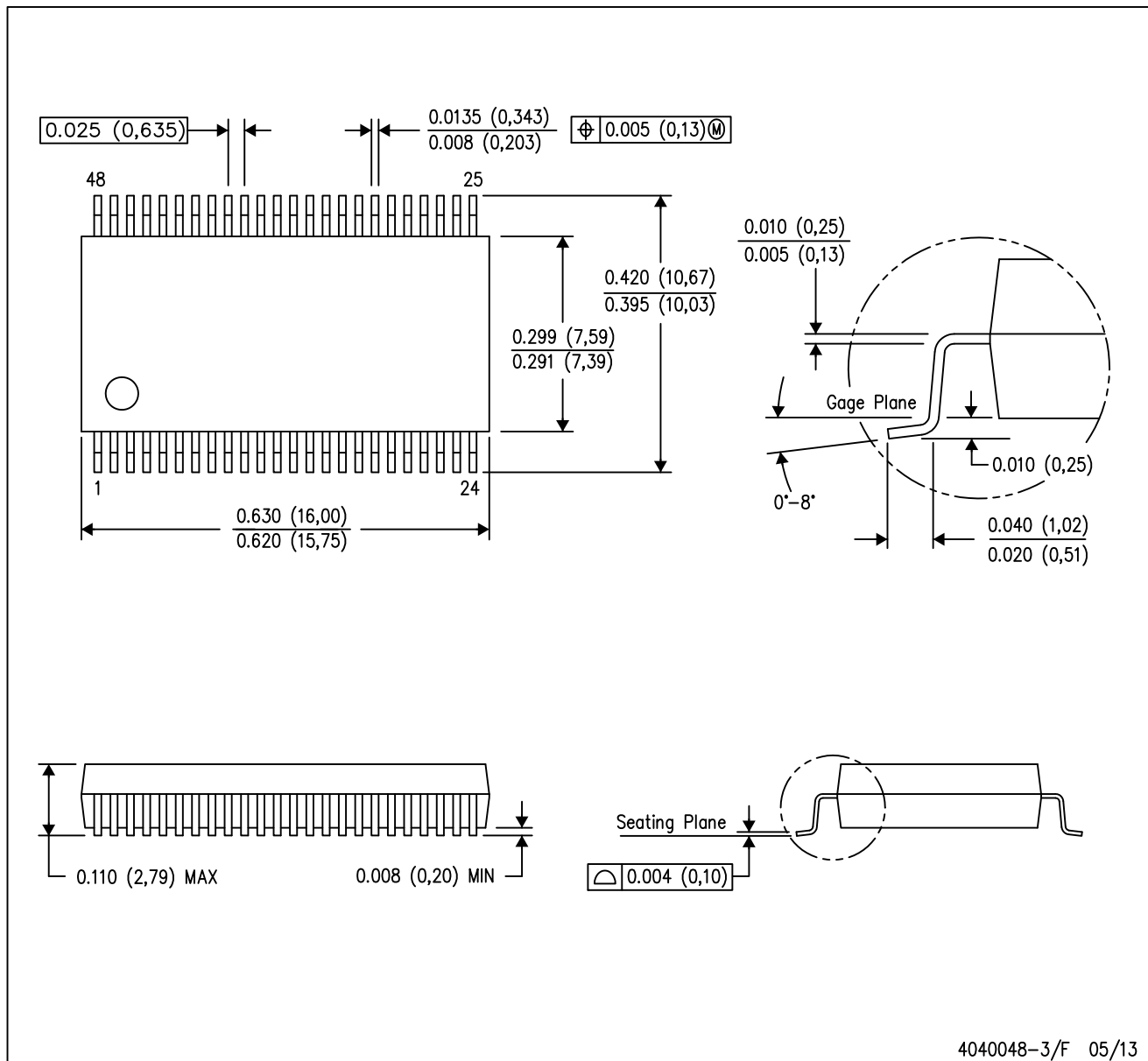

\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ABT16640DL | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |

# MECHANICAL DATA

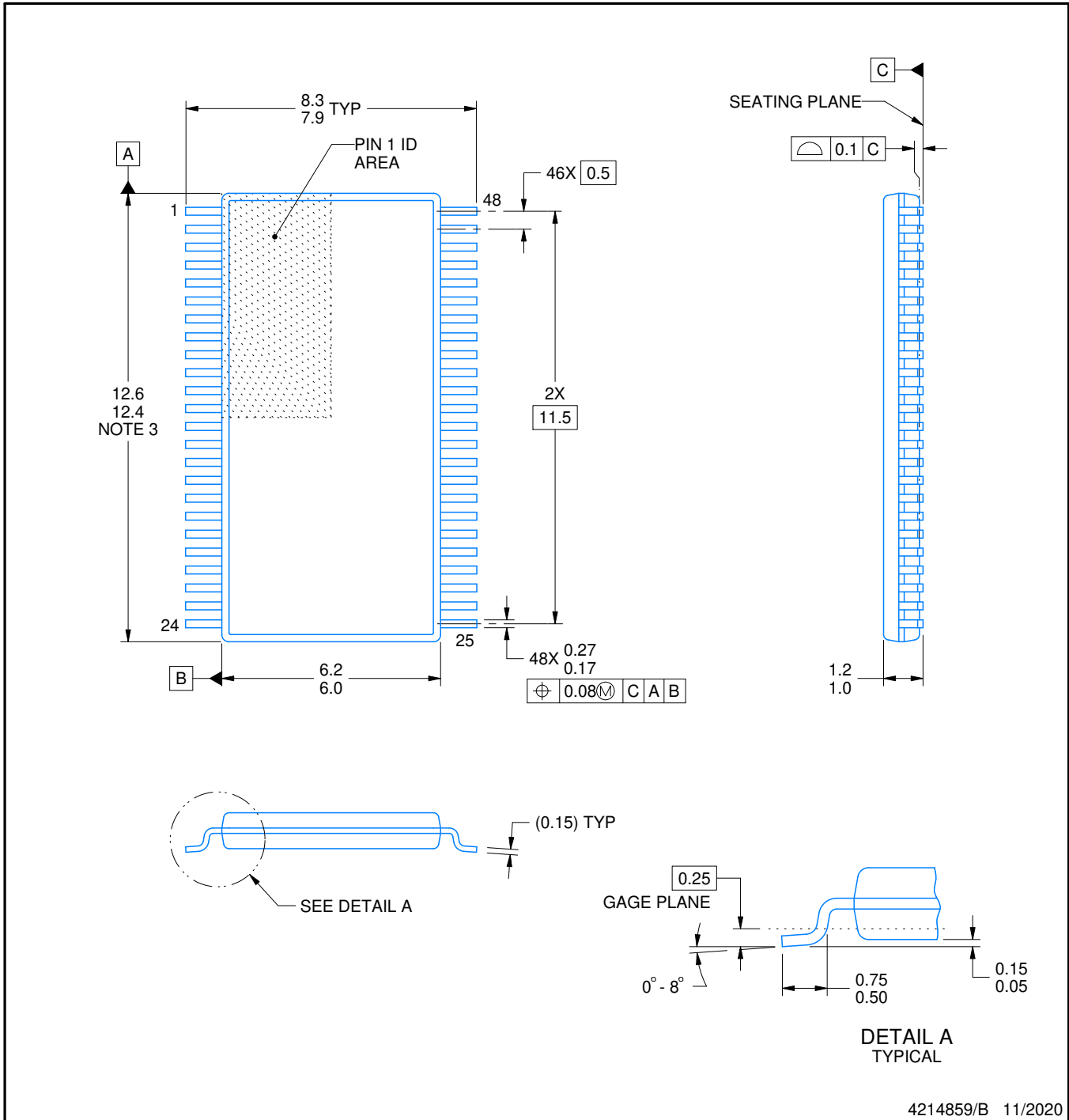
DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



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NOTES:

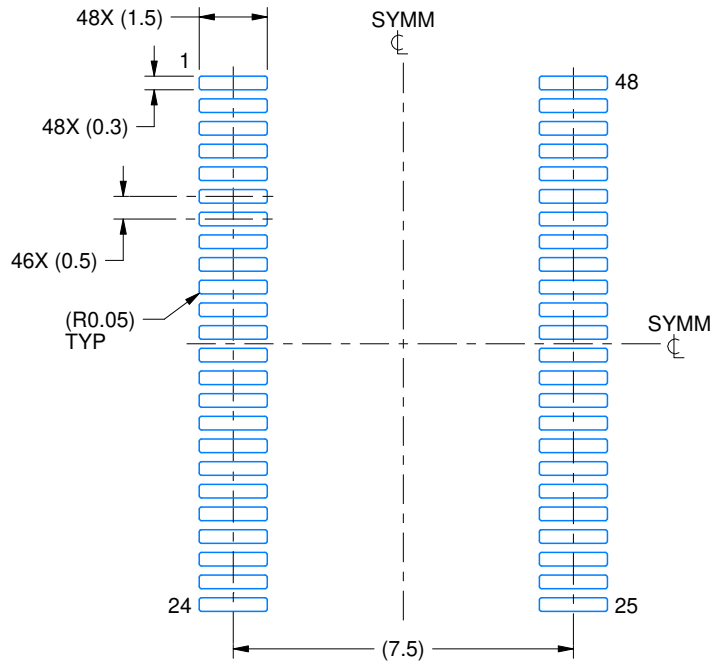
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

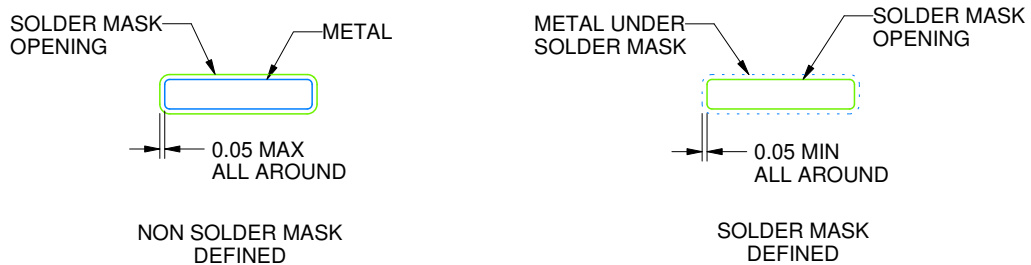
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

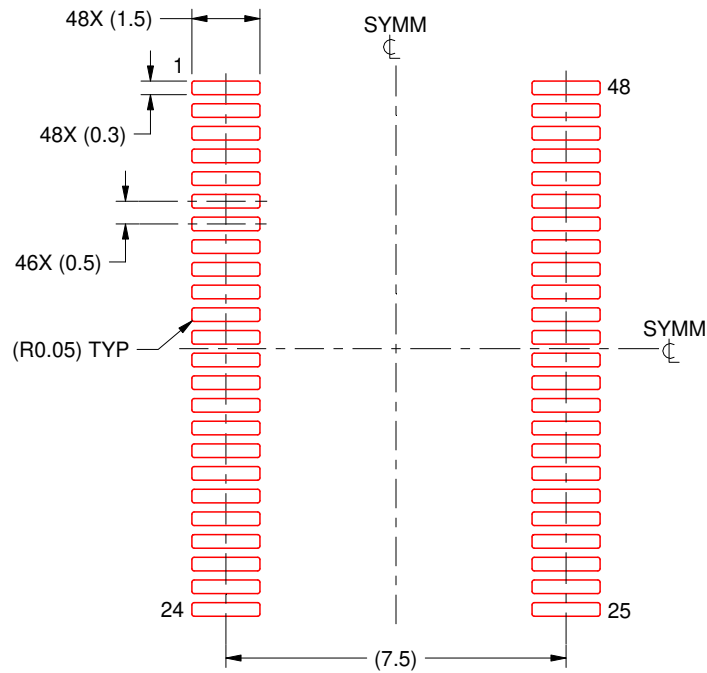
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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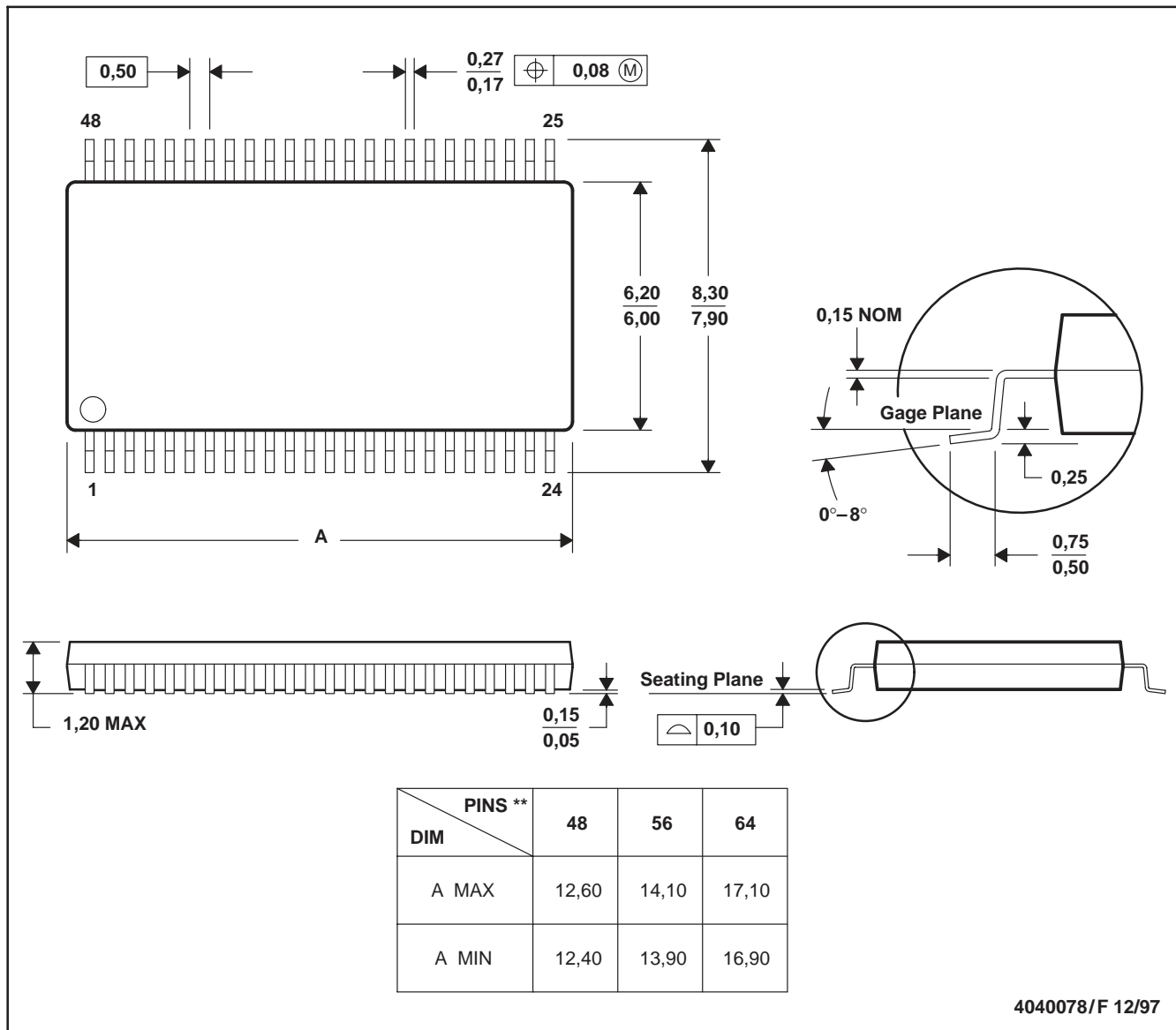
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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