System Clock for Embedded AMDTM based Systems

•

Recommended Application:

AMD M690T/780E systems

Output Features:

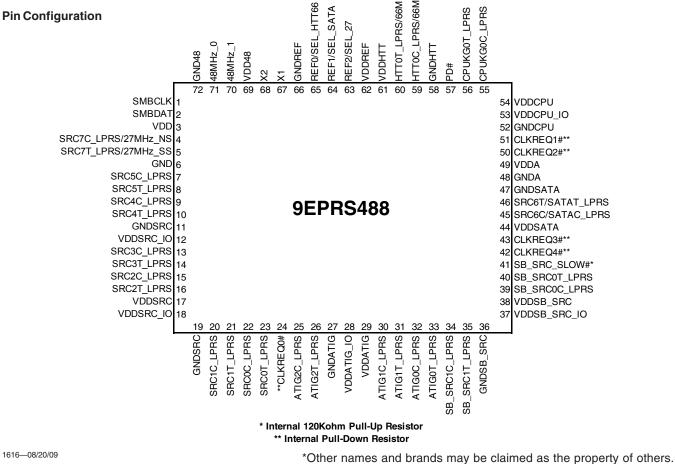
- Integrated series resistors on all differential outputs.
- 1 Greyhound compatible low-power CPU pair
- 6 low-power differential SRC pairs
- 2 low-power differential chipset SouthBridge SRC pairs
- 1 Selectable low-power differential 100MHz non-spread SATA/ SRC output
- 1 Selectable low-power differential SRC / 27MHz Single Ended output
- 1 Selectable HT3 100MHz low-power differential hypertransport clock / HT66MHz Single Ended output
- 2 48MHz USB clock
- 3 14.318MHz Reference clock
- 3 low-power differential ATIG pairs
- 5- Dedicated CLKREQ# pins

Kev Specifications:

- CPU outputs cycle-to-cycle jitter < 150ps
- SRC outputs cycle-to-cycle jitter < 125ps
- SB_SRC outputs cycle-to-cycle jitter < 125ps
- +/- 100ppm frequency accuracy on CPU, SRC, ATIG
- Oppm frequency accuracy on 48MHz

Features/Benefits:

- **Power Saving Features:** SB_SRC_SLOW# input to throttle Chipset clocks (SB_SRC) to 80% of normal. Optional Separate supply rail for SRC low Voltage I/O - ~33% power saving when 1.5V is used for this rail
 - Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus .
- External crystal load capacitors for maximum frequency accuracy



Pin Description

	Description		
PIN #		PIN TYPE	DESCRIPTION
1	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
2	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
3	VDD	PWR	Power supply for SRC7/27MHz
4	SRC7C_LPRS/27MHz_NS	OUT	True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
7		001	series resistor needed)/27MHz 3.3V Single-ended non-spread output for discrete graphics
5	SRC7T_LPRS/27MHz_SS	OUT	Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
5	SHC/1_EFH3/27MH2_33	001	ohm series resistor needed)/27MHz 3.3V Single-ended spreading output for discrete graphics
6	GND	GND	Ground pin for SRC7/27MHz
7	SRC5C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
'	SHUSU_LFHS	001	ohm series resistor needed)
8	SRC5T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
0	SHOST_EFHS	001	series resistor needed)
9	SRC4C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
9	311040_EF113	001	ohm series resistor needed)
10	SRC4T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
10	Sh041_LFh3	001	series resistor needed)
11	GNDSRC	GND	Ground pin for the SRC outputs
12	VDDSRC_IO	PWR	Power supply for differential SRC outputs, nominal 1.05V to 3.3V
13	SRC3C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
13	SRU3U_LPRS	001	ohm series resistor needed)
14			True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
14	SRC3T_LPRS	OUT	series resistor needed)
4.5			Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
15	SRC2C_LPRS	OUT	ohm series resistor needed)
4.0	ODOOT I DDO		True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
16	SRC2T_LPRS	OUT	series resistor needed)
17	VDDSRC	PWR	Supply for SRC core, 3.3V nominal
18	VDDSRC_IO	PWR	Power supply for differential SRC outputs, nominal 1.05V to 3.3V
19	GNDSRC	GND	Ground pin for the SRC outputs
			Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
20	SRC1C_LPRS	OUT	ohm series resistor needed)
			True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
21	SRC1T_LPRS	OUT	series resistor needed)
			Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33
22	SRC0C_LPRS	OUT	ohm series resistor needed)
			True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
23	SRC0T_LPRS	OUT	series resistor needed)
			Clock Request pin for SRC0 outputs. If output is selected for control, then that output is controlled as
24	**CLKREQ0#	IN	follows:
			0 = enabled, 1 = Low-Low
		_	Complementary clock of low-power differential push-pull PCI-Express pair with integrated series
25	ATIG2C_LPRS	OUT	resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
		-	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no
26	ATIG2T_LPRS	OUT	50ohm shunt resistor to GND and no 33 ohm series resistor needed)
27	GNDATIG	GND	Ground pin for the ATIG outputs
28	VDDATIG_IO	PWR	Power supply for differential ATIG outputs, nominal 1.05V to 3.3V
29	VDDATIG	PWR	Power supply for ATIG core, nominal 3.3V
			Complementary clock of low-power differential push-pull PCI-Express pair with integrated series
30	ATIG1C_LPRS	OUT	resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
			True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no
31	ATIG1T_LPRS	OUT	500hm shunt resistor to GND and no 33 ohm series resistor needed)
			Complementary clock of low-power differential push-pull PCI-Express pair with integrated series
32	ATIG0C_LPRS	OUT	
			resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
33	ATIG0T_LPRS	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no
			50ohm shunt resistor to GND and no 33 ohm series resistor needed)
34	SB_SRC1C_LPRS	OUT	Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor
<u> </u>			to GND and no 33 ohm series resistor needed
35	SB_SRC1T_LPRS	OUT	True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND
-		0115	and no 33 ohm series resistor needed
36	GNDSB_SRC	GND	Ground pin for the SB_SRC outputs

Pin Description (Continued)

41 SB_SRC_SLOW#* IN lower frequency to save power. The default (over frequency is 80 MHz. 0 = Siow Down, 1 = normal operation. Clock Request pin for SRC45 outputs. If output is selected for control, then that output is controlled and the selected for control, then that output is controlled and 0 = enabled, 1 = Low-Low 42 CLKREC4#** IN Information of SRC3 outputs. If output is selected for control, then that output is controlled and 0 = enabled, 1 = Low-Low 44 VDDSATA PVM Power supply for SATA core logic, nominal 3.3V 45 SRCcC/SATAC_LPRS OUT The dock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND no 33 ohm series resistor needed) 46 SRCcC/SATAC_LPRS OUT The dock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND no 33 ohm series resistor needed) 47 ONDA GND Ground pin for the RC outputs 48 GNDA GND Ground pin for the RC outputs 50 CLKREQ2#** IN Clock Request pin tor SRC2 outputs. It output is selected for control, then that output is controlled a lottors: 51 CLKREQ2#** IN Clock Request pin for SRC2 outputs. It outputs is selected for control, then that output is controlled a lottors: 52 CLKREQ2#** IN Clock Request pin for SRC2 outputs. It outputs		Description (Cont		
38 VDDSR_SRC FWR Supply for SB SRC PLL core, 33 vnminal 39 SR_SRC0C_LPRS OUT Complement clock of low power differential Chipset-Chipset SRC clock pair. (no 500hm shunt resistor to and no 33 ohm series resistor needed 40 SB_SRC0T_LPRS OUT The dock of low power differential Chipset-Chipset SRC clock pair. (no 500hm shunt resistor to and no 33 ohm series resistor needed 41 SB_SRC_SLOW# IN When low in series resistor needed 42 CLKREQ4#** IN Clock Request pin for SRC45 outputs. If output is selected for control, then that output is controlled a low frequency is 80 MHz. 43 CLKREQ4#** IN Clock Request pin for SRC45 outputs. If output is selected for control, then that output is controlled a low power differential SRC GATA clock pair. (no 50ohm shunt resistor to GNL on some sensitient needed) 44 VDDSATA PWR Power supply for SRTA core logic, nominal 3 SV 45 SRC607SATAC_LPRS OUT no 33 ohm series resistor needed) The dock of low power differential SRC dlock pair. (no 50ohm shunt resistor to GNL and no 33 ohm series resistor needed) 46 SRC607SATAC_LPRS OUT no 33 ohm series resistor needed) Corece and the net Analog Core 47 GNDSATA GND Gound for ne Analog Core				
39 SR_SRC0C_LPRS OUT Complement lock of low power differential Chipset-0-Chipset SRC clock pair. (no 500hm shunt resistor to 30 hm series resistor needed 40 SR_SRC0_LPRS OUT The dock of low power differential Chipset-0-Chipset SRC clock pair. (no 500hm shunt resistor to 30 hm series resistor needed 41 SR_SRC_SLOW#* IN Non to 33 hm series resistor needed 42 CLREC4#** IN Non tereation power. The default lower frequency is as 00 MHz. 42 CLREC4#** IN Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled a 43 CLKREC4#** IN Note the requency to asset of RC45 outputs. If output is selected for control, then that output is controlled a 44 VDDSATA PWR Power supply of SRC4 outputs. If output is selected for control, then that output is controlled a 45 SRC6C6XTAL_LPRS OUT True clock of low power differential SRC SICA clock pair. (no 500hm shunt resistor to GNL no 33 on term sensistor needed) 46 SRC6TATAT_LPRS OUT True clock of low power differential SRC flock pair. (no 500hm shunt resistor to GNL no 33 on term sensistor needed) 47 ODDA PWR Power state and and cloce 48 NDCA				
193 193 <td>38</td> <td>VDDSB_SRC</td> <td>PWR</td> <td></td>	38	VDDSB_SRC	PWR	
40 SB_SCCU_LINS UVI and no 33 ohm series resistor needed 41 SB_SRC_SLOWF IN Idver frequency to save power. The default lowr frequency is 80 MHz. 42 CLKREC4II** IN follows: o = show Down, 1 = normal operation. 42 CLKREC4II** IN follows: o = enabled, 1 = Low-Low 43 CLKREC3I*** IN follows: o = enabled, 1 = Low-Low 44 VDDSATA PVFR Power supply for SATA core logic, nominal 3.3V 45 SRC6CRATAC_LPRS OUT To clock flow power differential SRC SATA clock pair. (no 50ohm shunt resistor to GND na 30 oh series resistor needed) 46 SRC6TSATAT_LPRS OUT To clock flow power differential SRC clock pair. (no 50ohm shunt resistor to GND na 30 oh series resistor needed) 47 GNDA GND Ground pin for the SRC cluputs. fouputs. 48 GNDA GND Ground pin for the SRC cluputs. fouputs. fouputs. 50 CLKREC2I** IN Glows: 0 = enabled, 1 = Low-Low 0 0 = enabled, 1 = Low-Low 61 CLKREC2I** IN Glows: 0 = enabled, 1 = Low-Low 0 0 = enabled, 1 = Low-Low	39	SB_SRC0C_LPRS	OUT	to GND and no 33 ohm series resistor needed
41 SB_SRC_SLOW# IN lower frequency to save power. The default (over frequency is 80 MHz. 0 = 500 Dom, 1 = normal operation. Clock Request pin for SRC45 outputs. If output is selected for control, then that output is controlled a CLREC04#** 42 CLREC04#** IN Clock Request pin for SRC45 outputs. If output is selected for control, then that output is controlled a follows: 0 = enabled, 1 = Low-Low 0 = enabled, 1 = Low-Low 0 = anabled, 1 = Low	40	SB_SRC0T_LPRS	OUT	
Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled a 42 CLKREQ4#** IN N follows: 0 = enabled.1 = Low-Low 43 CLKREQ3#** IN follows: 0 = enabled.1 = Low-Low 44 VDDSATA PWR Power supply for SATC outputs. If output is selected for control, then that output is controlled a 45 SRCcC/SATAC_LPRS OUT Complement lock of low power differential SRC/GATA clock pair. (no 50ohm shunt resistor to GND and no 33 oh 46 SRCcT/SATA_LPRS OUT True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 oh 47 GNDATA GND Ground pin for the Analog Core Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a 48 GNDA GND Ground pin for the Analog Core 0 = enabled, 1 = Low-Low 50 CLKREQ2#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a 51 CLKREQ2#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a 52 GNDCPU	41	SB_SRC_SLOW#*	IN	
CLKRE03#** Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled a 43 CLKRE03#** IN No 44 VDDSATA PWR Power supply for SATA core logic, nominal 3.3V 45 SRC6C/SATAC_LPRS OUT Complement clock of low power differential SRC dock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed). 46 SRC6T/SATAT_LPRS OUT The clock of low power differential SRC dock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed). 47 GNDSATA GND Ground pin for the SRC outputs. Thoutput is selected for control, then that output is controlled a 48 GNDA GND Ground pin for SRC1 outputs. If output is selected for control, then that output is controlled a 50 CLKRE02#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a 51 CLKRE01#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a 52 GNDCPU GND Ground pin for the CPU outputs. If output is selected for control, then that output is controlled a 54 VDDCPU GND Ground pin fo	42	CLKREQ4#**	IN	Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows:
45 SRC6C/SATAC_LPRS OUT Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GNL no 3 ohm series resistor needed). 46 SRC6T/SATAT_LPRS OUT The clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GNL no 3 ohm series resistor needed). 47 GNDSATA GND Ground pin for the SRC outputs 48 GNDA GND Ground pin for the Analog Core 49 VDDA PWR 3.3V Power for the Analog Core 50 CLKRE02#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a follows: 51 CLKRE01#** IN follows: 0 = enabled, 1 = Low-Low 52 GNDCPU GND Ground pin for the CPU outputs follows: 53 VDDCPU PWR Supply for CPU core, 3.3 nominal follow-power differential push-pull AMD K8 "Greyhound" clock with integrate series resistor needed) 54 VDDCPU PWR Supply for CPU core, 3.3 nominal for wpower differential push-pull AMD K8 "Greyhound" clock with integrated series resistor needed) 56 CPUKGO_LPRS OUT Forererereference clock / 3.3 vorentrefie	43	CLKREQ3#**	IN	Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows:
45 SHCBC/SATAC_LPHS OUT no 33 ohm series resistor needed) 46 SRC6T/SATAT_LPRS OUT Thre clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 oh series resistor needed) 47 GNDSATA GND Ground p in for the SRC cuputs 48 GNDA GND Ground p in for the SRC cuputs. If output is selected for control, then that output is controlled a follows: 49 VDDA PWR 3.3V Power for the Analog Core 50 CLKREC2#** IN follows: 0 = enabled, 1 = Low-Low 51 CLKREQ1#** IN follows: 0 = enabled, 1 = Low-Low 52 GNDCPU GND Ground p in for the CPU outputs. If output is selected for control, then that output is controlled a follows: 53 VDDCPU GND Ground p in for the CPU outputs. To utputs. If output is selected for control, then that output is controlled a follows: 54 VDDCPU GND Ground p in for the CPU outputs. To utputs. To utputs. 55 CDUCPU GND Ground p in for the CPU outputs. To utputs. To utputs. 54 VDDCPU PVM Supreverown, 1 = normal opower differential puts-pull AMD K8 "Greyhou	44	VDDSATA	PWR	Power supply for SATA core logic, nominal 3.3V
40 SNC017SATA_CHRS OUT Series resistor needed) 47 GNDSATA GND Ground pin to the SRC outputs 48 GNDA GND Ground pin to the SRC outputs. If output is selected for control, then that output is controlled a follows: 50 CLKREQ2#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 51 CLKREQ1#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 52 GRNCPU GRUA Ground pin for the CPU outputs. If output is selected for control, then that output is controlled a follows: 53 CLKREQ1#** IN Bollows: 0 = enabled, 1 = Low-Low 54 VDDCPU GRUA Ground pin for the CPU outputs. Ground pin for the CPU outputs, nominal 1.05V to 3.3V 54 VDDCPU PWR Supply for CPU core, 3.3V nominal 0.5V to 3.3V 55 CPUKG0C_LPRS OUT True signal of Iow-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor (no 33 ohm series resistor needed) 56 CPUKG0C_LPRS OUT True signal of Iow-power differential push-pull MAD K8 "Greyhound" clock with integrated series resistor (no 50 ohm shuru resistor to 6ND and no 33 ohm series re	45	SRC6C/SATAC_LPRS	OUT	Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)
47 GNDSATA GND Ground pin for the SRC outputs 48 GNDA GND Ground for the Analog Core 49 VDDA PWR 3.3V Power for the Analog Core 50 CLKREQ2#** IN Globs Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a follows: 61 CLKREQ1#** IN Globs Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 62 GNDCPU GND Ground pin for the CPU outputs. If outputs is selected for control, then that output is controlled a follows: 63 VDDCPU GND Ground pin for the CPU outputs. If outputs is selected for control, then that output is controlled a follows: 54 VDDCPU GND Ground pin for the CPU oren, 3.3V nominal If outputs, nominal 1.05V to 3.3V 55 CPUKG0C_LPRS OUT Complementary signal of low-power differential push-pull AND K8 "Greyhound" clock with integrated series resistor needed) 56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AND K8 "Greyhound" clock with integrated series 57 PD# IN Enter /Exit Power Down. Complementary signal of low-power differential push-pull hypertransport clock with integrated series </td <td>46</td> <td>SRC6T/SATAT_LPRS</td> <td>OUT</td> <td>True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)</td>	46	SRC6T/SATAT_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
48 GNDA GND Ground for the Analog Core 49 VDDA PWR 3.3V Power for the Analog Core 50 CLKREQ2#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a follows: 51 CLKREQ1#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 52 GNDCPU GND Ground pin for the CPU outputs. 53 VDDCPU_IO PWR Supply for CPU core, 3.3V nominal 54 VDDCPU_IO PWR Supply for CPU core, 3.3V nominal 55 CPUKG0C_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrate series resistor needed) 56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor needed) 57 PD# IN Enter Fxit Power Down, 1 = normal operation. 58 GNDHTT PWR Ground pin for the HTT outputs 60 HTT0_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor needed) 70 HTT0_LPRS/66M OUT True signal of l	47	GNDSATA	GND	
49 VDDA PWR 3.3V Power for the Analog Core 50 CLKREQ2#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a follows: 61 CLKREQ1#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 62 Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 63 CLKREQ1#** IN Ground pin for the CPU outputs 64 GRDCPU GND Ground pin for the CPU outputs. nominal 0.50 S.3V 54 VDDCPU PWR Supply for CPU core, 3.3V nominal 0.50 S.3V 56 CPUKG0C_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor needed) 57 PD# IN Enter /Exit Power Down. 0.50 Power Down. 58 GNDHTT PWR Ground pin for the HTT outputs Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. 59 HTTO_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor.				
50 CLKREQ2#** IN Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled a follows: 0 = enabled, 1 = Low-Low 51 CLKREQ1#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC1 outputs. Follows: 0 = follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC1 outputs. Follows: 0 = follows: 0 = follow follows: 0 = CPUKG0C_LDRS Clock Request pin for the CPU outputs. Follows: 0 = follow follows: 0 = CPUKG0C_LPRS OUT Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor needed) True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. 56 CPUKg0T_LPRS OUT Enter /Exit Power Down. 1 = normal operation. Complementary signal of low-power differential push-pull MD K8 "Greyhound" clock with integrated series resistor. 58 GNDHTT PWR Ground pin for the HTT outputs Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. 59 HTT0C_LPRS/66M OUT				
51 CLKREQ1#** IN Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled a follows: 52 GNDCPU GND Ground pin for the CPU outputs. 54 VDDCPU_IO PWR Power supply for differential CPU outputs. nominal 1.05V to 3.3V 54 VDDCPU PWR Supply for CPU core, 3.3V nominal Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrate series resistor needed) 55 CPUKGOC_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor needed) 56 CPUKGOT_LPRS OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor needed) 57 PD# IN Enter /Exit Power Down. 0 61 VDDK QUT Ground pin for the HTT outputs Complementary signal of low-power differential push-pull hypertransport clock with integrated serier resistor needed) 1.8V single ended 66MHz hy transport clock 61 VDDHT PWR Supply for HTT clocks, nominal 3.3V. 1.4.318 MHz reference clock/ 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 63 REF2/SEL_27 OUT Ref. XTAL power				Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled as follows:
52 GNDCPU GND Ground pin for the CPU outputs 53 VDDCPU_IO PWR Power supply for differential CPU outputs, nominal 1.05V to 3.3V 54 VDDCPU PWR Supply for CPU core, 3.3V nominal 55 CPUKG0C_LPRS OUT Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrate series resistor needed) 56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 57 PD# IN Enter Fxit Power Down. 58 GNDHTT PWR Ground pin for the HTT outputs 59 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock 60 HTT0T_LPRS/66M OUT True signal of low-power supply. nominal 3.3V. 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref X1AL power supply. nominal 3.3V. 64 REF1/SEL_SATA I/O 14.318 MHz reference clock / 3.3V loterant latched input to select 27MHz SS and non SS on SRC7	51	CLKREQ1#**	IN	Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled as follows:
53 VDDCPU_IO PWR Power supply for differential CPU outputs, nominal 1.05V to 3.3V 54 VDDCPU PWR Supply for CPU core, 3.3V nominal 55 CPUKG0C_LPRS OUT Complementary signal of Iow-power differential push-pull AMD K8 "Greyhound" clock with integrate series resistor. (no 33 ohm series resistor needed) 56 CPUKG0T_LPRS OUT True signal of Iow-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 57 PD# IN Enter /Exit Power Down. 58 GNDHTT PWR Ground pin for the HTT outputs 59 HTT0C_LPRS/66M OUT complementary signal of Iow-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hypertransport clock 61 VDDHTT PWR Ref.XTAL power supply, rominal 3.3V. 62 VDDREF PWR Ref.XTAL power supply, rominal 3.3V. 64 REF1/SEL_SATA I/O 14.318 MHz reference clock, 3.3V (a).2V Latched input to select 27MHz SS and non SS on SRC7 65 REF0/SEL_HTT66 I/O 14.318 MHz 3.3V reference clock/.3.3V tolerant latched input to select Hyper	52	GNDCPU	GND	
54 VDDCPU PWR Supply for CPU core, 3.3V nominal 55 CPUKG0C_LPRS OUT Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 57 PD# IN Enter Fxit Power Down. 58 GNDHTT PWR Ground pin for the HTT outputs 60 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated serie resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock 60 HTT0T_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated serie resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock 61 VDDHTT PWR Ref. XTAL power supply, nominal 3.3V. 62 VDDREF PWR Ref. XTAL power supply, nominal 3.3V. 63 REF2/SEL_27 OUT 1 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on				
55 CPUKG0C_LPRS OUT Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) 57 PD# IN Enter /Exit Power Down. 0 = Power Down. 58 GNDHTT PWR Ground p in for the HTT outputs Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hypertransport clock 60 HTTOT_LPRS/66M OUT Signal of Iow-power differential push-pull hypertransport clock with integrated series resistor. 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V. 63 REF2/SEL_27 OUT 0 = 100MHz differential preading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on pin 5. 64 REF1/SEL_SATA I/O I 4.318 MHz 3.3V reference clock/3.3V tolerant latched input to select Hyper Transport Clock Frequency. 65 REF0/SEL_HTT66 I/O	54	VDDCPU	PWR	
56 CPUKG0T_LPRS OUT True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor (no 33 ohm series resistor needed) 57 PD# IN 0 = Power Down, 1 = normal operation. 58 GNDHTT PWR Ground pin for the HT outputs 59 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. 59 HTT0C_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor. 60 HT0T_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor. 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref.XTAL power supply, nominal 3.3V 63 REF1/SEL_27 OUT 0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz 3.3V reference clock/ 3.3V tolerant latched input to select function of SRC6/SATA outp 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock/ 3.3V tolerant latched input to select Hyper Transport Clock Frequency.	55	CPUKG0C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed)
57 PD# IN 0 = Power Down, 1 = normal operation. 58 GNDHTT PWR Ground pin for the HTT outputs 59 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor needed) / 1.8V single ended 66MHz hyper transport clock 60 HTT0T_LPRS/66M OUT Soohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V. 63 REF2/SEL_27 OUT 0 = 100MHz differential spreading SRC clock, 1 = 27MHz son-spreading singled clock on pin 4 and 27MHz spread clock on pin 5. 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock/3.3V tolerant latched input to select function of SRC6/SATA outp 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O Frequency. 0 = 100MHz 3.3V reference clock/3.3V tolerant latched input to select Hyper Transport Clock 66 GNDREF GND Ground pin for the REF outputs. 0 = 100MHz 3.3V reference clock/3.3V tolerant latched input to select Hyper Transport Clock 67 X1 IN Cr	56	CPUKG0T_LPRS	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series
58 GNDHTT PWR Ground pin for the HTT outputs 59 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ender 66MHz hyper transport clock 60 HTT0T_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor. 500hm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hy transport clock 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V. 63 REF2/SEL_27 OUT 0 14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA outp 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O Frequency. 0 = 100MHz differential HTT clock, 3.3V tolerant latched input to select Hyper Transport Clock 66 GNDREF GND Ground pin for the REF outputs. 67 X1 67 X1 IN Crystal input, nominally 14.318MHz 6	57	PD#	IN	
59 HTT0C_LPRS/66M OUT Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock 60 HTT0T_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor. 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V 63 REF2/SEL_27 OUT 14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 63 REF1/SEL_SATA I/O 14.318 MHz reference clock, 3.3V/3.3V Latched input to select function of SRC6/SATA outpower differential spreading SRC clock, 1 = 27MHz non-spreading differential SATA clock 64 REF1/SEL_SATA I/O 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock 66 GNDREF GND Ground pin for the REF outputs. 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock 67 X1 IN Crystal output, nominally 14.318MHz 68 68 <	58	GNDHTT	PWR	
60 HTT0T_LPRS/66M OUT True signal of low-power differential push-pull hypertransport clock with integrated series resistor. 61 VDDHTT PWR Supply for HTT clocks, nominal 3.3V. 62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V. 63 REF2/SEL_27 OUT 0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on pin 5. 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock/ 3.3V tolerant latched input to select function of SRC6/SATA outp 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O Frequency. 66 GNDREF GND Ground pin for the REF outputs. 67 X1 IN Crystal input, nominally 14.318MHz 68 X2 OUT Crystal input, nominally 14.318MHz 68 X2 OUT Crystal input, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 67 X1 IN Crystal output, nominally 14.318MHz 68 X2 OUT Crystal output, nominally 14.318MHz 69 VDD48 P				Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock
62 VDDREF PWR Ref, XTAL power supply, nominal 3.3V 63 REF2/SEL_27 OUT 14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 63 REF2/SEL_27 OUT 0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on pin 5. 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA outp 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock 66 GNDREF GND Ground pin for the REF outputs. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock 67 X1 IN Crystal input, nominally 14.318MHz 0 68 X2 OUT Crystal output, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output.	60	HTT0T_LPRS/66M	OUT	True signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) /1.8V single ended 66MHz hyper transport clock
63 REF2/SEL_27 OUT 14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock, 3.3V/3.3V tolerant latched input to select function of SRC6/SATA outpower of the select function of the select function of SRC6/SATA outpower outpower of the select function of SRC6/SATA outpower outpower of the select function of SRC6/SATA outpower ou	61		PWR	Supply for HTT clocks, nominal 3.3V.
63 REF2/SEL_27 OUT 0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on pin 5. 64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA output 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock 66 GNDREF GND Ground pin for the REF outputs. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock 68 X2 OUT Crystal input, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs	62	VDDREF	PWR	
64 REF1/SEL_SATA I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA output 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock 65 REF0/SEL_HTT66 I/O 14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock 66 GNDREF GND Ground pin for the REF outputs. 67 X1 IN Crystal input, nominally 14.318MHz 68 X2 OUT Crystal output, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs	63	REF2/SEL_27	OUT	0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and
65 REF0/SEL_HTT66 I/O Frequency. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock 66 GNDREF GND Ground pin for the REF outputs. 67 X1 IN Crystal input, nominally 14.318MHz 68 X2 OUT Crystal output, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs	64	REF1/SEL_SATA	I/O	14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA output
66GNDREFGNDGround pin for the REF outputs.67X1INCrystal input, nominally 14.318MHz68X2OUTCrystal output, nominally 14.318MHz69VDD48PWRPower pin for the 48MHz outputs and core. 3.3V7048MHz_1OUT48MHz clock output.7148MHz_0OUT48MHz clock output.72GND48GNDGround pin for the 48MHz outputs	65	_	I/O	Frequency. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock
68 X2 OUT Crystal output, nominally 14.318MHz 69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs	66	GNDREF	GND	
69 VDD48 PWR Power pin for the 48MHz outputs and core. 3.3V 70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs				Crystal input, nominally 14.318MHz
70 48MHz_1 OUT 48MHz clock output. 71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs	68	X2	OUT	
71 48MHz_0 OUT 48MHz clock output. 72 GND48 GND Ground pin for the 48MHz outputs				
72 GND48 GND Ground pin for the 48MHz outputs				
	-			
1616—08/20/09			GND	Ground pin for the 48MHz outputs

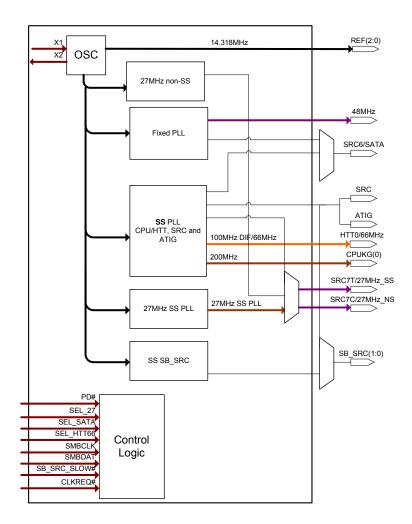
© 2019 Renesas Electronics Corporation



General Description

The **ICS9EPRS488** is a main clock synthesizer chip that provides all clocks required for AMD M690T or 780E embedded systems. An SMBus interface allows full control of the device.

Block Diagram



Power Groups

	Pin Number		Description
VDD	VDDIO	GND	Description
69		72	USB_48 outputs
3		6	SRC/27MHz Outputs
17		11,19	SRC Logic Core
	12,18		SRC differential outputs (IO's)
38		36	SB_SRC Core Logic
	37		SB_SRC differential outputs (IO's)
44		47	SRC/SATA differential output
29		27	ATIG Core Logic
	28		ATIG differential outputs (IO's)
49		48	3.3V Analog
54		52	CPUKG Core Logic
	53		CPUKG differential outputs (IO's)
61		58	HTTCLK output
62		66	REF outputs

^{© 2019} Renesas Electronics Corporation

Byte 0		Byt	te 3		•	HTT	Differential			
Bit0	Bit3	Bit2	Bit1	Bit0	CPU (MHz)	Single- ended	HTT	SRC/ATIG	Spread %	CPU OverClock
SS_EN	CPU FS3	CPU FS2	CPU FS1	CPU FS0	(11172)	SEL_HTT66 = 1	SEL_HTT66 = 0		/0	%
0	0	0	0	0	173.63	57.88	86.81	86.81		-13%
0	0	0	0	1	177.17	59.06	88.58	88.58		-11%
0	0	0	1	0	180.78	60.26	90.39	90.39		-10%
0	0	0	1	1	184.47	61.49	92.24	92.24		-8%
0	0	1	0	0	188.24	62.75	94.12	94.12		-6%
0	0	1	0	1	192.08	64.03	96.04	96.04		-4%
0	0	1	1	0	196.00	65.33	98.00	98.00		-2%
0	0	1	1	1	200.00	66.67	100.00	100.00	Off	0%
0	1	0	0	0	204.00	68.00	102.00	102.00		2%
0	1	0	0	1	208.08	69.36	104.04	104.04		4%
0	1	0	1	0	212.24	70.75	106.12	106.12		6%
0	1	0	1	1	216.49	72.16	108.24	108.24		8%
0	1	1	0	0	220.82	73.61	110.41	110.41		10%
0	1	1	0	1	225.23	75.08	112.62	112.62		13%
0	1	1	1	0	229.74	76.58	114.87	114.87		15%
0	1	1	1	1	234.33	78.11	117.17	117.17		17%
1	0	0	0	0	173.63	57.88	86.81	86.81		-13%
1	0	0	0	1	175.00	59.06	88.58	88.58		-11%
1	0	0	1	0	180.78	60.26	90.39	90.39		-10%
1	0	0	1	1	184.47	61.49	92.24	92.24		-8%
1	0	1	0	0	188.24	62.75	94.12	94.12		-6%
1	0	1	0	1	192.08	64.03	96.04	96.04		-4%
1	0	1	1	0	196.00	65.33	98.00	98.00		-2%
1	0	1	1	1	200.00	66.67	100.00	100.00	-0.5%	0%
1	1	0	0	0	204.00	68.00	102.00	102.00	0.070	2%
1	1	0	0	1	208.08	69.36	104.04	104.04]	4%
1	1	0	1	0	212.24	70.75	106.12	106.12		6%
1	1	0	1	1	216.49	72.16	108.24	108.24		8%
1	1	1	0	0	220.82	73.61	110.41	110.41		10%
1	1	1	0	1	225.23	75.08	112.62	112.62		13%
1	1	1	1	0	229.74	76.58	114.87	114.87]	15%
1	1	1	1	1	234.33	78.11	117.17	117.17		17%

Table1: CPU/HTT, SRC and ATIG Frequency Selection Table

Table 2	: SB_S			y Sele	ction Table)	
Byte 0		By	te 4				
Bit0	Bit3	Bit2	Bit1	Bit0	SRC	Spread	SB_SRC
SS_EN	SB FS3	SB FS2	SB FS1	SB FS0	(MHz)	%	OverClock %
0	0	0	0	0	80.00		-20%
0	0	0	0	1	81.25	Ι	-19%
0	0	0	1	0	82.63	Ι	-17%
0	0	0	1	1	84.00	Ī	-16%
0	0	1	0	0	85.25	Ī	-15%
0	0	1	0	1	86.63	Ī	-13%
0	0	1	1	0	88.00	t f	-12%
0	0	1	1	1	89.25	Off	-11%
0	1	0	0	0	90.63		-9%
0	1	0	0	1	92.00	t f	-8%
0	1	0	1	0	93.25	t f	-7%
0	1	0	1	1	94.63	t f	-5%
0	1	1	0	0	96.00	t f	-4%
0	1	1	0	1	97.25	İ F	-3%
0	1	1	1	0	98.63	Ī	-1%
0	1	1	1	1	100.00		0%
1	0	0	0	0	80.00		20%
1	0	0	0	1	175.00	Ι	-19%
1	0	0	1	0	82.63	Ι	-17%
1	0	0	1	1	84.00		-16%
1	0	1	0	0	85.25		-15%
1	0	1	0	1	86.63		-13%
1	0	1	1	0	88.00		-12%
1	0	1	1	1	89.25	-0.50%	-11%
1	1	0	0	0	90.63	0.0070	-9%
1	1	0	0	1	92.00	ļ	-8%
1	1	0	1	0	93.25	ļ	-7%
1	1	0	1	1	94.63	ļļ	-5%
1	1	1	0	0	96.00	ļ	-4%
1	1	1	0	1	97.25	ļļļ	-3%
1	1	1	1	0	98.63	ļ	-1%
1	1	1	1	1	100.00		0%

Table 2: SB_SRC Frequency Selection Table

SS Enable	SS3	SS2	SS1	SS0	27MHz_Spread	Spr	ead	
B2b1	Byte 4	Byte 4	Byte 4	Byte 4	(MHz)	% (whon	enabled)	
0201	bit 7	bit 6	bit 5	bit 4	(1112)		enableu)	
0	0	0	0	0	27.00			
0	0	0	0	1	27.00			
0	0	0	1	0	27.00			
0	0	0	1	1	27.00	_		
0	0	1	0	0	27.00			
0	0	1	0	1	27.00			
0	0	1	1	0	27.00			
0	0	1	1	1	27.00	No S	nroad	
0	1	0	0	0	27.00	100.5	pieau	
0	1	0	0	1	27.00			
0	1	0	1	0	27.00			
0	1	0	1	1	27.00			
0	1	1	0	0	27.00			
0	1	1	0	1	27.00			
0	1	1	1	0	27.00			
0	1	1	1	1	27.00			
1	0	0	0	0	27.00	-0.50	Down	
1	0	0	0	1	27.00	-1.00	Down	
1	0	0	1	0	175.00	-1.50	Down	
1	0	0	1	1	27.00	-2.00	Down	
1	0	1	0	0	27.00	-0.75	Down	
1	0	1	0	1	27.00	-1.25	Down	
1	0	1	1	0	27.00	-1.75	Down	
1	0	1	1	1	27.00	-2.25	Down	
1	1	0	0	0	27.00	+/-0.25	Center	
1	1	0	0	1	27.00	+/-0.5	Center	
1	1	0	1	0	27.00	+/-0.75	Center	
1	1	0	1	1	27.00	+/-1.0	Center	
1	1	1	0	0	27.00	+/-0.25	Center	
1	1	1	0	1	27.00	+/-0.5	Center	
1	1	1	1	0	27.00	+/-0.75	Center	
1	1	1	1	1	27.00	+/-1.0	Center	

Table 3: 27Mhz_Spread and Frequency Selection Table



Table 4: CPU Divider Ratios

				Divi	der	(3:2)			
	Bit	00		01		10		11	MSB
(1:0)	00	0000	2	0100	4	1000	8	1100	16
ir (1	01	0001	3	0101	6	1001	12	1101	24
Divider	10	0010	5	0110	10	1010	20	1110	40
Div	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 5: SRC, SB_SRC, ATIG Divider Ratios

				Divi	der	(3:2)			
	Bit	00		01		10		11	MSB
(1:0)	00	0000	2	0100	4	1000	8	1100	16
ir (1	01	0001	3	0101	6	1001	12	1101	24
Divider	10	0010	5	0110	10	1010	20	1110	40
<u>è</u>	11	0011	15	0111	14	1011	28	1111	56
	LSB	Address	Div	Address		Address	Div	Address	Div

Differential Output Power Management Table

PD#	CLKREQ#	SMBus	True output	Complement Output	True output	Complement Output
		Register OE	Fre	ee-Run	CLKREQ# Selected	
1	0	Enable	Running	Running	Running	Running
0	Х	Х	Low/20K	Low	Low/20K	Low
1	1	Enable	Running	Running	Low/20K	Low
Х	Х	Disable	Low/20K	Low	Low/20K	Low

Note: 20K means 20Kohm Pull Down

Singled-ended Power Management Table

PD#	SMBus Register OE	48MHz	27MHz	HTT66MHz	REF(2:0)	
1	Enable	Running	Running	Running	Running	
0	Enable	Low	Low	Low	Hi-Z	



Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-		3.3	GND + 3.9V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	С°	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

		ppy/common output Pa					-
PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP		UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-	3.135	3.3	3.465	V	1
Input High Voltage	V _{IH}	VDD = 3.3 V +/-5%	2		V _{DD} + 0.3	V	1
Input Low Voltage	VIL	VDD = 3.3 V +/-5%	V _{SS} - 0.3		0.8	V	1
Input High Current	I _{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I _{IL1}	V _{IN} = 0 V; Inputs with no pull- up resistors	-5			uA	1
	I _{IL2}	V _{IN} = 0 V; Inputs with pull-up resistors	-200			V _{DD} + 0.3 V 0.8 V 5 uA uA uA	1
Low Threshold Input- High Voltage	V _{IH_FS}	VDD = 3.3 V +/-5%	0.7		V _{DD} + 0.3	v	1
Low Threshold Input- Low Voltage	V _{IL_FS}	VDD = 3.3 V +/-5%	V _{SS} - 0.3		0.35	V	1
Operating Current	I _{DD3.3OP}	3.3V VDD current, all outputs driven			175	mA	1
Powerdown Current	I _{DD3.3PD}	all diff pairs low/low			2	mA	1
Input Frequency	Fi	VDD = 3.3 V +/-5%		14.31818		MHz	2
Pin Inductance	L _{pin}				7	nH	1
	C _{IN}	Logic Inputs			5	pF	1
Input Capacitance	C _{OUT}	Output pin capacitance			6	pF	1
	C _{INX}	X1 & X2 pins			5	uA uA uA 0.3 V 35 V 5 mA MHz nH pF pF pF generation 0 us 3 kHz 0 us 55 V	1
Clk Stabilization	T _{STAB}	From VDD Power-Up or de- assertion of PD to 1st clock			3	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V _{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	1
Current sinking at V _{OL} = 0.4 V	I _{PULLUPSMB}		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T _{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T _{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V + -5%

¹Guaranteed by design and characterization, not 100% tested in production.

² Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics - Low-Power DIF Outputs: CPUKG and HTT

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
Frequency - CPU	f _{CPU}	Spread Specturm On	198.8		200	MHz	1,3
Frequency - HTT	f _{нтт}	Spread Specturm On	99.4		100	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-300		+300	ppm	1,11
Rising Edge Slew Rate	S _{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S _{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t _{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	CPUJ _{C2C}	Differential Measurement			150	ps	1,6
Accumulated Jitter	t _{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	V _{D(PK-PK)}	Differential Measurement	400		2400	mV	1,8
Differential Voltage	VD	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D _{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in $V_D DC$ cycle to cycle	-75		75	mV	1,10
CPU[1:0] Skew	CPU _{SKEW10}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

²Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not ³Minimum Frequency is a result of 0.5% down spread spectrum

⁴Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

⁵ Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

 $^{\rm 6}\,{\rm Max}$ difference of $t_{\rm CYCLE}$ between any two adjacent cycles.

⁷ Accumulated tjc.over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

⁸ VD(PK-PK) is the overall magnitude of the differential signal.

⁹ VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

¹⁰ The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of

¹¹ All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics - Low-Power DIF Outputs: SRC, SB_SRC and ATIG

		•	-				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t _{SLR}	Differential Measurement	0.6		4	V/ns	1,2
Falling Edge Slew Rate	t _{FLR}	Differential Measurement	0.6		4	V/ns	1,2
Slew Rate Variation	t _{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V _{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V _{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V _{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V _{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	VXABSVAR	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D _{CYC}	Differential Measurement	45		55	%	1
SRC, ATIG, Jitter - Cycle to Cycle	SRCJ _{C2C}	Differential Measurement			125	ps	1
SRC[5:0] Skew	SRC _{SKEW}	Differential Measurement			250	ps	1
SB_SRC[1:0] Skew	SRC _{SKEW}	Differential Measurement			100	ps	1
ATIG[2:0] Skew	SRC _{SKEW}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through Vswing centered around differential zero

³ Vxabs is defined as the voltage where CLK = CLK#

⁴ Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵ Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of

⁶ All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - Single-ended HTT 66MHz Clock

<u> </u>						
SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
ppm	see Tperiod min-max values	-100		100	ppm	1,2
т	66.67MHz output nominal	14.9955		15.0045	ns	2
High Voltage V_{OH} $I_{OH} = -1 \text{ mA}$	14.9955		15.0799	ns	2	
V _{OH}	I _{OH} = -1 mA	1.6	1.8	3.3	V	1
V _{OL}	I _{OL} = 1 mA		0	0.2	V	1
t _{r1}	$V_{OL} = 0.36 \text{ V}, V_{OH} = 1.44 \text{ V}$			1.5	ns	1
t _{f1}	$V_{OH} = 1.44 \text{ V}, V_{OL} = 0.36 \text{ V}$			1.5	ns	1
d _{t1}	$V_{T} = 0.9 V$	45		55	%	1
t _{jcyc-cyc}	$V_{T} = 0.9 V$			300	ps	1
t _{LTJ}	$V_{T} = 0.9 V$			1	ns	1
	SYMBOL ppm T _{period} V _{OH} V _{OL} t _{r1} t _{f1} d _{t1} t _{jcyc-cyc}	$\begin{tabular}{ c c c c c } \hline SYMBOL & CONDITIONS \\ \hline ppm & see Tperiod min-max values \\ \hline T_{period} & \hline 66.67MHz output nominal \\ \hline 66.67MHz output spread \\ \hline V_{OH} & I_{OH} = -1 mA \\ \hline V_{OL} & I_{OL} = 1 mA \\ \hline V_{OL} & I_{OL} = 1 mA \\ \hline t_{r1} & V_{OL} = 0.36 V, V_{OH} = 1.44 V \\ \hline t_{f1} & V_{OH} = 1.44 V, V_{OL} = 0.36 V \\ \hline d_{t1} & V_{T} = 0.9 V \\ \hline t_{jcyc-cyc} & V_{T} = 0.9 V \\ \hline \end{array}$	$\begin{tabular}{ c c c c c c } \hline SYMBOL & CONDITIONS & MIN \\ \hline ppm & see Tperiod min-max values & -100 \\ \hline T_{period} & 66.67MHz output nominal & 14.9955 \\ \hline V_{OH} & I_{OH} = -1 mA & 1.6 \\ \hline V_{OL} & I_{OL} = 1 mA & 1.6 \\ \hline V_{OL} & I_{OL} = 0.36 \ V, \ V_{OH} = 1.44 \ V & \\ \hline t_{f1} & V_{OH} = 1.44 \ V, \ V_{OL} = 0.36 \ V & \\ \hline d_{t1} & V_{T} = 0.9 \ V & 45 \\ \hline t_{jcyc-cyc} & V_{T} = 0.9 \ V & \\ \hline \end{array}$	$\begin{tabular}{ c c c c c c c } \hline SYMBOL & CONDITIONS & MIN & TYP \\ \hline ppm & see Tperiod min-max values & -100 \\ \hline T_{period} & 66.67MHz output nominal & 14.9955 \\ \hline V_{OH} & I_{OH} = -1 mA & 1.6 & 1.8 \\ \hline V_{OL} & I_{OL} = 1 mA & 0 \\ \hline t_{r1} & V_{OL} = 0.36 \ V, \ V_{OH} = 1.44 \ V & \\ \hline t_{f1} & V_{OH} = 1.44 \ V, \ V_{OL} = 0.36 \ V & \\ \hline d_{t1} & V_{T} = 0.9 \ V & 45 \\ \hline t_{jcyc-cyc} & V_{T} = 0.9 \ V & \\ \hline \end{array}$	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T _{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T _{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T _{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output Llink Current		V _{OH} @MIN = 1.0 V	-33			mA	1
Output High Current	I _{OH}	V _{OH} @MAX = 3.135 V			-33	mA	1
Output Low Current	I	V _{OL} @ MIN = 1.95 V	30			mA	1
Output Low Current	I _{OL}	V _{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t _{r_USB}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5		1.5	ns	1
Fall Time	t _{f_USB}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5		1.5	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	V _T = 1.5 V			130	ps	1,2

Electrical Characteristics - USB - 48MHz

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics - 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	nnm	see Tperiod min-max values	-50		50	000	1,2
Long Accuracy	ppm	see thenou min-max values	-15		15	ppm	1,2,3
Clock period	T _{period}	27.000MHz output nominal	37.0365		37.0376	ns	2
Output High Voltage(27SS)	V _{OH}	I _{OH} = -1 mA	2.1			V	1,10
Output High Voltage (27NSS)	V _{OH}	I _{OH} = -1 mA	0.8			V	1,11
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	1	V _{OH} = 1.0 V	-29			mA	1,10
Output High Current	I _{OH}	V _{OH} = 3.135 V			-23	mA	1,10
Output Low Current		V _{OL} = 1.95 V	29			0 ppm 5 ppm 376 ns V V 55 V 55 V 3 mA 3 mA 7 mA 4 V/ns 5 % 00 ps	1,10
Output Low Current	I _{OL}	V _{OL} = 0.4 V			27		1,10
Edge Rate	t _{slewr/f}	Rising/Falling edge rate	1	2	4	V/ns	1
Edge Hate	slewr/f	V _T @ 20%-80%	'	2	-	V/113	1
Duty Cycle	d _{t1}	$V_{T} = 1.5 V$	45		55	%	1
Jitter	t _{iti}	Long Term (10us)			300	ps	1
Jitter	t _{jcyc-cyc}	V _T = 1.5 V			200	ps	1

¹Guaranteed by design and characterization, not 100% tested in production.

 $^{\rm 2}\,{\rm Slew}$ rate measured through Vswing centered around differential zero

 3 Vxabs is defined as the voltage where CLK = CLK#

10
 V_{DD} = 3.3V

 $^{11}\,V_{DD}=\,1.1V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Clock Low Time	T _{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T _{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.4	V	1
Output High Current	I _{OH}	V _{OH} @MIN = 1.0 V, V _{OH} @MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I _{OL}	V _{OL} @MIN = 1.95 V, V _{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t _{r1}	$V_{OL} = 0.4 V, V_{OH} = 2.4 V$	1		1.5	ns	1
Fall Time	t _{f1}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	1		1.5	ns	1
Skew	t _{sk1}	V _T = 1.5 V			250	ps	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Jitter	t _{jcyc-cyc}	V _T = 1.5 V			200	ps	1

Electrical Characteristics - REF-14.318MHz

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



General SMBus serial interface information for the ICS9EPRS488

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will *acknowledge*
- Controller (host) sends the begining byte location = N
- ICS clock will *acknowledge*
- Controller (host) sends the data byte count = X
- ICS clock will acknowledge
- Controller (host) starts sending *Byte N through Byte N + X -1*
- ICS clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will acknowledge
- ICS clock will send the data byte count = X
- ICS clock sends Byte N + X -1
- ICS clock sends Byte 0 through byte X (if X_(H) was written to byte 8).
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

In	dex Block W	/rit	e Operation
Сог	ntroller (Host)		ICS (Slave/Receiver)
Т	starT bit		
Slav	e Address D2 _(H)		
WR	WRite		
			ACK
Beginning Byte = N			
		ACK	
Data	Byte Count = X		
			ACK
Begir	nning Byte N		
			ACK
	0	te	
	0	Byte	0
	0	\times	0
			0
Byte	e N + X - 1		
			ACK
Р	stoP bit	_	

In	dex Block Rea	ad (Operation	
Cor	ntroller (Host)	IC	S (Slave/Receiver)	
Т	starT bit			
Slav	e Address D2 _(H)			
WR	WRite			
			ACK	
Begi	nning Byte = N			
	-	ACK		
RT	Repeat starT			
Slav	e Address D3 _(H)			
RD	ReaD			
		ACK		
		D	ata Byte Count = X	
	ACK			
			Beginning Byte N	
	ACK			
		X Byte	0	
	0	ы	0	
	0		0	
	0			
			Byte N + X - 1	
N	Not acknowledge			
Р	stoP bit			

1616—08/20/09

Byte	0	Name	Description	Туре	0	1	Default
	Bit 7	SEL_HTT66 readback	Hypertransport Select	R	100MHz Differential HTT clock	66 MHz 3.3V Single- ended HTT clock	Latch
	Bit 6	SEL_SATA readback	SATA Select	R	SRC6/SATA pair is SRC SS capable output	SRC6/SATA pair is SATA non-spread output	Latch
	Bit 5	REF0_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 4	REF1_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 3	REF2_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 2	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
	Bit 1	48MHz_0_OE	Output Enable	RW	Low	Enabled	1
	Bit 0	SS_Enable	Spread Spectrum Enable (CPU, SRC, SB_SRC, ATIG)	RW	Spread Off	Spread On	0

SMBus Table: Latched Input Readback Output Enable Control Register

SMBus Table:Output Enable Control Register

Byte	1	Name	Control Function	Туре	0	1	Default
	Bit 7	SRC7/27MHz_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	SRC6/SATA_OE Enable	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	SRC5_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	SRC4_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 2	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 1	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 0	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: Output Enable and 48MHz Slew Rate Control Register

Byte	2	Name	Control Function	Туре	0	1	Default
	Bit 7	SB_SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	SB_SRC0_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	48MHz_0_Slew Rate	Slew Rate Control	RW	These bits program the ended outputs. The m 1.9V/ns and the minimu The slew rate selec 11 = 1.	1	
	Bit 4				10 = 1. 01 = 1. 00 = tris	1V/ns	1
	Bit 3	ATIG1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 2	ATIG0_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 1	27MHz_SS_Enable	27MHz_SS_Enable Spread Spectrum Enable 27MHz_SS RW Spread Off Spread On		0		
	Bit 0	Reserved	Reserved	RW	-	-	Х

SMBus Table: CPU/HTT Frequency Control Register

Byte	3	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU0_OE	Output enable	RW	Low/Low	Enable	1
	Bit 6	SEL_27 readback	SRC7/27MHz Select	R	SRC7 Output	27MHz Output	Latch
	Bit 5	ATIG2_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	HTT/66MHz_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	CPU_FS3	CPU Frequency Select	RW	See CPU/HTT/SRC/A1	IG Frequency Select	0
	Bit 2	CPU_FS2	CPU Frequency Select	RW	Tab Default value corres		1
	Bit 1	CPU_FS1	CPU Frequency Select	RW	Note that the HTT frequ	•	1
	Bit 0	CPU_FS0	CPU Frequency Select LSB	RW	freque	1	

1616-08/20/09

© 2019 Renesas Electronics Corporation

Byte	4	Name	Control Function	Туре	0	1	Default
	Bit 7	S3		RW	S[1:0]: 00 = -0.5% Default,		0
	Bit 6	S2	27 SSC RW 01 =1.0%, 10 = -1.5%, 11 = -2%.		0		
	Bit 5	S1	RW See Table 3: 27Mhz_Spread, LCDCLK Spread Spread Select RW and Frequency Selection Table for additional selections. SB_SRC Frequency Select RW selections.	0			
ſ	Bit 4	SO		RW			0
Γ	Bit 3	SB_SRC_FS3			1		
Γ	Bit 2	SB_SRC_FS2	SB_SRC Frequency Select	RW	See SB_SRC Frequ	ency Select Table.	1
Γ	Bit 1	SB_SRC_FS1	SB_SRC Frequency Select	RW			1
Γ	Bit 0	SB_SRC_FS0	SB_SRC Freq. Select LSB	RW			1

SMBus Table: 27MHz Slew Rate Control Register

Byte	5	Name	Control Function	Туре	0	1	Default
	Bit 7	27M SS Slew Rate	Slew Rate Control	BW	These bits program the ended outputs. The n	0	1
	Bit 6		Siew Hate Control	1100	1.9V/ns and the minimu The slew rate selec		1
	Bit 5	27M NS Slew Rate	Slew Rate Control	RW	11 = 1. 10 = 1.	6V/ns	1
	Bit 4	27M_NO_Olew hale	Siew Rate Control	ΠVV	01 = 1.1V/ns 00 = tristated		1
Ē	Bit 3	SB_SRC Source	SB_SRC Source Selection	RW	SB_SRC PLL	SRC PLL	1
	Bit 2	Reserved Reserved					0
	Bit 1						
	Bit 0		Reserv	ved			0

SMBus Table: I/O Vout Control Register

Byte	6	Name	Control Function	Туре	0	1	Default
	Bit 7	SRC Diff AMP	SRC Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 6	SRC Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 5	CPU Diff AMP	CPU Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 4	CPU Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 3	SB_SRC Diff AMP	SB_SRC Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 2	SB_SRC Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 1		Reserv	red			X
	Bit 0		Reserv	red			Х

SMBus Table: Vendor &	Revision ID Register
-----------------------	-----------------------------

Byte	7	Name	Control Function	Туре	0	1	Default
	Bit 7	RID3		R	-	-	0
	Bit 6	RID2	REVISION ID	R	-	-	1
	Bit 5	RID1		R	-	-	0
	Bit 4	RID0		R	-	-	0
	Bit 3	VID3		R	-	-	0
Γ	Bit 2	VID2	VENDOR ID	R	-	-	0
	Bit 1	VID1	VENDORID	R	-	-	0
	Bit 0	VID0		R	-	-	1

		SMBus Table: Byte Count	t Register				
Byte	8	Name	Control Function	Туре	0	1	Default
	Bit 7		Reser	ved			0
	Bit 6 Reserved					0	
Ĩ	Bit 5	BC5	Byte Count bit 5 (MSB)	RW			0
	Bit 4	BC4	Byte Count bit 4	RW	V		0
	Bit 3	BC3	Byte Count bit 3	RW	Determines the number	1	
	Bit 2	BC2	Byte Count bit 2	RW	back from the device	e. Default is 0F hex.	1
	Bit 1	BC1	Byte Count bit 1	RW			1
	Bit 0	BC0	Byte Count bit 0 (LSB)	RW			1

SMBus Table: WatchDog Timer Control Register

Byte	9	Name	Control Function	Туре	0	1	Default
	Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hartd Alarm Timer, Clear WD Hard status bit.	Enable Timer	0
ſ	Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Ē	Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	Х
	Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	Х
	Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
	Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent the	number of Watch Dog	1
	Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW	Time Base Units that p	ass before the Watch	1
ſ	Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW	Alarm expires. Defau	lt is 7 X 290ms = 2s.	1

SMBus Table: WD Timer Safe Frequency Control Register

Byte	10	Name	Control Function	Туре	0	1	Default		
	Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent the	e number of Watch Dog	1		
	Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW	Time Base Units that p	ass before the Watch	1		
	Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW	Alarm expires. Defau	Alarm expires. Default is 7 X 290ms = 2s.			
	Bit 4	WD SF4		RW	These bits configure the	igure the safe frequency that the	0		
	Bit 3	WD SF3		RW	device returns to if the W	vice returns to if the Watchdog Timer expires. ne value show here corresponds to the power			
	Bit 2	WD SF2	Watch Dog Safe Freq	RW	The value show here co				
	Bit 1	WD SF1	Programming bits	RW		up default of the device. See the various	1		
	Bit 0	WD SF0		RW	Frequency Select T freque		1		

SMBus Table: CPU PLL Frequency Control Register

Byte	11	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW			Х
	Bit 6	N Div1	N Divider Prog bit 1	RW	Ī		Х
	Bit 5	M Div5		RW	The decimal representati	on of M and N Divider in	Х
	Bit 4	M Div4		RW	Byte 11 and 12 will configure the VCO frequency.	Х	
	Bit 3	M Div3	M Divider Programming bits	RW	Default at power up = B	,	Х
	Bit 2	M Div2	RW Frequency = 14.318 x Ndiv(10:0)/Mdiv(5	RW	Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0) .		Х
	Bit 1	M Div1			Х		
	Bit 0	M Div0		RW			Х

Byte	12	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div10		RW			Х
	Bit 6	N Div9		RW	RW RW The decimal representation of M and N Divider in RW Byte 11 and 12 will configure the VCO frequency.	Х	
[Bit 5	N Div8		RW		Х	
	Bit 4	N Div7	N Divider Programming	RW			
	Bit 3	N Div6	b(10:3)	RW	Default at power up = E	Byte 3 Rom table. VCO	Х
Ē	Bit 2	N Div5		RW	Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0) .		Х
_	Bit 1	N Div4		RW			Х
	Bit 0	N Div3		RW			Х

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	13	Name	Control Function	Туре	0	1	Default
	Bit 7	SSP7		RW			Х
	Bit 6	SSP6	1	RW			Х
	Bit 5	SSP5		RW	Bytes 13 and 14 set the CPU/HTT/SRC/ATIG		Х
	Bit 4	SSP4	Spread Spectrum	RW		d pecentage. Please contact ICS for the	Х
	Bit 3	SSP3	Programming b(7:0)	RW	appropriat		Х
	Bit 2	SSP2		RW	αρριοριαι	appropriate values.	
	Bit 1	t 1 SSP1 RW		Х			
	Bit 0	SSP0		RW			Х

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	14	Name	Control Function	Туре	0	1	Default
	Bit 7		Reser	ved			Х
	Bit 6	SSP14		RW			Х
	Bit 5	SSP13		RW	Bytes 13 and 14 set the CPU/HTT/SRC/ATIG		Х
	Bit 4	SSP12	Enroad Engatrum	RW			Х
	Bit 3	SSP11	Spread Spectrum Programming b(14:8)	RW	spread pecentage.Plea	se contact ICS for the	Х
	Bit 2	SSP10	1 Togramming b(14.0)	RW	appropriat	e values.	Х
	Bit 1	SSP9		RW			Х
	Bit 0	SSP8		RW			Х

SMBUS Table: CPU Output Divider Register

Byte	15	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU NDiv0	LSB N Divider Programming	RW	CPU M/N pr	ogramming.	Х
ſ	Bit 6		Reserv	ved			Х
	Bit 5		Reserv	/ed			Х
	Bit 4		Reserv	/ed			Х
	Bit 3	CPUDiv3		RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	Х
	Bit 2	CPUDiv2	CPU Divider Ratio	RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	Х
	Bit 1	CPUDiv1	Programming Bits	RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	Х
Ī	Bit 0	CPUDiv0		RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	Х

SMBUS Table: SB_SRC Frequency Control Register

Byte	16	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW			Х
	Bit 6	N Div1	N Divider Prog bit 1	RW			Х
	Bit 5	M Div5		RW	The decimal representation	on of M and N Divider in	Х
	Bit 4	M Div4		RW	Byte 16 and 17 configu	Ire the SB_SRC VCO	Х
	Bit 3	M Div3	M Divider Programming	RW	frequency. See M/N Cac		Х
	Bit 2	M Div2	bit (5:0)	RW	frequency	formulas.	Х
	Bit 1	M Div1		RW			Х
	Bit 0	M Div0		RW			Х

SMBUS Table: SB_SRC Frequency Control Register

			iequeinej eenarei negia				
Byte	17	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div10		RW			Х
	Bit 6	N Div9		RW			Х
	Bit 5	N Div8		RW	The decimal representati	on of M and N Divider in	Х
	Bit 4	N Div7	N Divider Programming	RW	Byte 16 and 17 configu	ire the SB_SRC VCO	Х
	Bit 3	N Div6	Byte16 bit(7:0) and Byte15 bit(7:6)	RW	frequency. See M/N Cad	ulation Tables for VCO	Х
	Bit 2	N Div5	511(7.0)	RW	frequency	formulas.	Х
	Bit 1	N Div4	I	RW			Х
	Bit 0	N Div3		RW			Х

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	18	Name	Control Function	Туре	0	1	Default
	Bit 7	SSP7		RW			Х
	Bit 6	SSP6		RW			Х
	Bit 5	SSP5		RW	Butes 19 and 10 act th	the CR CRC enreed	Х
	Bit 4	SSP4	Spread Spectrum	RW	Bytes 18 and 19 set the pecentages. Please		Х
	Bit 3	SSP3	Programming bit(7:0)	RW	appropriat		Х
	Bit 2	SSP2		RW	appropriat	e values.	Х
	Bit 1	SSP1		RW			Х
	Bit 0	SSP0	ſ	RW			Х

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	19	Name	Control Function	Туре	0	1	Default
	Bit 7	SSP15		RW			Х
	Bit 6	SSP14		RW			Х
	Bit 5	SSP13		RW	Butes 19 and 10 act th	the SB_SRC spread	Х
	Bit 4	SSP12	Spread Spectrum	RW	pecentages. Please		Х
	Bit 3	SSP11	Programming bit(14:8)	RW	appropriat		Х
	Bit 2	SSP10		RW	appropriat	le values.	Х
	Bit 1	SSP9		RW			Х
	Bit 0	SSP8		RW			Х

SMBUS Table: SB_SRC Output Divider Control Register

Byte	20	Name	Control Function	Туре	0	1	Default
	Bit 7	SB_SRC NDiv0	LSB N Divider Programming	RW	SB_SRC M/N	orogramming.	Х
	Bit 6		Reserv	/ed			Х
	Bit 5		Reserv	/ed			Х
	Bit 4		Reserv	/ed			Х
	Bit 3	SB_SRCDiv3		RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	Х
	Bit 2	SB_SRCDiv2	SRC Divider Ratio	RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	Х
	Bit 1	SB_SRCDiv1	Programming Bits	RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	Х
	Bit 0	SB_SRCDiv0	Ī	RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	Х

SMBus Table: Device ID register

Byte	21	Name	Control Function	Туре	0	1	Default
	Bit 7	Device ID7		R			0
	Bit 6	Device ID6		R			
	Bit 5	Device ID5		R			
	Bit 4	Device ID4	Davias ID	R	70 6		1
	Bit 3	Device ID3	Device ID	R	76 h	lex	0
	Bit 2	Device ID2		R			1
	Bit 1	Device ID1		R			1
	Bit 0	Device ID0		R			0

		SMBus Table: CLKREQ#	Configuration Register				
Byte	22	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU/HTT/SRC/ATIG M/N En	CPU/HTT/SRC/ATIG PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
ſ	Bit 6	SB_SRC M/N En	SB_SRC M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
	Bit 5	Reserved	Reserved	RW	-	-	0
ſ	Bit 4	Reserved	Reserved	RW	-	-	0
	Bit 3	Reserved	Reserved	RW	-	-	0
ſ	Bit 2	Reserved	Reserved	RW	-	-	Х
Ē	Bit 1	Reserved	Reserved	RW	-	-	Х
	Bit 0	Reserved	Reserved	RW	-	-	Х

SMBus Table: CLKREQ# Configuration Register

		SIVIDUS TADIE: CERNEQ#	Configuration negister				
Byte	23	Name	Control Function	Туре	0	1	Default
	Bit 7	Reserved	Reserved	RW	-	-	0
	Bit 6	Reserved	Reserved	RW	-	-	0
	Bit 5	CLKREQ4#_Enable	CLKREQ4# controls SRC5	RW	Not Controlled	Controlled	1
	Bit 4	CLKREQ4#_Enable	CLKREQ4# controls SRC4	RW	Not Controlled	Controlled	1
	Bit 3	CLKREQ3#_Enable	CLKREQ3# controls SRC3	RW	Not Controlled	Controlled	1
	Bit 2	CLKREQ2#_Enable	CLKREQ2# controls SRC2	RW	Not Controlled	Controlled	1
	Bit 1	CLKREQ1#_Enable	CLKREQ1# controls SRC1	RW	Not Controlled	Controlled	1
	Bit 0	CLKREQ0#_Enable	CLKREQ0# controls SRC0	RW	Not Controlled	Controlled	1

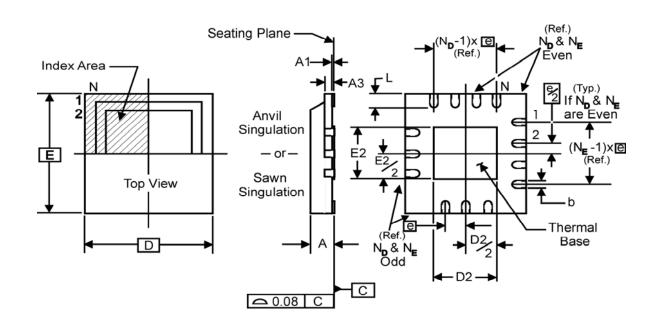
SMBus Table: Test Mode Configuration Register

Byte	24	Name	Control Function	Туре	0	1	Default
	Bit 7	Test_Md_Sel	Selects Test Mode	RW	Normal mode	All ouputs are REF/N	0
	Bit 6	DIAG Enable#	DIAG enable CPU and LCD PLL	RW	Reset forces B24[6:4,2,0] to 0	DIAG mode Enabled	0
	Bit 5	CPU PLL_LOCK signal	CPU PLL Lock Detect	R	unlocked	Locked	HW
	Bit 4	27MHz PLL_LOCK signal	27MHz PLL Lock Detect	R	unlocked	Locked	HW
	Bit 3	Fixed PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
	Bit 2	SRC PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
	Bit 1	Frequency Check	Primary PLL or external crystal Frequency Accuracy	R	Not Accurate	Accurate	HW
	Bit 0	PWRGD Status	Power on Reset Status	R	Invalid voltage levels on any of the VDDs. CKPWRGD is not asserted or external XTAL not detected.	Valid voltage levels exist on all the VDD. CKPWRGD is asserted and external XTAL is detected.	HW

SMBus Table:Slew Rate Select Register

Byte	25	Name	Control Function	Туре	0	1	Default
	Bit 7	48MHz 1 Slew Rate	Slew Rate Control	BW	These bits program the	slew rate of the single	1
	Bit 6			1100	ended outputs. The maximum slew rate is		1
	Bit 5	REF2 Slew Rate	Slew Rate Control	RW	1.9V/ns and the minimur	9V/ns and the minimum slew rate is 1.1V/ns.	1
	Bit 4			1100	The slew rate selec	tion is as follows:	1
	Bit 3	REF1 Slew Rate	Slew Rate Control	RW	11 = 1.9		1
	Bit 2			1100	10 = 1.6V/ns 01 = 1.1V/ns 00 = tristated	1	
	Bit 1	REF0 Slew Rate	Slew Rate Control	RW		1	
	Bit 0			1100	00 = tris	stated	1

^{1616-08/20/09}



THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS					
SYMBOL	MIN.	MAX.			
А	0.8	1.0			
A1	0	0.05			
A3	0.25 Reference				
b	0.18	0.3			
е	0.50 BASIC				

DIMENSIONS	
------------	--

	ICS 72L	
SYMBOL	TOLERANCE	
N	72	
N _D	18	
N _E	18	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75 / 6.15	
E2 MIN. / MAX.	5.75 / 6.15	
L MIN. / MAX.	0.30/ 0.50	

Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9EPRS488CKLF	Tubes	72-pin MLF	0 to +70° C
9EPRS488CKLFT	Tape and Reel	72-pin MLF	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant. Due to package size constraints, actual top-side marking may differ from the full orderable part number.

^{1616-08/20/09}



Revision History

Rev.	Issue Date	Description	Page #
0.1	7/31/2009	Initial Release	-
Α	8/20/2009	Release to final	-

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners. **Contact Information**

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: <u>www.renesas.com/contact/</u>